Twin Builder® Components: SMPS

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1 - SMPS Library

The models of the SMPS library were developed by a power electronics group of the Universidad Politécnica de Madrid, División de Ingeniería Electrónica

The library provides most of the models required to build and evaluate complex power electronics systems. It covers all the power processing steps from the source, storage elements, protection systems, power converters, the load and the controls. The models in the library allow the designer the concentration on higher level tasks. The SMPS Power Library is divided into the following:

Common References

[1] Henry Oman: Power for New Aerospace Missions, IEEE Aerospace and Electronics Systems Magazine Vol. 14 Issue 11, Nov. 1999 pp. 30-33

[2] Rogers, B.E.: Expert system based tool for aerospace power analysis, Energy Conversion Engineering Conference, 1997, Vol. 1 pp. 253-255

[3] Hans-Peter Schöner, Peter Hille: Automotive Power Electronics-New Challenges for Power Electronics, PESC 2000, Vol. 1, pp. 6-11

[4] Mistry, K., Silverman, E., Taylor, T., Willis, R.: Telecommunications power architectures: distributed or centralized, INTELEC '89, vol.1, pp. 1-11

[5] R.D. Middlebrook, S. Cuk: A General Unified Approach to Modeling Switching Converter Power Stages, IEEE PESC 1976, pp. 18-31

[6] V. Vorperian: Simplified Analysis of PWM Converters Using Model of PWM Switch Part I: Continuous Conduction Mode, IEEE Transactions on Aerospace and Electronic Systems 1990, Vol 26, nº3, pp. 490-496

[7] V. Vorperian: Simplified Analysis of PWM Converters Using Model of PWM Switch Part II: Distinuous Conduction Mode, IEEE Transactions on Aerospace and Electronic Systems, 1990, Vol 26, nº3, pp. 497-505

[8] V. M. Canalli, J. A. Cobos, J. A. Oliver, J. Uceda: Behavioral Large Signal Averaged Model for DC/DC Switching Power Converters, IEEE PESC 1996, pp. 1675-1681

[9] D. Maksimovic and R. W. Erickson: Advances in Averaged Switch Modeling and Simulation, IEEE PESC Tutorial 1999

[10] R. W. Erickson: Fundamentals of Power Electronics, Kluwer Academic Publisher

Advanced

- AC-DC
- Three-Phase Averaged
- Three-Phase dq
- Transformation

Advanced AC-DC

- Single-Phase
- Three-Phase

Advanced AC-DC, Single-Phase

- Fully Controlled Rectifier (B1phC)
- Diode Bridge (B1phU)

B1phC Fully Controlled Rectifier

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

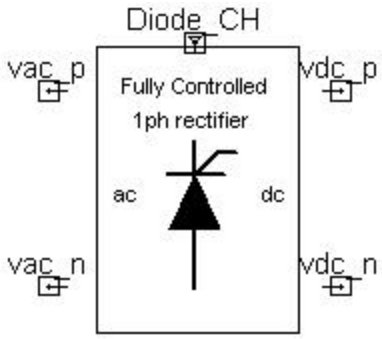

Figure 1. Component symbol

Description

Fully controlled single-phase bridge rectifier performs AC rectification by means of a bridge of controlled switches. The static characteristic of the switches can be defined by means of a characteristic component from the Tools section or an appropriate quantity of a component. The user has to define the frequency of the source and the firing angle of the switches. The firing angle can also be varied during simulation.

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Netlist Syntax

MODEL B1phC ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_p:= %0, vac_n:= %1, vdc_p:= %2, vdc_n:= %3 (Diode_CH:= @Diode_CH, alpha:= @alpha, line_freq:= @line_freq) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_p	AC Input positive pin	Electrical terminal
vac_n	AC Input negative pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
alpha	Firing Angle	real	0 [Deg]
line_freq	Line Frequency	real	50 [Hz]
Diode_CH	Diode Characteristics	real	

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Example

This example is a typical fully controlled full bridge rectifier with an inductor filter at the output. The results show the input voltage and the current through the load. The current through the load can be controlled with the firing angle. The switch characteristic is defined with an external function.

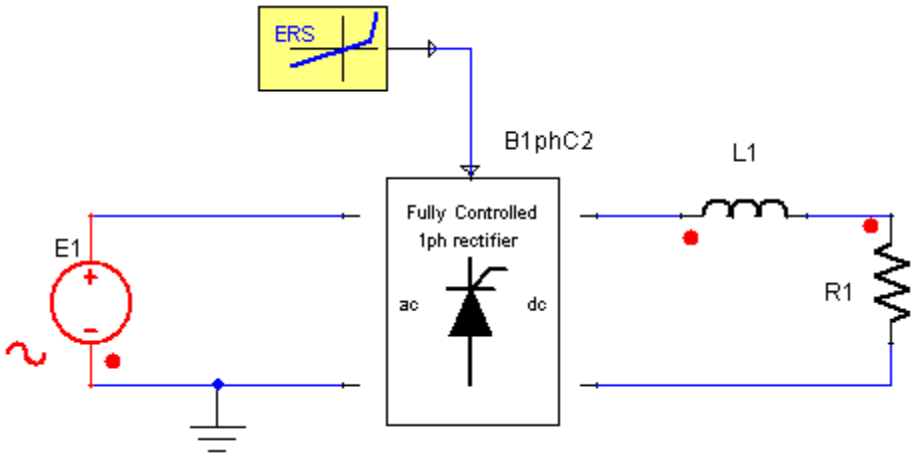

Figure 2. Application examples of the Single Phase Fully Controlled Rectifier model

Table 3. System Parameters

Component	Parameter	Value [unit]
Fully Controlled Rectifier B1phC1	Diode_CH	EQUL1.VAL
	alpha	30 [deg]
Equivalent Line EQUL1	VF	0.6 [V]
Resistor R1	R	1 [Ohm]
Inductor L1	L	0.01 [H]
Voltage Source E1	AMPL	326 [V]
	Freq	50 [Hz]
	Type	ESINE
	TPERIO	Tend+1

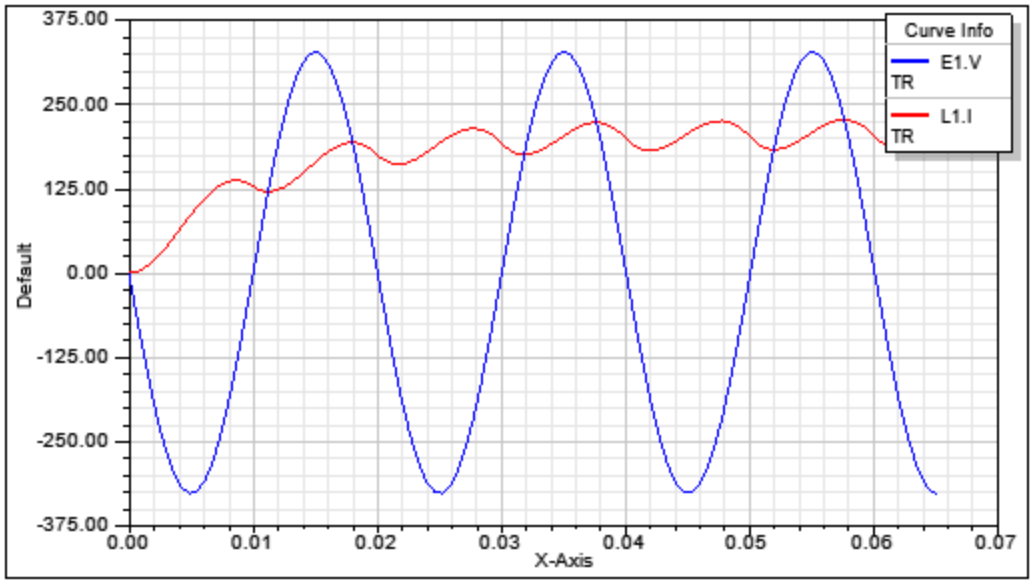

Figure 3. Simulation results-voltage output from source (E1.V) and the rectified output of the bridge (L1.V).

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B1phU Diode Bridge

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

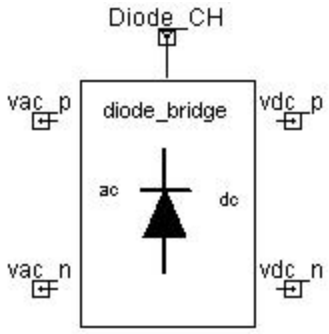

Figure 1. Component symbol

Description

Diode Bridge rectifier is a block that performs AC rectification through a diode bridge rectifier. It employs System level diodes for faster simulations. The diode characteristic can be defined by means of a characteristic component from the Tools section or an appropriate quantity of a component.

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Netlist Syntax

MODEL B1phU ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_p:= %0, vac_n:= %1, vdc_p:= %2, vdc_n:= %3 (Diode_CH:= @Diode_CH) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_p	AC Input positive pin	Electrical terminal
vac_n	AC Input negative pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Diode_CH	Diode Characteristics	real	

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Example

This example is a typical full bridge rectifier with a capacitor filter at the output. The results show the input voltage and the voltage applied to the load. The switch characteristic is defined with an external function.

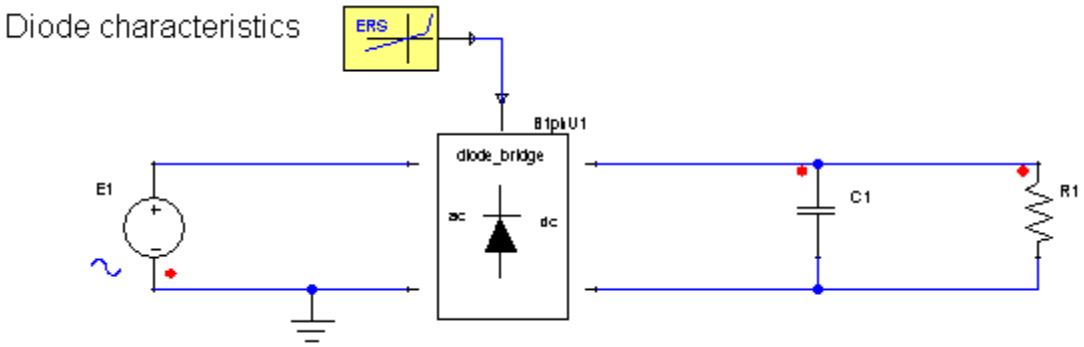

Figure 2. Application examples of the Single Phase Diode Bridge model

Table 3. System Parameters

Component	Parameter	Value [unit]
Diode Bridge B1phU1	Diode_CH	EQUL1.VAL
Equivalent Line EQUL1	VF	0.6 [V]
Resistor R1	R	100 [Ohm]
Capacitor C1	C	0.0001 [F]
Voltage Source E1	AMPL	326 [V]
	Freq	50 [Hz]
	Type	ESINE
	TPERIO	Tend+1

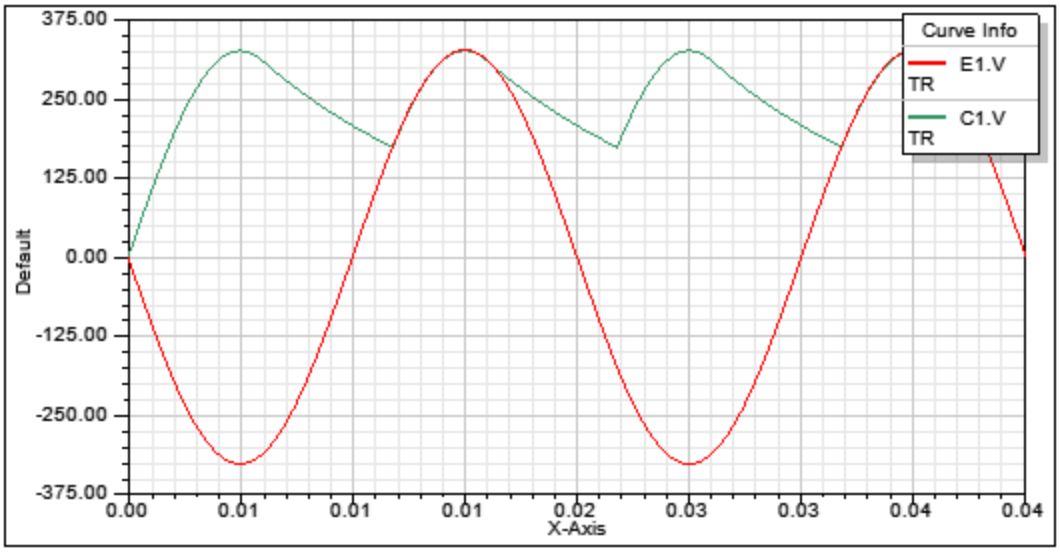

Figure 3. Simulation results-voltage output from source (E1.V) and the rectified output of the bridge (C1.V).

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References

Advanced AC-DC, Three-Phase

- Half-Controlled Rectifier (B3phHC)
- Diode Bridge (B3phU)
- B6C with Additional Inputs for Signal Generation and Pulse Enable (B6C_E_SMPS)
- Fully-Controlled 6-Pulse Bridge Connection with Static Models for Thyristors (B6C_SMPS)

B3phHC Half Controlled Rectifier

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

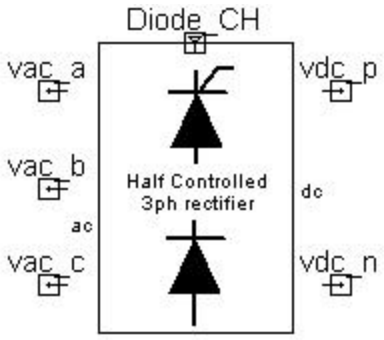

Figure 1. Component symbol

Description

The Half-Controlled Three-Phase Rectifier contains three controlled switches and three diodes (uncontrolled). The static characteristic of the switches can be defined by means of a characteristic component from the Tools section or an appropriate quantity of a component. The user has to define the frequency of the source and the firing angle of the controlled switches. The firing angle can also be varied during simulation.

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Netlist Syntax

MODEL B3phHC ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_a:= %0, vac_b:= %1, vdc_p:= %2, vdc_n:= %3, vac_c:= %4 (Diode_CH:= @Diode_CH, alpha:= @alpha, line_freq:= @line_freq) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_a	AC Input Phase A pin	Electrical terminal
vac_b	AC Input Phase B pin	Electrical terminal
vac_c	AC Input Phase C pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
alpha	Firing Angle	real	0 [Deg]
line_freq	Line Frequency	real	50 [Hz]
Diode_CH	Diode Characteristics	real	

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Example

This example is a typical half-controlled full-bridge rectifier with a inductor filter at the output. The results show the input voltage and the current through the load. The current through the load can be controlled with the firing angle. The switch characteristic is defined with an external function.

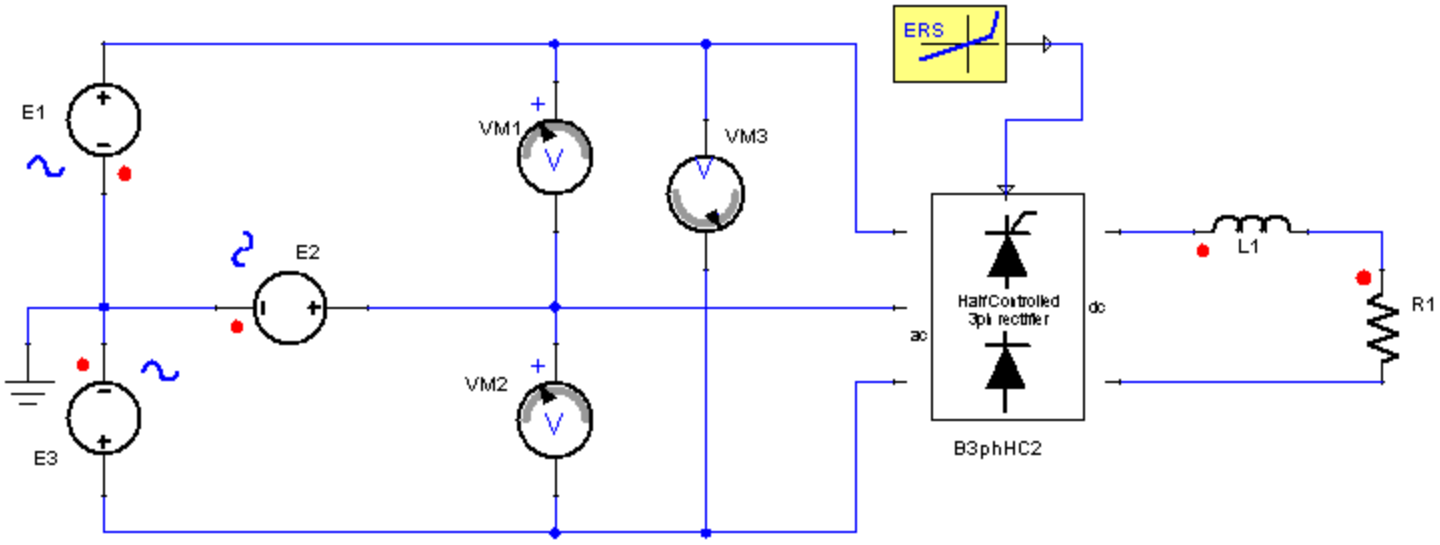

Figure 2. Application examples of the Semi-Controlled Three-Phase Rectifier model

Table 3. System Parameters

Component	Parameter	Value [unit]
Half-Controlled Three-Phase Rectifier B3PHHC2	Diode_CH	EQUL1.VAL
	alpha	22.5 [deg]
Equivalent Line EQUL1	VF	0.6 [V]
Resistor R1	R	1 [Ohm]
Inductor L1	L	0.01 [H]
Voltage Source (Sinusoidal) E1/E2/E3	AMPL	326 [V]
	Freq	50 [Hz]
	Phase	0/120/-120 [deg]

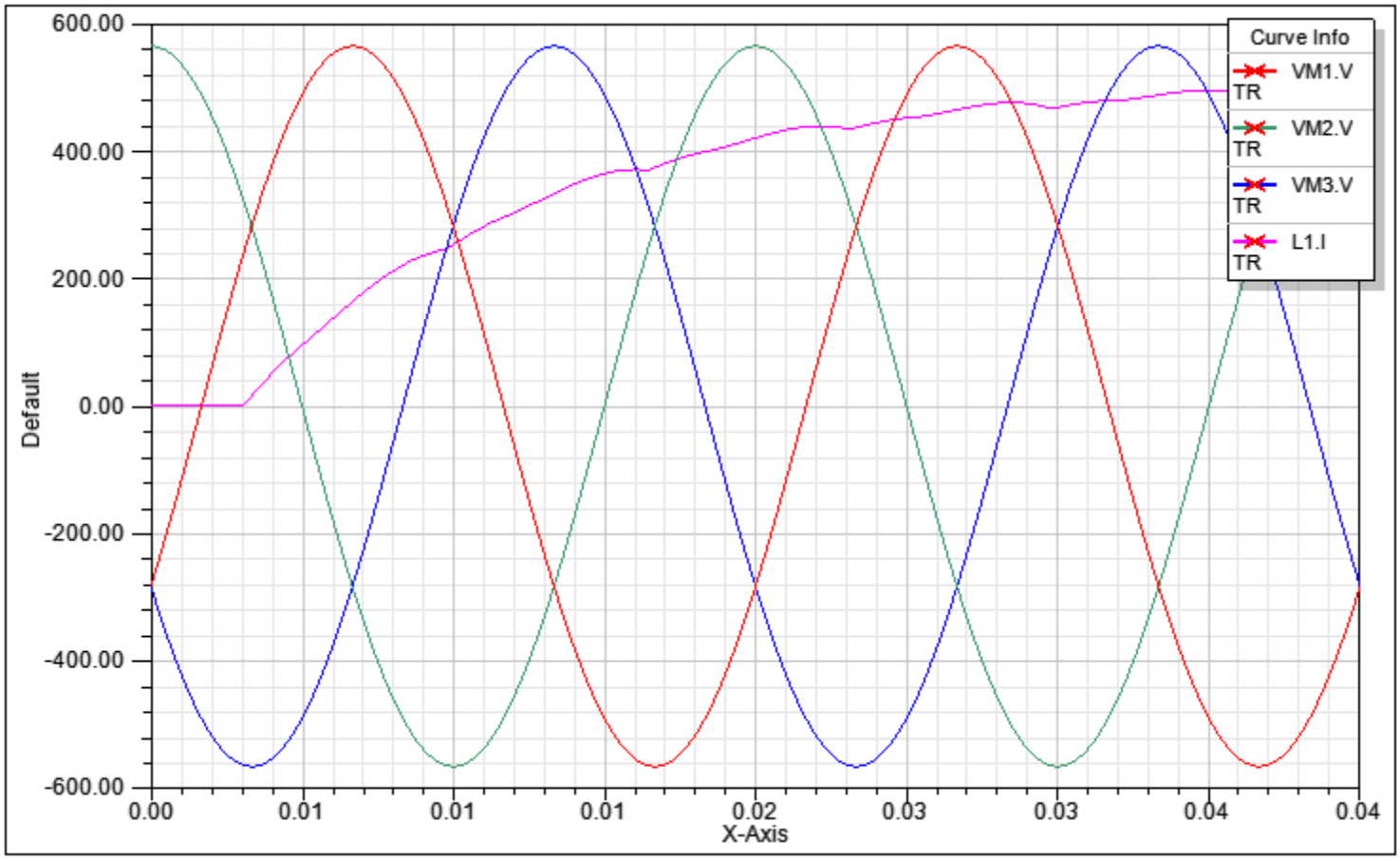

Figure 3. Simulation results-voltage current through inductor (L1.I) and the 3 phase source voltages (VM1.V, VM2.V, VM3.V).

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References

B3phU Diode Bridge

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

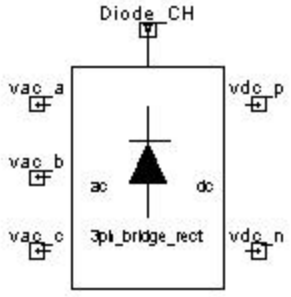

Figure 1. Component symbol

Description

The three-phase diode bridge rectifier block performs AC rectification through a 3 leg diode bridge rectifier. Each leg is connected to one of the phases of the three-phase voltage. It employs System level diodes for faster simulations. The diode characteristic can be defined by means of a characteristic component from the Tools section or an appropriate quantity of a component.

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Netlist Syntax

MODEL B3phU ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_a:= %0, vac_b:= %1, vdc_p:= %2, vdc_n:= %3, vac_c:= %4 (Diode_CH:= @Diode_CH) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_a	AC Input Phase A pin	Electrical terminal
vac_b	AC Input Phase B pin	Electrical terminal
vac_c	AC Input Phase C pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Diode_CH	Diode Characteristics	real	

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Example

This example is a typical three-phase rectifier bridge with a capacitive filter at the output. The results show the input voltage and the voltage applied to the load. The switch characteristic is defined with an external function.

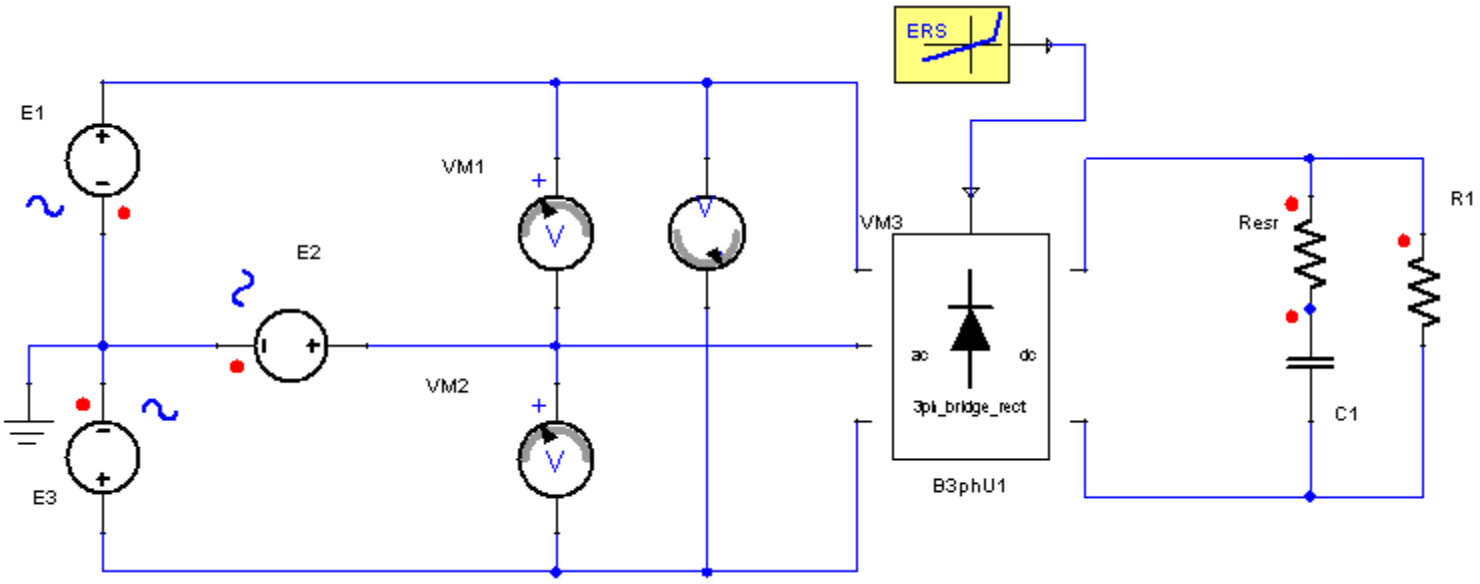

Figure 2. Application examples of the Three-Phase Diode Bridge model

Table 3. System Parameters

Component	Parameter	Value [unit]
Three-Phase Diode Bridge Rectifier B3PHU1	Diode_CH	EQUL1.VAL
Equivalent Line EQUL1	VF	0.6 [V]
	RB	0.1 [Ohm]
Resistor R1	R	100 [Ohm]
Resistor Resr	R	0.05 [Ohm]
Capacitor C1	C	0.0001 [F]
Voltage Source (Sinusoidal) E1/E2/E3	AMPL	326 [V]
	Freq	50 [Hz]
	Phase	0/120/-120 [deg]

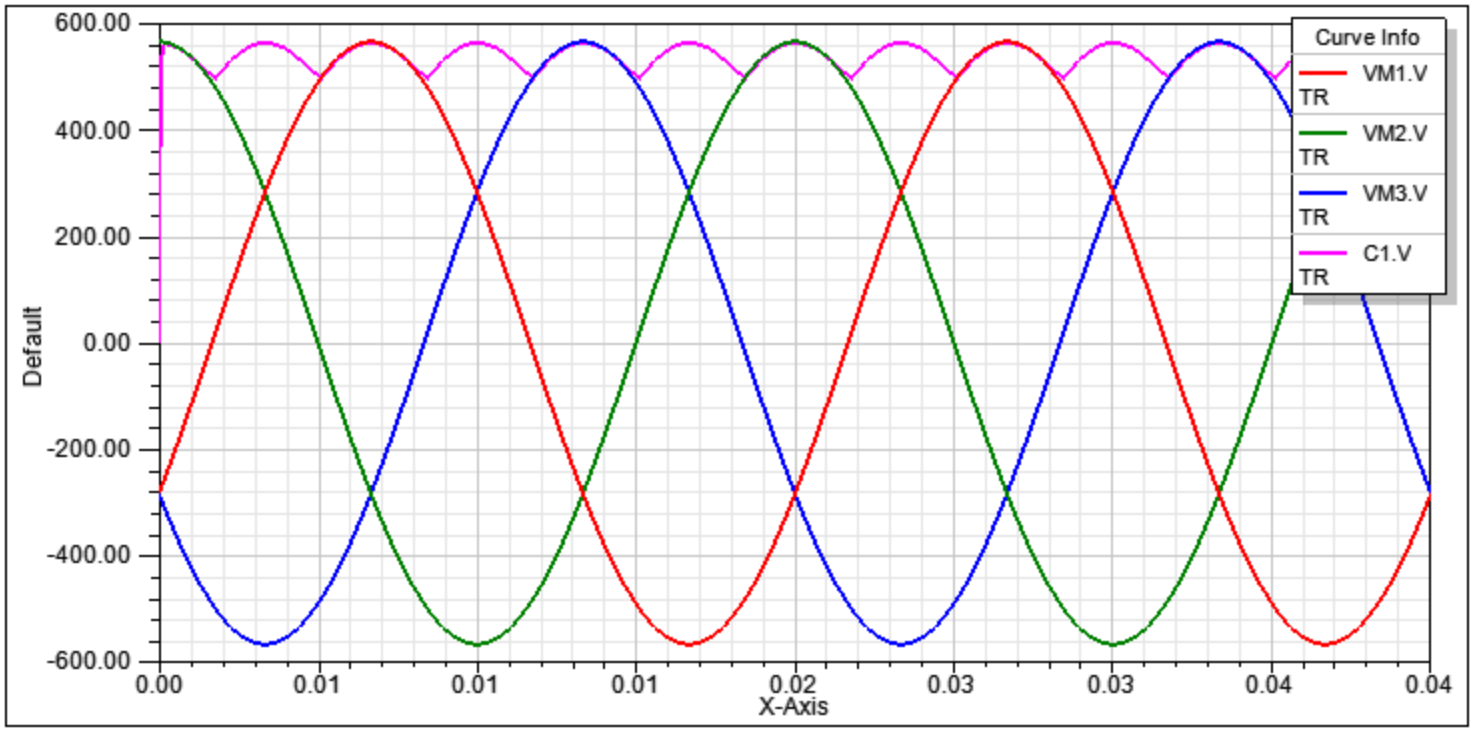

Figure 3. Simulation results-Voltage Output across capacitor (C1.V) and the 3 phase source voltages (VM1.V, VM2.V, VM3.V).

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References

(B6C_E_SMPS) B6C With Additional Inputs for Signal Generation and Pulse Enable

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

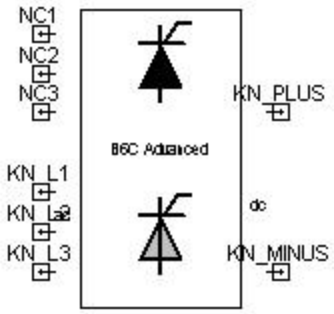

Figure 1. Component symbol

Description

The B6C Thyristor Bridge Enhanced performs AC rectification by means of six controlled switches. Each leg is connected to one of the phases of the three-phase voltage. It employs System level switches for faster simulations. The switches characteristic can be defined by means of its forward voltage drop, its bulk resistance and its reverse resistance. The user has to define the frequency of the source and the firing angle of the controlled switches. Both can be time dependent.

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Netlist Syntax

MODEL B6C_E_SMPS ?InstanceName(@InstanceName):(@(Refbase)@(ID)) KN_L1:= %0, KN_L2:= %1, KN_L3:= %2, KN_PLUS:= %3, KN_MINUS:= %4, NC1:= %5, NC2:= %6, NC3:= %7 (ALPHA:= @ALPHA, FREQUENCY:= @FREQUENCY, ENABLE:= @ENABLE, START:= @START, TON:= @TON, VF:= @VF, RB:= @RB, RR:= @RR) SRC: DB(Lib:- :=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
KN_L1	AC Input Phase 1 pin	Electrical terminal
KN_L2	AC Input Phase 2 pin	Electrical terminal
KN_L3	AC Input Phase 3 pin	Electrical terminal
KN_PLUS	DC Side positive pin	Electrical terminal
KN_MINUS	DC Side negative pin	Electrical terminal
NC1	Control Input (Phase 1)	Electrical terminal
NC2	Control Input (Phase 2)	Electrical terminal
NC3	Control Input (Phase 3)	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
ALPHA	Delay Angle	real	30 [Deg]
FREQUENCY	Supply Frequency	real	50 [Hz]
TON	Pulse Length	real	0.006 [s]
ENABLE	Enable for Thyristor Control Signals	real	1
START	Start Flag for Angle Calculation	real	1
VF	Forward Voltage of Thyristors	real	0.8
RB	Bulk Resistance of Thyristors	real	0.001 [Ohm]
RR	Reverse Resistance of	real	100000

	Thyristors		[Ohm]

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Example

This example is a typical fully controlled full bridge rectifier with an inductor filter at the output. The results show the input voltage and the current through the load. The current through the load can be controlled with the firing angle. The switch characteristic is defined with an external function.

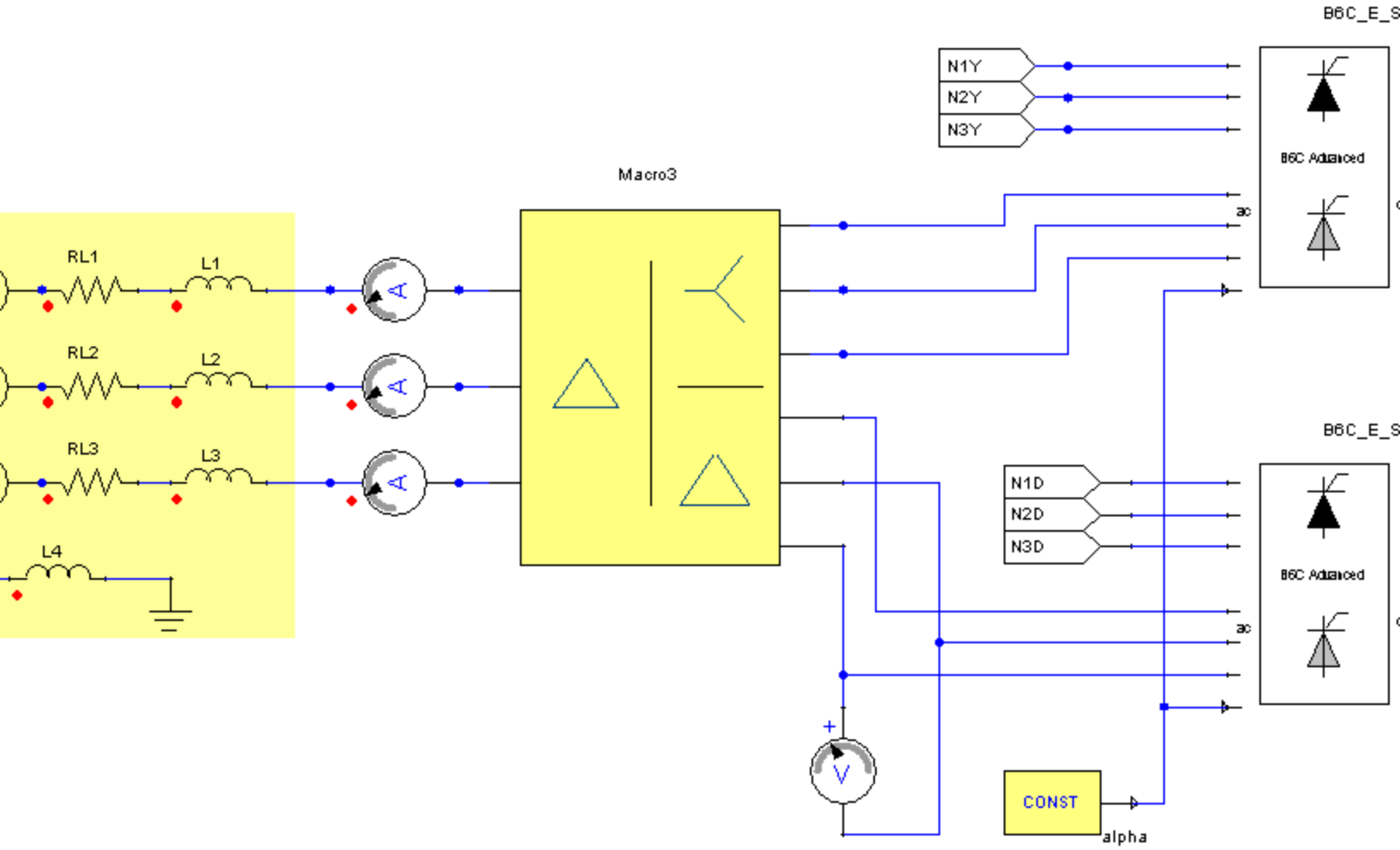

Figure 2. Application example of the Fully-controlled 6-Pulse Bridge Rectifier.

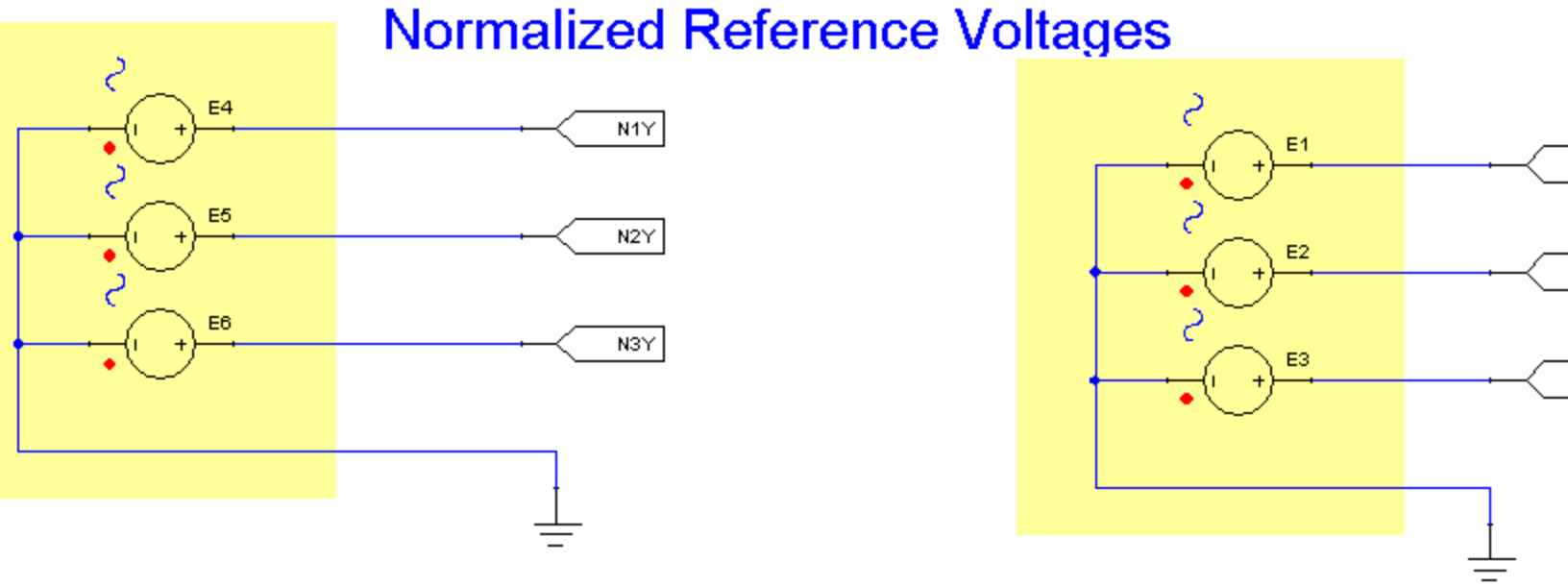

Figure 3. References Voltages for Fully-controlled 6-Pulse Bridge Rectifiers.

Table 3. System Parameters

Component	Parameter	Value [unit]
Fully-Controlled 6-Pulse Bridge B6C_E_SMPS1/B6C_E_SMPS2	ALPHA	ALPHA.VAL
	FREQUENCY	60 [Hz]
	TON	0.00555 [s]
Constant Value ALPHA	Value	35 [Deg]
Resistor R1	R	25 [Ohm]
Inductor L1/L2/L3	L	1.5e-007 [H]
Inductor L4	L	0.0001 [H]
Resistor RL1/RL2/RL3	R	0.001 [Ohm]
Resistor RL31	R	0.16 [Ohm]
Voltage Source (Sinusoidal) E7/E8/E9	AMPL	750 [V]
	Freq	60 [Hz]
	Phase	0/-120/-240 [deg]
Voltage Source (Sinusoidal) E1/E2/E3	AMPL	1 [V]
	Freq	60 [Hz]
	Phase	0/-120/-240 [deg]
Voltage Source (Sinusoidal) E4/E5/E6	AMPL	1 [V]
	Freq	60 [Hz]
	Phase	-30/-150/-270

		[deg]

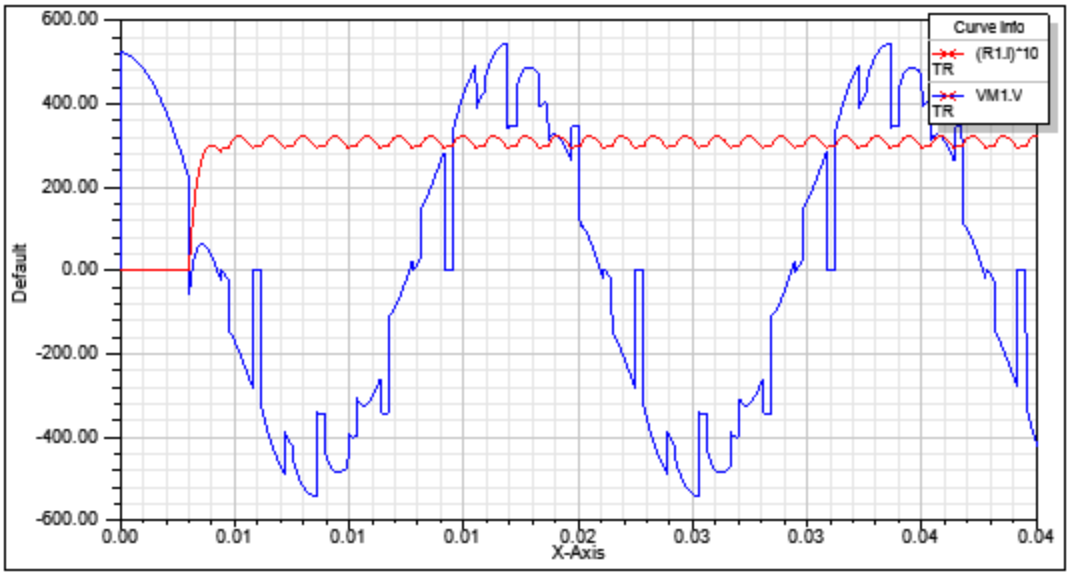

Figure 4. Simulation results-Transformer voltage output (VM1.V) and the rectified load current (x10) delivered from the bridge to the load resistor (R1.I * 10).

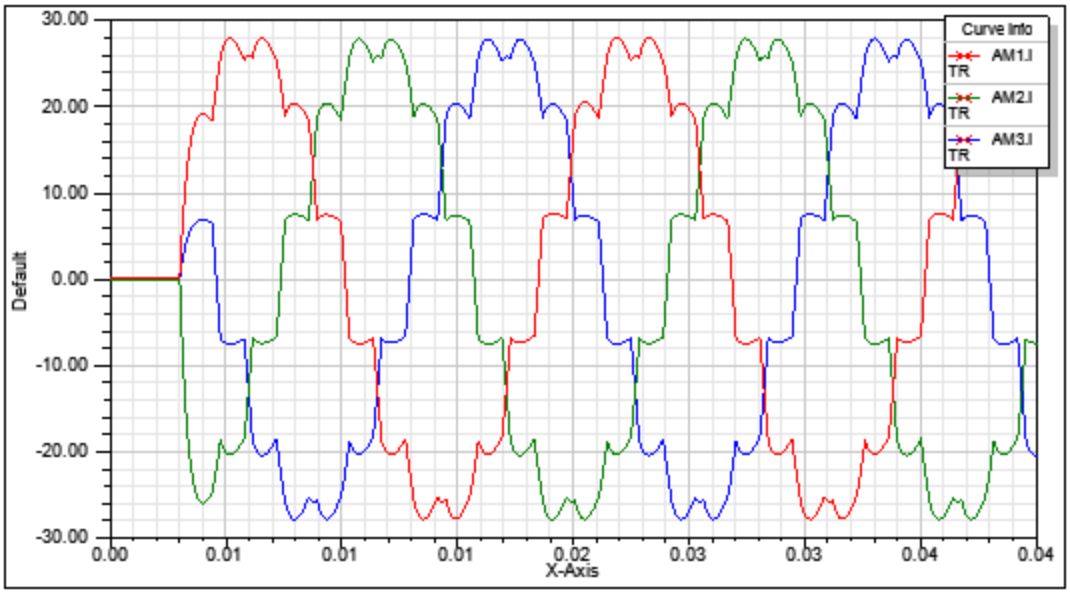

Figure 5. Simulation results-source currents provided to the MACRO3 subcircuit.

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References

B6C_SMPS Fully-controlled 6-Pulse Bridge Connection with Static Models For Thyristors

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

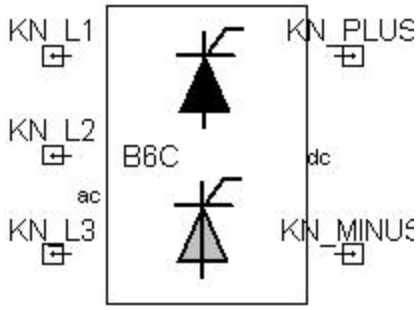

Figure 1. Component symbol

Description

The B6C Thyristor Bridge performs AC rectification by means of six controlled switches. Each leg is connected to one of the phases of the three-phase voltage. It employs System level switches for faster simulations. The switches characteristic can be defined by means of its forward voltage drop, its bulk resistance and its reverse resistance. The user has to define the frequency of the source and the firing angle of the controlled switches. Both can be time dependent.

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Netlist Syntax

MODEL B6C_SMPS ?InstanceName(@InstanceName):(@(Refbase)@(ID)) KN_L1:= %0, KN_L2:= %1, KN_L3:= %2, KN_PLUS:= %3, KN_MINUS:= %4 (ALPHA:= @ALPHA, FREQUENCY:= @FREQUENCY, VF:= @VF, RB:= @RB, RR:= @RR) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_a	AC Input Phase A pin	Electrical terminal
vac_b	AC Input Phase B pin	Electrical terminal
vac_c	AC Input Phase C pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
ALPHA	Delay Angle	real	30 [Deg]
FREQUENCY	Frequency of Input Voltage	real	50 [Hz]
VF	Forward Voltage of Thyristors	real	0.8 [V]
RB	Bulk Resistance of Thyristors	real	0.001 [Ohm]
RR	Reverse Resistance of Thyristors	real	100000 [Ohm]

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Example

This example is a typical fully controlled three-phase full bridge rectifier with an inductor filter at the output. The results show the input voltage and the current through the load. The current

through the load can be controlled with the firing angle. The switch characteristic is defined with an external function.

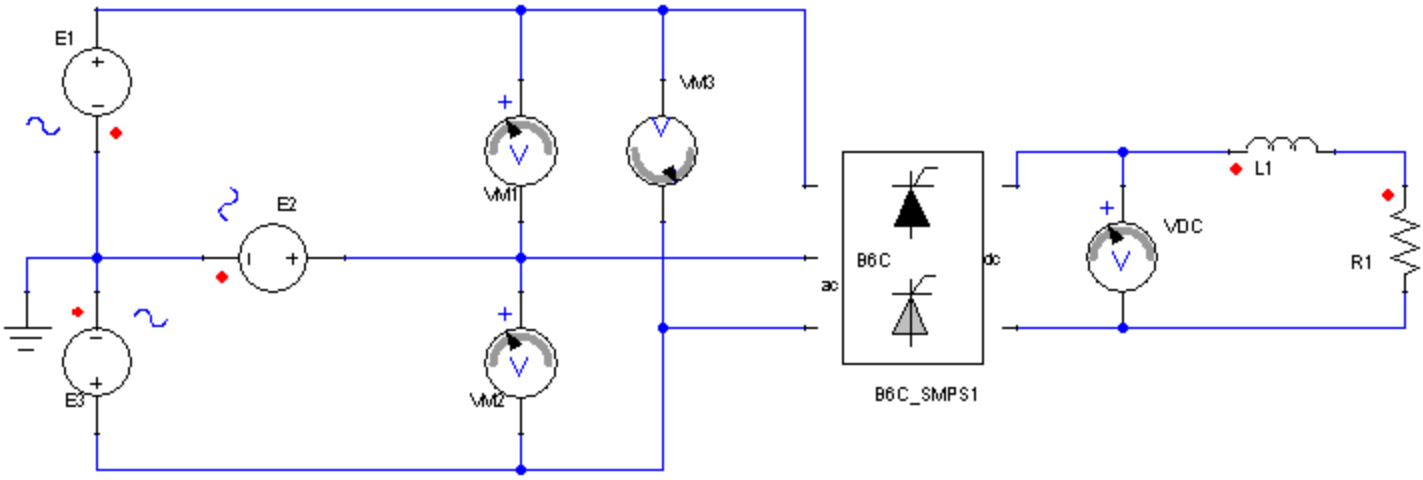

Figure 2. Application example of the Fully-controlled Three-Phase Bridge Rectifier.

Table 3. System Parameters

Component	Parameter	Value [unit]
Fully-Controlled Three-Phase Bridge Rectifier B6C_SMPS1	ALPHA	30
	FREQUENCY	50 [Hz]
	VF	0.8 [V]
Resistor R1	R	1 [Ohm]
Inductor L1	L	0.1 [H]
Voltage Source (Sinusoidal) E1/E2/E3	AMPL	326 [V]
	Freq	50 [Hz]
	Phase	0/120/-120 [deg]

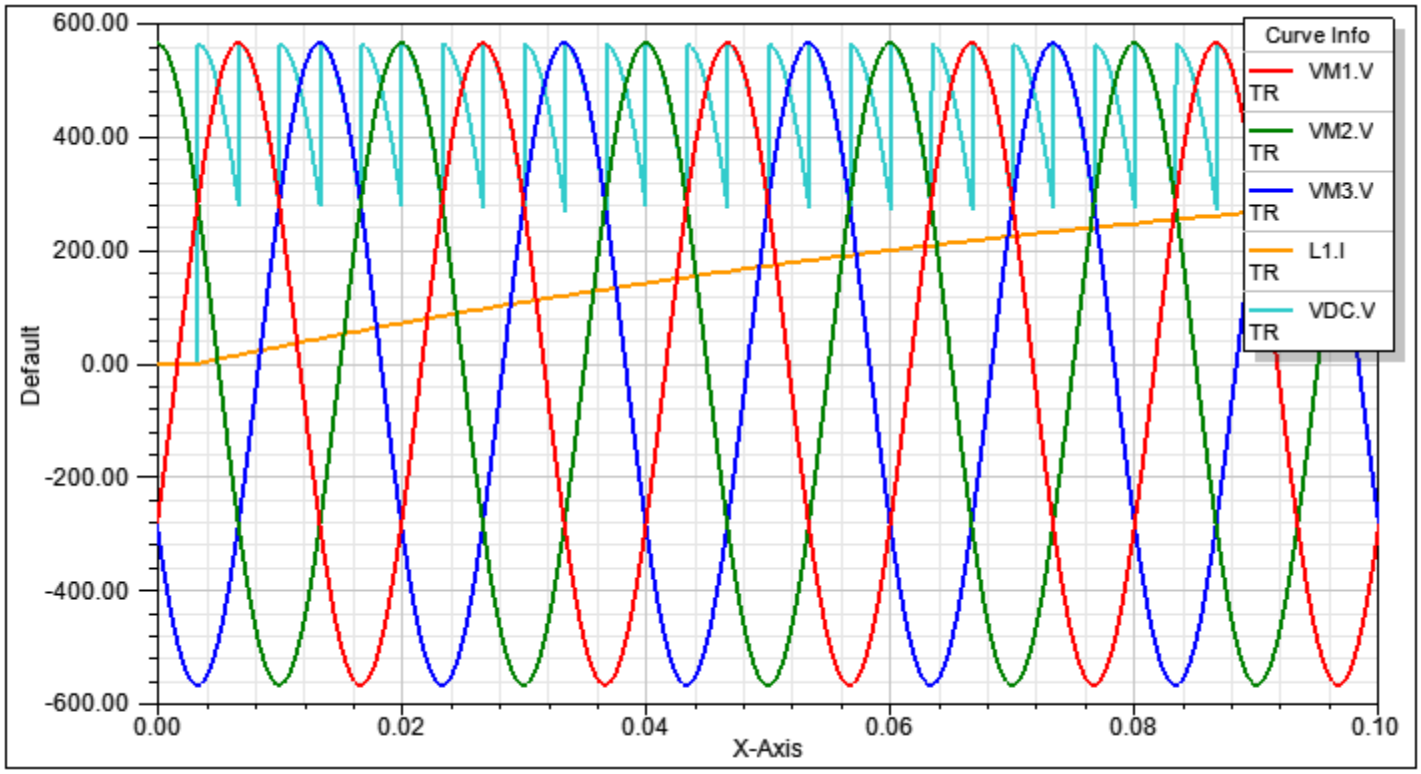

Figure 3. Simulation results-Line Voltage output (VM1.V, VM2.V, VM3.V) and the rectified load current (L1.I) the output voltage(VDC.V).

Top

References

Advanced Three-Phase Averaged

The components of this section are average large-signal models of the most common three-phase converters.

- Boost (Boost3ph_A)
- Buck (Buck3ph_A)
- Current Source Inverter (CSI3ph_A)
- Voltage Source Inverter (VSI3ph_A)

See also:

- Advanced Three-Phase dq

Boost3ph_A Boost Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

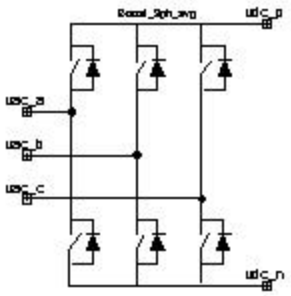

Figure 1. Component symbol

Description

This block represents the averaged level model of the three-phase boost converter. The equivalent circuit schematic is shown in Figure 2.

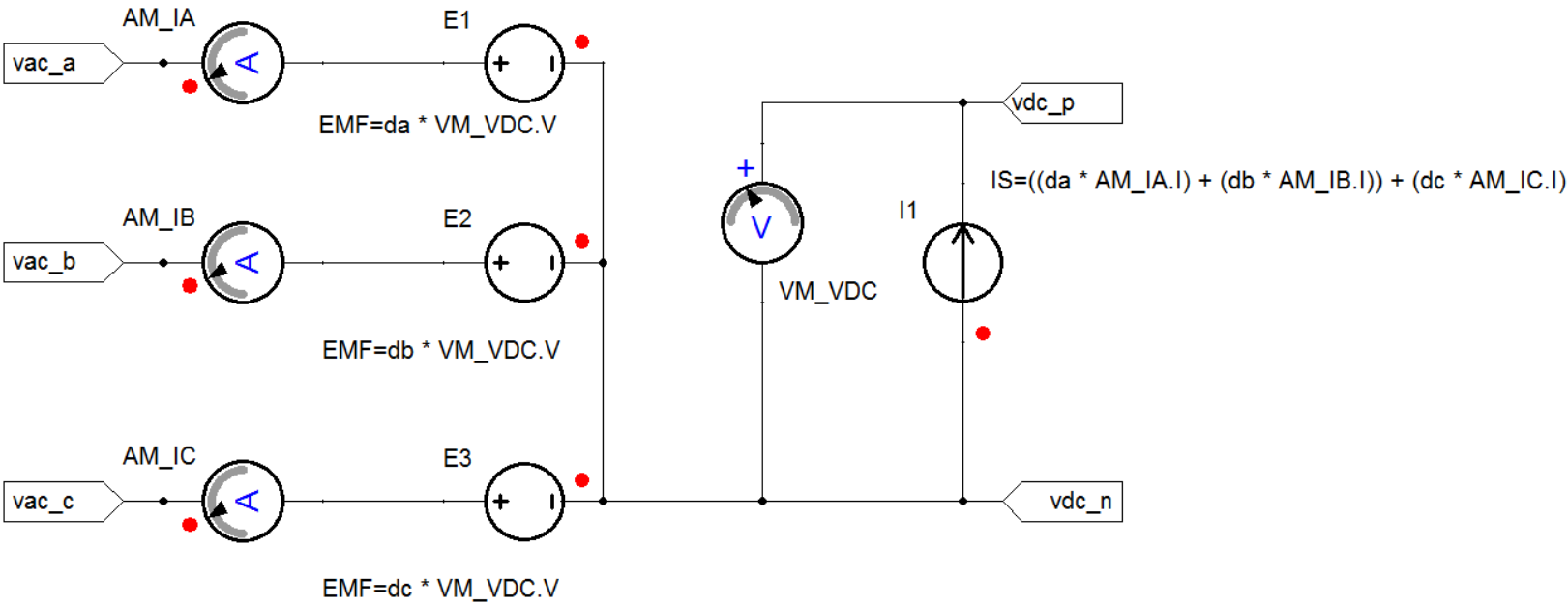

Figure 2. Equivalent Circuit Schematic

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Assumptions and Limitations

This block assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The duty cycles can be calculated by means of the following relation:

$$d_{\phi} = \frac{T_1}{T}$$

Where d_{Φ} represents the duty cycle for the considered leg, T1 is the on time of the upper switch of this leg and T the switching period as shown:

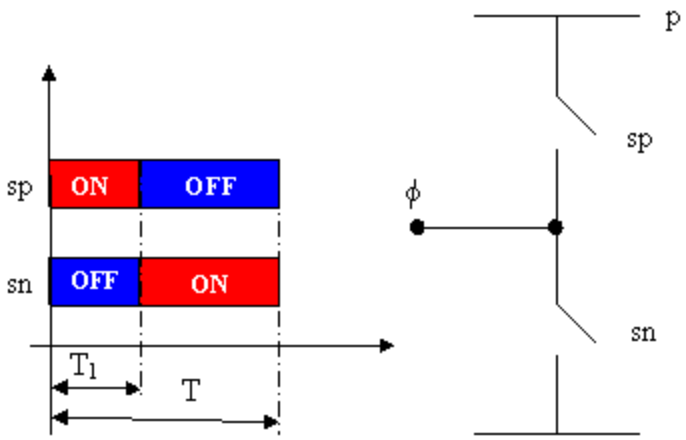

Figure 3. Switching Diagram

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Mathematical Description

Top

Netlist Syntax

MODEL Boost3ph_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_a:= %0, vac_b:= %1, vdc_p:= %2, vdc_n:= %3, vac_c:= %4 (da:= @da, db:= @db, dc:= @dc) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_a	AC Input Phase A pin	Electrical terminal
vac_b	AC Input Phase B pin	Electrical terminal
vac_c	AC Input Phase C pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
da	Duty Cycle of Phase A	real	0
db	Duty Cycle of Phase B	real	0
dc	Duty Cycle of Phase C	real	0

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Example

This example is a Three-Phase Boost converter using averaged models. The results show the line currents and the output voltage. The duty cycles controls the energy transferred to the load.

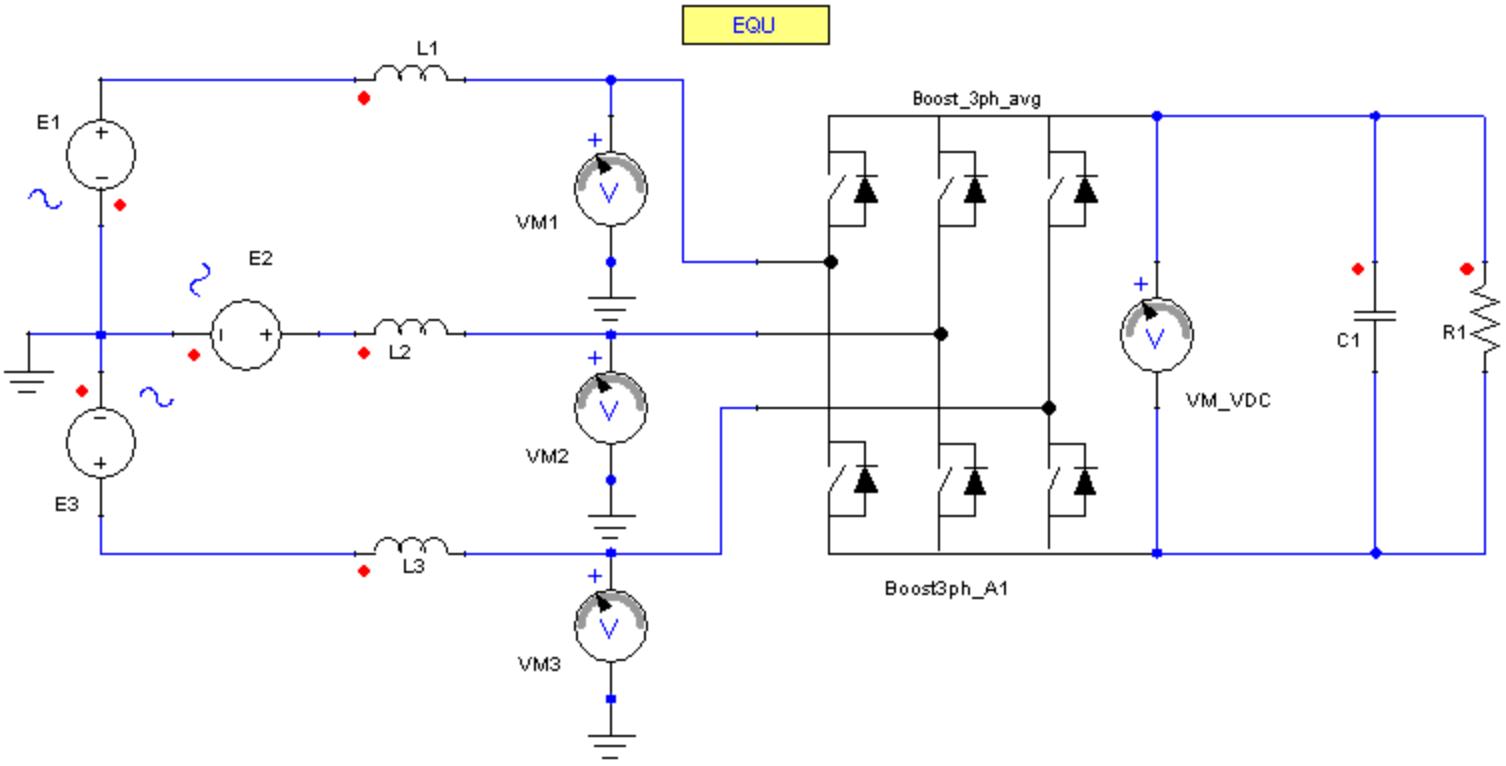

Figure 4. Application example of an Average Model of Three-Phase Boost Converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Average Three-Phase Boost Converter Boost3ph_A1	da	da
	db	db
	dc	dc
Equation Block FML2	EQU0	da:=0.5+0.45*sin (314.15926*Time-2.0944)
	EQU1	db:=0.5+0.45*sin (314.15926*Time)
	EQU2	dc:=0.5+0.45*sin (314.15926*Time+2.0944)
Resistor R1	R	1 [Ohm]
Capacitor C1	C	0.001 [F]
Inductor L1/L2/L3	L	0.0001 [H]
Voltage Source (Sinus-oidal) E1/E2/E3	AMPL	300 [V]
	Freq	50 [Hz]
	Phase	0/120/-120 [deg]

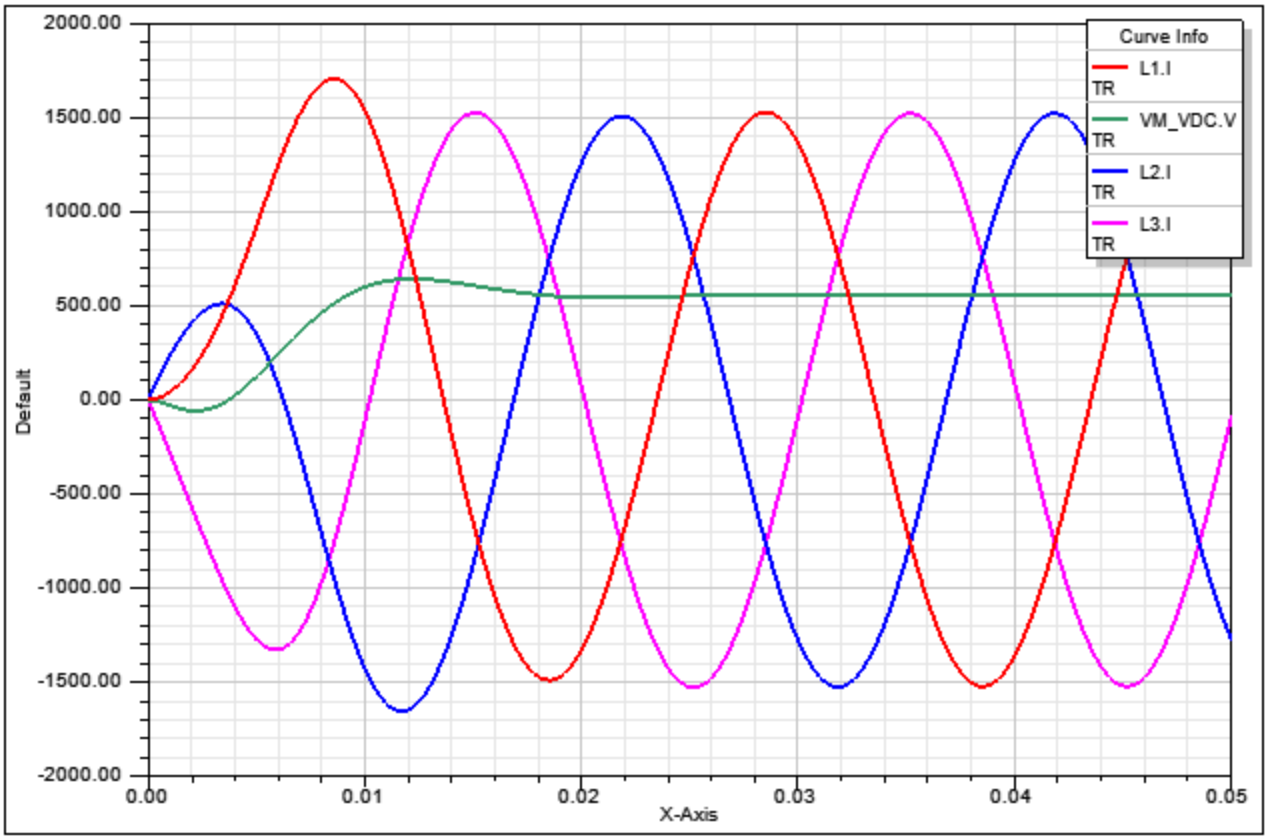

Figure 5. Simulation results-Voltage output (VM_VDC.V) and input line currents to the rectifier (L1.I, L2.I, L3.I).

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References

Buck3ph_A Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

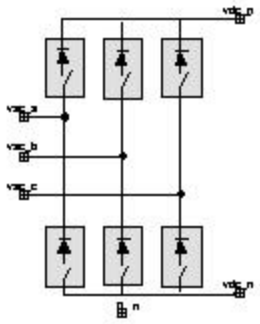

Figure 1. Component symbol

Description

This block represents the averaged level model of the three-phase buck converter. The equivalent circuit schematic is shown in Figure 2.

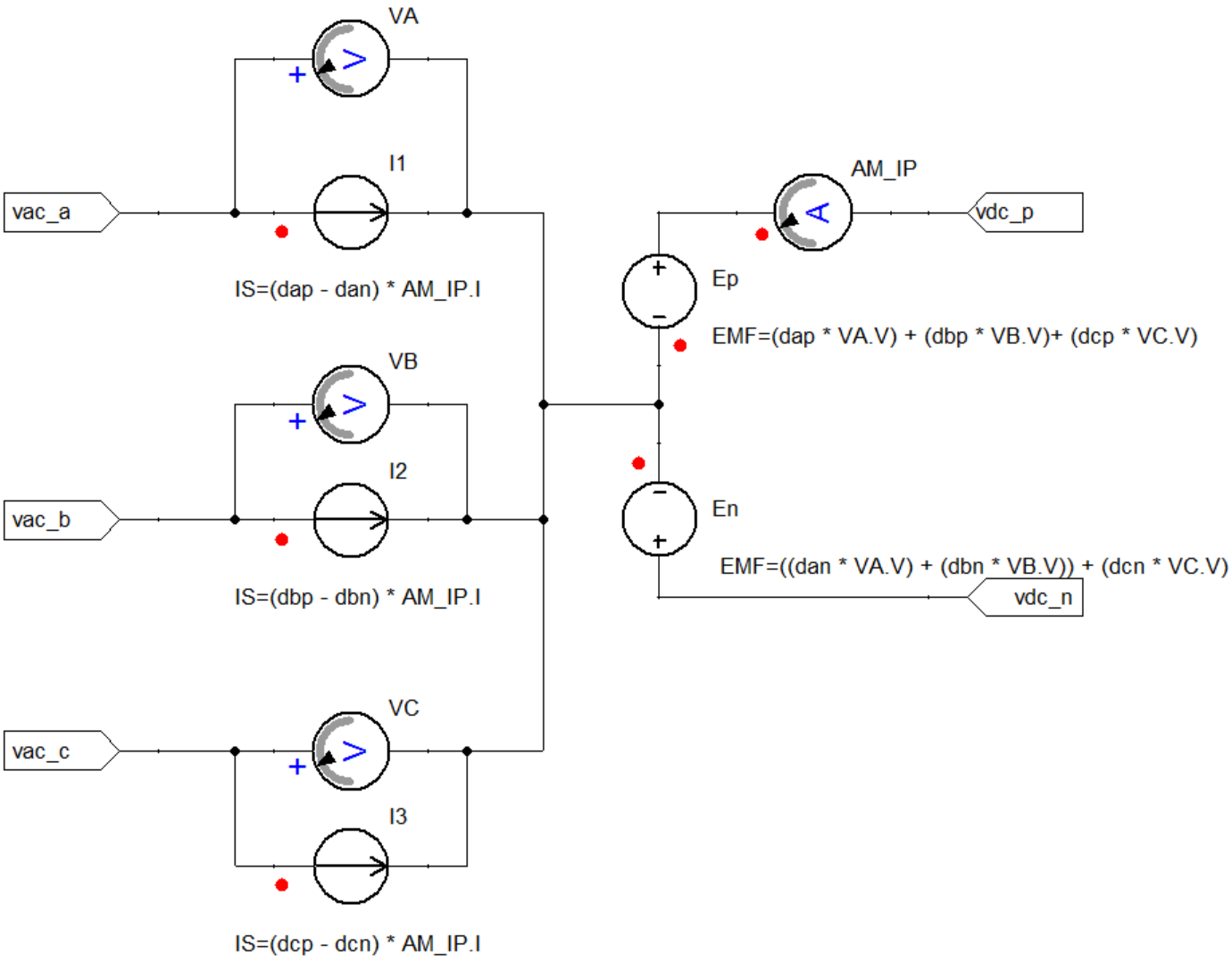

Figure 2. Equivalent Circuit Schematic

Top

Assumptions and Limitations

This block assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The duty cycles can be calculated by means of the following relation:

$$d_{\phi} = \frac{T_1}{T}$$

Where d_{Φ} represents the duty cycle for the considered switch, T1 is the on time of this switch in a switching period and T is the switching period.

A restriction to be taken into account is that:

$$d_{ap} + d_{bp} + d_{cp} = 1$$

$$d_{an} + d_{bn} + d_{cn} = 1$$

It means that there must be a path for the current to flow, at any time, through some of the upper switches and some of the lower switches.

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Mathematical Description

Top

Netlist Syntax

MODEL Buck3ph_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_a:= %0, vac_b:= %1, vdc_p:= %2, vdc_n:= %3, vac_c:= %4, n:= %5 (dap:= @dap, dbp:= @dbp, dcp:= @dcp, dan:= @dan, dbn:= @dbn, dcn:= @dcn) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_a	AC Input Phase A pin	Electrical terminal
vac_b	AC Input Phase B pin	Electrical terminal
vac_c	AC Input Phase C pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal
n	Neutral pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
dap	Duty Cycle of Upper Switch of Phase A	real	0
dbp	Duty Cycle of Upper Switch of Phase B	real	0
dcp	Duty Cycle of Upper Switch of	real	0

	Phase C		
dan	Duty Cycle of Lower Switch of Phase A	real	0
dbn	Duty Cycle of Lower Switch of Phase B	real	0
dcn	Duty Cycle of Lower Switch of Phase C	real	0

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Example

This example uses a three-phase Buck converter using Averaged models. The results show the output voltage and the input line voltages. The duty cycles control the energy transferred to the load.

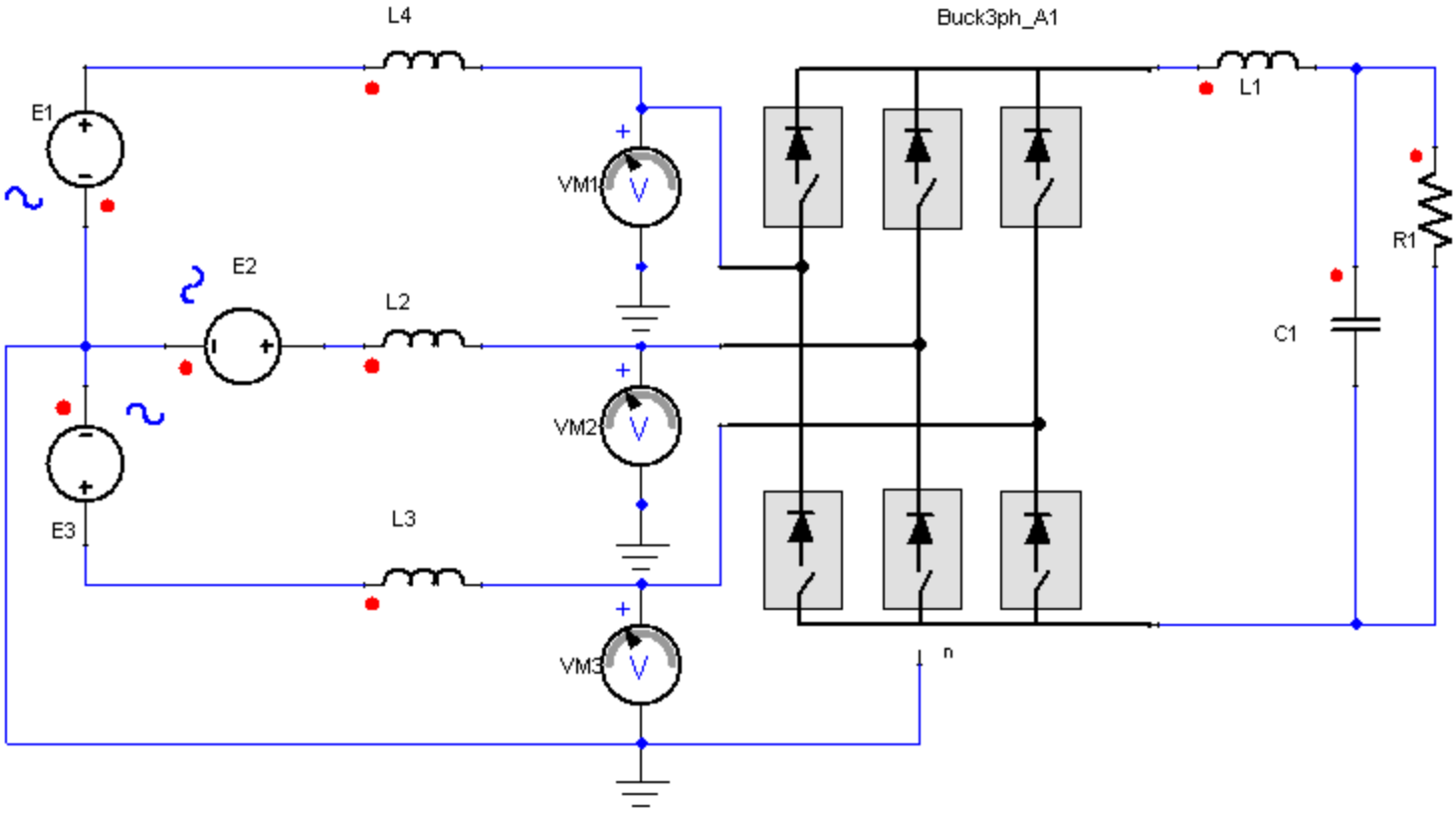

Figure 3. Application example of an Average Model of Three-Phase Buck Converter.

Table 3. System Parameters

Component	Parameter	Value [unit]

Average Three-Phase Buck Converter Buck3ph_A1	dap	dap
	dbp	dbp
	dcp	dcp
	dan	dan
	dbn	dbn
	dcn	dcn
Equation Block FML1	EQU0	dap:=0.3333333333+(0.2*sin(314.15926*Time))
	EQU1	dan:=0.3333333333-(0.2*sin(314.15926*Time))
	EQU2	dbp:=0.3333333333+(0.2*sin(314.15926*Time-2.0943951))
	EQU3	dbn:=0.3333333333-(0.2*sin(314.15926*Time-2.0943951))
	EQU4	dcp:=0.3333333333+(0.2*sin(314.15926*Time+2.0943951))
	EQU5	dcn:=0.3333333333-(0.2*sin(314.15926*Time+2.0943951))
Resistor R1	R	1 [Ohm]
Capacitor C1	C	0.0001 [F]
Inductor L1	L	0.0001 [H]
Inductor L2/L3/L4	L	1e-006 [H]
Voltage Source (Sinusoidal) E1/E2/E3	AMPL	300 [V]
	Freq	50 [Hz]

	Phase	0/-120/120 [deg]

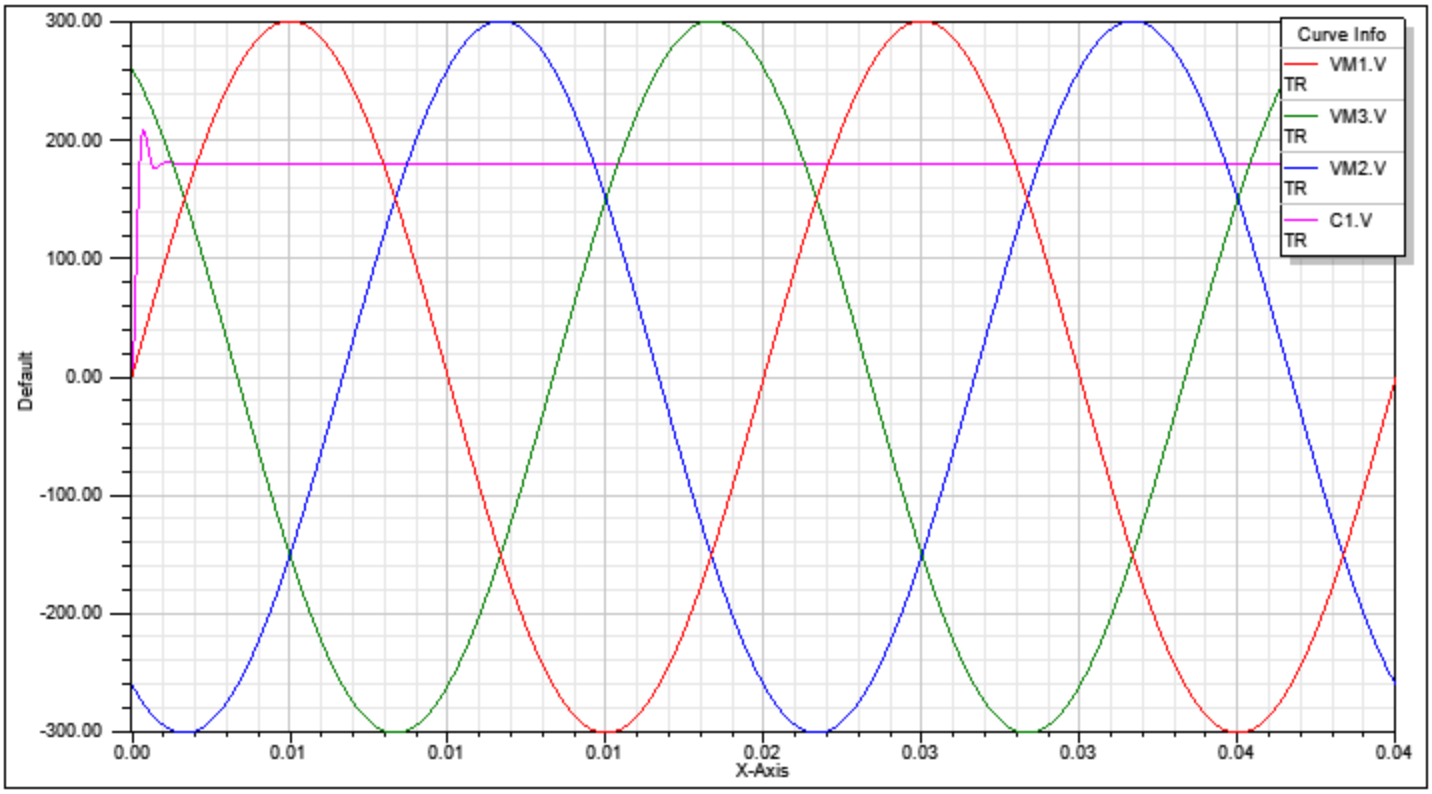

Figure 4. Simulation results-Voltage output (C1.V) and input line voltages to the rectifier (VM1.V, VM2.V, VM3.V).

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References

CSI3ph_A Current Source Inverter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

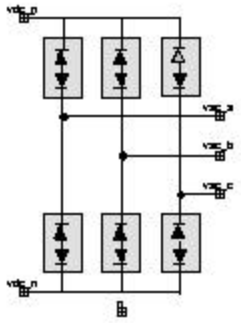

Figure 1. Component symbol

Description

This block represents the averaged level model of the three-phase Current Source Inverter (CSI). The equivalent circuit schematic is shown in Figure 2.

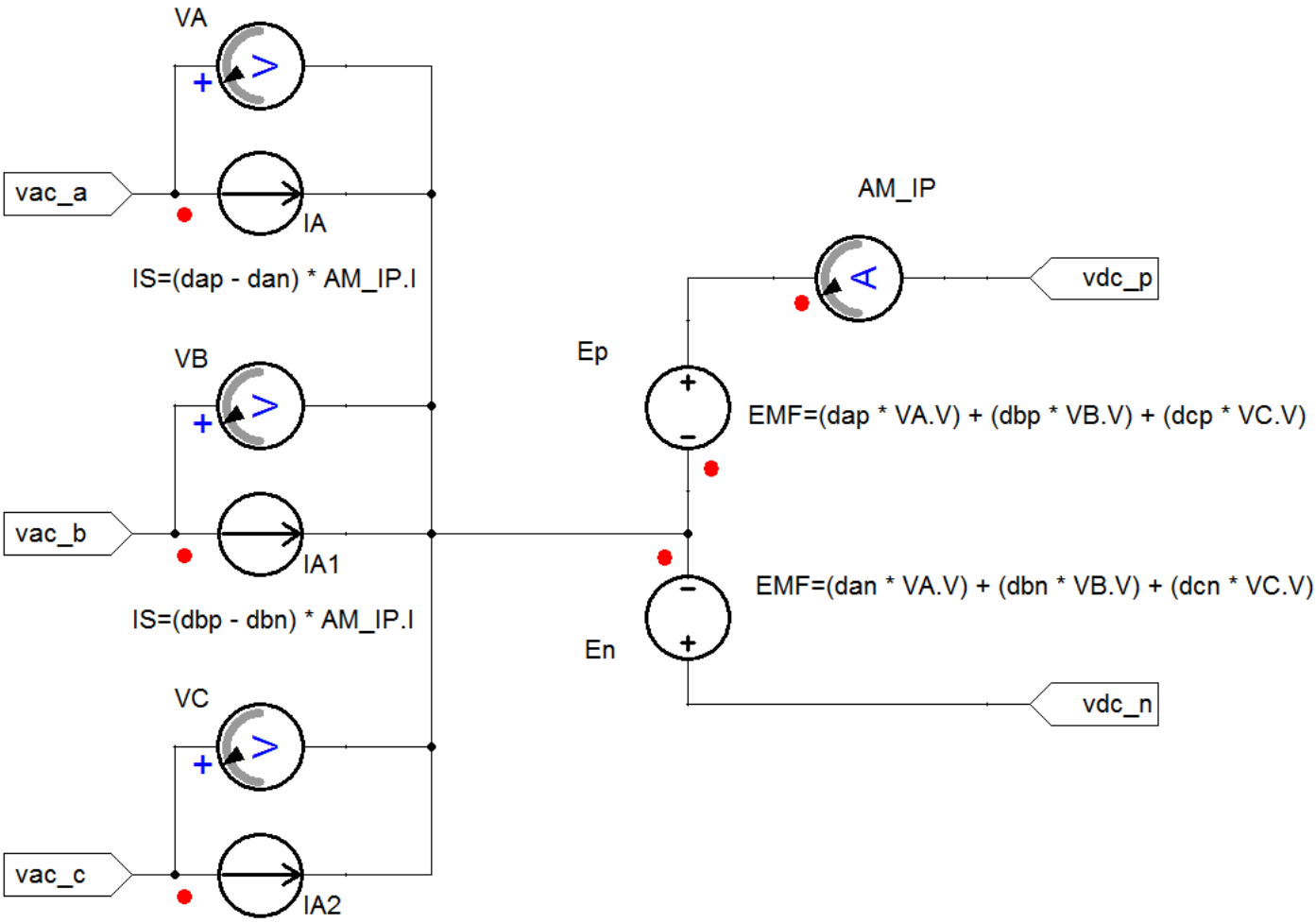

Figure 2. Equivalent Circuit Schematic

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Assumptions and Limitations

This block assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The duty cycles can be calculated by means of the following relation:

$$d_{\phi} = \frac{T_1}{T}$$

Where d_{Φ} represents the duty cycle for the considered switch, T1 is the on time of this switch in a switching period and T is the switching period.

A restriction to be taken into account is that:

$$d_{ap} + d_{bp} + d_{cp} = 1$$

$$d_{an} + d_{bn} + d_{cn} = 1$$

It means that there must be a path for the current to flow, at any time, through some of the upper switches and some of the lower switches.

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Mathematical Description

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Netlist Syntax

MODEL CSI3ph_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_a:= %0, vac_b:= %1, vdc_p:= %2, vdc_n:= %3, vac_c:= %4, n:= %5 (dap:= @dap, dbp:= @dbp, dcp:= @dcp, dan:= @dan, dbn:= @dbn, dcn:= @dcn) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_a	AC Input Phase A pin	Electrical terminal
vac_b	AC Input Phase B pin	Electrical terminal
vac_c	AC Input Phase C pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal
n	Neutral pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
dap	Duty Cycle of Upper Switch of Phase A	real	0
dbp	Duty Cycle of Upper Switch of Phase B	real	0
dcp	Duty Cycle of Upper Switch of Phase C	real	0
dan	Duty Cycle of Lower Switch of Phase A	real	0

dbn	Duty Cycle of Lower Switch of Phase B	real	0
dcn	Duty Cycle of Lower Switch of Phase C	real	0

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Example

This example is a current source inverter using averaged models. The line currents are shown in the results. The duty cycles control the energy transferred to the load.

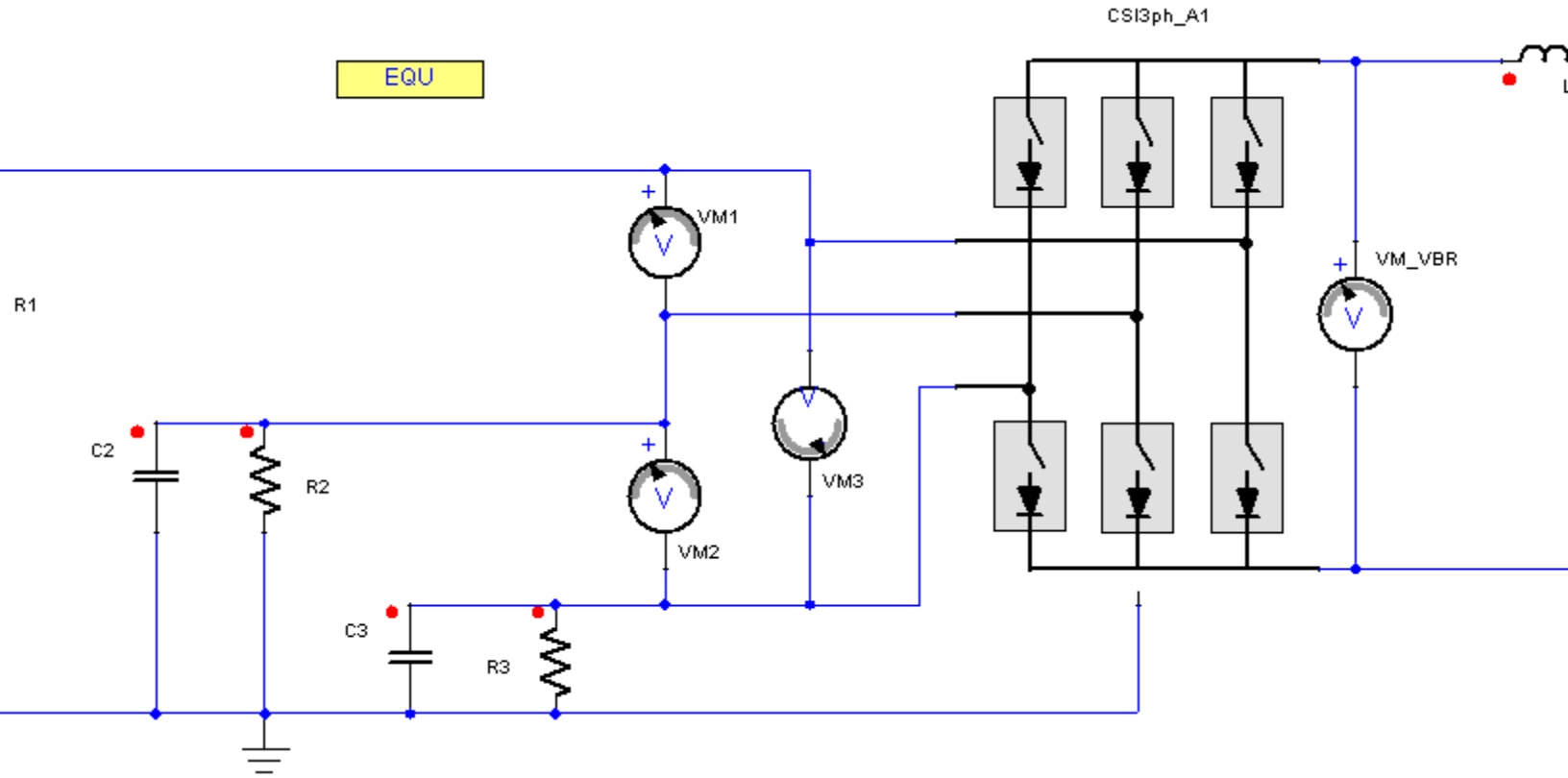

Figure 3. Application example of an Average Model of Current Source Inverter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Average Current Source Inverter	dap	dap

CSI3ph_A1		
	dbp	dbp
	dcp	dcp
	dan	dan
	dbn	dbn
	dcn	dcn
Equation Block FML1	EQU0	dap:=0.3333333333+(0.2*sin (314.1592*Time))
	EQU1	dan:=0.3333333333-(0.2*sin (314.1592*Time))
	EQU2	dbp:=0.3333333333+(0.2*sin (314.1592*Time-2.0943951))
	EQU3	dbn:=0.3333333333-(0.2*sin (314.1592*Time-2.0943951))
	EQU4	dcp:=0.3333333333+(0.2*sin (314.1592*Time+2.0943951))
	EQU5	dcn:=0.3333333333-(0.2*sin (314.1592*Time+2.0943951))
Resistor R1/R2/R3	R	10 [Ohm]
Capacitor C1/C2/C3	C	0.0001 [F]
Inductor L1	L	0.01 [H]
Voltage Source E1	EMF Value	400 [V]

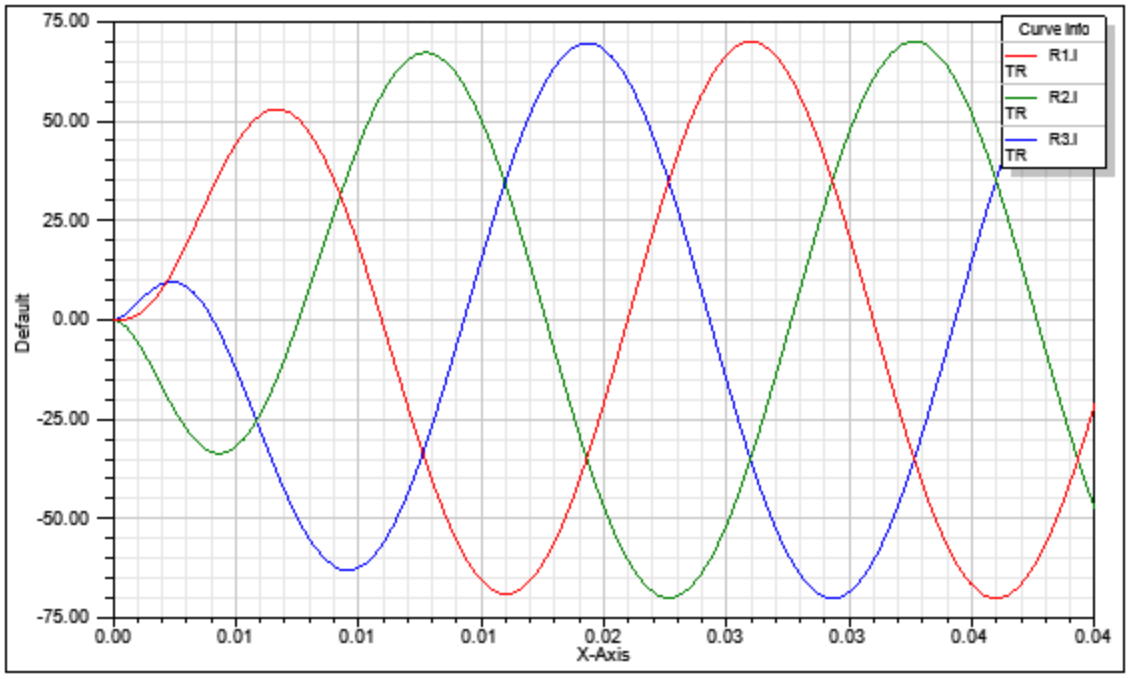

Figure 4. Simulation results-Line Currents (R1.I, R2.I, R3.I).

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References

VSI3ph_A Voltage Source Inverter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

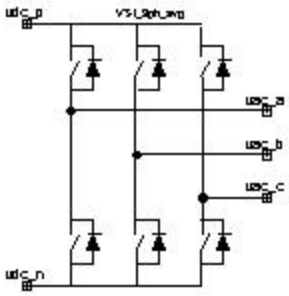

Figure 1. Component symbol

Description

This block represents the averaged level model of the three-phase VSI (Voltage Source Inverter). The equivalent circuit schematic is shown in Figure 2.

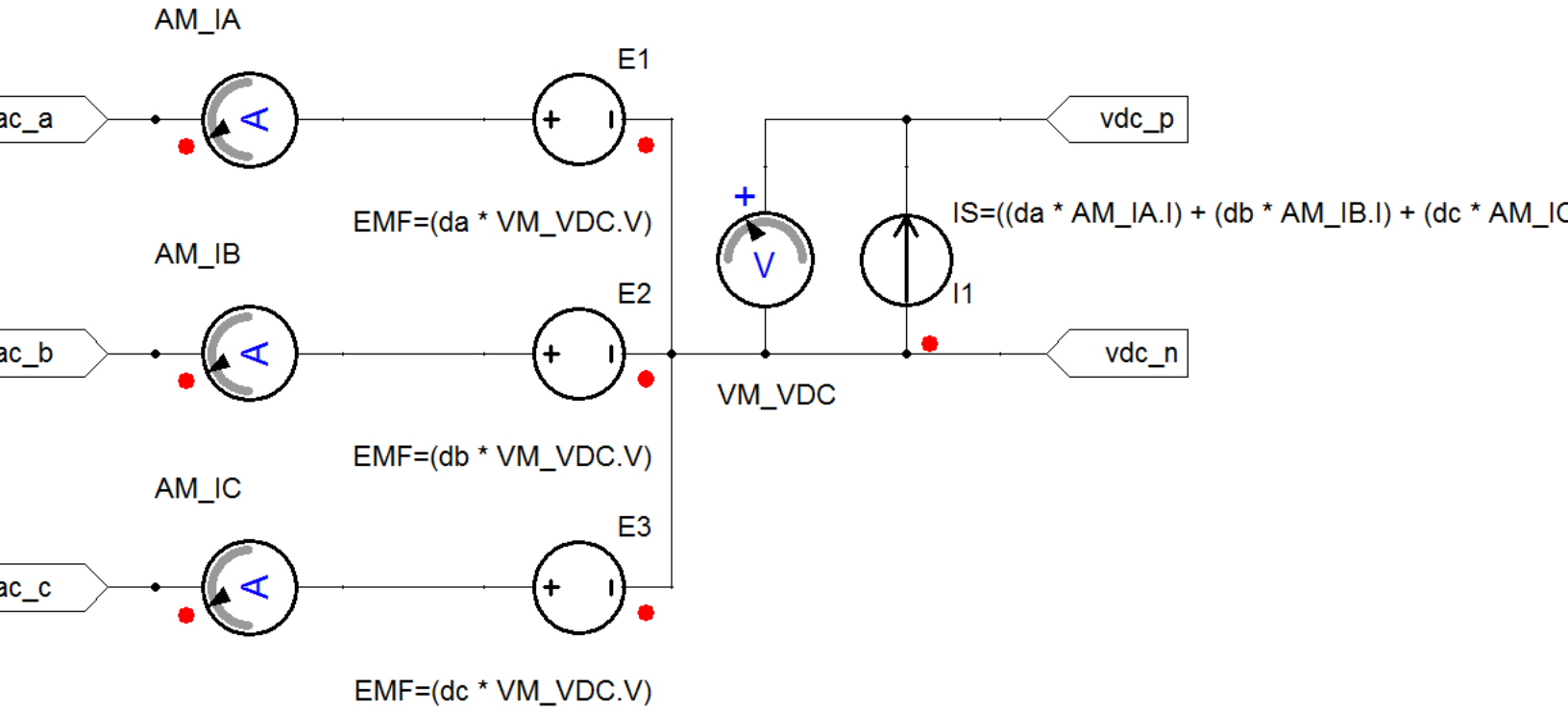

Figure 2. Equivalent Circuit Schematic

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Assumptions and Limitations

This block assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero.

The parameters to be provided to the model are:

• da duty cycle of the leg corresponding to phase A

• db duty cycle of the leg corresponding to phase B

• dc duty cycle of the leg corresponding to phase C

The duty cycles can be calculated by means of the following relation:

$$d_{\phi} = \frac{T_1}{T}$$

Where d_{Φ} represents the duty cycle for the considered leg, T1 is the on time of the upper switch in this leg and T is the switching period as shown in Figure 2:

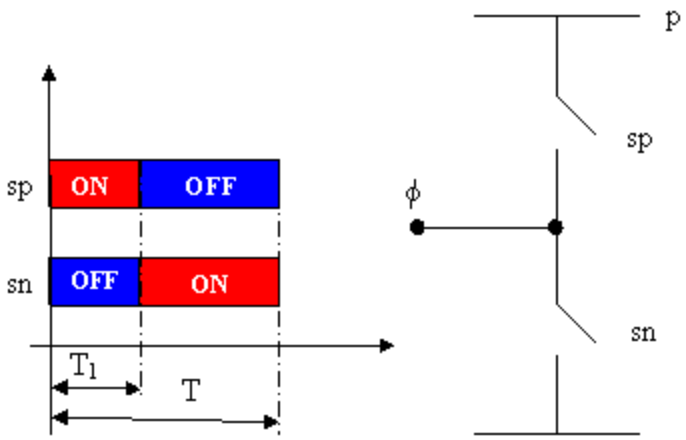

Figure 3. Switching Diagram

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Mathematical Description

Top

Netlist Syntax

MODEL VSI3ph_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vac_a:= %0, vac_ b:= %1, vdc_p:= %2, vdc_n:= %3, vac_c:= %4 (da:= @da, db:= @db, dc:= @dc) SRC: DB(Lib:- :=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vac_a	AC Input Phase A pin	Electrical terminal
vac_b	AC Input Phase B pin	Electrical terminal
vac_c	AC Input Phase C pin	Electrical terminal
vdc_p	DC Side positive pin	Electrical terminal
vdc_n	DC Side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
da	Duty Cycle of Phase A	real	0
db	Duty Cycle of Phase B	real	0
dc	Duty Cycle of Phase C	real	0

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Example

This example is a voltage source inverter using averaged models. The output voltages are shown in the results. The duty cycles control the energy transferred to the load.

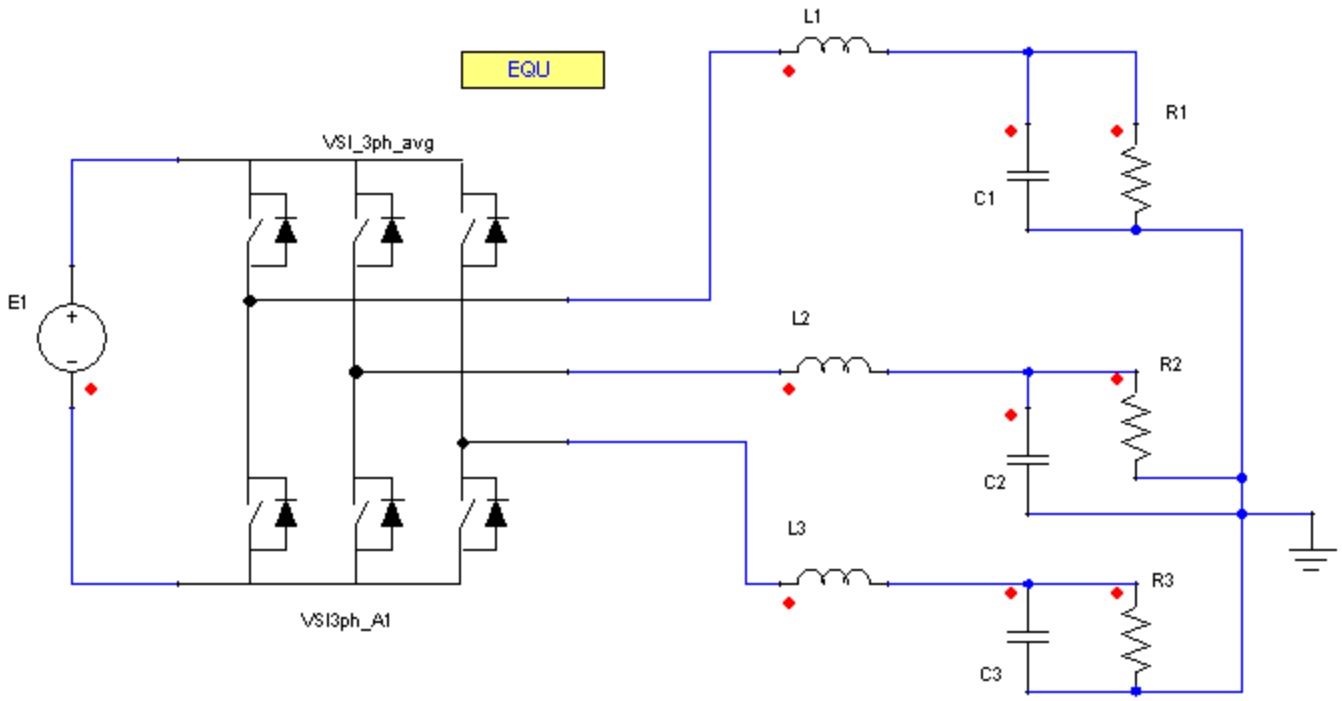

Figure 4. Application example of an Average Model of Voltage Source Inverter.

Table 3. System Parameters

Component	Parameter	Value [unit]

Average Voltage Source Inverter VSI3ph_A1	da	dap
	db	dbp
	dc	dcp
Equation Block FML1	EQU0	dc:=1+sin(314*Time)
	EQU1	db:=1+sin(314*Time-2.0944)
	EQU2	da:=1+sin (314*Time+2.0944)
Resistor R1/R2/R3	R	1 [Ohm]
Capacitor C1/C2/C3	C	0.001 [F]
Inductor L1/L2/L3	L	0.01 [H]
Voltage Source E1	EMF Value	400 [V]

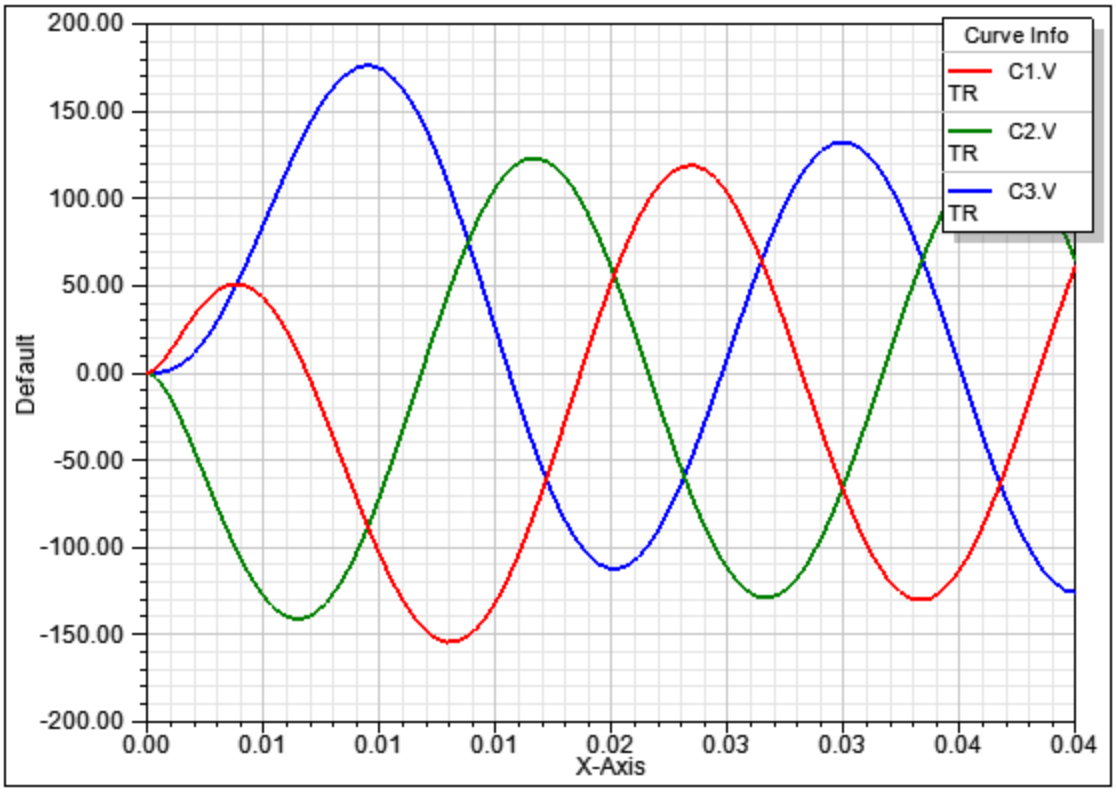

Figure 5. Simulation results-Voltage outputs (C1.V, C2.V, C3.V).

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References

Advanced Three-Phase dq

The components of this section are average large-signal models of the most common three-phase converters. There are two models for each converter:

The rotating coordinates (dq) models also allow AC analysis of the converters, a powerful tool for control design.

- Boost (Boost3ph_DQ)
- Buck (Buck3ph_DQ)
- Current Source Inverter (CSI3ph_DQ)
- Sinusoidal PWM (SPWM)
- Voltage Source Inverter (VSI3ph_DQ)

See also:

- Advanced Three-Phase Average

Boost DQ

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

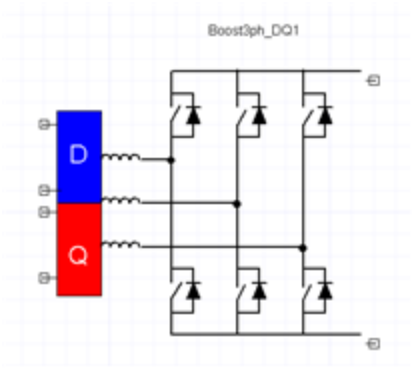

Figure 1. Component symbol

Description

This block represents the dq averaged model of the three-phase boost converter. It assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero.

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Assumptions and Limitations

Top

Mathematical Description

The model implements the following differential equations:

$$3 \cdot L \cdot \frac{di_d}{dt} = v_d + 3 \cdot \omega L \cdot i_q - v_0 \cdot d_d$$

$$3 \cdot L \cdot \frac{di_q}{dt} = v_d - 3 \cdot \omega L \cdot i_d - v_0 \cdot d_q$$

$$i_0 = d_d i_d + d_q \cdot i_q$$

Where:

L is the line inductance of the boost converter

v_d is the d coordinates input voltage

v_q is the q coordinates input voltage

i_d is the d coordinates input current

i_q is the q coordinates input current

ω is the pulsating frequency

d_d is the d coordinates duty cycle

d_q is the q coordinates duty cycle

i_0 is the dc output current

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Netlist Syntax

MODEL Boost3ph_DQ ?InstanceName(@InstanceName):(@(Refbase)@(ID)) v_dp:= %0, v_dn:= %1, v_qp:= %2, v_qn:= %3, vdc_p:= %4, vdc_n:= %5 (dd:= @dd, dq:= @dq, frequency:= @frequency, L:= @L) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
v_dp	d channel positive pin	Electrical terminal

v_dn	d channel negative pin	Electrical terminal
v_qp	q channel positive pin	Electrical terminal
v_qn	q channel negative pin	Electrical terminal
vdc_p	DC side positive pin	Electrical terminal
vdc_n	DC side negative pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
frequency	Rotating Reference Frequency	real	50 [Hz]
L	Line Inductance	real	0.001 [H]
dd	d Channel Duty Cycle	real	0
dq	q Channel Duty Cycle	real	0

Top

Example

This example illustrates the Three-Phase Boost converter using averaged dq model. The results show the output voltage and the step on the control signal. The duty cycles controls the energy transfered to the load.

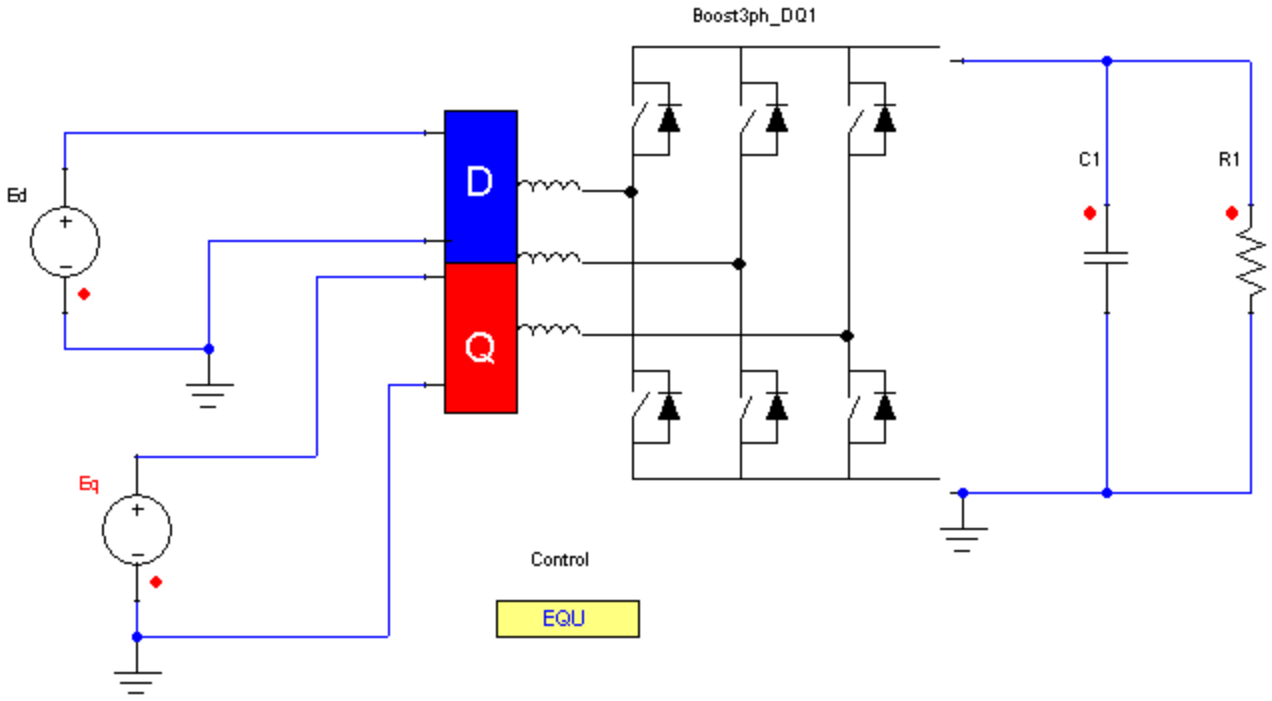

Figure 2. Application examples of the Three-Phase Boost converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Three-Phase Boost converter BOOST3PH_DQ1	dd	dd
	dq	dq
Equation Block CONTROL	EQU0	dd:=0.4 + 0.2* (Time > 0.1)
	EQU1	dq:=0
Resistor R1	R	1 [Ohm]
Capacitor C1	C	0.001 [F]
Voltage Source Ed	EMF Value	400*3/2 [V]
Voltage Source Eq	EMF Value	400 [V]

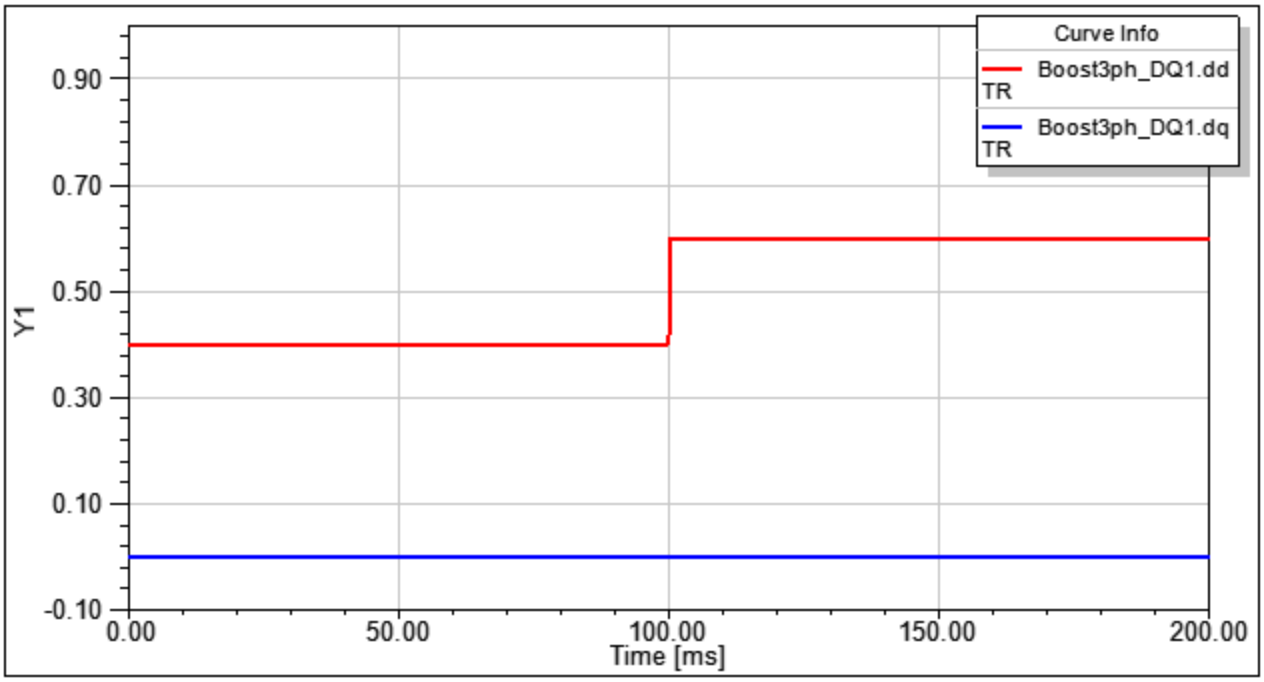

Figure 3. Simulation results-DQ duty cycles.

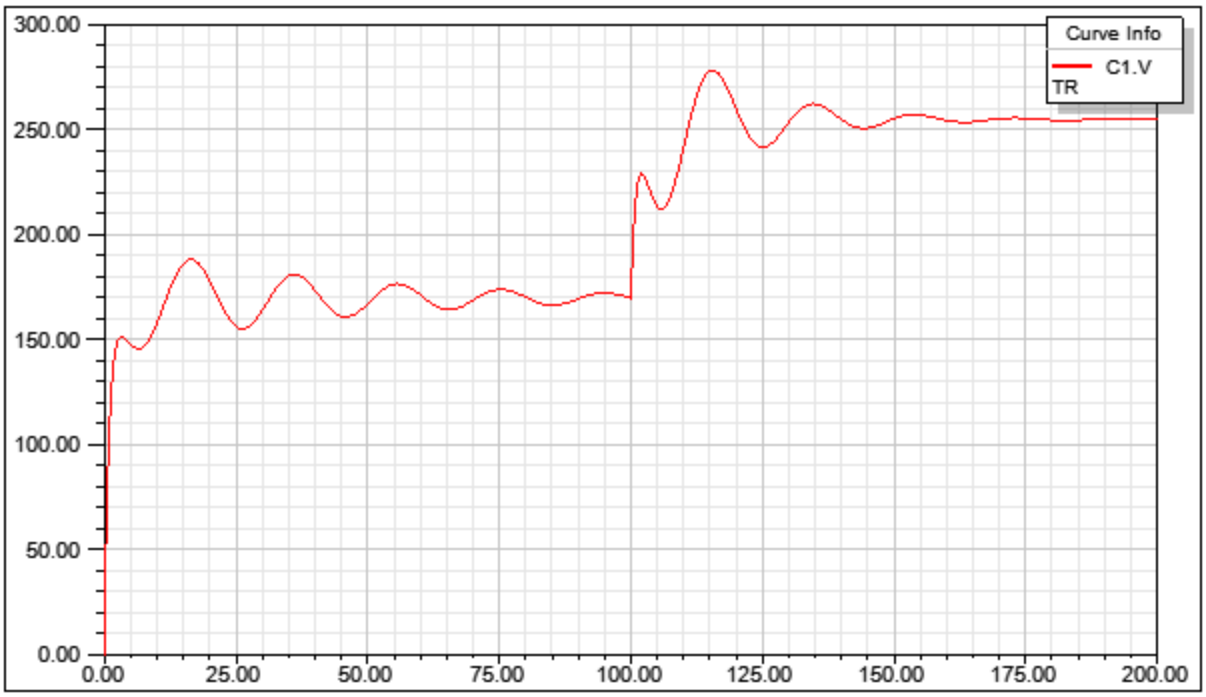

Figure 4. Simulation results-voltage output (C1.V).

Top

References

Buck DQ

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

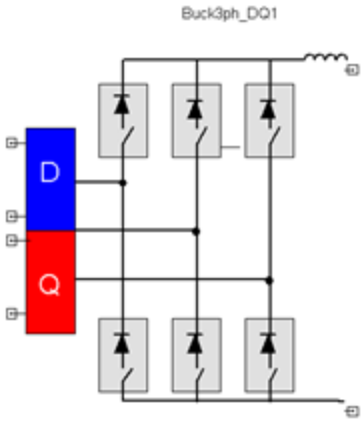

Figure 1. Component symbol

Description

This block represents the dq averaged model of the three-phase buck converter. It assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero.

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Assumptions and Limitations

Top

Mathematical Description

The model implements the following differential equations:

$$i_d = d_d \cdot i_L$$

$$i_q = d_q \cdot i_L$$

$$L \cdot \frac{di_L}{dt} = v_d \cdot d_d + v_q \cdot d_q - v_0$$

Where:

L is the dc inductance of the buck converter

v_d is the d coordinates input voltage

v_q is the q coordinates input voltage

i_d is the d coordinates input current

i_q is the q coordinates input current

ω is the pulsating frequency

d_d is the d coordinates duty cycle

d_q is the q coordinates duty cycle

v_0 is the dc output voltage

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Netlist Syntax

MODEL Buck3ph_DQ ?InstanceName(@InstanceName):(@(Refbase)@(ID)) v_dp:= %0, v_dn:= %1, v_qp:= %2, v_qn:= %3, vdc_p:= %4, vdc_n:= %5 (dd:= @dd, dq:= @dq, frequency:= @frequency, L:= @L) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
v_dp	d channel positive pin	Electrical terminal

v_dn	d channel negative pin	Electrical terminal
v_qp	q channel positive pin	Electrical terminal
v_qn	q channel negative pin	Electrical terminal
vdc_p	DC side positive pin	Electrical terminal
vdc_n	DC side negative pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
frequency	Rotating Reference Frequency	real	50 [Hz]
L	Line Inductance	real	0.001 [H]
dd	d Channel Duty Cycle	real	0
dq	q Channel Duty Cycle	real	0

Top

Example

This example illustrates the Three-Phase Buck converter using averaged dq model. The results show the output voltage and the step on the control signal. The duty cycles controls the energy transfered to the load.

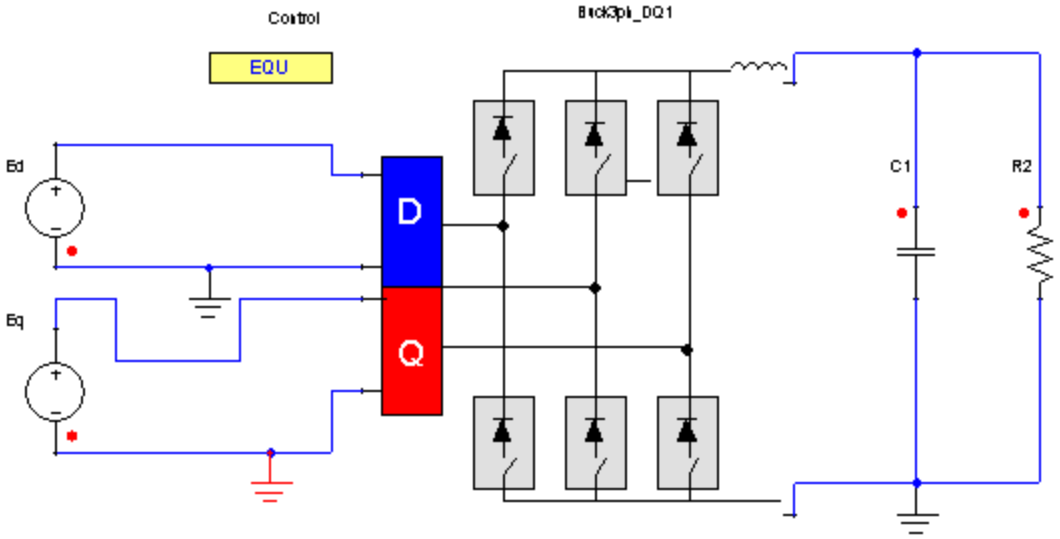

Figure 2. Application examples of the Three-Phase Buck converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Three-Phase Buck converter BUCK3PH_DQ1	dd	dd
	dq	dq
Equation Block CONTROL	EQU0	dd:=0.4 + 0.2* (Time > 0.1)
	EQU1	dq:=0
Resistor R2	R	1 [Ohm]
Capacitor C1	C	0.001 [F]
Voltage Source Ed	EMF Value	400*3/2 [V]
Voltage Source Eq	EMF Value	400 [V]

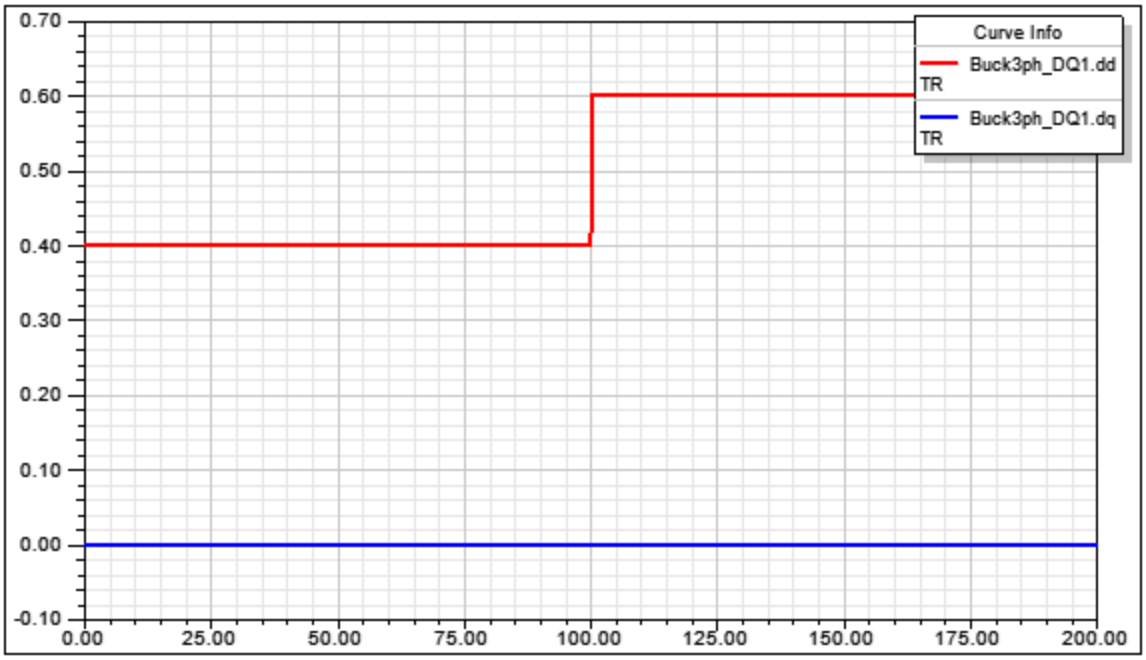

Figure 3. Simulation results-DQ duty cycles.

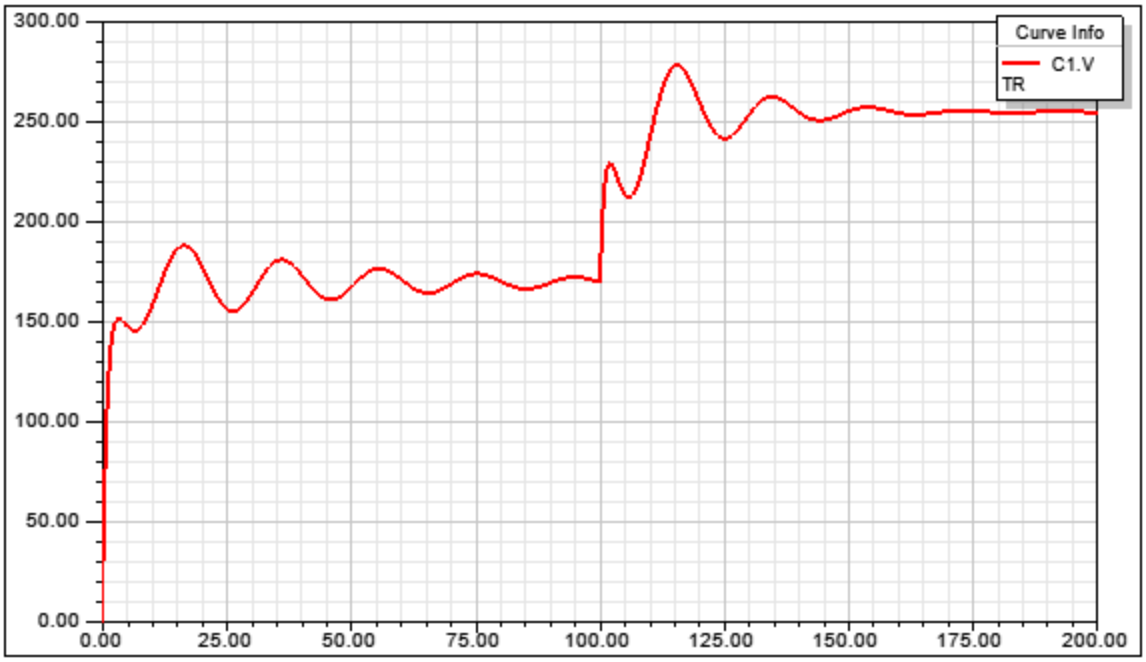

Figure 4. Simulation results-voltage output (C1.V).

Top

References

Current Source Inverter DQ

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

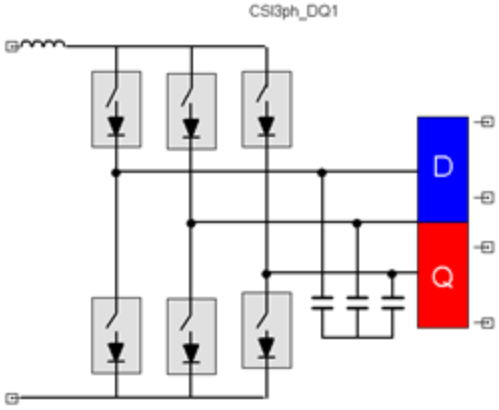

Figure 1. Component symbol

Description

This block represents the dq averaged model of the three-phase Current Source Inverter. It assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero.

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Assumptions and Limitations

Top

Mathematical Description

The model implements the following differential equations:

$$L \cdot \frac{di_L}{dt} = v_g - (v_d \cdot d_d + v_q \cdot d_q)$$

$$C \cdot \frac{dv_d}{dt} = d_d \cdot i_L + \omega \cdot C \cdot v_q - i_{0d}$$

$$C \cdot \frac{dv_q}{dt} = d_q \cdot i_L - \omega \cdot C \cdot v_q - i_{0q}$$

Where:

L is the dc inductance

C is the capacitance per phase

v_d is the d coordinates output voltage

v_q is the q coordinates output voltage

i_{0d} is the d coordinates output current

i_{0q} is the q coordinates output current

ω is the pulsating frequency

d_d is the d coordinates duty cycle

d_q is the q coordinates duty cycle

i_L is the dc input current

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Netlist Syntax

MODEL CSI3ph_DQ ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vdc_p:= %0, vdc_n:= %1, v_dp:= %2, v_dn:= %3, v_qp:= %4, v_qn:= %5 (frequency:= @frequency, L:= @L, dd:= @dd, dq:= @dq, L_IC:= @L_IC, C:= @C, Cd_IC:= @Cd_IC, Cq_IC:= @Cq_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
v_dp	d channel positive pin	Electrical terminal
v_dn	d channel negative pin	Electrical terminal
v_qp	q channel positive pin	Electrical terminal
v_qn	q channel negative pin	Electrical terminal
vdc_p	DC side positive pin	Electrical terminal
vdc_n	DC side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
frequency	Rotating Reference Frequency	real	50 [Hz]
L	Line Inductance	real	0.001 [H]
dd	d Channel Duty Cycle	real	0.5
dq	q Channel Duty Cycle	real	0

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Example

This example illustrates the Three-Phase CSI converter using averaged dq model. The results show the output voltage and the step on the control signal. The duty cycles controls the energy transfered to the load.

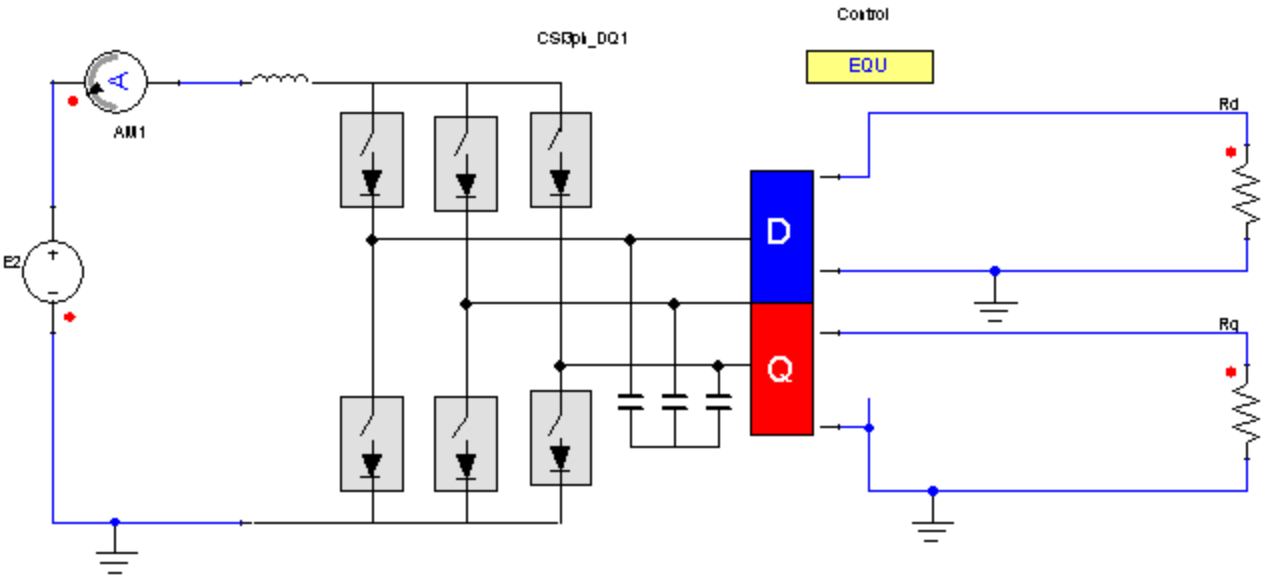

Figure 2. Application examples of the Three-Phase CSI converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Three-Phase CSI converter CSI3PH_DQ1	dd	dd
	dq	dq
Equation Block CONTROL	EQU0	dd:=0.4 + 0.2* (Time > 0.1)
	EQU1	dq:=0
Resistor Rd/Rq	R	1 [Ohm]
Voltage Source E2	EMF Value	400 [V]

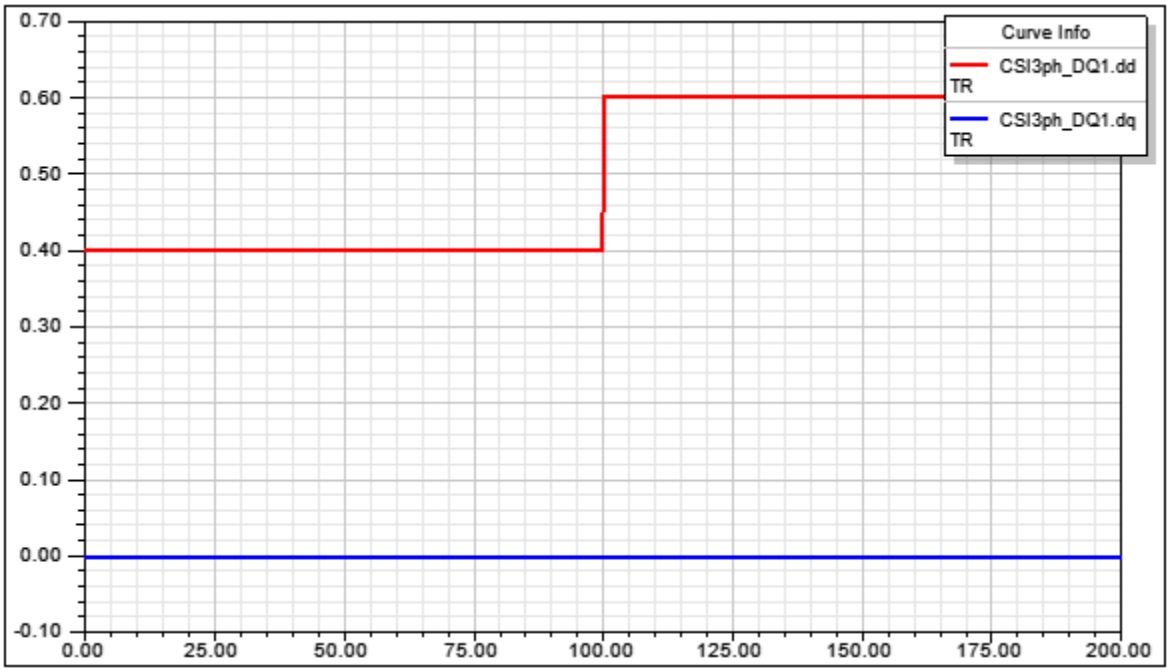

Figure 3. Simulation results-DQ duty cycles.

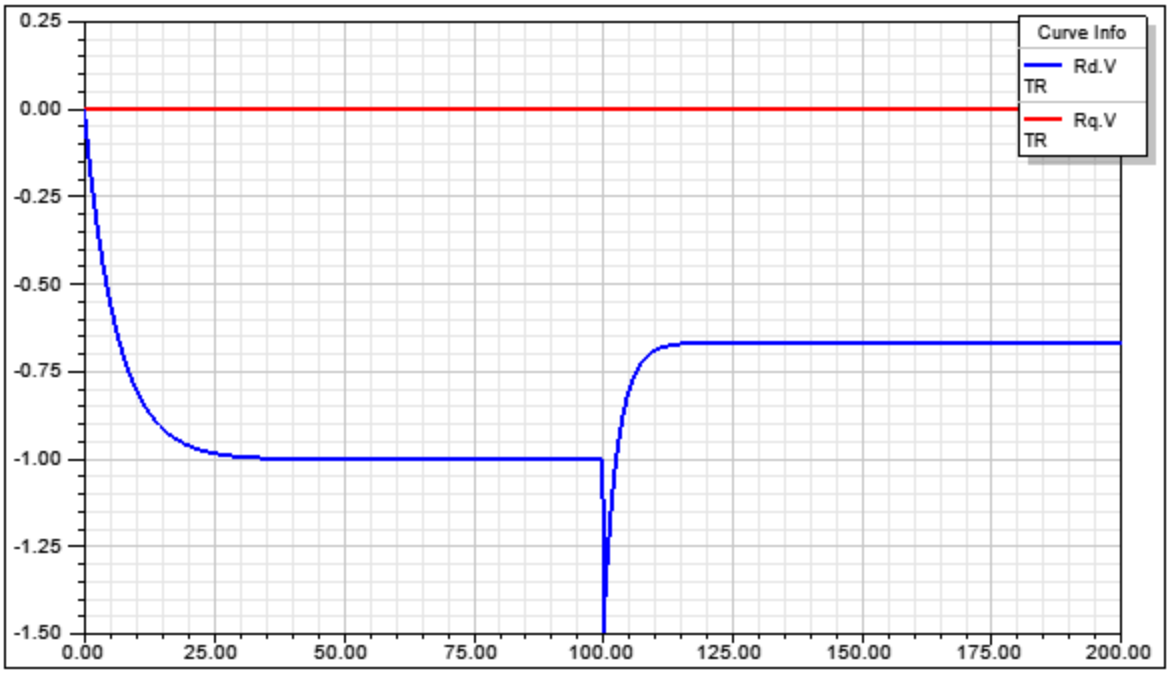

Figure 4. Simulation results-voltage outputs (Rd.V, Rq.V).

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References

Sinusoidal PWM

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

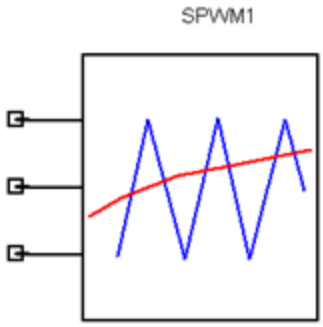

Figure 1. Component symbol

Description

This block represents the averaged model of a Sinusoidal PWM. It assumes that the carrier frequency is much higher than the modulating signals.

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Assumptions and Limitations

Top

Mathematical Description

The model implements the following equations:

$$d_j = \begin{cases} \dfrac{v_{jref}(t)}{V_{carr}} \; if \left| v_{jref}(t) \right| < V_{carr} \\ \operatorname{sgn}(v_{jref}(t)) \; \text{if} \left| v_{jref}(t) \right| > V_{carr} \end{cases}$$

Where:

d_j is the duty cycle of phase j (j=A, B, or C)

v_{jref} is the modulating voltage of phase j

V_{carr} is the amplitude of the carrier signal

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Netlist Syntax

MODEL SPWM ?InstanceName(@InstanceName):(@(Refbase)@(ID)) Varef:= %0, Vbref:= %1, Vcref:= %2 (Vcarr:= @Vcarr) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
Varef	Modulating voltage of phase A	Electrical terminal
Vbref	Modulating voltage of phase B	Electrical terminal
Vcref	Modulating voltage of phase C	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Vcarr	Amplitude of the Carrier	real	1 [V]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
da	Duty cycle for phase A	Output	real
db	Duty cycle for phase B	Output	real
dc	Duty cycle for phase C	Output	real

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Example

This example illustrates a Voltage Source Inverter with Sinusoidal Pulse Width Modulation and an inductive load. The simulation uses an averaged model of the Voltage Source Inverter. The amplitude modulation index is defined by ma.

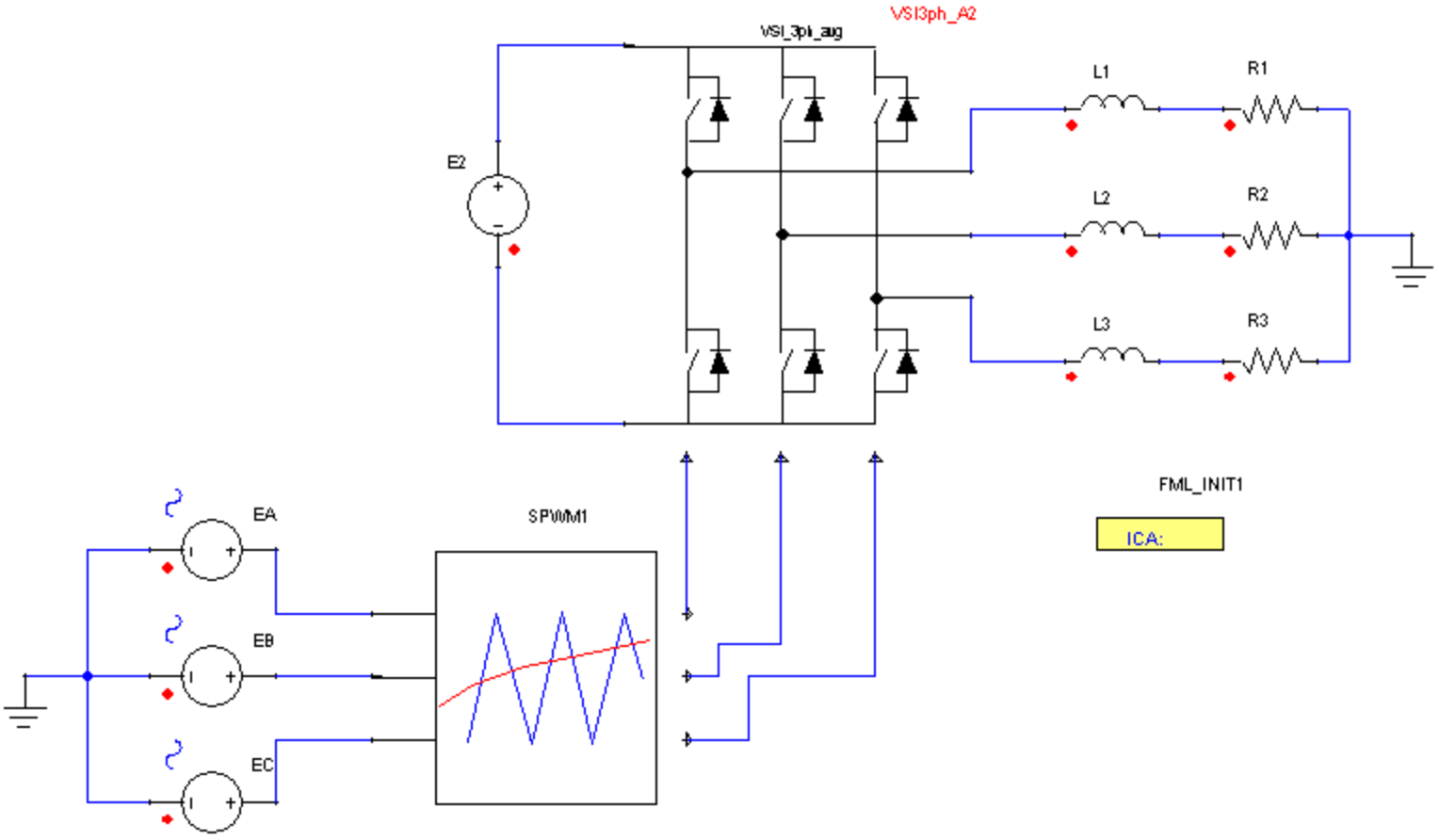

Figure 2. Application examples of the Sinusoidal PWM model.

Table 3. System Parameters

Component	Parameter	Value [unit]
Three-Phase VSI converter VSI3PH_A2	da	SPWM1.da
	db	SPWM1.db
	dc	SPWM1.dc
Initial Values FML_INIT1	EQU0	ma:=0.8
Resistor R1/R2/R3	R	1 [Ohm]
Inductor L1/L2/L3	L	0.01 [H]
Voltage Source E2	EMF Value	400 [V]
Voltage Source (Sinusoidal) EA/EB/EC	AMPL	ma [V]
	FREQ	50 [Hz]
	Phase	0/-120/-240 [Deg]
Sinusoidal PWM SPWM1	Vcarr	1

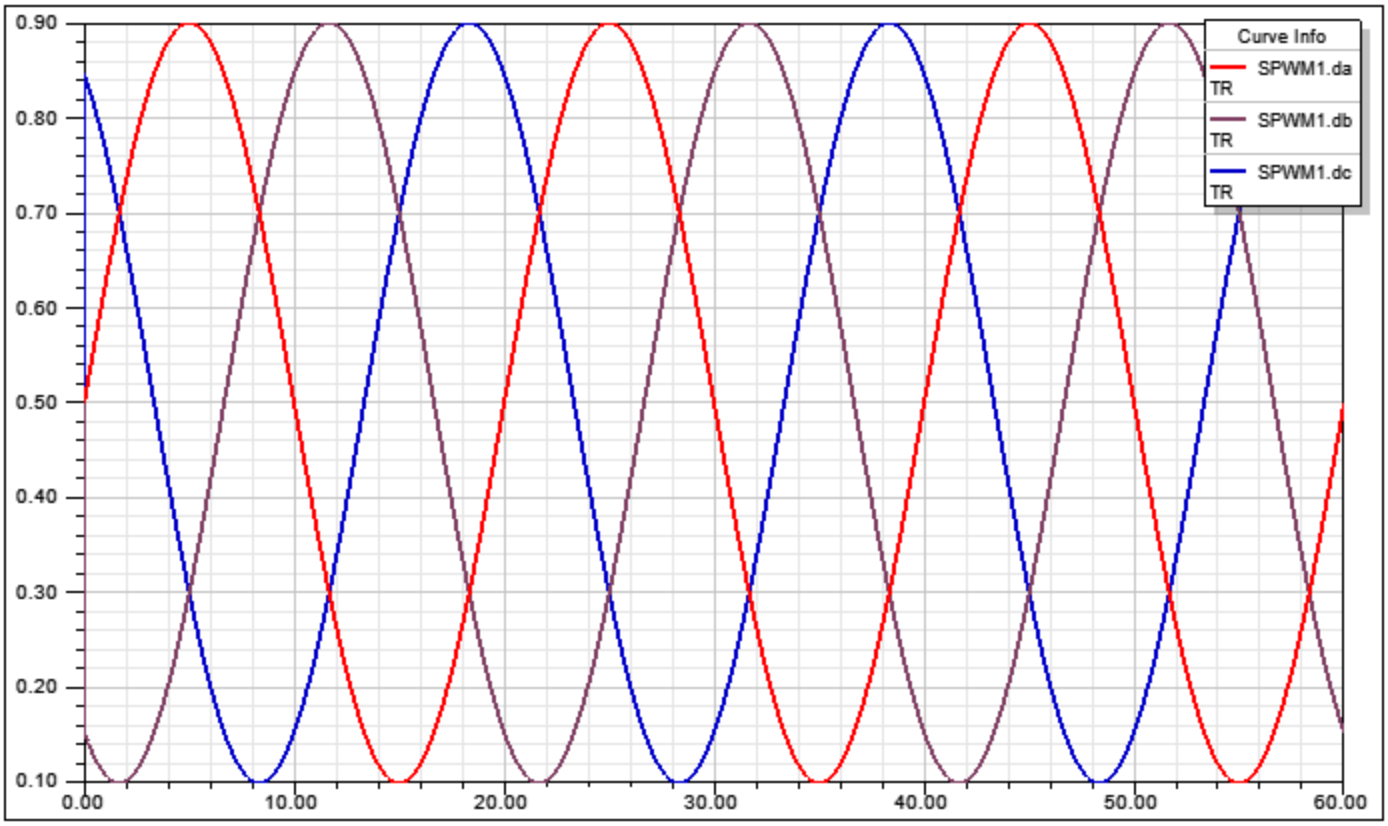

Figure 3. Simulation results-Duty cycles (SPWM1.da, SPWM1.db, SPWM1.dc).

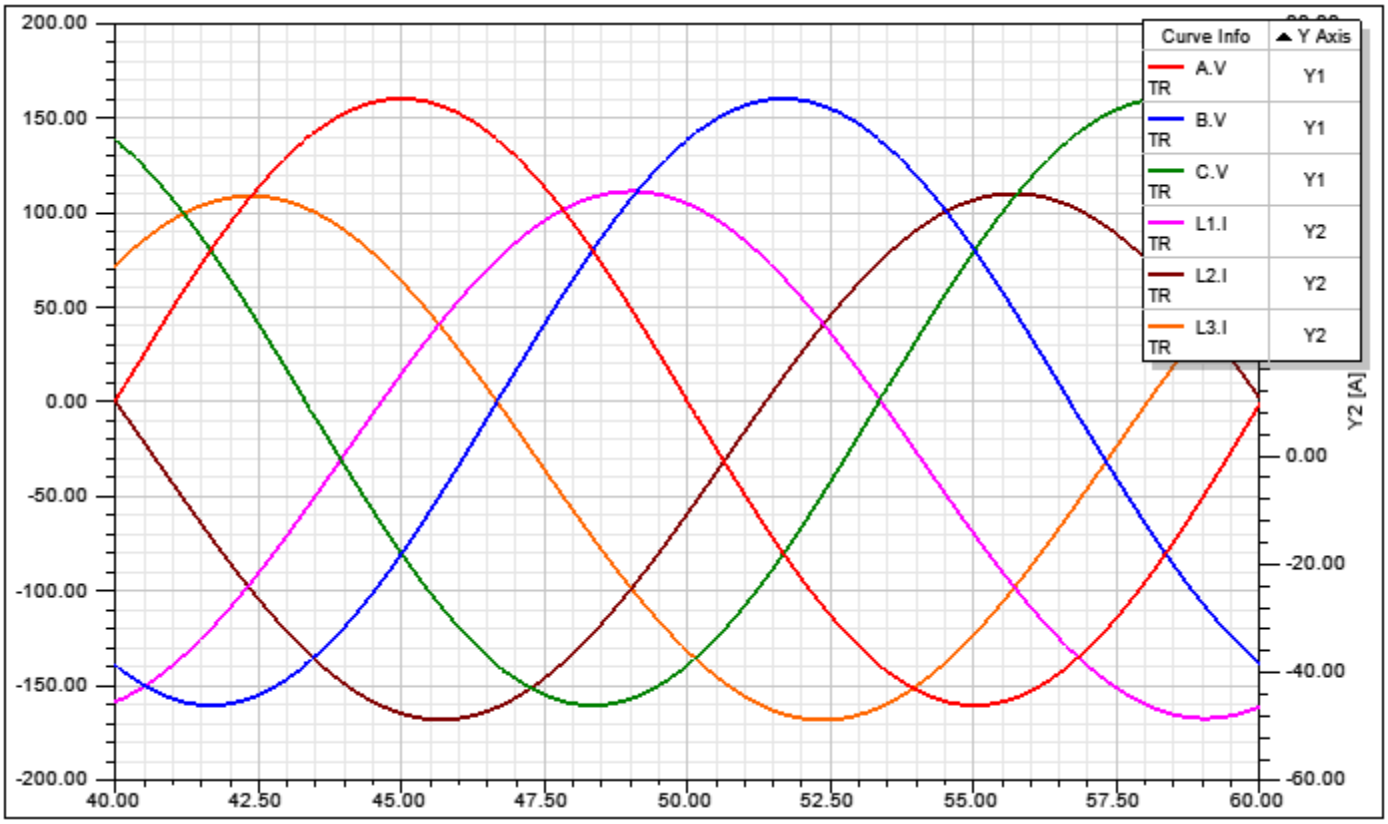

Figure 4. Simulation results-Phase neutral voltages (A.V, B.V, C.V) and phase currents (L1.I, L2.I, L3.I).

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References

Voltage Source Inverter DQ

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

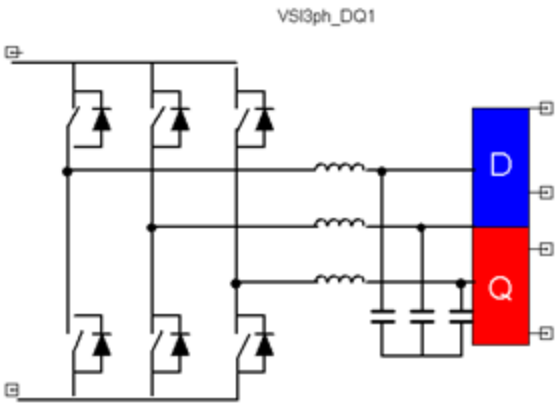

Figure 1. Component symbol

Description

This block represents the dq averaged model of the three-phase Voltage Source Inverter. It assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero.

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Assumptions and Limitations

Top

Mathematical Description

The model implements the following differential equations:

$$i_d = d_d \cdot i_{Ld}$$

$$i_q = d_q \cdot i_{Lq}$$

$$3 \cdot L \cdot \frac{di_{Ld}}{dt} = v_g \cdot d_d - v_{0d}$$

$$3 \cdot L \cdot \frac{di_{Lq}}{dt} = v_g \cdot d_q - v_{0q}$$

$$C \cdot \frac{dv_d}{dt} = i_{Ld} + \omega \cdot C \cdot v_q - i_{0d}$$

$$C \cdot \frac{dv_q}{dt} = i_{Lq} - \omega \cdot C \cdot v_q - i_{0q}$$

Where:

L is the inductance per phase

C is the capacitance per phase

v_d is the d coordinates output voltage

v_q is the q coordinates output voltage

i_{Ld} is the d coordinates inductor current

i_{Lq} is the q coordinates inductor current

ω is the pulsating frequency

d_d is the d coordinates duty cycle

d_q is the q coordinates duty cycle

i_{0d} is the d coordinates output current

i_{0q} is the q coordinates output current

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Netlist Syntax

MODEL VSI3ph_DQ ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vdc_p:= %0, vdc_n:= %1, v_dp:= %2, v_dn:= %3, v_qp:= %4, v_qn:= %5 (frequency:= @frequency, L:= @L, C:= @C, dd:= @dd, dq:= @dq, Cd_IC:= @Cd_IC, Cq_IC:= @Cq_IC, Ld_IC:= @Ld_IC, Lq_IC:= @Lq_IC) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
v_dp	d channel positive pin	Electrical terminal
v_dn	d channel negative pin	Electrical terminal
v_qp	q channel positive pin	Electrical terminal
v_qn	q channel negative pin	Electrical terminal
vdc_p	DC side positive pin	Electrical terminal
vdc_n	DC side negative pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
frequency	Rotating Reference Frequency	real	50 [Hz]
L	Line Inductance	real	0.001 [H]
dd	d Channel Duty Cycle	real	0.5
dq	q Channel Duty Cycle	real	0

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Example

This example illustrates the Three-Phase VSI converter using averaged dq model. The results show the output dq voltage and the step on the control signal. The duty cycles controls the energy transfered to the load.

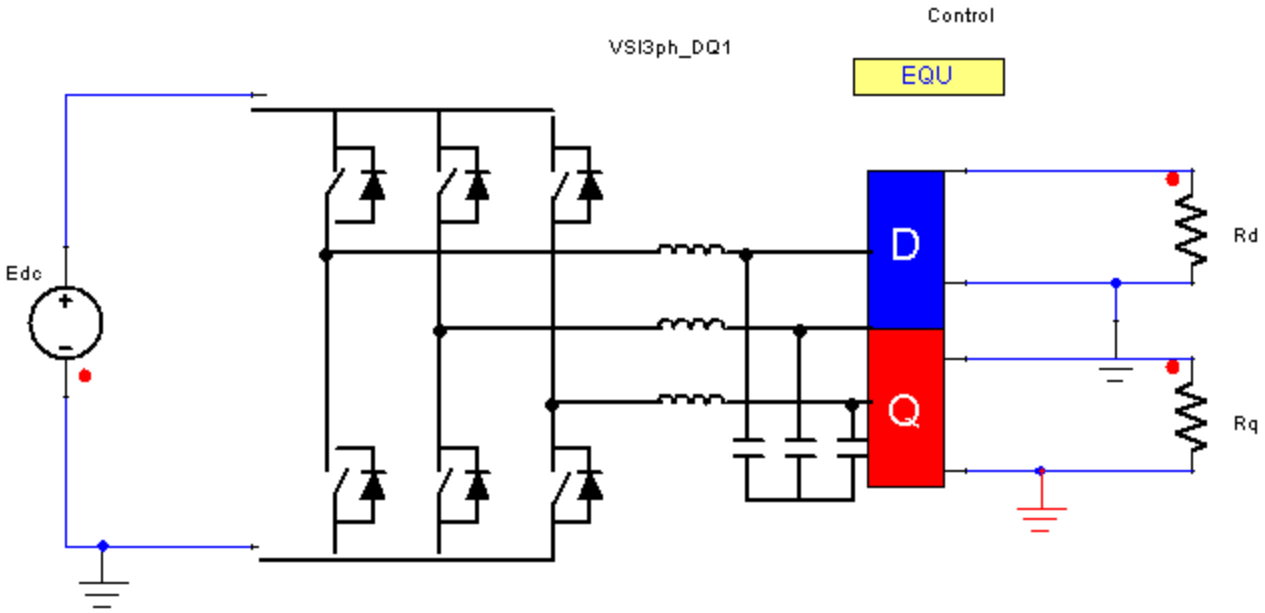

Figure 2. Application examples of the Three-Phase VSI converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Three-Phase VSI converter VSI3PH_DQ1	dd	dd
	dq	dq
Equation Block CONTROL	EQU0	dd:=0.4 + 0.2* (Time > 0.1)
	EQU1	dq:=0
Resistor Rd/Rq	R	1 [Ohm]
Voltage Source E_{dc}	EMF Value	400 [V]

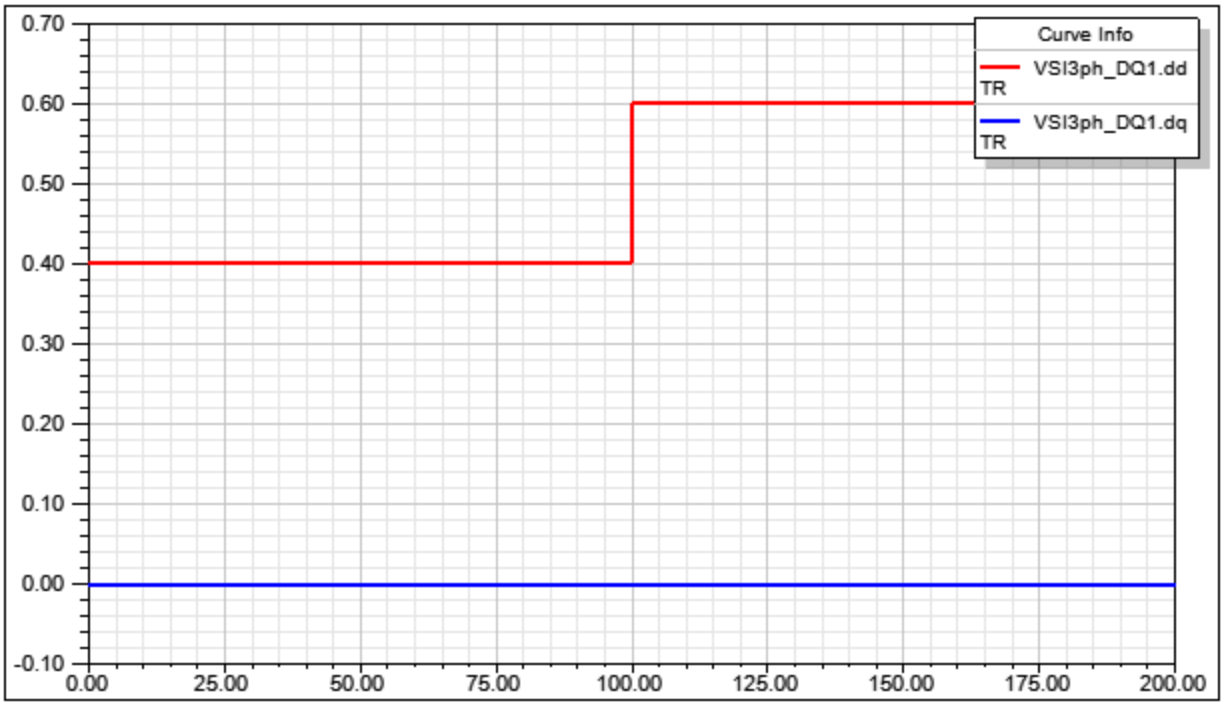

Figure 3. Simulation results-DQ duty cycles.

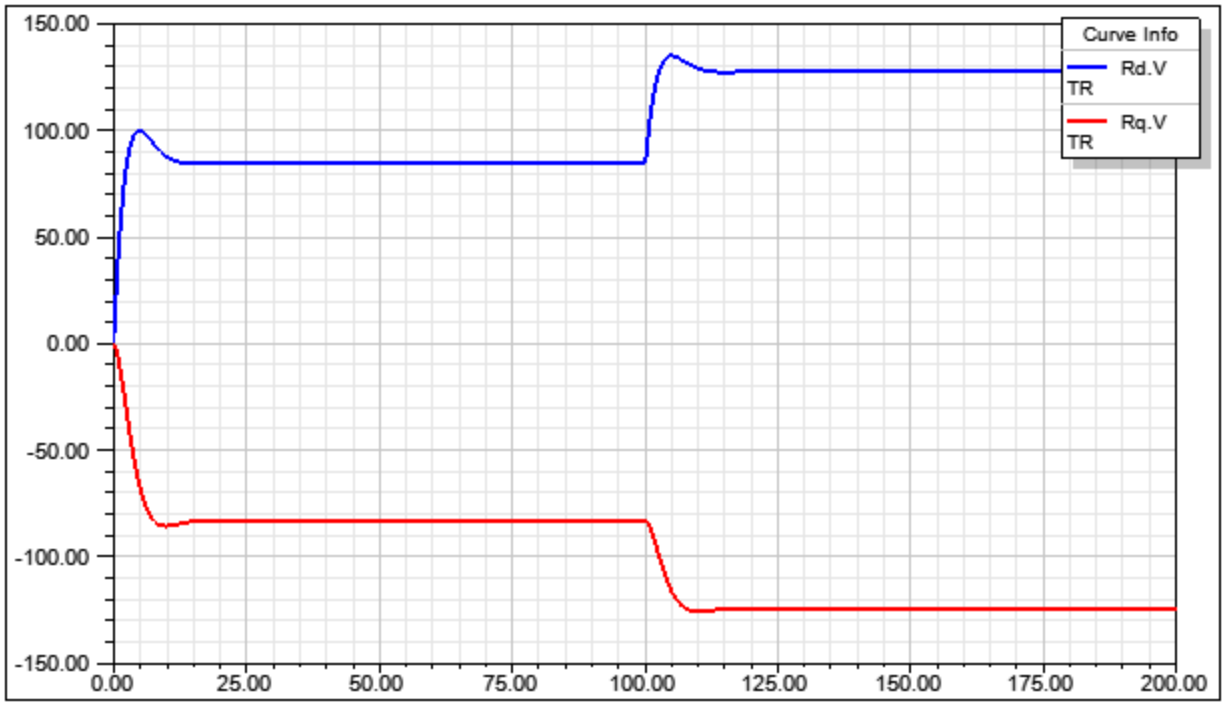

Figure 4. Simulation results-voltage outputs (Rd.V, Rq.V).

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References

Advanced Transformation

- Inverse Park Transformation (T_abc_dqz)
- Park Transformation (T_dqz_abc)

T_abc_dqz Inverse Park Transformation

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

Figure 1. Component symbol

Description

This block performs an inverse Park transformation.

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Assumptions and Limitations

Top

Mathematical Description

The block performs the inverse Park's transformation given by:

$$T_{abc\_dqz} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & \frac{1}{\sqrt{2}} \\ \cos\left(\omega t - \frac{2}{3}\pi\right) & \sin\left(\omega t - \frac{2}{3}\pi\right) & \frac{1}{\sqrt{2}} \\ \cos\left(\omega t + \frac{2}{3}\pi\right) & \sin\left(\omega t + \frac{2}{3}\pi\right) & \frac{1}{\sqrt{2}} \end{bmatrix}$$

so that:

$$X_{abc} = T_{abc\_dqz} \cdot X_{dqz}$$

where:

$$\omega = 2 \cdot \pi \cdot frequency$$

$$X_{dqz} = \begin{bmatrix} X_d \\ X_q \\ X_z \end{bmatrix}$$

$$X_{abc} = \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix}$$

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Netlist Syntax

MODEL T_abc_dqz ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (d:= @d, q:= @q, frequency:= @frequency, z:= @z) SRC: DB(Lib:=@ModelLibraryName) ;

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Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
frequency	Frequency	real	50 [Hz]

d	D Component Input	real	0
q	Q Component Input	real	0
z	Z Component Input	real	0

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
a	A component output	Output	real
b	B component output	Output	real
c	C component output	Output	real

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Example

This example a Park and Inverse Park Transformation. The currents through the resistors are input to the Park transformation where they are converted to Direct, Quadrature and Homopolar currents. These currents are in turn transformed by the Inverse Park transformation back into a,b, and c phase currents.

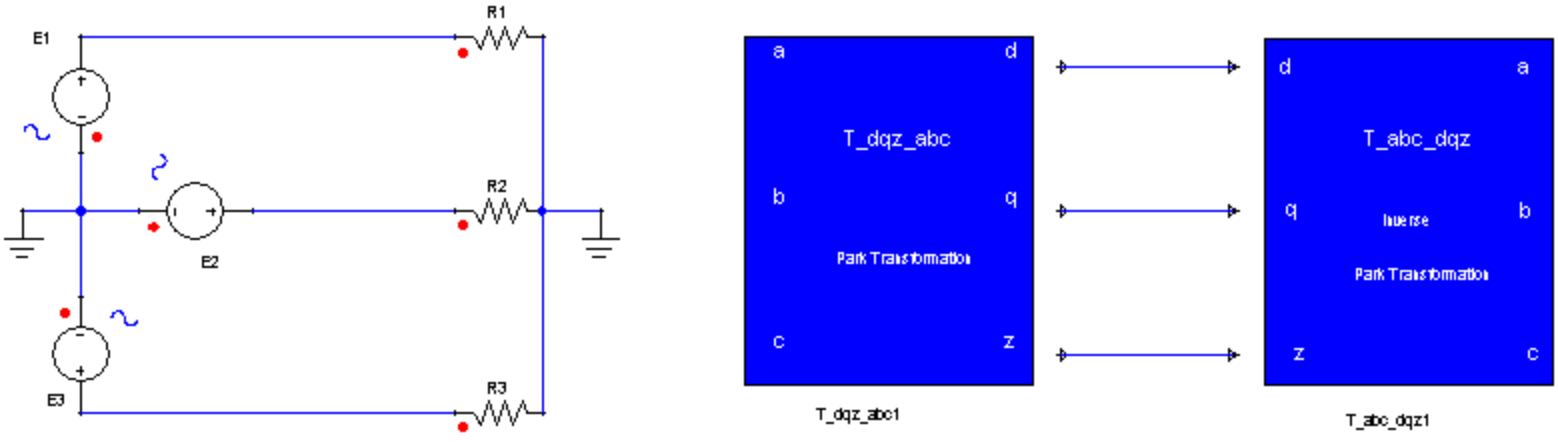

Figure 2. Application example of the Park and Inverse Park Transformation

Table 3. System Parameters

Component	Parameter	Value [unit]
Park Transformation T_DQZ_ABC1	a	R1.I
	b	R2.I
	c	R3.I
Inverse Park Transformation T_ABC_DQZ1	d	T_dqz_abc1.d
	q	T_dqz_abc1.q
	z	T_dqz_abc1.z
Resistor R1/R3	R	1 [Ohm]
Resistor R2	R	2 [Ohm]
Voltage Source (Sinusoidal) E1/E2/E3	AMPL	326 [V]
	Freq	50 [Hz]
	Phase	0/-120/120 [deg]

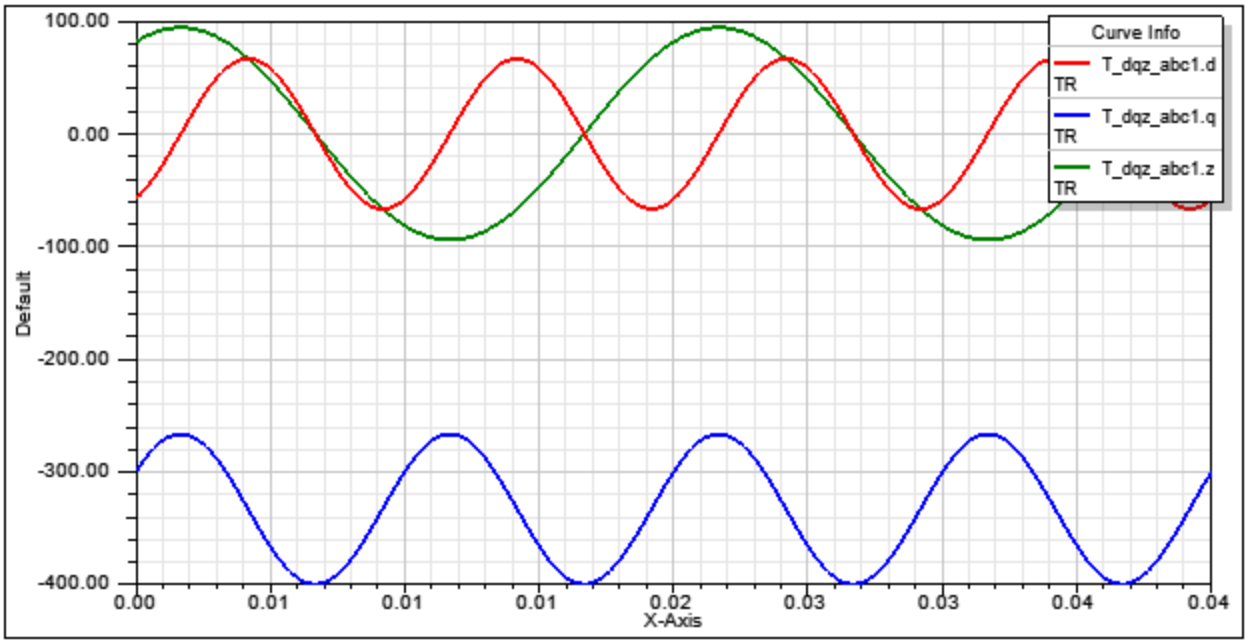

Figure 3. Simulation results-Direct, Quadrature, and Homopolar currents from Park transformation.

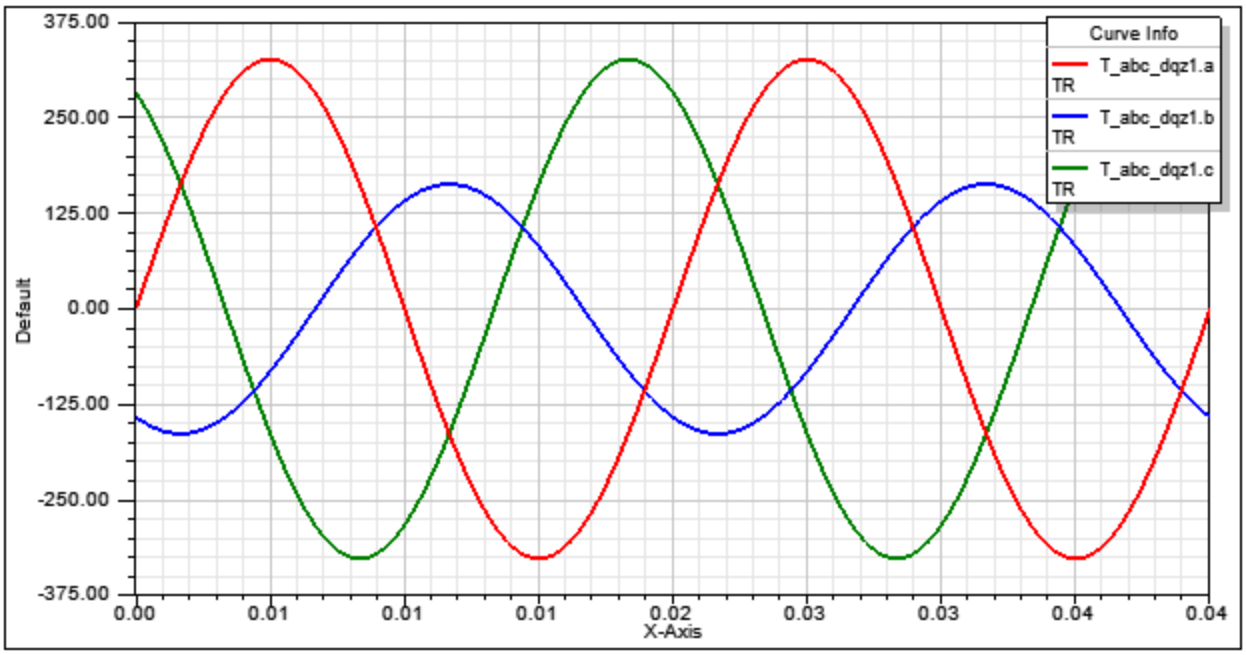

Figure 4. Simulation results-Phase currents from Inverse Park transformation.

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References

T_dqz_abc Park Transformation

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

Figure 1. Component symbol

Description

This block performs a Park transformation.

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Assumptions and Limitations

Top

Mathematical Description

The block performs the Park's transformation given by:

$$T_{dqz\_abc} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2}{3}\pi\right) & \cos\left(\omega t + \frac{2}{3}\pi\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2}{3}\pi\right) & \sin\left(\omega t + \frac{2}{3}\pi\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

so that:

$$X_{dqz} = T_{dqz\_abc} \cdot X_{abc}$$

where:

$$\omega = 2 \cdot \pi \cdot frequency$$

$$X_{dqz} = \begin{bmatrix} X_d \\ X_q \\ X_z \end{bmatrix}$$

$$X_{abc} = \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix}$$

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Netlist Syntax

MODEL T_dqz_abc ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (a:= @a, b:= @b, frequency:= @frequency, c:= @c) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
frequency	Frequency	real	50 [Hz]
a	A Component Input	real	0

b	B Component Input	real	0
c	C Component Input	real	0

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
d	d component output	Output	real
q	q component output	Output	real
z	z component output	Output	real

Top

Example

This example a Park and Inverse Park Transformation. The currents through the resistors are input to the Park transformation where they are converted to Direct, Quadrature and Homopolar currents. These currents are in turn transformed by the Inverse Park transformation back into a,b, and c phase currents.

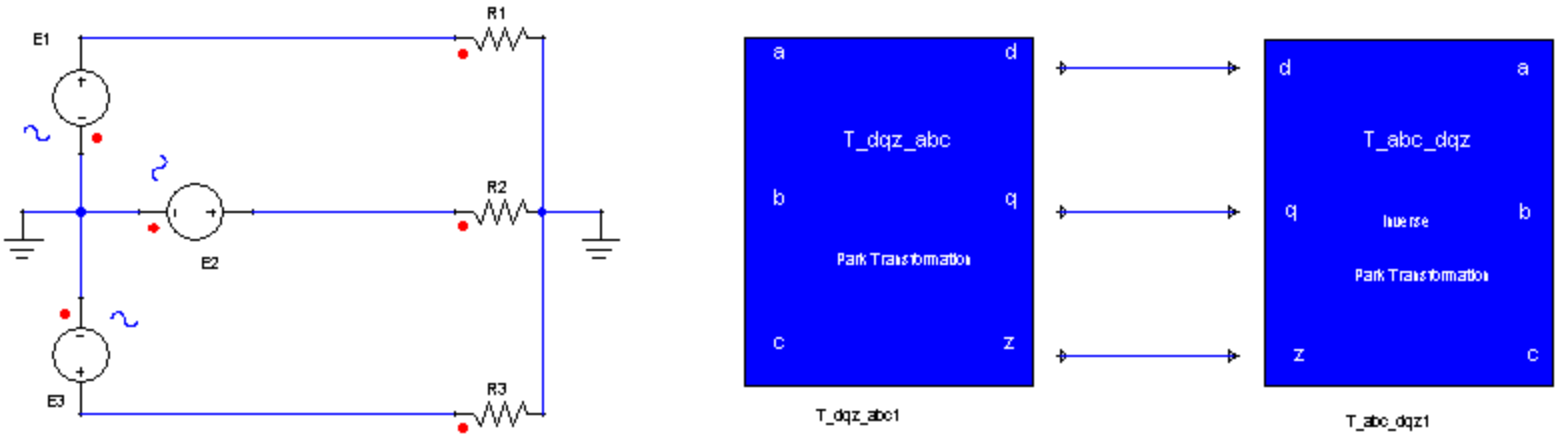

Figure 2. Application example of the Park and Inverse Park Transformation

Table 3. System Parameters

Component	Parameter	Value [unit]

Park Transformation T_DQZ_ABC1	a	R1.I
	b	R2.I
	c	R3.I
Inverse Park Transformation T_ABC_DQZ1	d	T_dqz_abc1.d
	q	T_dqz_abc1.q
	z	T_dqz_abc1.z
Resistor R1/R3	R	1 [Ohm]
Resistor R2	R	2 [Ohm]
Voltage Source (Sinusoidal) E1/E2/E3	AMPL	326 [V]
	Freq	50 [Hz]
	Phase	0/-120/120 [deg]

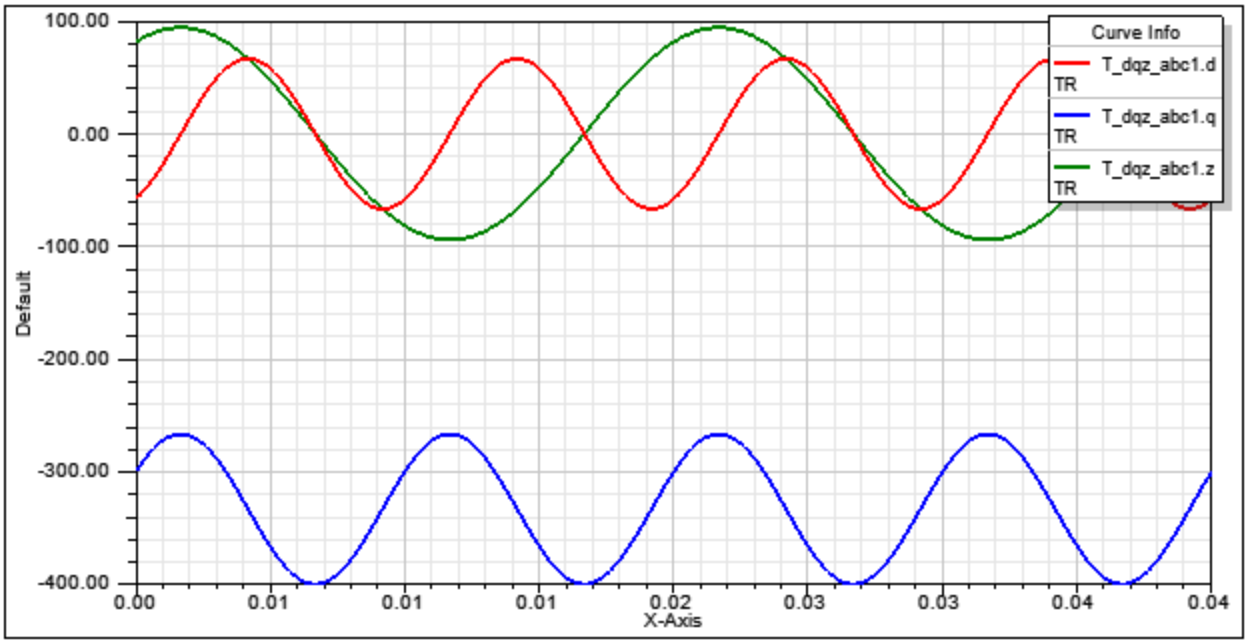

Figure 3. Simulation results-Direct, Quadrature, and Homopolar currents from Park transformation.

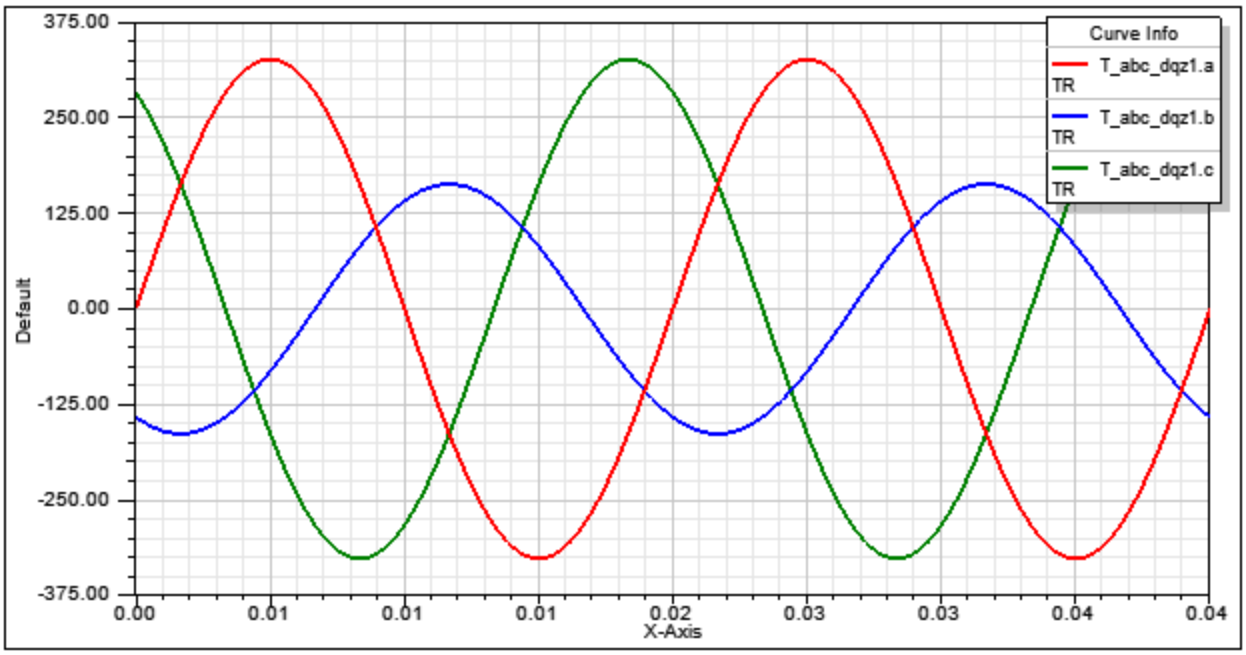

Figure 4. Simulation results-Phase currents from Inverse Park transformation.

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References

Control Modules

- COMPARATOR with DIGITAL OUTPUT (COMP_DIG)
- Electromagnetic Circuit Breaker (EM_CB)
- Fuse (FUSE_UPM)
- MOSFET with BODY DIODE (M_BD)
- MOSFET LEG (M_LEG)
- MOSFET Bridge (MOSFET_BRIDGE)
- Optocoupler (OPTOB)
- PWM (PWM_UPM)
- Load Share Controller (UC3907)
- Electronic Circuit Breaker (UCC3912)

COMP_DIG Comparator with Digital Output

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

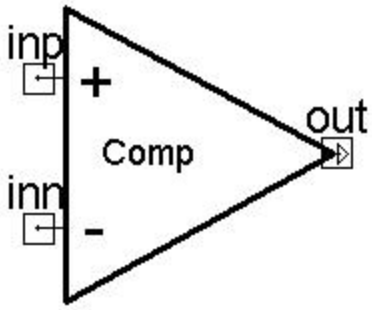

Figure 1. Component symbol

Description

The block is a classical comparator with digital output. The output parameter (out) is a variable with two possible values depending on the input:

- if inp > inn → out = 1
- if inp < inn → out = 0

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

MODEL COMP_DIG ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1 ( ) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	positive input pin	Electrical terminal
inn	negative input pin	Electrical terminal

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
out	Comparator Output(0-1)	Output	real

Top

Example

In this example, a digital comparator is used to compare the outputs of two voltage sources and provide a digital output. The schematic of the example is shown in Figure 2, system parameters are listed in the table 3, and the simulation results are shown in Figure 3.

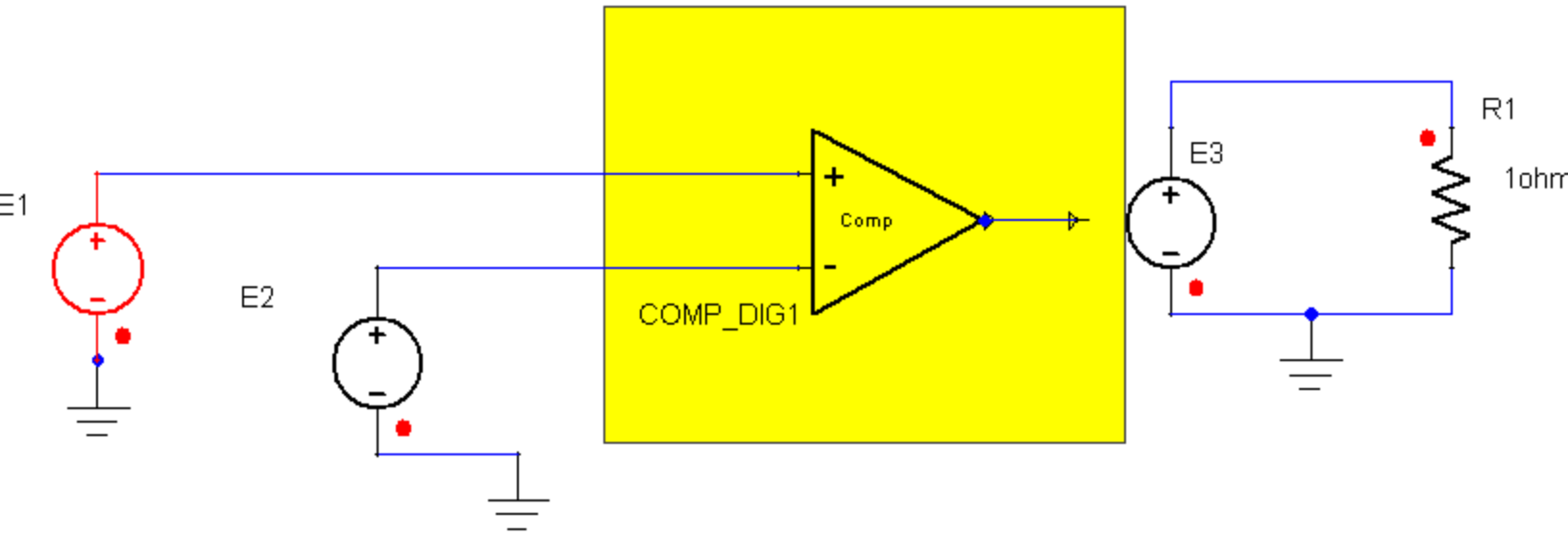

Figure 2. Application example of the Comparator with Digital Output component.

Table 3. System Parameters

Component	Parameter	Value [unit]
Comparator with Digital Output COMP_DIG1	out	0 [V]
Voltage Source (Sinusoidal) E1	AMPL Value	10 [V]
	FREQ	50 [Hz]
Voltage Source E2	EMF Value	3 [V]
Voltage Source E3	EMF Value	COMP_ DIG1.out
Resistor R1	Resistance	1 [Ohm]

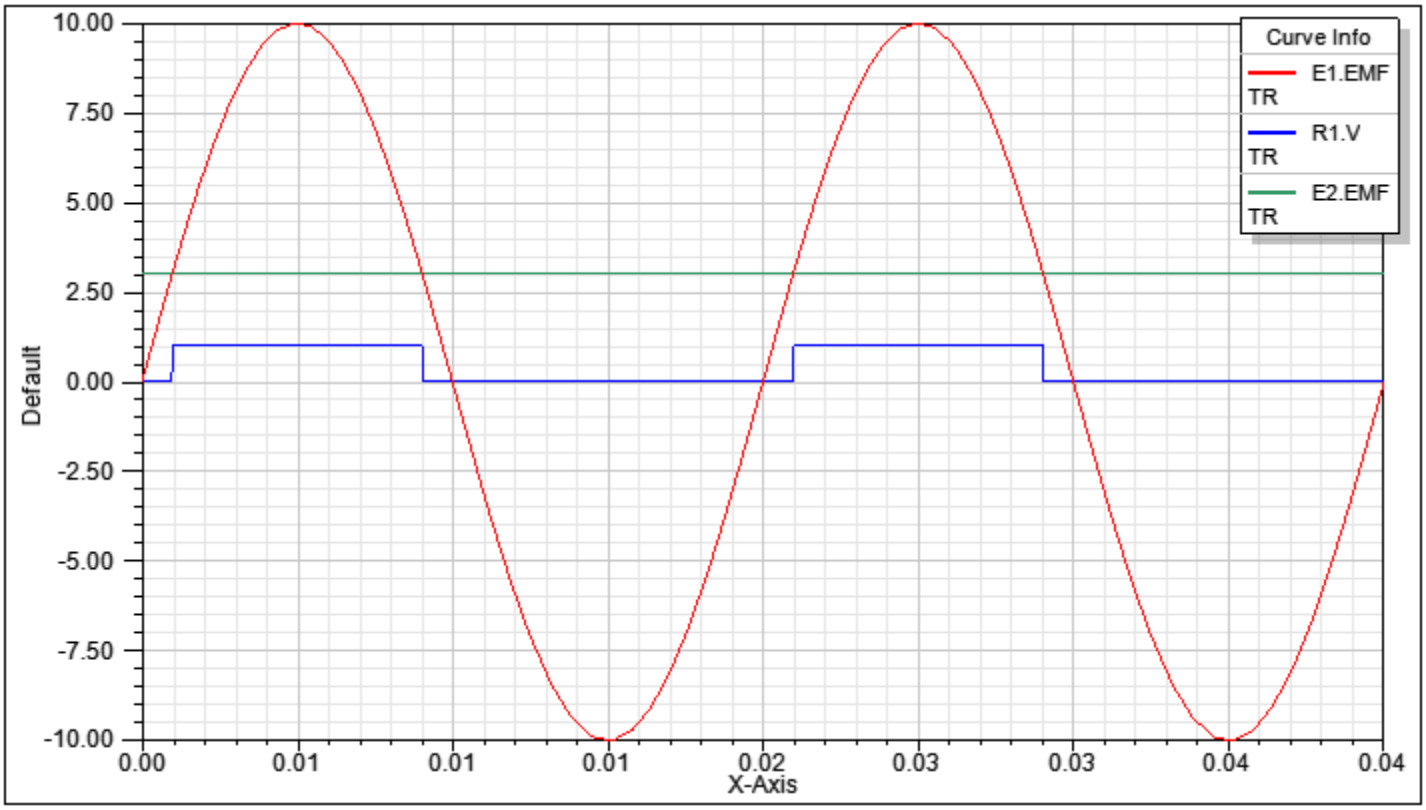

Figure 3. Simulation results – Input Voltages (E1.EMF and E2.EMF) and digital output across output resistor R1.

Top

References

EM_CB Electromagnetic Circuit Breaker

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

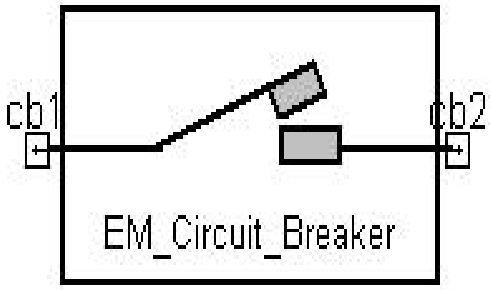

Figure 1. Component symbol

Description

When RESET = 0 and TRIP = 0 the Circuit Breaker acts as a resistor. When the TRIP signal is set to 1 the Circuit Breaker starts to open. If the RESET is set to 1 the circuit breaker will come to its initial state, that is, acting as a resistor.

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Assumptions and Limitations

Top

Mathematical Description

The model of the circuit breaker is based on the differential equations of Cassie y Mayr that model the electric arc according to:

$$\frac{dg_m}{dt} = \frac{1}{\tau_m} \cdot \left[\frac{i_b^{\,2}}{P_0} - g_m \right] \qquad Mayr$$

$$\frac{dg_c}{dt} = \frac{1}{\tau_c} \cdot \left[\frac{i_b^{\,2}}{u_c^{\,2} \cdot g_c} - g_c \right] \qquad Cassie$$

where:

g_m: conductance of the arc for Mayr's model

g_c: conductance of the arc for Cassie's model

i_b: current through the circuit

u_b: electric arc voltage

t_c, t_m, P_0, u_c: electric arc parameters

The conductance of the electric arc is given by:

$$\frac{1}{g} = \frac{1}{g_c} + \frac{1}{g_m}$$

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Netlist Syntax

MODEL EM_CB ?InstanceName(@InstanceName):(@(Refbase)@(ID)) cb1:= %0, cb2:= %1 (TRIP:= @TRIP, RESET:= @RESET, Tm:= @Tm, P0:= @P0, Uc:= @Uc, Tc:= @Tc) SRC: DB (Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
ctr1	Pin 1	Electrical terminal
ctr2	Pin 2	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
TRIP	Trip signal	real	1
RESET	RESET signal	real	0
Tm	Mayr's time constant	real	2.2e-7 [sec]
PO	Mayr's cooling power	real	8800 [W]
Tc	Cassie's time constant	real	8e-8 [sec]
Uc	Electric arc voltage	real	2350 [V]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
I	Circuit Breaker Current	Output	real
V	Circuit Breaker Voltage	Output	real

Top

Example

In this example, a circuit breaker is tripped with an external signal created with a state diagram. The schematic of the example is shown in Figure 2, system parameters are listed in the table 4, and the simulation results are shown in Figure 3.

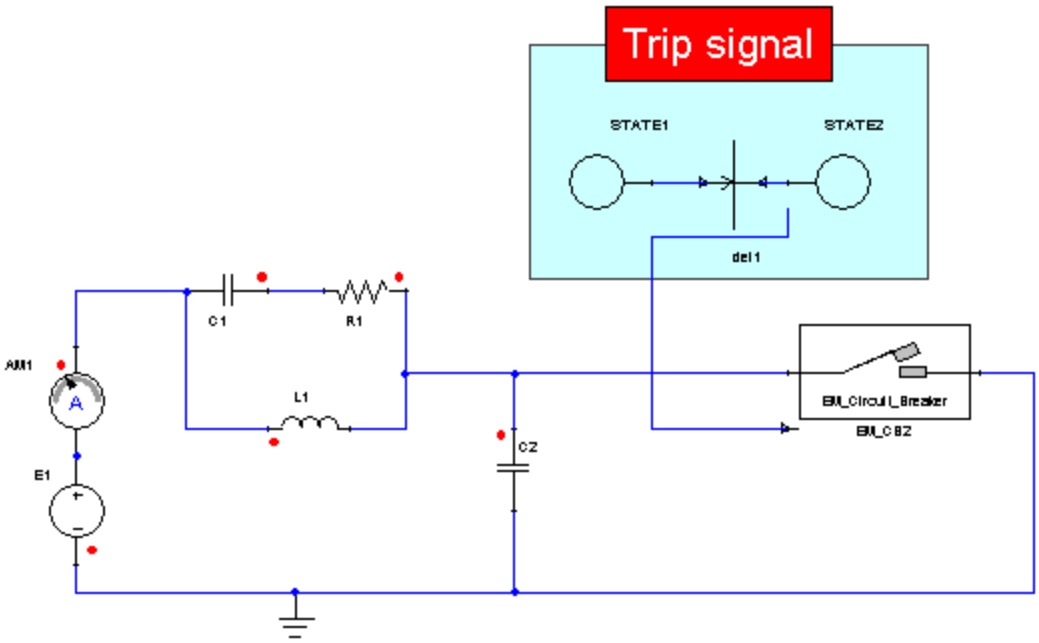

Figure 2. Application example of the Electromagnetic Circuit Breaker (EM_CB2).

Table 4. System Parameters

Component	Parameter	Value [unit]
Electromagnetic Circuit Breaker (EM_CB2)	TRIP	1
	RESET	0
	Tm	2.2e-007
	P0	8800 [W]
	Tc	8e-007[s]
	Uc	2350[V]
Voltage Source E1	EMF Value	51000 [V]
PWM (PWM1)	Period Value	5e-005 [s]
	DC	0.75
Inductor L1	Resistance	0.003 [H]
Resistor R1	Resistance	450 [Ohm]
Capacitor C1	Capacitance	9.6e-009 [F]
Capacitor C2	Capacitance	1.1e-009 [F]

State STATE1	EQU0	del1:=0.001
	EQU1	trip:=0
State STATE2	EQU0	trip:=1
Transition TRANS2	TRC	del1
	ST_PRE	STATE1.ST (0)
	ST_SUC	STATE2.ST (0)

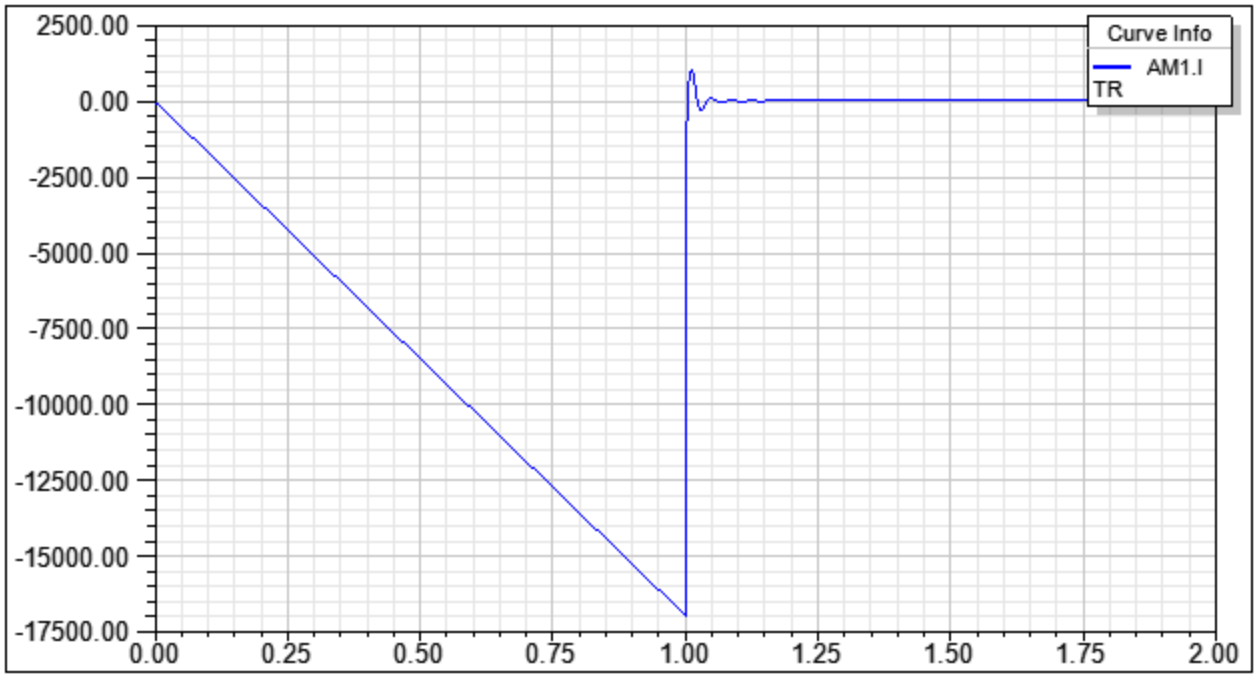

Figure 3. Simulation results – Source Output Current (AM1.I) showing circuit breaker tripping at 1ms.

Top

References

FUSE_UPM Fuse

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

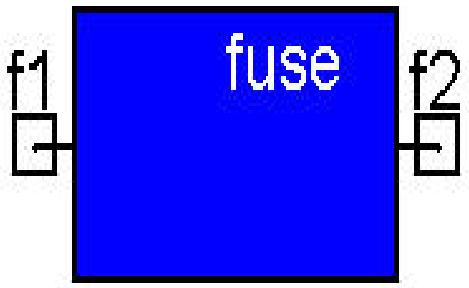

Figure 1. Component symbol

Description

Typical parameters for a fuse operating in a circuit with a given time constant and prospective current are rated current $i_{r,peak}$, peak current i_{pk}, pre-arcing time t_{pa}, arcing time t_a, total operating time t_t, prearcing i^2t $(i^2t)_p$, arcing i^2t $(i^2t)_a$ and total i^2t $(i^2t)_t$. The prospective current is the maximum current that would be reached if the fuse did not operate. The i^2t: current-squared time rating is a commonly used fuse characteristic when operating current levels are much higher than the rated fuse current i_r. The circuit time constant defines the ratio L/R, where L and R are

the effective circuit inductance and resistance components in series with the fuse and energy source.

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Assumptions and Limitations

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Mathematical Description

The model accurately represents the following four fuse characteristics:

• Rated current: The current controlled switch Wfuse starts to turn on when the fuse current exceeds rated current i_r, and is fully on when fuse current reaches 110% of i_r.

• Pre-arcing i^2t: The voltage developed across Cfuse is,

$$V_{Cfuse} = \int_0^t (i_f)^2 dt \equiv i^2 t$$

where $i_f > i_r$:

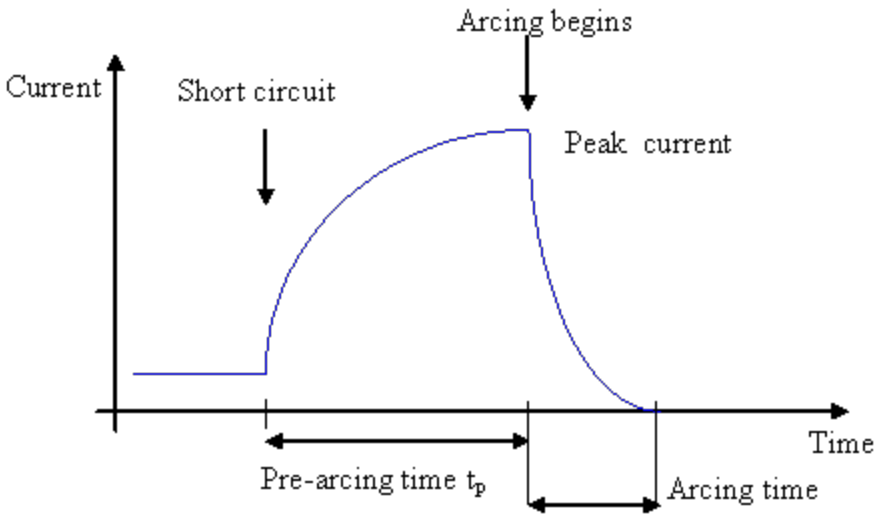

Figure 2. Characteristic of fuse current versus time

By making the capacitor Cfuse value equal to $(i^2t)p$, in A^2s, the voltage developed across Cfuse at the end of the pre-arcing time is normalized to 1V. When the voltage across Cfuse reaches 1V the voltage controlled switch Sfuse starts to turn off, and is fully off when the voltage reaches 1.3V. The R_c/C_c network introduces a small time delay to ensure one-way operation of the switch, and the delay can typically be minimized to an insignificant time of less than 0.1ms.

• Arcing i^2t: The time duration t_a for the current to reduce to zero after the onset of arcing can be modelled by the turn-off characteristic of the switch Sfuse. Varying the transition range of the switch Sfuse controlling voltage adjusts the arcing time t_a and hence the arcing i^2t.

• Resistance increase and thermal loss: during the application of a fault current, the fuse resistance increases toward the melting point. The resistance increase and resulting voltage drop across the fuse can be substantial. If the fault current is reduced before the i^2t level reaches the pre-arcing level, then the fuse element cools and resistance reduces back to the nominal resistance at ambient temperature R_F.

The fuse resistance is modelled by a combination of the constant resistance of the switch Sfuse, and the non linear resistance of the voltage source Efuse.

The thermal loss of the fuse element is modelled by the resistor R_b, which discharges the voltage across capacitor Cfuse. Reducing the value of R_b increases the thermal loss, returning the fuse to its pre-fault state in a faster time.

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Netlist Syntax

MODEL FUSE_UPM ?InstanceName(@InstanceName):(@(Refbase)@(ID)) f1:= %0, f2:= %1 (Ir:= @Ir, i2t_p:= @i2t_p, Rf:= @Rf, Rh:= @Rh, ta:= @ta, Ra:= @Ra) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
f1	Fuse Pin 1	Electrical terminal
f2	Fuse Pin 2	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Ir	Rating Current	real	20 [A]
i2t_p	Pre-arcing Current-squared-time rating	real	540 [A^2s]
Rf	Cold Resistance under normal operation	real	0.002 [Ohm]
Rh	Heat Resistance (voltage divided by current before melting)	real	0.01 [Ohm]
Ra	Arcing Resistance (measurement, voltage divided by current when it blows or melts)	real	0.1 [Ohm]
ta	Arcing time	real	0.001 [s]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
I	Fuse Current [A]	Output	real
I2t_ state	Normalized I2t integral. If I2t_ state>1, the fuse opens [nu]	Output	real
state	Status of the fuse. State=1 fuse blows, State =0 fuse conducts [nu]	Output	real
vpost	Voltage across the arc capacitor that provides the arc time constant [v]	Output	real

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Example

This example demonstrates the operation of a fuse where the characteristics of the device determine the length of time before the fuse blows. In this example, the switch is closed at 1 millisecond and the current begins to climb until the fuse blows at approximately 1.5 ms. The schem-

atic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

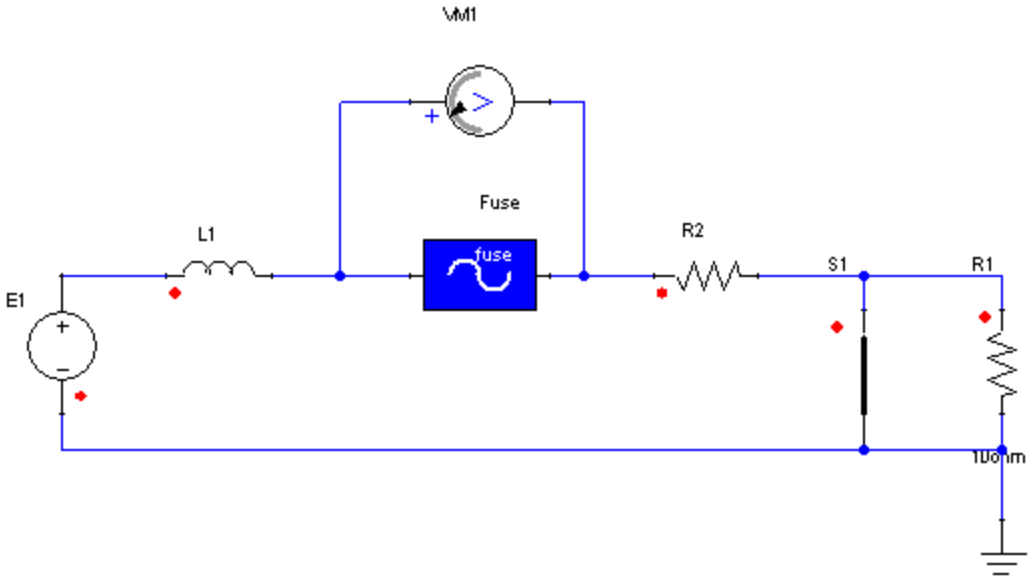

Figure 3. Application example of the 2 Phase Buck Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Fuse FUSE_UPM	Ir	30 [A]
	i2t_p	450 [A^2s]
	Rf	0.002 [Ohm]
	Rh	0.01 [Ohm]
	Ra	0.1 [Ohm]
	ta	0.001 [s]
Voltage Source E1	EMF Value	50 [V]
Inductor L1	Inductance	1e-005 [H]
Resistor R1	Resistance	10 [Ohm]
Resistor R2	Resistance	0.02 [Ohm]
Switch S	CTRL	(Time > 0.001)

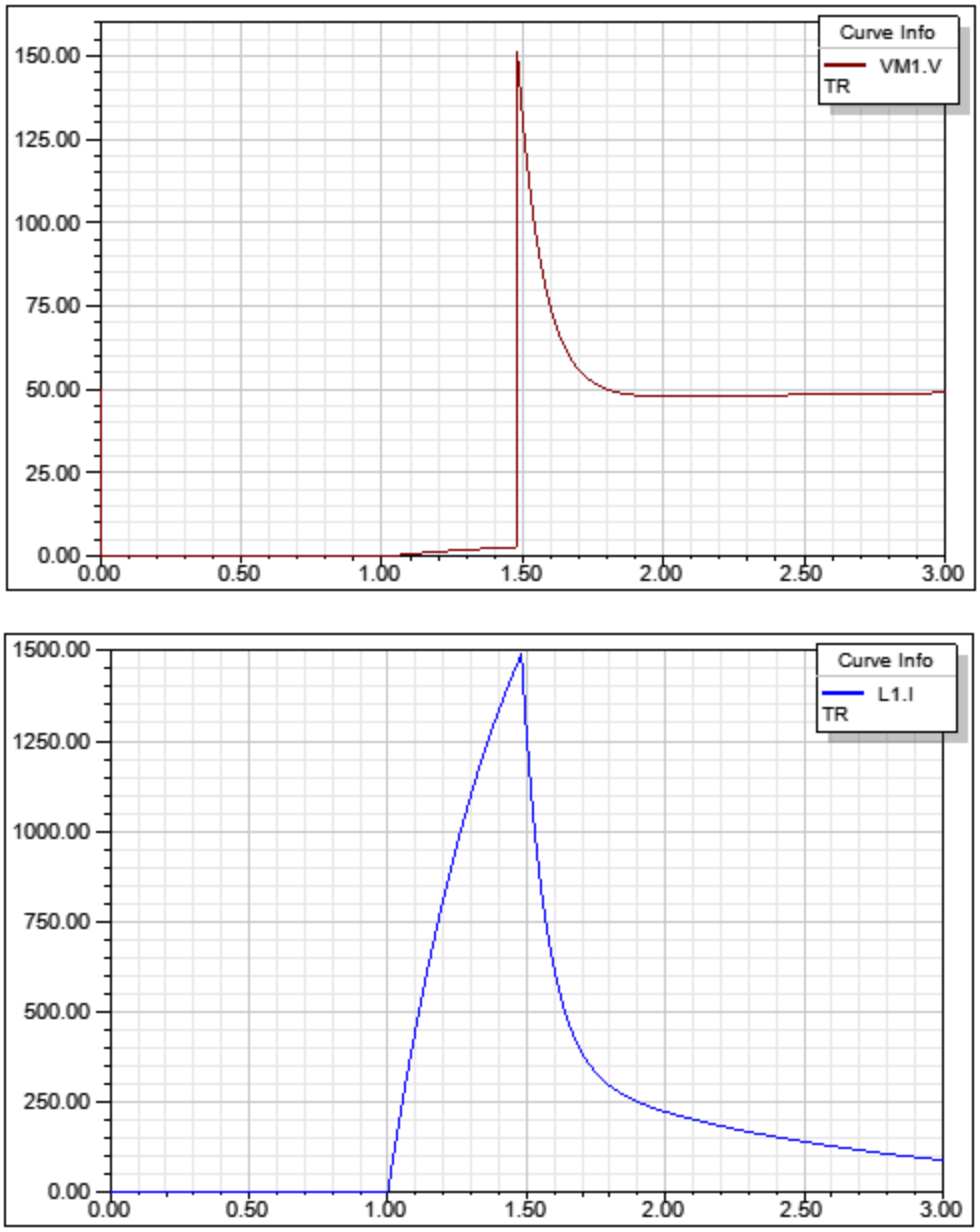

Figure 4. Simulation results – Voltage across the fuse (VM1.V) and Inductor Current (L1.I).

Top

References

M_BD MOSFET with Body Diode

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

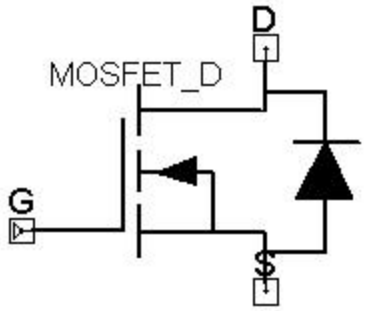

Figure 1. Component symbol

Description

When the gate signal (G) is set to ‘1’ the MOSFET is ON and when the gate signal is set to 0 the MOSFET is OFF. When the MOSFET is OFF it still can conduct current from source to drain through the body diode.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

MODEL M_BD ?InstanceName(@InstanceName):(@(Refbase)@(ID)) D:= %0, S:= %1 (G:= @G, Ron:= @Ron, Vfd:= @Vfd, Rd:= @Rd) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
D	Drain pin	Electrical terminal
S	Source pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
G	Gate signal	real	0
Ron	Drain-Source On resistance	real	0.01 [Ohm]
Vfd	Body diode forward voltage drop	real	0.6 [V]
Rd	Body diode forward res-istance	real	0.01 [Ohm]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Vds	Drain-Source Voltage	Output	real
ID	Drain current	Output	real

Top

Example

In this example, a MOSFET with a body diode is used to drive a resistive load. The schematic of the example is shown in Figure 2, system parameters are listed in the table 4, and the simulation results are shown in Figure 3.

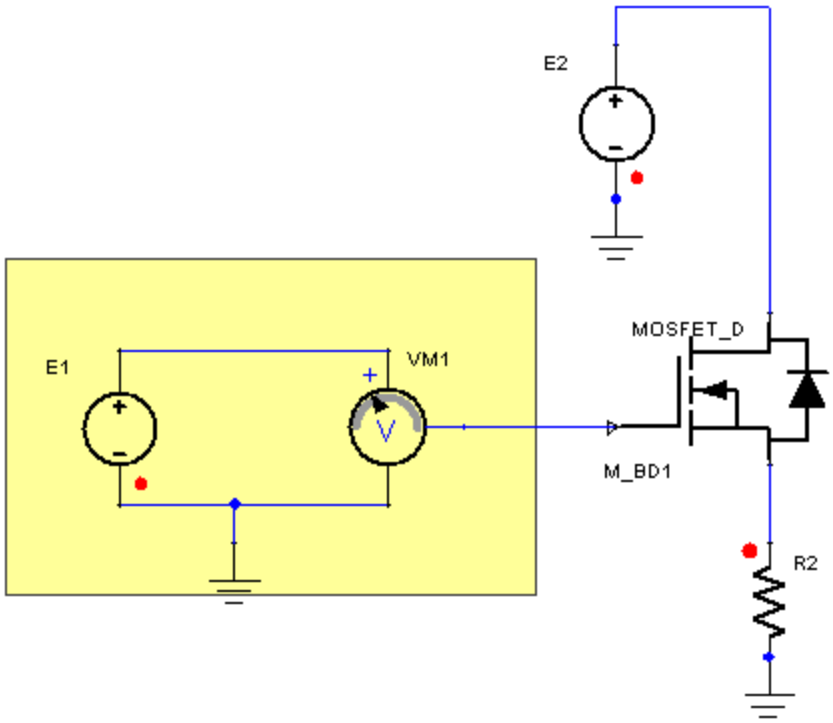

Figure 2. Application example of the MOSFET with Body Diode M_BD.

Table 4. System Parameters

Component	Parameter	Value [unit]
MOSFET with Body Diode M_ BD1	Gate Signal (G)	VM1.V
	Ron	0.01 [Ohm]
	Vfd	0.6 [V]
	Vds	0 [V]
	Rd	0.01 [Ohm]
Voltage Source (Pulse) E1	AMPL Value	0.5 [V]
	FREQ	50 [Hz]
	OFF	0.5 [V]

Voltage Source E2	EMF Value	10 [V]
Voltage Source E3	EMF Value	COMP_ DIG1.out
Resistor R2	Resistance	1 [Ohm]

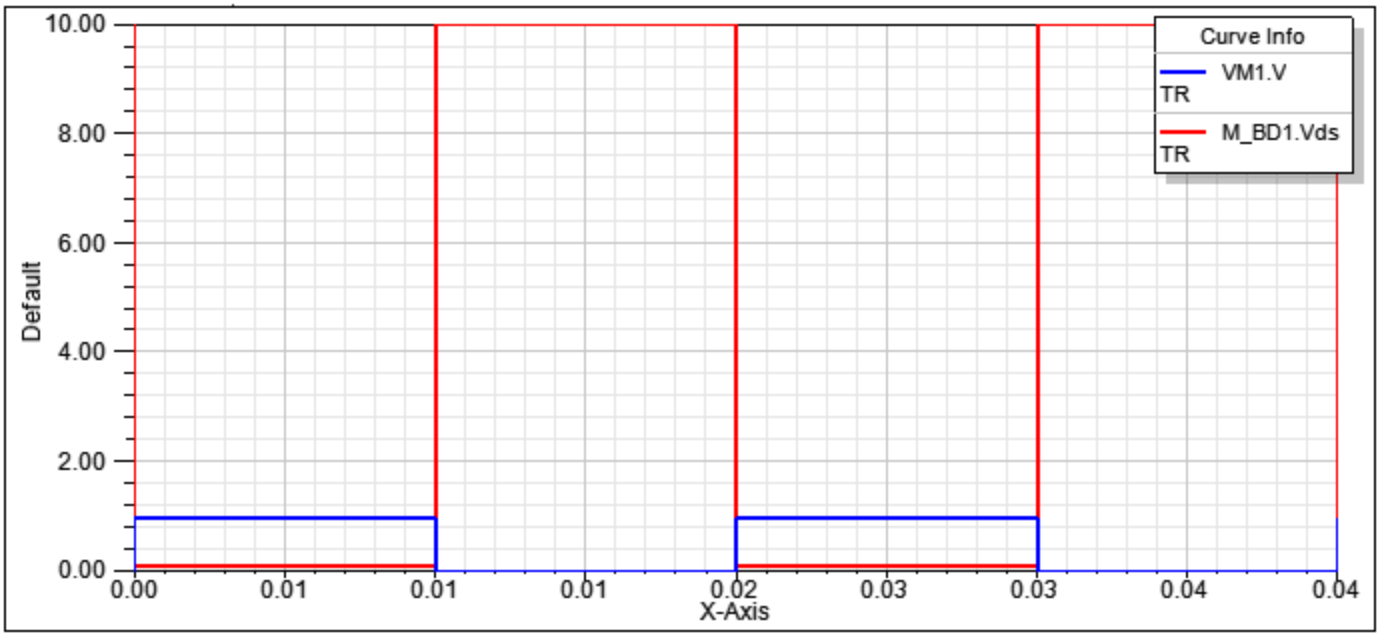

Figure 3. Simulation results – Gate Signal (VM1.V) and the Drain-Source Voltage (M_DB1.Vds).

Top

References

(M_LEG) MOSFET LEG

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

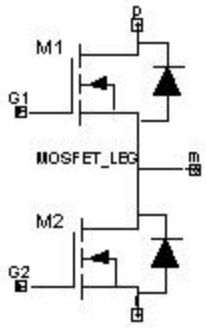

Figure 1. Component symbol

Description

The MOSFETs with body diodes are driven by the gate signals G1 and G2. The conduction characteristics of the MOSFETs are given by a forward voltage drop (Vfd) and a Resistance (Ron).

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

MODEL M_LEG ?InstanceName(@InstanceName):(@(Refbase)@(ID)) p:= %0, n:= %1, m:= %2 (G1:= @G1, Ron:= @Ron, Vfd:= @Vfd, Rd:= @Rd, G2:= @G2) SRC: DB(Lib:- :=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
p	Upper pin	Electrical terminal
m	Middle pin	Electrical terminal
n	Lower pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
G1	Gate 1 control	real	0
G2	Gate 2 control	real	0
Ron	MOSFETs On resistance	real	0.01 [Ohm]
Vfd	MOSFET forward voltage drop	real	0.6 [V]
Rd	Body diode forward res- istance	real	0.01 [Ohm]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Vds1	MOSFET 1 drain-source voltage	Output	real

Id1	MOSFET 1 drain current	Output	real
Vds2	MOSFET 2 drain-source voltage	Output	real
Id2	MOSFET 2 drain current	Output	real

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Example

In this example, a MOSFETs in a half-bridge configuration are used to drive an inductive load. The schematic of the example is shown in Figure 2, system parameters are listed in the table 4, and the simulation results are shown in Figure 3.

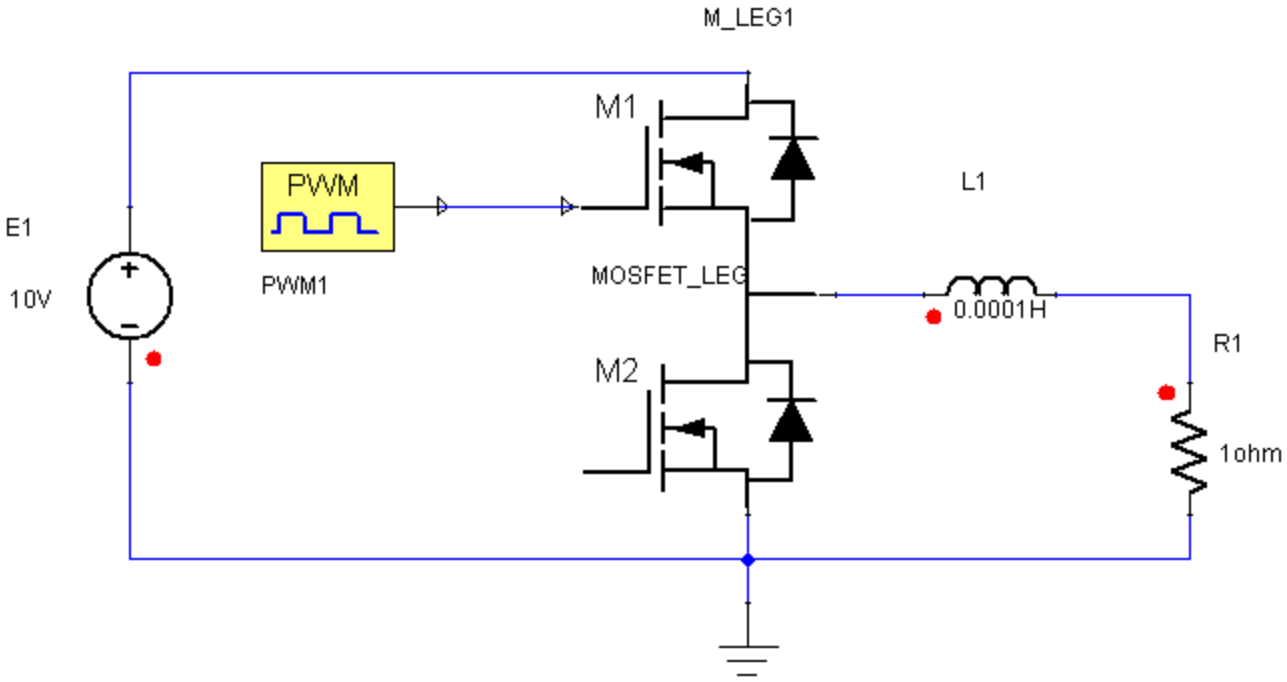

Figure 2. Application example of the MOSFET LEG (M_LEG1).

Table 4. System Parameters

Component	Parameter	Value [unit]

MOSFET LEG (M_LEG1)	Gate1 Control (G1)	PWM1.VAL
	Gate 2 Control (G2)	(1-PWM1.VAL)
	Vfd	0.6 [V]
	Ron	0.01 [Ohm]
Voltage Source E1	EMF Value Value	10 [V]
PWM (PWM1)	Period Value	1e-005 [s]
	DC	0.5
Inductor L1	Resistance	0.0001 [H]
Resistor R1	Resistance	1 [Ohm]

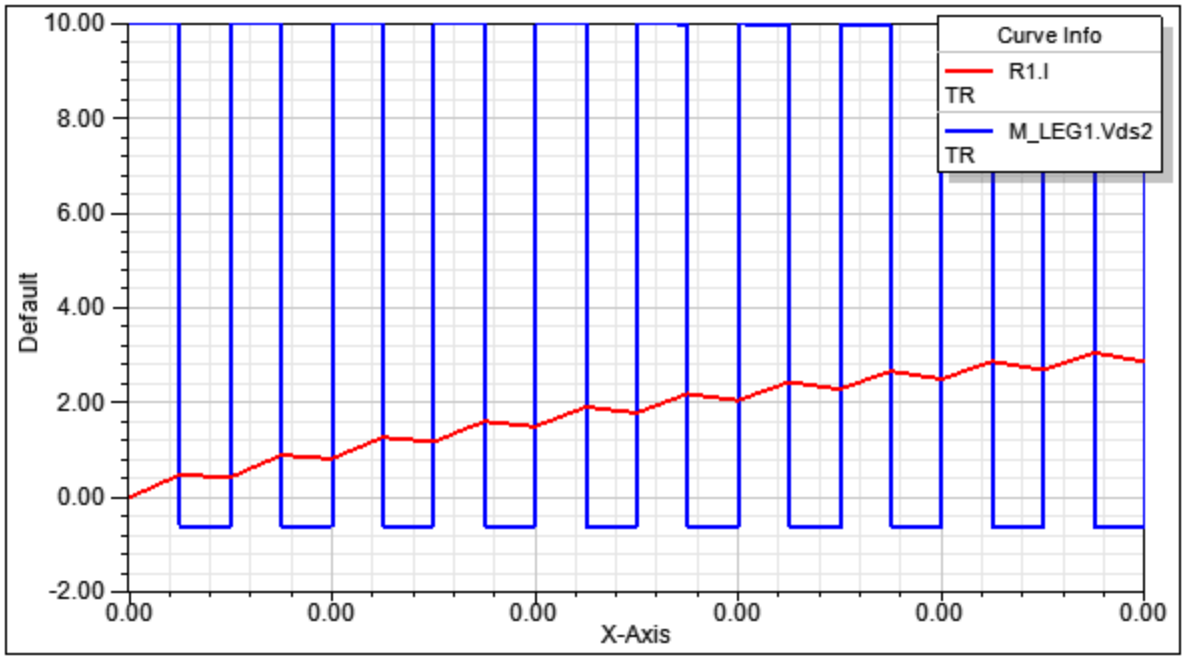

Figure 3. Simulation results – Output Voltage (M_LEG1.Vds2) and the Output Current (R1.I).

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References

(MOSFET_BRIDGE) MOSFET BRIDGE

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

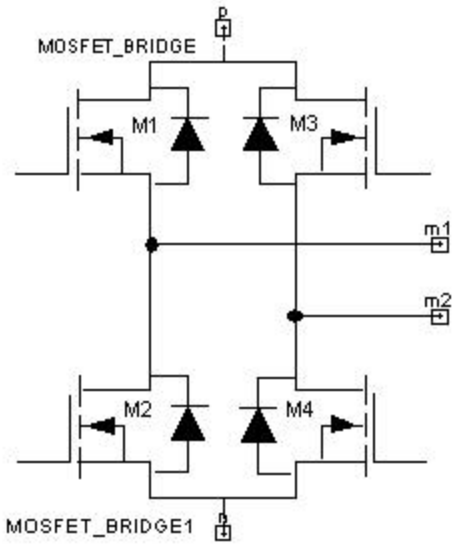

Figure 1. Component symbol

Description

The MOSFETs with body diodes are driven by the gate signals G1, G2, G3 and G4. The conduction characteristics of the MOSFETs are given by a forward voltage drop (Vfd) and a Resistance (Ron).

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Netlist Syntax

MODEL MOSFET_BRIDGE ?InstanceName(@InstanceName):(@(Refbase)@(ID)) p:= %0, n:= %1, m1:= %2, m2:= %3 (G1:= @G1, Ron:= @Ron, Vfd:= @Vfd, Rd:= @Rd, G2:= @G2, G3:= @G3, G4:= @G4) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
p	Upper pin	Electrical terminal
m1	Middle pin 1	Electrical terminal
m2	Middle pin 2	Electrical terminal
n	Lower pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
G1	Gate 1 control	real	0
G2	Gate 2 control	real	0
G3	Gate 3 control	real	0
G4	Gate 4 control	real	0
Ron	MOSFETs On resistance	real	0.01 [Ohm]
Vfd	MOSFET forward voltage drop	real	0.6 [V]
Rd	Body diode forward resistance	real	0.01 [Ohm]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Vds1	MOSFET 1 drain-source voltage	Output	real
Id1	MOSFET 1 drain current	Output	real
Vds2	MOSFET 2 drain-source voltage	Output	real
Id2	MOSFET 2 drain current	Output	real
Vds3	MOSFET 3 drain-source voltage	Output	real
Id3	MOSFET 3 drain current	Output	real
Vds4	MOSFET 4 drain-source voltage	Output	real
Id4	MOSFET 4 drain current	Output	real

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Example

In this example, a MOSFETs in a full-bridge configuration are used to drive an inductive load. The schematic of the example is shown in Figure 2, system parameters are listed in the table 4, and the simulation results are shown in Figure 3.

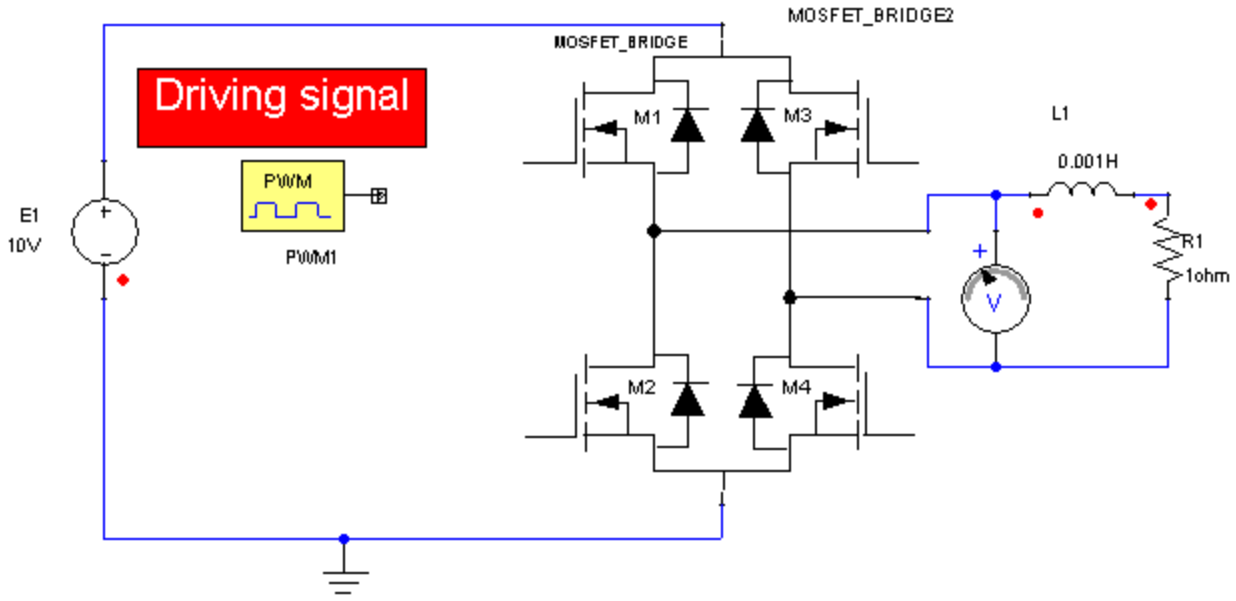

Figure 2. Application example of the MOSFET BRIDGE (MOSFET_BRIDGE2).

Table 4. System Parameters

Component	Parameter	Value [unit]
MOSFET BRIDGE (MOSFET_ BRIDGE2)	Gate1 Control (G1)	PWM1.VAL
	Gate 2 Control (G2)	(1-PWM1.VAL)
	Gate 3 Control (G3)	(1-PWM1.VAL)
	Gate 4 Control (G4)	PWM1.VAL
	Vfd	0.6 [V]
	Ron	0.1 [Ohm]
Voltage Source E1	EMF Value	10 [V]
PWM (PWM1)	Period Value	5e-005 [s]
	DC	0.75
Inductor L1	Resistance	0.001 [H]
Resistor R1	Resistance	1 [Ohm]

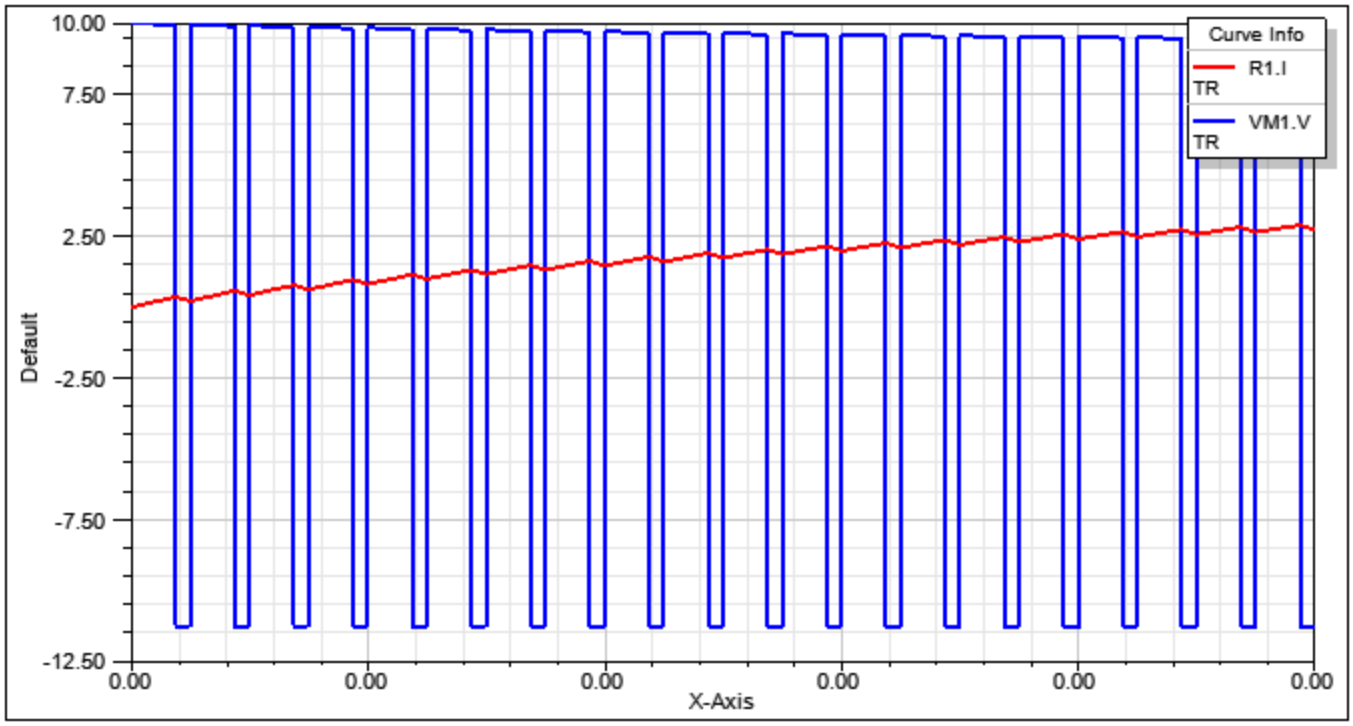

Figure 3. Simulation results – Output Voltage (VM1.V) and the Output Current (R1.I).

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References

OPTOB Optocoupler

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

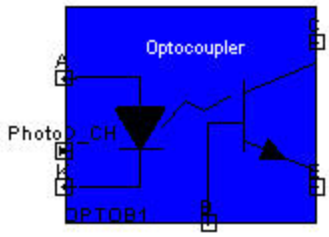

Figure 1. Component symbol

Description

It models a generic optocoupler. The model is based on the models of the diode and the bipolar transistor presents in the device. The diode characteristic is given by means of a characteristic component from the Tools section. The Phototransistor model is based on a simplified Ebers-Moll model of a transistor.

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Mathematical Description

The parameter Current Transfer Ration (CTR) allows changing the gain of the optocoupler since this value is very variable in the manufacturing process.

The gain is dependent on the temperature according to:

$$CTR = CTR_{Nom} \cdot \left(TC1 \cdot (T - T_{nom}) + TC2 \cdot (T - T_{nom})^2 \right)$$

Where TC1 and TC2 are the temperature coefficients, CTR_{Nom} is the Current Transfer Ration at nominal Temperature and CTR is the actual Current Transfer Ratio.

The current transfer ratio (CTR) refers to the ratio of the collector current at the output side I_c to the input current passed to the LED at the input side I_F expressed as a percentage. It is defined by the following formula:

CTR = $(I_C/I_F) \times 100$ (%)

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Netlist Syntax

MODEL OPTOB ?InstanceName(@InstanceName):(@(Refbase)@(ID)) C:= %0, B:= %1, E:= %2, A:= %3, K:= %4 (BF:= @BF, BR:= @BR, IS_BJT:= @IS_BJT, PhotoD_CH:= @PhotoD_CH, CTRNOM:= @CTRNOM, TC1:= @TC1, TC2:= @TC2, Tnom:= @Tnom) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
C	Collector	Electrical terminal
B	Base	Electrical terminal
E	Emisor	Electrical terminal
A	Anode	Electrical terminal
K	Cathode	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
BF	Bipolar Transistor Forward Beta Gain	real	100
BR	Bipolar Transistor Reverse Beta Gain	real	1
TC1	Temperature coefficient 1	real	0 [1/ºC]
TC2	Temperature coefficient 2	real	0 [1/ºC^2]
Tnom	Nominal Temperature	real	23 [ºC]
IS_BJT	Bipolar Junction Saturation Current	real	1e-012 [A]
CTRNOM	Nominal Current Transfer Ratio	real	1
PhotoD_CH	Photo Diode Characteristics	real	

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Example

In this example, an optocoupler photodiode is driven by a source. The diode current drives the phototransistor and allows current to flow through resistor R3. The schematic of the example is shown in Figure 2, system parameters are listed in the table 3, and the simulation results are shown in Figure 3.

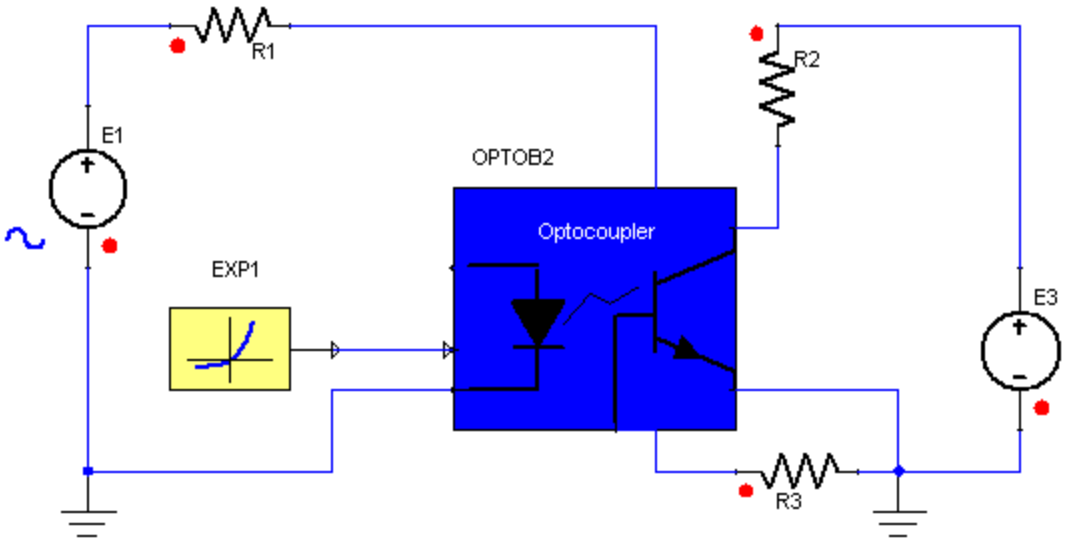

Figure 2. Application example of the Opto Coupler component (OPTOB2)

Table 3. System Parameters

Component	Parameter	Value [unit]
Optocoupler OPTOB2	BF	200
	PhotoD_CH	EXP1.VAL
	TC1	-0.01127 [1/ºC]
	TC2	-4.346e-005 [1/ (ºC)^2]
	CTRNOM	2
Voltage Source (Sinusoidal) E1	AMPL Value	10 [V]
	FREQ	50 [Hz]
Voltage Source E3	EMF Value	1 [V]
Resistor R1	Resistance	1000 [Ohm]
Resistor R2	Resistance	10 [Ohm]
Resistor R3	Resistance	100000 [Ohm]
Exponential Function EXP1	VT	0.0007 [V]
	ISAT	1e-12 [A]
	RR	100000 [Ohm]

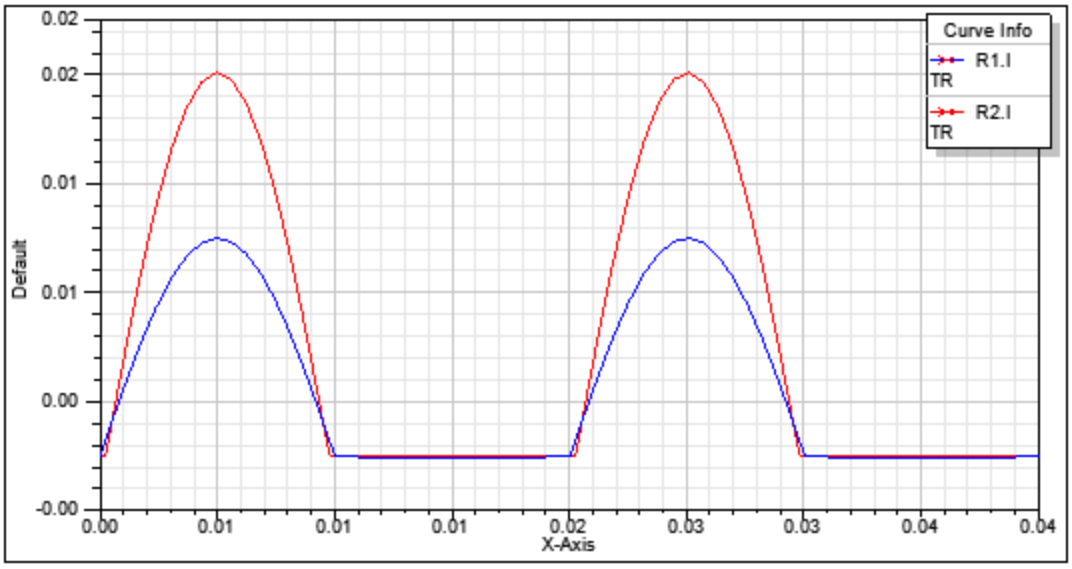

Figure 3. Simulation results – Photodiode current (R1.I) and Phototransistor current (R2.I)

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References

(PWM_UPM) PWM

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

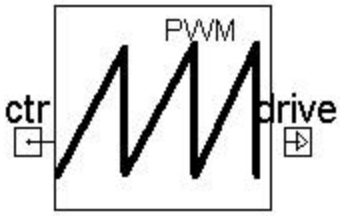

Figure 1. Component symbol

Description

The PWM model provides a pulse-width modulated signal with amplitude of "1". The time that the modulated signal is set to 1 depends on the voltage on pin ctr and the values of Vmin and Vmax. For a voltage lower than Vmin the duty cycle is set to zero and for a voltage higher than Vmax the duty cycle is set to ”1”. The duty cycle increases linearly from 0% to 100% when the control voltage varies from Vmin to Vmax.

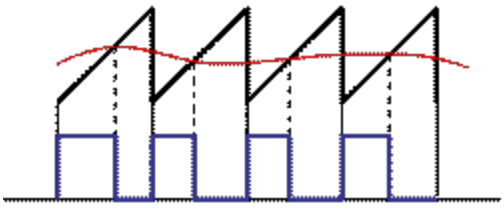

Figure 2. Duty cycle as a function of control voltage

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Netlist Syntax

MODEL PWM_UPM ?InstanceName(@InstanceName):(@(Refbase)@(ID)) ctr:= %0 (Vmax:= @Vmax, Vmin:= @Vmin, Fs:= @Fs, Phase_DEG:= @Phase_DEG) SRC: DB(Lib:- :=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
ctr	control voltage pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Vmax	Maximum Sawtooth Voltage	real	0 [V]
Vmin	Minimum Sawtooth Voltage	real	0 [V]
Fs	Switching Frequency	real	0 [Hz]
Phase_ DEG	Phase delay	real	0 [deg]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type

drive	PWM Output	Output	real
sawtooth	Sawtooth Output	Output	real

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Example

In this example, a triangular wave input signal is modulated and delivered to a load resistor. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

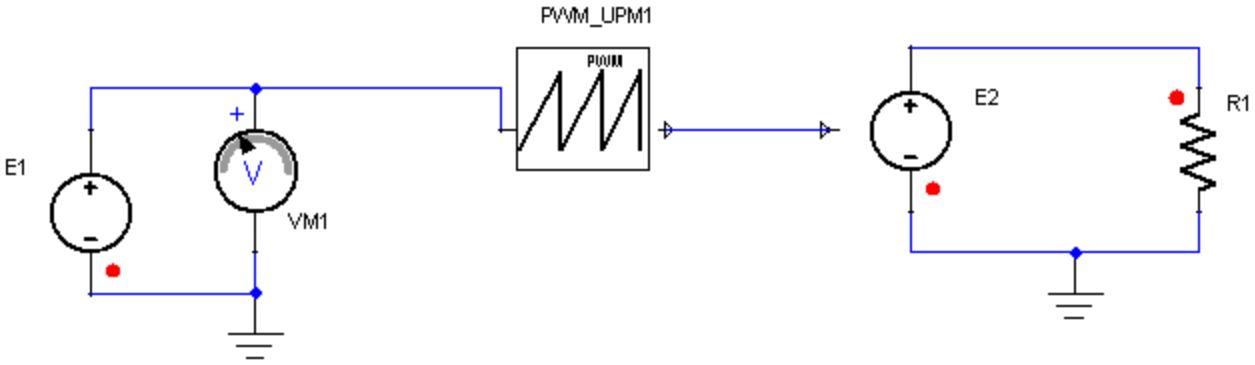

Figure 3. Application example of the Pulse Width Modulator PWM_UPM1

Table 4. System Parameters

Component	Parameter	Value [unit]
PWM Controller PWM_UPM1	Vmax	3 [V]
	Vmin	1 [V]
	Fs	50000 [Hz]
Voltage Source (Triangular) E1	AMPL	1 [V]
	FREQ	5000 [Hz]
	Offset	2 [V]
Voltage Source E2	EMF Value	PWM_UPM1.drive
Resistor R1	Resistance	1 [Ohm]

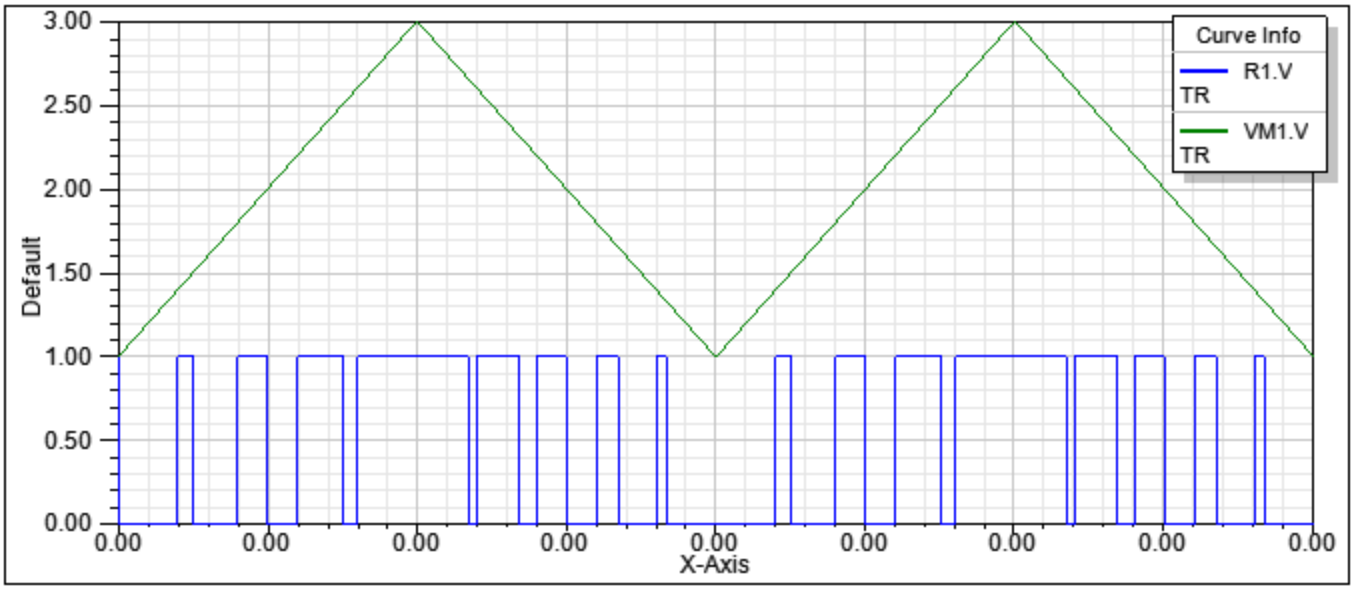

Figure 4. Simulation results – Input triangular wave (VM1.V) and modulated output signal (R1.V) delivered to the load.

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References

UC3907 Load Share Controller

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

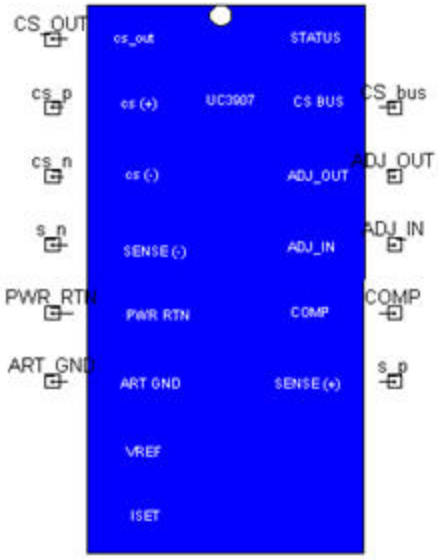

Figure 1. Component symbol

Description

The UCx907 family of load share controller ICs provides all the necessary features to allow multiple-independent-power modules to be paralleled such that each module supplies only its proportionate share to total-load current.

This sharing is accomplished by controlling each module's power stage with a command generated from a voltage-feedback amplifier whose reference can be independently adjusted in response to a common-share-bus voltage. By monitoring the current from each module, the current share bus circuitry determines which paralleled module would normally have the highest output current and, with the designation of this unit as the primary unit, adjusts all the other modules to increase their output current to within 2.5% of that of the primary unit.

The current share bus signal interconnecting all the paralleled modules is a low-impedance, noise-insensitive line which will not interfere with allowing each module to act independently should the bus become open or shorted to ground. The UC3907 controller will reside on the output side of each power module and its overall function is to supply a voltage feedback loop. The specific architecture of the power stage is unimportant. Either switching or linear designs may be utilized and the control signal may be either directly coupled or isolated though the use of an optocoupler or other isolated medium.

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Netlist Syntax

MODEL UC3907 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) cs_p:= %0, cs_n:= %1, s_p:= %2, s_n:= %3, PWR_RTN:= %4, CS_OUT:= %5, CS_bus:= %6, COMP:= %7, ART_GND:= %8, ADJ_OUT:= %9, ADJ_IN:= %10 ( ) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
cs_p	Positive current sense pin	Electrical terminal
cs_n	Negative current sense pin	Electrical terminal
s_p	Voltage amplifier input	Electrical terminal
s_n	Voltage reference ground	Electrical terminal
PWR_RTN	Lowest voltage of the IC	Electrical terminal
CS_out	Current Amplifier Output	Electrical terminal
CS_bus	Current share bus voltage	Electrical terminal
COMP	Voltage error amplifier output	Electrical terminal
ART_GND	Current adjust amplifier ground	Electrical terminal
ADJ_OUT	Current adjust amplifier output	Electrical terminal
ADJ_IN	Current adjust amplifier input	Electrical terminal

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Example

In this example, two buck converters are connected in parallel to drive a load. Two cases are used in this example. The first uses voltage controllers in the control loop. The second case uses the current share controller in the control loop. It can be seen that the current is unbalanced in the left case because there is a difference of 5% in the voltage reference (typical in a real case). However, using the current share controller the current at the output of both converters is balanced. The schematics of the example are shown in Figures 2 and 3, system parameters are listed in tables 2 and 3, and the simulation results are shown in Figure 4.

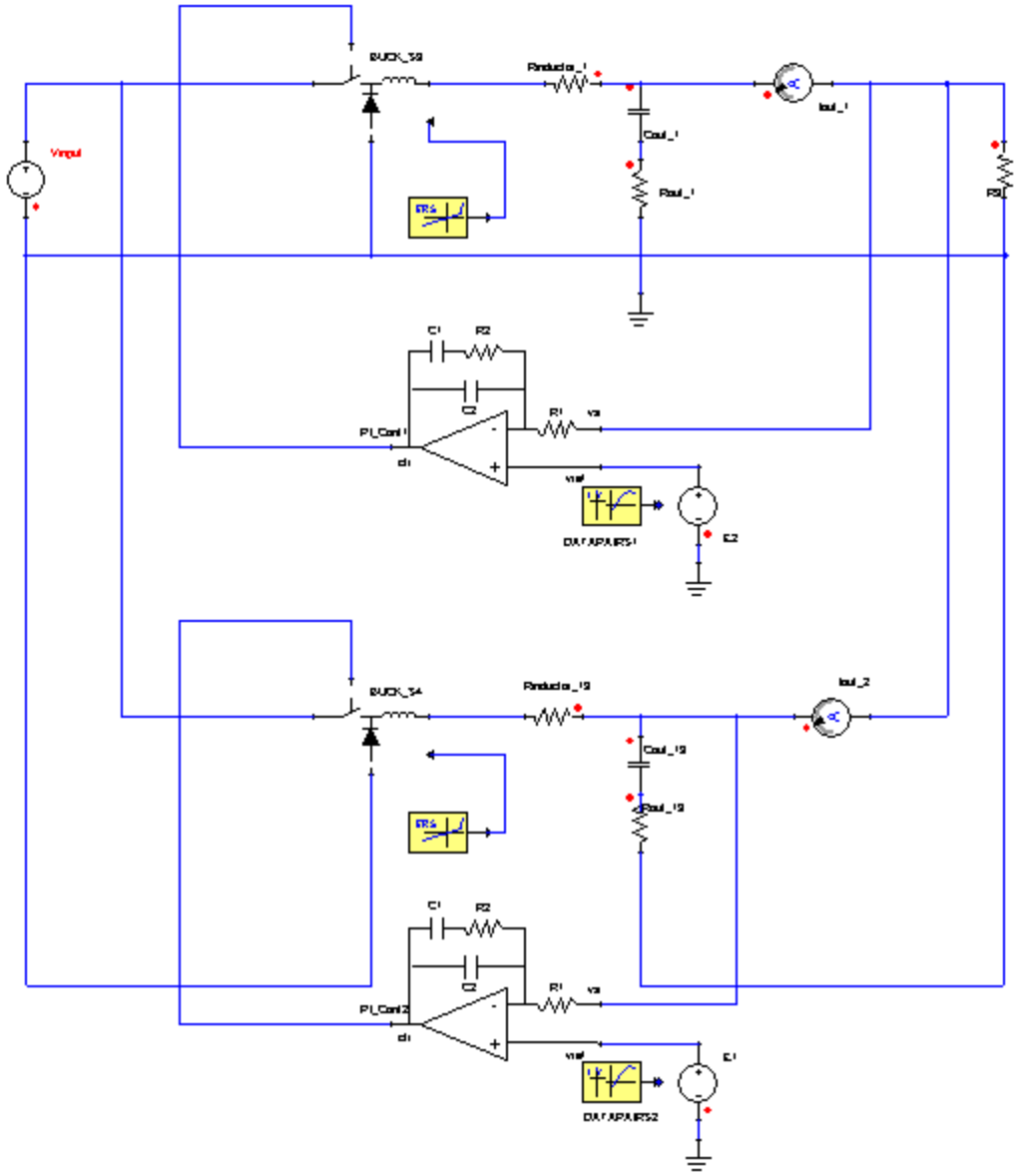

Figure 2. Application example of parallel buck converters without the UC3907 Current Share controller.

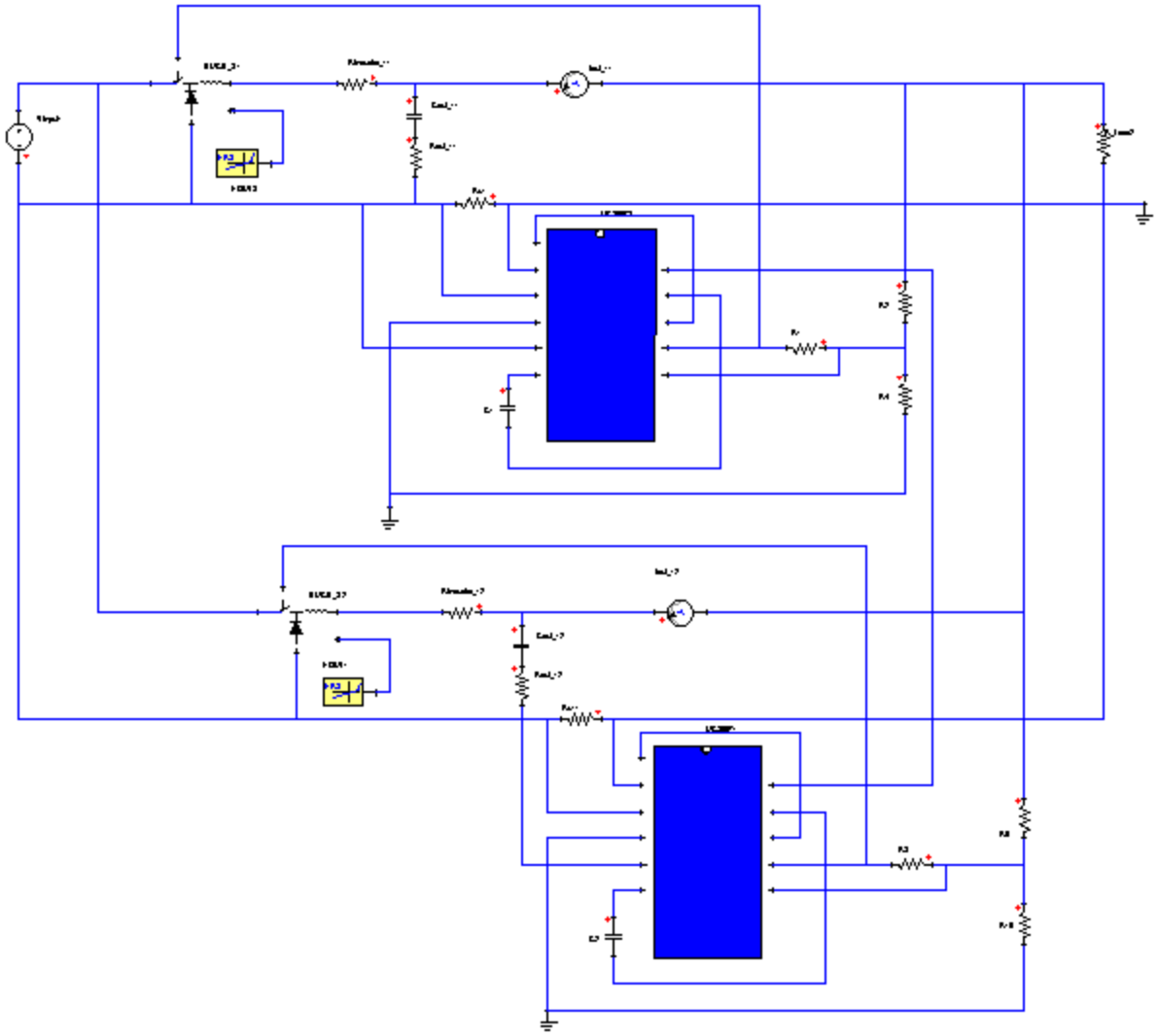

Figure 3. Application example of parallel buck converters using the UC3907 Current Share controller in the control loop.

Table 2. System Parameters (Voltage Controller case)

Component	Parameter	Value [unit]
Voltage Source VINPUT	EMF Value	12 [V]
Voltage Source E1	EMF Value	DATAPAIRS1.VAL
Voltage Source E2	EMF Value	DATAPAIRS2.VAL

Voltage Controller PI_CONT1/PI_ CONT2	C1	6.7e-011 [F]
	C2	9e-013 [F]
	R1	100000 [Ohm]
	R2	1000000 [Ohm]
	Vmin	-15 [V]
	Vmax	15 [V]
Buck Controller BUCK_S3/BUCK_S4	Fs	100000 [Hz]
	L	7.5e-005 [H]
	Rsa	0.01 [Ohm]
	DIODE_CH	EQUL4.VAL/EQUL2.VAL
Equivalent Line EQUL4/EQUL2	VF	0.8 [V]
	RB	0.01 [Ohm]
	RR	100000 [Ohm]
	Output	EQUL4.VAL/EQUL2.VAL
Capacitor COUT_ 1/COUT_13	Capacitance	0.00022 [F]
Resistor RINDUCTOR_ 1/RINDUCTOR_13	Resistance	0.1 [Ohm]
Resistor ROUT_ 1/ROUT_13	Resistance	0.07 [Ohm]
Resistor R3	Resistance	5 [Ohm]

Table 3. System Parameters (UC3907 Current Controller case)

Component	Parameter	Value [unit]
Voltage Source VINPUT1	EMF Value	12 [V]
Buck Controller BUCK_S1/BUCK_S2	Fs	100000 [Hz]
	L	7.5e-005 [H]
	Rsa	0.01 [Ohm]
	DIODE_CH	EQUL3.VAL/EQUL1.VAL
Equivalent Line EQUL3/EQUL1	VF	0.8 [V]
	RB	0.01 [Ohm]
	RR	100000 [Ohm]
	Output	EQUL4.VAL/EQUL2.VAL
Capacitor COUT_ 11/COUT_12	Capacitance	0.00022 [F]
Resistor RINDUCTOR_ 11/RINDUCTOR_12	Resistance	0.1/0.095 [Ohm]
Resistor ROUT_ 11/ROUT_12	Resistance	0.07 [Ohm]
Resistor R_Load2	Resistance	5 [Ohm]
Resistor Rs1/Rs11	Resistance	0.01 [Ohm]
Resistor R1/R8	Resistance	300000 [Ohm]
Resistor R2/R9	Resistance	30000 [Ohm]
Resistor R4/R10	Resistance	20000 [Ohm]
Capacitor C1/C2	Capacitance	1e-006 [F]

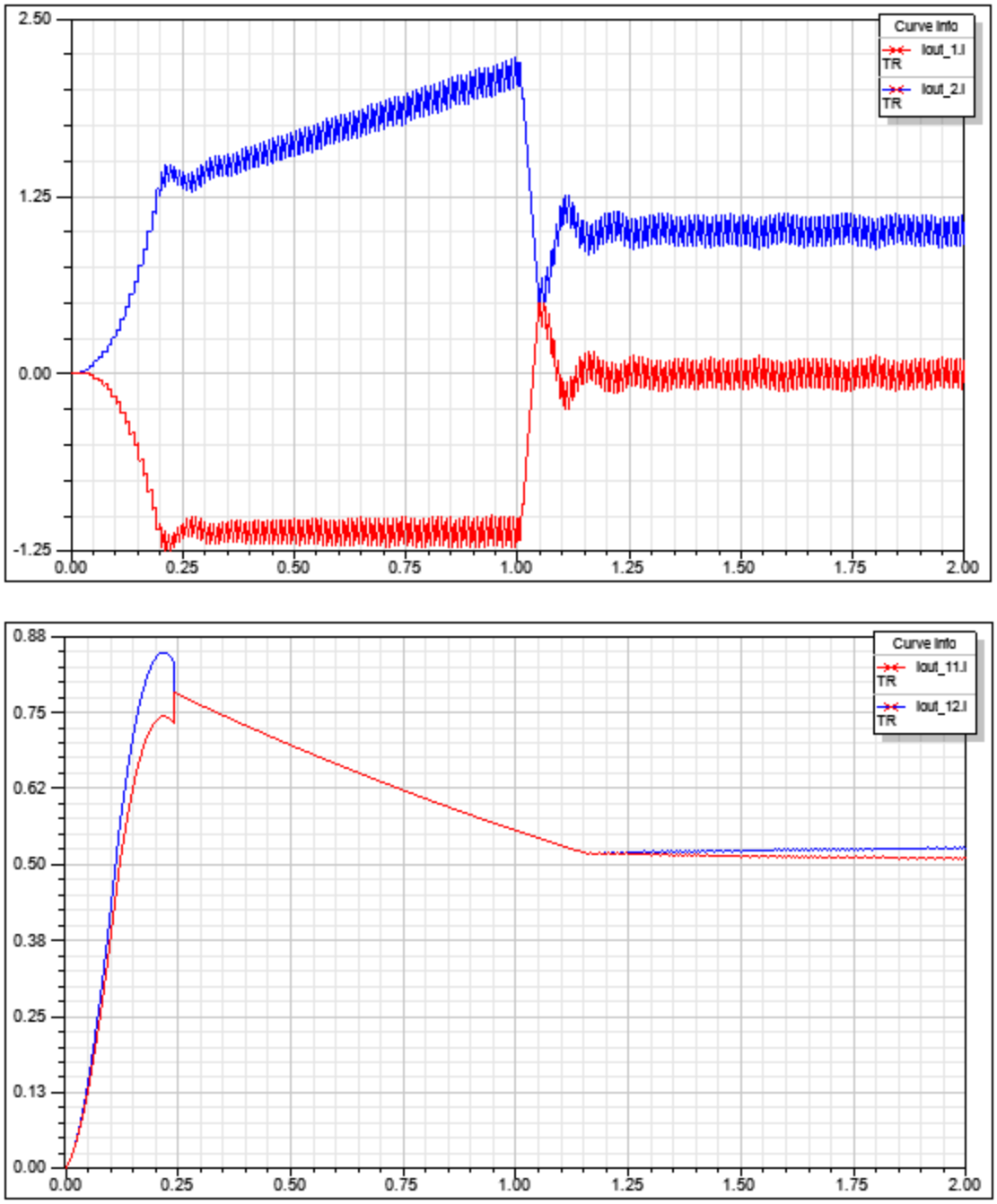

Figure 4. Simulation results – Load Current Without (IOUT_1.I/IOUT_2.I) and With (IOUT_11.I/IOUT_12.I) Current Share Controller

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References

For further information see Texas Instruments Datasheet or the Texas Instruments Application Note

UCC3912 Electronic Circuit Breaker

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

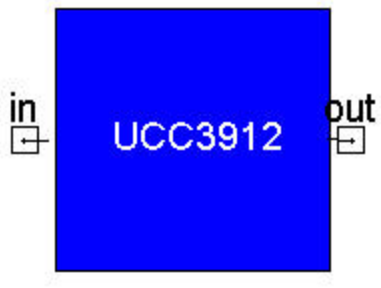

Figure 1. Component symbol

Description

The UCC3912 is an electronic circuit breaker IC designed to provide power management and hot swap capability in addition to its basic circuit breaker function. Performance features of UCC3912 include:

• Integrated power MOSFET

• Switch mode short circuit protection

• Automatic short circuit recovery

• Programmable maximum current limit

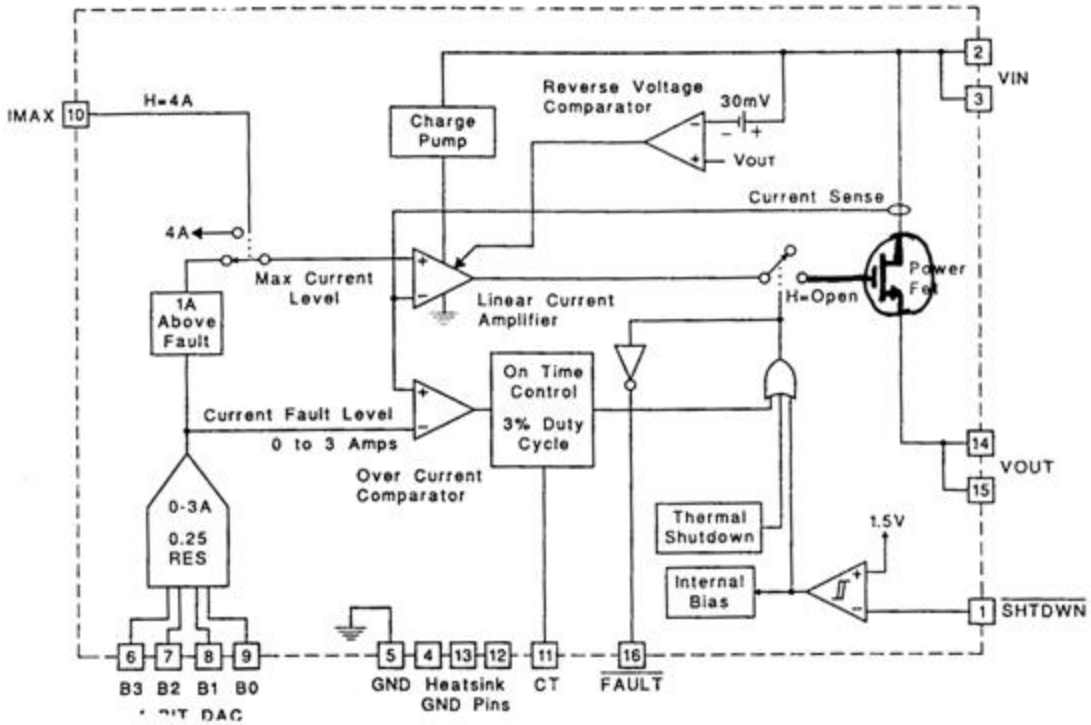

Figure 2. Block Diagram of UCC3912

The block diagram of the UCC3912 is shown in Figure 2. Under normal operating conditions the MOSFET is biased “on”. Output current is sensed and is compared to rating current level . When the output current exceeds the rating current level, the fault timer begins to charge the timing capacitor CT. If the output current does not fall bellow the rating current level, the output is switched off and the capacitor is discharged. Once the capacitor ‘s voltage has reached a low level, the circuit breaker attempts to return power to the load. At this point the timer cycle will repeat as long as the fault is present, resulting in an output duty cycle of 3%. If at any time the output current reaches the maximum current level, the MOSFET transitions into linear mode, providing constant output current until the fault time expires.

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Netlist Syntax

MODEL UCC3912 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) in:= %0, out:= %1 (Ron:= @Ron, I_max:= @I_max, I_trip:= @I_trip, Fault_time:= @Fault_time) SRC: DB(Lib:- :=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
in	input pin	Electrical terminal
out	output pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Ron	Conduction Resistance of the MOSFET	real	0.15 [Ohm]
I_max	Maximum current that the MOSFET can draw	real	4 [A]
I_trip	Trip current	real	3 [A]
Fault_ time	Time that the current can exeed the trip current	real	0.001 [sec]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
fault	Fault Flag	Output	real

Top

Example

In this example, an electronic circuit breaker is used to limit the source current as a capacitor is charged to 8 volts. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

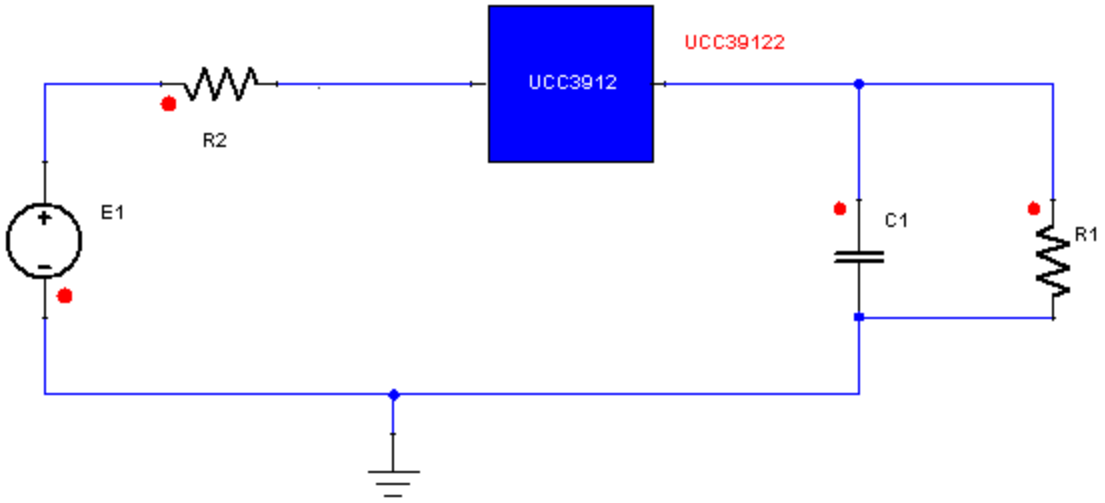

Figure 3. Application example of the UCC3912 Electronic Circuit Breaker (UCC39122)

Table 4. System Parameters

Component	Parameter	Value [unit]
Electronic Circuit Breaker UCC39122	Ron	0.15 [Ohm]
	I_max	4 [A]
	I_trip	3 [A]
	Fault_time	0.001 [s]
Voltage Source E1	EMF Value	8 [V]
Resistor R1	Resistance	70 [Ohm]
Resistor R2	Resistance	1 [Ohm]
Capacitor C1	Capacitance	0.001 [F]

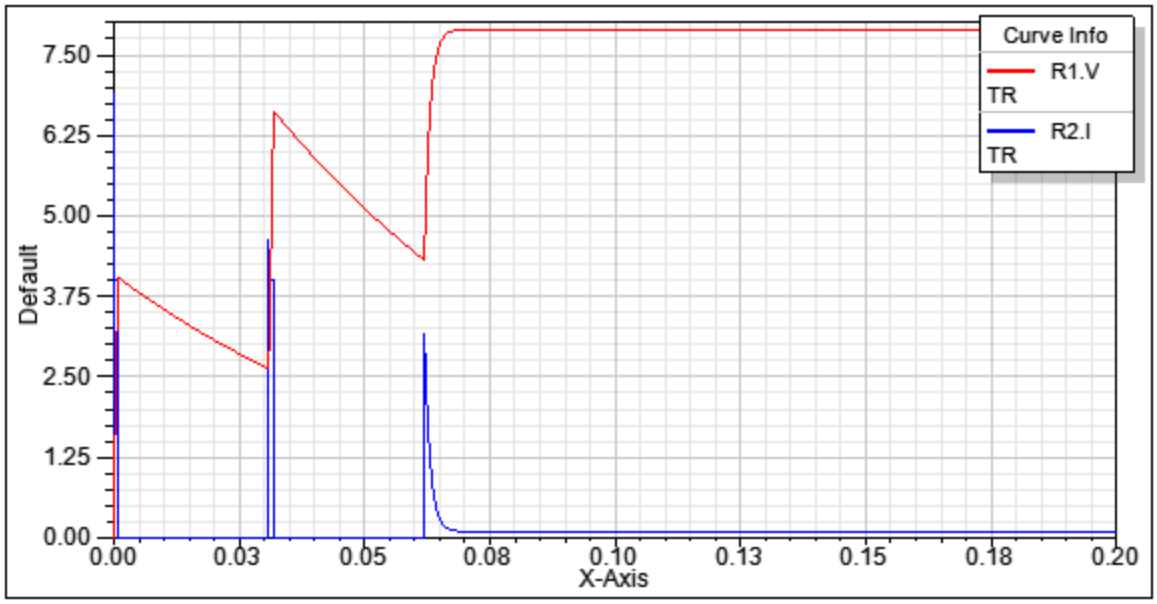

Figure 4. Simulation results – Source Current (R2.I) and Output Voltage (R2.V)

Top

References

Controllers

I_Cont Type I Controller

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

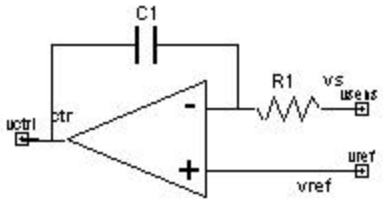

Figure 1. Component symbol

Description

This block represents an integral type controller.

Top

Assumptions and Limitations

Top

Mathematical Description

The sensed to output transfer function of this controller is given by:

$$G(s) = \frac{1}{R_1 \cdot C_1 \cdot s}$$

where s represents the Laplace's variable.

Top

Netlist Syntax

MODEL I_Cont ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vsens:= %0, vctrl:= %1, vref:= %2 (C1:= @C1, R1:= @R1, Vmin:= @Vmin, Vmax:= @Vmax) SRC: DB(Lib:-:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vsens	Sensed Voltage	Electrical terminal
vctrl	Controller Output Voltage	Electrical terminal
vref	Referenced Voltage	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
C1	Capacitance 1 Value	real	1e-9 [F]
R1	Resistor 1 Value	real	1000 [Ohm]
Vmin	Minimum output voltage	real	-15 [V]
Vmax	Maximum output voltage	real	15 [V]

Top

Example

This is an integral controller example. The example has both an AC and a Transient Solution Setup providing the frequency response of the controller and the transient response to an input square wave. The schematic of the example is shown in Figure 2, system parameters are listed in the table 3, and the simulation results are shown in Figure 3.

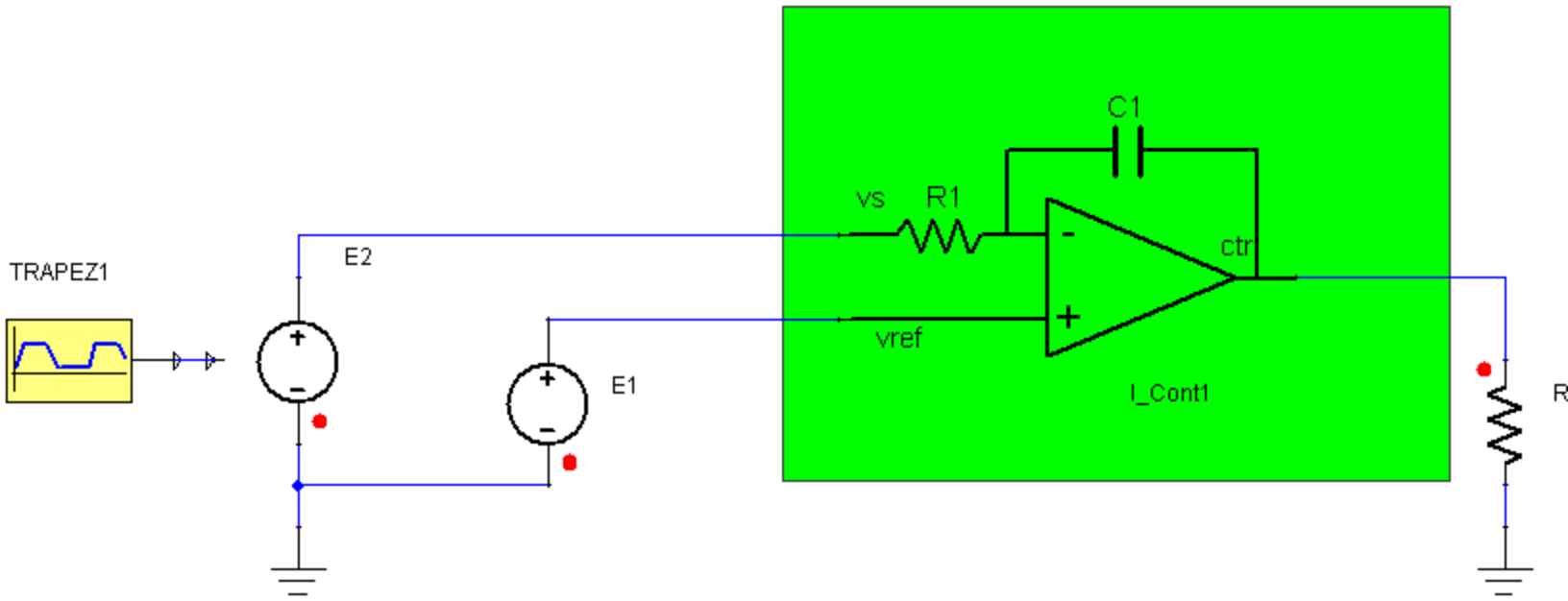

Figure 2. Application example of the Type I Integral Controller

Table 3. System Parameters

Component	Parameter	Value [unit]
Type I Integral Controller I_CONT1	C1	1e-007 [F]
	R1	1000 [Ohm]
	Vmin	-15 [V]
	Vmax	15 [V]
Voltage Source E1	EMF Value	0 [V]
Voltage Source E2	EMF Value	TRAPEZ1.VAL
Resistor R1	Resistance	1000[Ohm]
Trapezoidal Wave TRAPEZ1	TRISE	1e-006 [s]
	TFALL	1e-006 [s]
	PWIDTH	0.0005 [s]
	TPERIO	0.000502 [s]
	OFF	-0.5

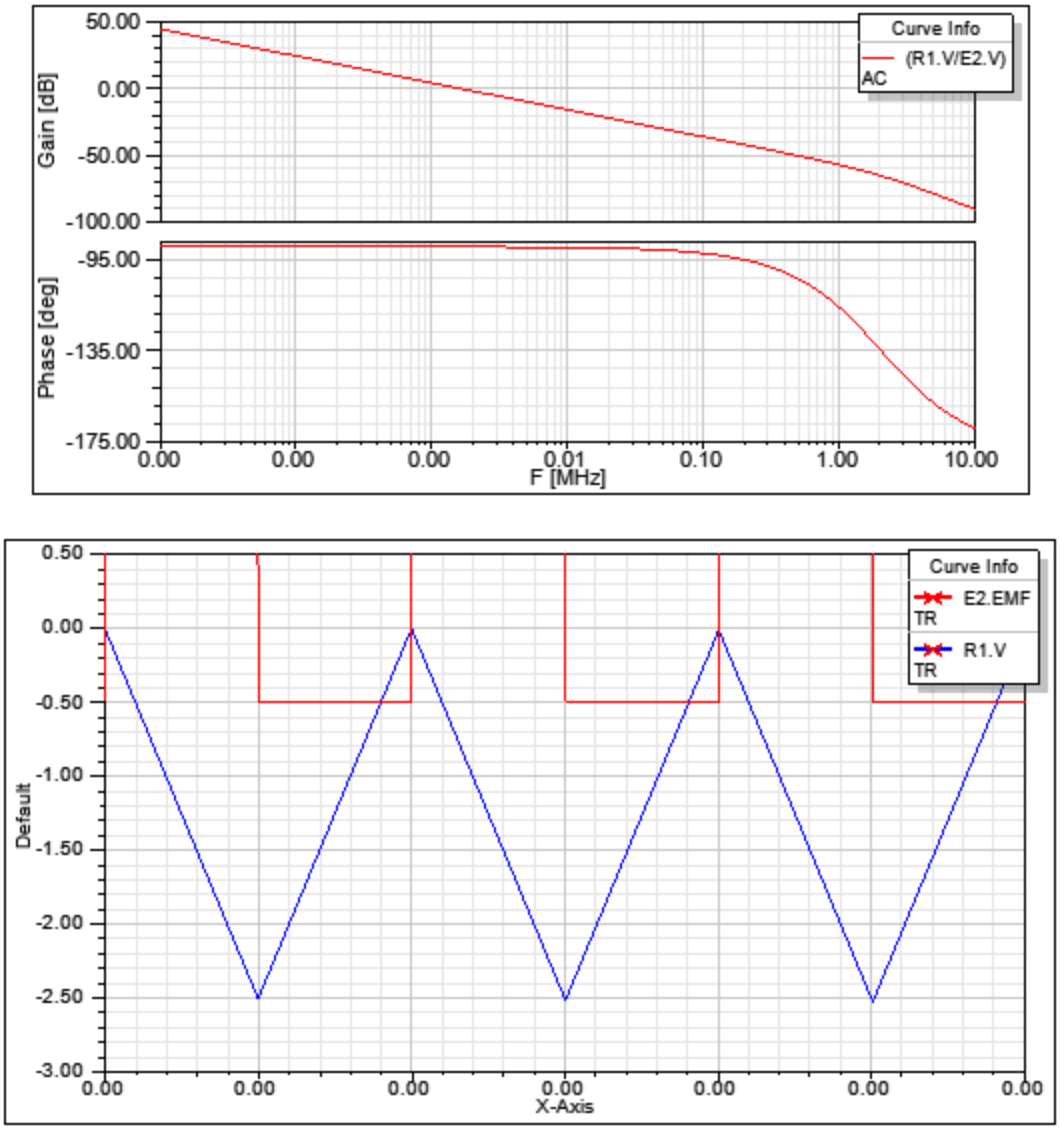

Figure 3. Simulation results – Frequency Response and Transient Response of the Type I Integral Controller I_CONT1

Top

References

PI_Cont Type II Controller

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

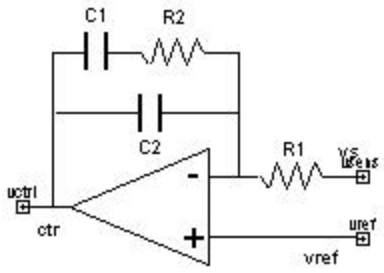

Figure 1. Component symbol

Description

This block represents a proportional-integral (PI) type controller.

Top

Assumptions and Limitations

Top

Mathematical Description

The sensed to output transfer function of this controller is given by:

$$G(s) = \frac{1 + \frac{s}{\omega z1}}{\frac{s}{\omega i} \cdot \left(1 + \frac{s}{\omega p1}\right)}$$

with:

$$\omega i = \frac{1}{R1 \cdot (C1 + C2)}$$

$$\omega z1 = \frac{1}{R2 \cdot C1}$$

$$\omega p1 = \frac{1}{R2 \cdot \frac{C1 \cdot C2}{C1 + C2}}$$

where s represents the Laplace's variable.

Top

Netlist Syntax

MODEL PI_Cont ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vsens:= %0, vctrl:= %1, vref:= %2 (C2:= @C2, C1:= @C1, R2:= @R2, R1:= @R1, Vmin:= @Vmin, Vmax:= @Vmax) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vsens	Sensed Voltage	Electrical terminal

vctrl	Controller Output Voltage	Electrical terminal
vref	Referenced Voltage	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
C1	Capacitance 1 Value	real	1e-8 [F]
R1	Resistor 1 Value	real	1000 [Ohm]
C2	Capacitance 2 Value	real	1e-8 [F]
R2	Resistor 2 Value	real	1000 [Ohm]
Vmin	Minimum output voltage	real	-15 [V]
Vmax	Maximum output voltage	real	15 [V]

Top

Example

This is an proportional-integral controller example. The example has both an AC and a Transient Solution Setup providing the frequency response of the controller and the transient response to an input square wave. The schematic of the example is shown in Figure 2, system parameters are listed in the table 3, and the simulation results are shown in Figure 3.

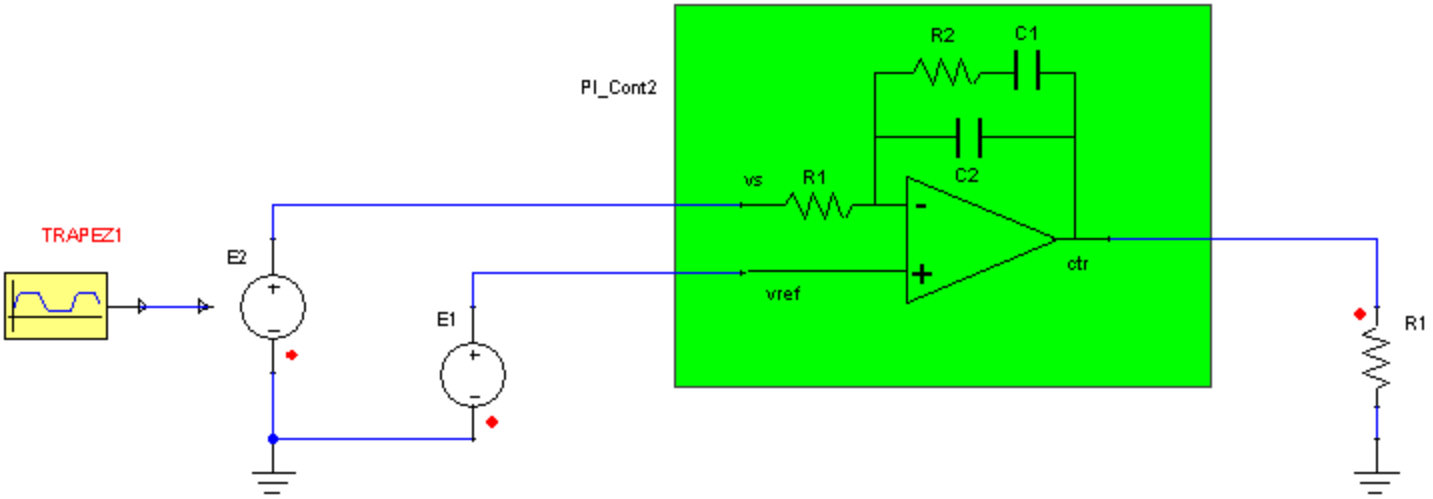

Figure 2. Application example of the Proportional Integral Controller

Table 3. System Parameters

Component	Parameter	Value [unit]
Proportional Integral Controller PI_CONT1	C1	2e-007 [F]
	R1	1000 [Ohm]
	C2	1e-008 [F]
	R2	10000 [Ohm]
	Vmin	-15 [V]
	Vmax	15 [V]
Voltage Source E1	EMF Value	0 [V]
Voltage Source E2	EMF Value	TRAPEZ1.VAL
Resistor R1	Resistance	1000[Ohm]
Trapezoidal Wave TRAPEZ1	TRISE	1e-006 [s]
	TFALL	1e-006 [s]
	PWIDTH	0.0005 [s]
	TPERIO	0.000502 [s]
	OFF	-0.5

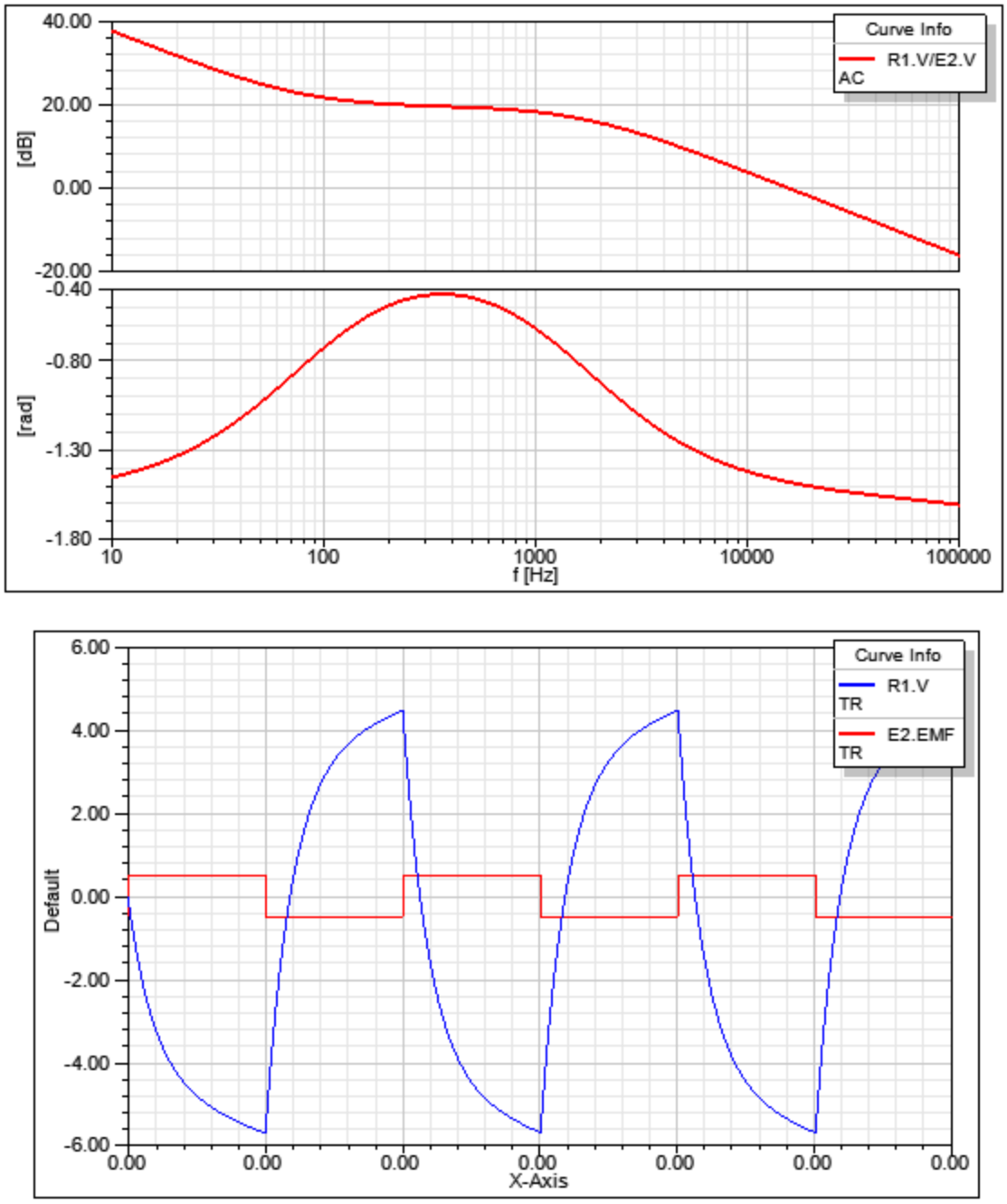

Figure 3. Simulation results – Frequency Response and Transient Response of the Proportional Integral Controller PI_CONT1

Top

References

PID_Cont Type III Controller

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

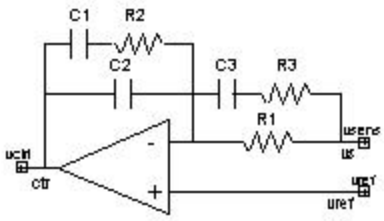

Figure 1. Component symbol

Description

This block represents a proportional-integral-derivative (PID) type controller.

Top

Assumptions and Limitations

Top

Mathematical Description

The sensed to output transfer function of this controller is given by:

$$G(s) = \frac{\left(1 + \frac{s}{\omega z1}\right) \cdot \left(1 + \frac{s}{\omega z2}\right)}{\frac{s}{\omega i} \cdot \left(1 + \frac{s}{\omega p1}\right) \cdot \left(1 + \frac{s}{\omega p2}\right)}$$

with:

$$\omega i = \frac{1}{R1 \cdot (C1 + C2)}$$

$$\omega z1 = \frac{1}{R2 \cdot C1}$$

$$\omega z2 = \frac{1}{(R1 + R3) \cdot C3}$$

$$\omega p1 = \frac{1}{R2 \cdot \frac{C1 \cdot C2}{C1 + C2}}$$

$$\omega p2 = \frac{1}{R3 \cdot C3}$$

where s represents the Laplace's variable.

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Netlist Syntax

MODEL PID_Cont ?InstanceName(@InstanceName):(@(Refbase)@(ID)) vsens:= %0, vctrl:= %1, vref:= %2 (C3:= @C3, C2:= @C2, C1:= @C1, R3:= @R3, R2:= @R2, R1:= @R1, Vmin:= @Vmin, Vmax:= @Vmax) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
vsens	Sensed Voltage	Electrical terminal
vctrl	Controller Output Voltage	Electrical terminal
vref	Referenced Voltage	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
C1	Capacitance 1 Value	real	1e-7 [F]
R1	Resistor 1 Value	real	1000 [Ohm]
C2	Capacitance 2 Value	real	1e-7 [F]
R2	Resistor 2 Value	real	1000 [Ohm]
C3	Capacitance 3 Value	real	1e-7 [F]
R3	Resistor 3 Value	real	1000 [Ohm]
Vmin	Minimum output voltage	real	-15 [V]
Vmax	Maximum output voltage	real	15 [V]

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Example

This is an proportional-integral-differential controller example. The example has both an AC and a Transient Solution Setup providing the frequency response of the controller and the transient response to an input square wave. The schematic of the example is shown in Figure 2, system parameters are listed in the table 3, and the simulation results are shown in Figure 3.

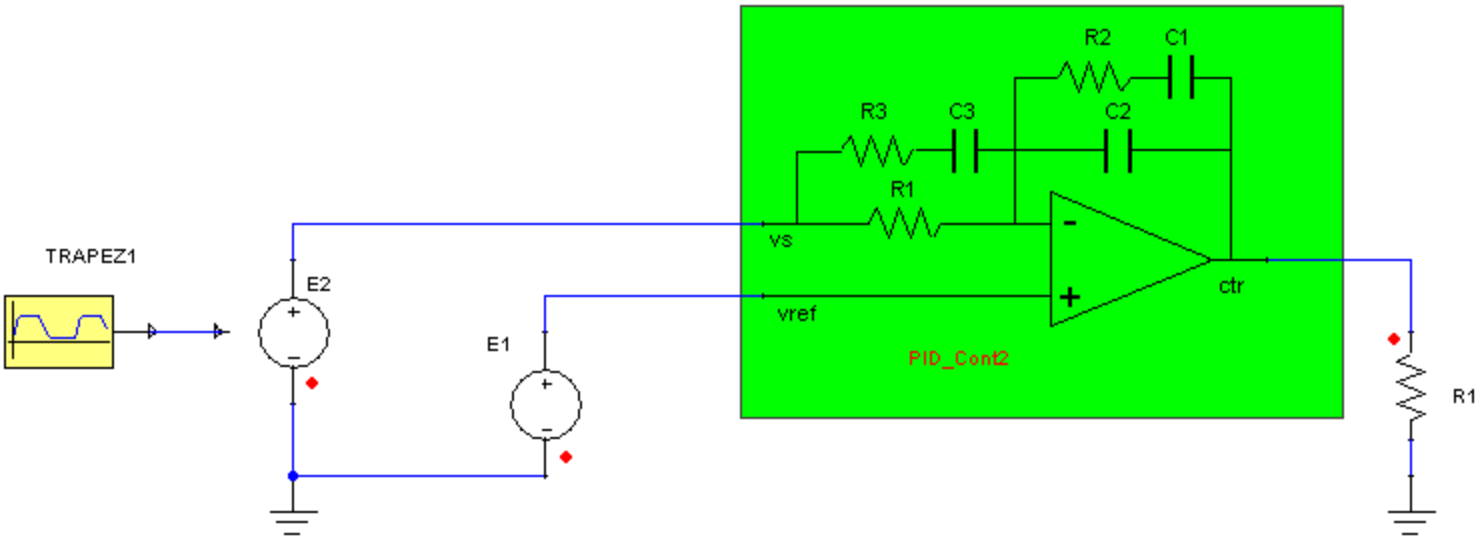

Figure 2. Application example of the Proportional Integral-Differential Controller

Table 3. System Parameters

Component	Parameter	Value [unit]
Proportional Integral-Differential Controller PID_CONT1	C1	1e-006 [F]
	R1	100000 [Ohm]
	C2	1e-007 [F]
	R2	1000 [Ohm]
	C3	1e-008 [F]
	R3	10000 [Ohm]
	Vmin	-15 [V]
	Vmax	15 [V]
Voltage Source E1	EMF Value	0 [V]
Voltage Source E2	EMF Value	TRAPEZ1.VAL
Resistor R1	Resistance	1000[Ohm]

Trapezoidal Wave TRAPEZ1	TRISE	1e-006 [s]
	TFALL	1e-006 [s]
	PWIDTH	0.0005 [s]
	TPERIO	0.000502 [s]
	OFF	-0.5

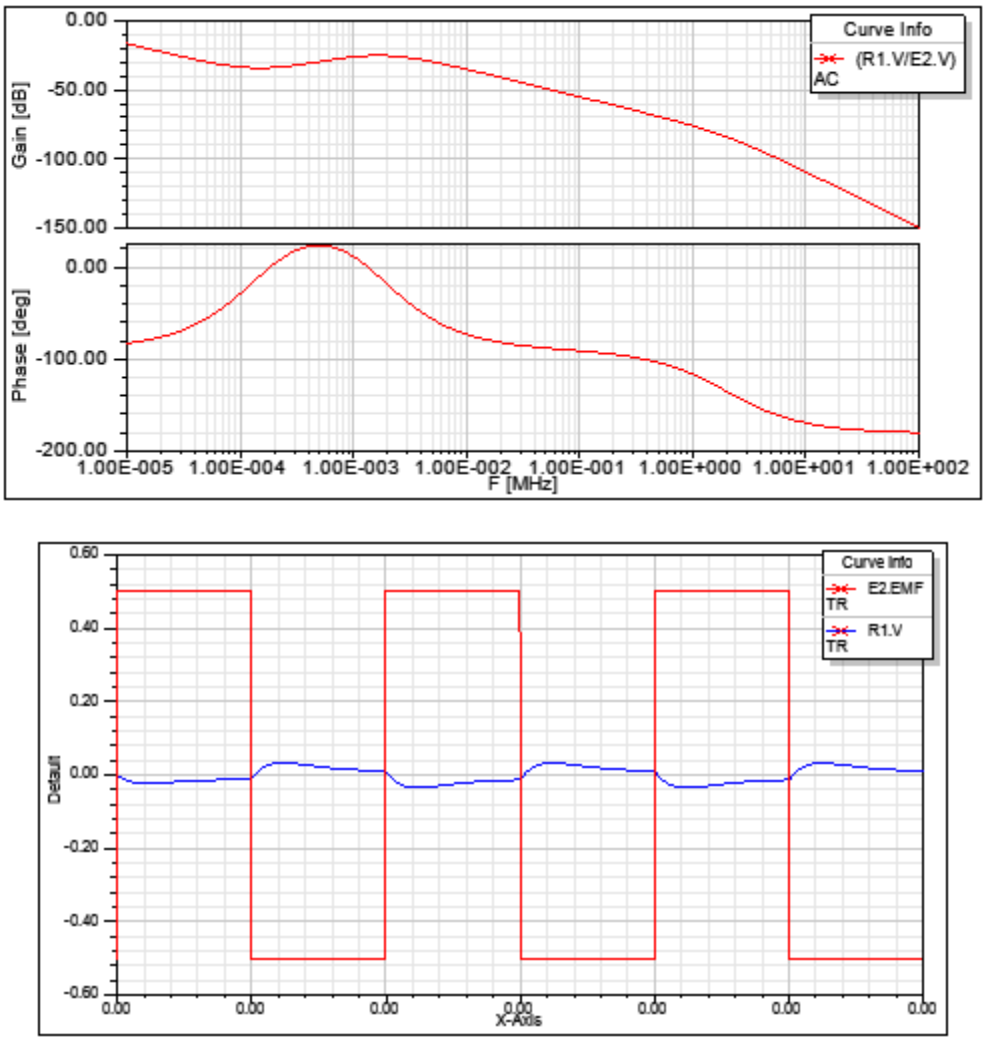

Figure 3. Simulation results – Frequency Response and Transient Response of the Proportional Integral Controller PI_CONT1

Top

References

Envelope Simulation

Complex Passive Elements

- Complex Capacitor (CCapacitor)
- Complex Inductor (CInductance)
- Complex Resistor (CResistor)

Complex Rectifiers

- Complex Full Wave Rectifier (CFullRectifier)
- Complex Half Wave Rectifier (CHallRectifier)

Complex Sources

- Complex Current Source (CCurrentSource)
- Complex Voltage Source (CVoltageSource)

Complex Transformers

- Complex Ideal Transformer (CIdealTransformer)

Envelope Simulation

Complex Passive Elements

- Complex Capacitor (CCapacitor)
- Complex Inductor (CInductance)
- Complex Resistor (CResistor)

Complex Rectifiers

- Complex Full Wave Rectifier (CFullRectifier)
- Complex Half Wave Rectifier (CHallRectifier)

Complex Sources

- Complex Current Source (CCurrentSource)
- Complex Voltage Source (CVoltageSource)

Complex Transformers

- Complex Ideal Transformer (CIdealTransformer)

Complex Capacitor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

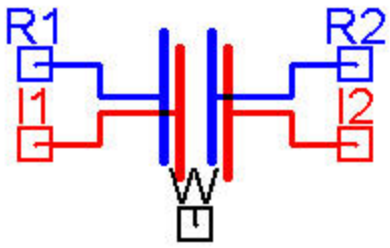

Figure 1. Component symbol

Description

This block models a complex capacitor.

Top

Assumptions and Limitations

Top

Mathematical Description

The complex capacitor behavior is described by:

$$i_R = C \cdot \frac{du_R}{dt} - C \cdot \omega \cdot u_I$$

$$i_I = C \cdot \frac{du_I}{dt} + C \cdot \omega \cdot u_R$$

Where U_R, U_I, and ω are functions of time.

The module of the voltage and the current are calculated according to:

$$|u| = \sqrt{u_R^{\,2} + u_I^{\,2}}$$

$$|i| = \sqrt{i_R^{\,2} + i_I^{\,2}}$$

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Netlist Syntax

MODEL CCapacitor ?InstanceName(@InstanceName):(@(Refbase)@(ID)) W:= %0, R1:= %1, R2:= %2, I1:= %3, I2:= %4 (C:= @C, MOD_IC:= @MOD_IC, PH_IC:= @PH_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
W	Frequency Node	Electrical terminal
R1	Real Node 1	Electrical terminal
R2	Real Node 2	Electrical terminal
I1	Imaginary Node 1	Electrical terminal
I2	Imaginary Node 2	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
C	Capacitance	real	[F]

MOD_IC	Initial Voltage Module	real	0 [V]
PH_IC	Initial Current Phase	real	0 [Deg]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Umodule	Voltage module [V]	Output	real
Imodule	Current module [A]	Output	real

Top

Example

See Example Power Converter Envelope Simulation

Top

References

Complex Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

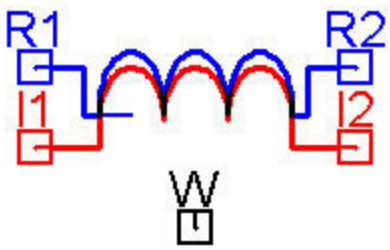

Figure 1. Component symbol

Description

This block models a complex inductor.

Top

Assumptions and Limitations

Top

Mathematical Description

The complex inductor behavior is described by:

$$u_R = L \cdot \frac{di_R}{dt} - L \cdot \omega \cdot i_I$$

$$u_I = L \cdot \frac{di_I}{dt} + L \cdot \omega \cdot i_R$$

Where U_R, U_I, and ω are functions of time.

The module of the voltage and the current are calculated according to:

$$|u| = \sqrt{u_R^{\,2} + u_I^{\,2}}$$

$$|i| = \sqrt{i_R^{\,2} + i_I^{\,2}}$$

Top

Netlist Syntax

MODEL CInductance ?InstanceName(@InstanceName):(@(Refbase)@(ID)) W:= %0, R1:= %1, R2:= %2, I1:= %3, I2:= %4 (L:= @L, PH_IC:= @PH_IC, MOD_IC:= @MOD_IC) SRC: DB (Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
W	Frequency Node	Electrical terminal
R1	Real Node 1	Electrical terminal
R2	Real Node 2	Electrical terminal
I1	Imaginary Node 1	Electrical terminal
I2	Imaginary Node 2	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Inductance	real	[H]

MOD_IC	Initial Current Module	real	0 [A]
PH_IC	Initial Current Phase	real	0 [Deg]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Umodule	Voltage module [V]	Output	real
Imodule	Current module [A]	Output	real

Top

Example

See Example Power Converter Envelope Simulation

Top

References

Complex Resistor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

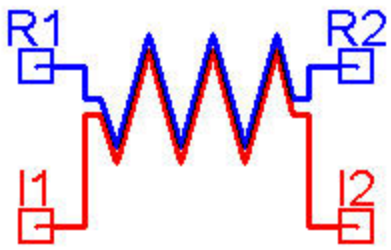

Figure 1. Component symbol

Description

This block models a complex resistor.

Top

Assumptions and Limitations

Top

Mathematical Description

The complex resistor behavior is described by:

$$u_R = R \cdot i_R$$

$$u_I = R \cdot i_I$$

Top

Netlist Syntax

MODEL CResistor ?InstanceName(@InstanceName):(@(Refbase)@(ID)) R1:= %0, R2:= %1, I1:= %2, I2:= %3 (R:= @R) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
R1	Real Node 1	Electrical terminal
R2	Real Node 2	Electrical terminal
I1	Imaginary Node 1	Electrical terminal
I2	Imaginary Node 2	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
R	Resistance	real	[Ohm]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Umodule	Voltage module [V]	Output	real
Imodule	Current module [A]	Output	real

Top

Example

See Example Power Converter Envelope Simulation

Top

References

Envelope Simulation

Complex Passive Elements

- Complex Capacitor (CCapacitor)
- Complex Inductor (CInductance)
- Complex Resistor (CResistor)

Complex Rectifiers

- Complex Full Wave Rectifier (CFullRectifier)
- Complex Half Wave Rectifier (CHallRectifier)

Complex Sources

- Complex Current Source (CCurrentSource)
- Complex Voltage Source (CVoltageSource)

Complex Transformers

- Complex Ideal Transformer (CIdealTransformer)

Complex Full-wave Rectifier

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

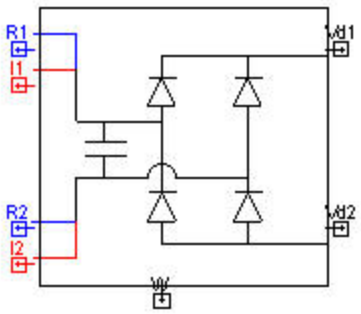

Figure 1. Component symbol

Description

This block models a complex full wave rectifier whose behavior is defined as:

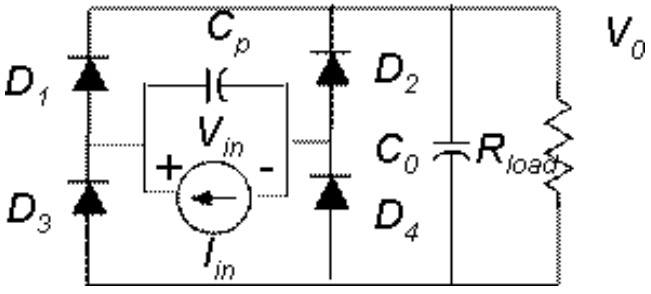

Figure 2. Full-Wave Rectifier

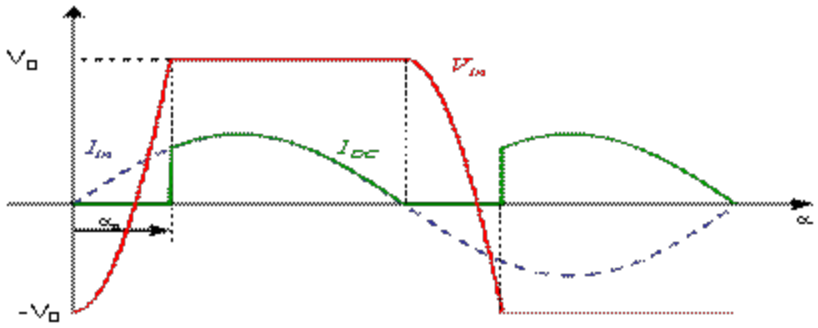

Figure 3. Main Waveforms of the Full-Wave Rectifier

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Assumptions and Limitations

Top

Mathematical Description

The complex full wave rectifier behavior is described by:

Table 1

Parameter	Full-wave Value
$\cos(\alpha_0)$	$1-\frac{2\cdot C_p\cdot\omega_s\cdot V_0}{I_m}$
Z_R	$\frac{1}{\pi\omega_s C_p}\cdot\sin(\alpha_0)^2$
Z_I	$\frac{1}{\pi\omega_s C_p}\cdot\left(\alpha_0-\sin(\alpha_0)\cos(\alpha_0)\right)$
I_{DC}	$\frac{1}{\pi}\cdot I_m\cdot\left(1+\cos(\alpha_0)\right)$

Where:

$$V_R = Z_R\cdot I_R - Z_I\cdot I_I$$

$$V_I = Z_R \cdot I_I + Z_I \cdot I_R$$

And the averaged current delivered to the DC load is:

$$I_{DC} = \frac{1}{\pi} \cdot I_m \cdot \left(1 + \cos(\alpha_0)\right)$$

Where V is the voltage module and φ is the phase. The module of the voltage and the current are calculated according to:

$$\left|u\right| = \sqrt{u_R{}^2 + u_I{}^2}$$

$$\left|i\right| = \sqrt{i_R{}^2 + i_I{}^2}$$

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Netlist Syntax

MODEL CFullRectifier ?InstanceName(@InstanceName):(@(Refbase)@(ID)) W:= %0, R1:= %1, R2:= %2, I1:= %3, I2:= %4, Vd1:= %5, Vd2:= %6 (C:= @C, Vd:= @Vd) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 2

Name	Port/Terminal description	Nature/Data type
W	Frequency Node	Electrical terminal
R1	AC Side Real Node 1	Electrical terminal
R2	AC Side Real Node 2	Electrical terminal
I1	AC Side Imaginary Node 1	Electrical terminal
I2	AC Side Imaginary Node 2	Electrical terminal
vd1	DC Side Positive Node	Electrical terminal
vd2	DC Side Negative Node	Electrical terminal

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Parameters

Table 3

Name	Description	Data Type	Default Value [Unit]
C	Input Capacitance	real	[F]
V_d	Diode Forward Voltage Drop	real	[V]

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Input/Output Quantities

Table 4

Name	Description [Unit]	Direction	Data Type
Umodule	Voltage module [V]	Output	real
Imodule	Current module [A]	Output	real

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Example

See Example Complex Power Converter Envelope Simulation

Top

References

Complex Half-wave Rectifier

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

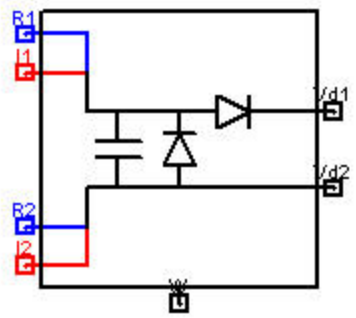

Figure 1. Component symbol

Description

This block models a complex half-wave rectifier whose behavior is defined as:

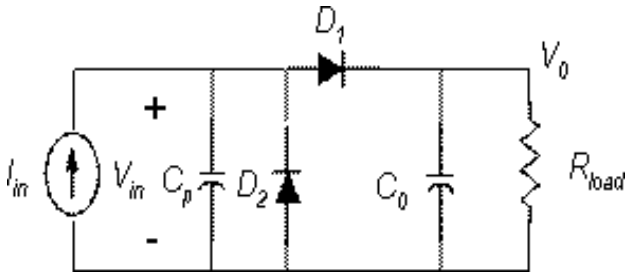

Figure 2. Half-Wave Rectifier

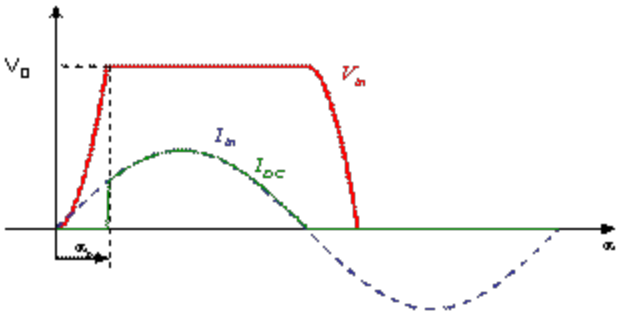

Figure 3. Main Waveforms of the Half-Wave Rectifier

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Assumptions and Limitations

Top

Mathematical Description

The complex half-wave rectifier behavior is described by:

Table 1

Parameter	Half-wave Rectifier Value
$\cos(\alpha_0)$	$1-\frac{C_p \cdot \omega_s \cdot V_0}{I_m}$
Z_R	$\frac{1}{\pi \omega_s C_p} \cdot \sin(\alpha_0)^2$
Z_I	$\frac{1}{\pi \omega_s C_p} \cdot (\alpha_0 - \sin(\alpha_0))$
I_{DC}	$\frac{1}{2\pi} \cdot I_m \cdot (1+\cos(\alpha_0))$

Where:

$$V_R = Z_R \cdot I_R - Z_I \cdot I_I$$

$$V_I = Z_R \cdot I_I + Z_I \cdot I_R$$

And the averaged current delivered to the DC load is:

$$I_{DC} = \frac{1}{\pi} \cdot I_m \cdot \left(1 + \cos(\alpha_0)\right)$$

Where V is the voltage module and φ is the phase. The module of the voltage and the current are calculated according to:

$$|u| = \sqrt{u_R{}^2 + u_I{}^2}$$

$$|i| = \sqrt{i_R{}^2 + i_I{}^2}$$

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Netlist Syntax

MODEL CHalfRectifier ?InstanceName(@InstanceName):(@(Refbase)@(ID)) W:= %0, R1:= %1, R2:= %2, I1:= %3, I2:= %4, Vd1:= %5, Vd2:= %6 (C:= @C, Vd:= @Vd) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 2

Name	Port/Terminal description	Nature/Data type
W	Frequency Node	Electrical terminal
R1	AC Side Real Node 1	Electrical terminal
R2	AC Side Real Node 2	Electrical terminal
I1	AC Side Imaginary Node 1	Electrical terminal
I2	AC Side Imaginary Node 2	Electrical terminal
vd1	DC Side Positive Node	Electrical terminal
vd2	DC Side Negative Node	Electrical terminal

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Parameters

Table 3

Name	Description	Data Type	Default Value [Unit]
C	Input Capacitance	real	[F]
V_d	Diode Forward Voltage Drop	real	[V]

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Input/Output Quantities

Table 4

Name	Description [Unit]	Direction	Data Type
Umodule	Voltage module [V]	Output	real
Imodule	Current module [A]	Output	real

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Example

See Example Power Converter Envelope Simulation

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References

Envelope Simulation

Complex Passive Elements

- Complex Capacitor (CCapacitor)
- Complex Inductor (CInductance)
- Complex Resistor (CResistor)

Complex Rectifiers

- Complex Full Wave Rectifier (CFullRectifier)
- Complex Half Wave Rectifier (CHallRectifier)

Complex Sources

- Complex Current Source (CCurrentSource)
- Complex Voltage Source (CVoltageSource)

Complex Transformers

- Complex Ideal Transformer (CIdealTransformer)

Complex Current Source

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

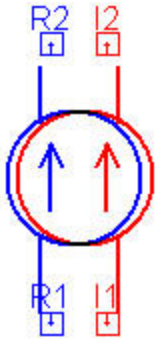

Figure 1. Component symbol

Description

This block models a complex current source.

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Assumptions and Limitations

Top

Mathematical Description

The complex complex current source behavior is described by:

$$I_R = I \cdot \cos(\varphi)$$

$$I_I = I \cdot \sin(\varphi)$$

Where V is the voltage module and φ is the phase. The module of the voltage and the current are calculated according to:

$$|u| = \sqrt{u_R{}^2 + u_I{}^2}$$

$$|i| = \sqrt{i_R{}^2 + i_I{}^2}$$

Top

Netlist Syntax

MODEL CCurrentSource ?InstanceName(@InstanceName):(@(Refbase)@(ID)) R1:= %0, R2:= %1, I1:= %2, I2:= %3 (PHI:= @PHI, I:= @I) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
R1	Real Node 1	Electrical terminal
R2	Real Node 2	Electrical terminal
I1	Imaginary Node 1	Electrical terminal
I2	Imaginary Node 2	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
I	Current Module	real	[A]
PHI	Current Phase	real	[Deg]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Umodule	Voltage module [V]	Output	real
Imodule	Current module [A]	Output	real

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Example

See Example Power Converter Envelope Simulation

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References

Complex Voltage Source

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

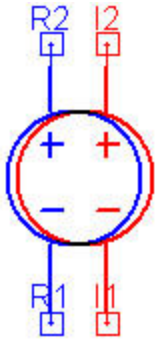

Figure 1. Component symbol

Description

This block models a complex voltage source.

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Assumptions and Limitations

Top

Mathematical Description

The complex complex current source behavior is described by:

$$V_R = V \cdot \cos(\varphi)$$

$$V_I = V \cdot \sin(\varphi)$$

Where V is the voltage module and φ is the phase. The module of the voltage and the current are calculated according to:

$$|u| = \sqrt{u_R^{\,2} + u_I^{\,2}}$$

$$|i| = \sqrt{i_R^{\,2} + i_I^{\,2}}$$

Top

Netlist Syntax

MODEL CVoltageSource ?InstanceName(@InstanceName):(@(Refbase)@(ID)) R1:= %0, R2:= %1, I1:= %2, I2:= %3 (V:= @V, PHI:= @PHI) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
R1	Real Node 1	Electrical terminal
R2	Real Node 2	Electrical terminal
I1	Imaginary Node 1	Electrical terminal
I2	Imaginary Node 2	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
V	Voltage Module	real	[V]
PHI	Voltage Phase	real	[Deg]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Umodule	Voltage module [V]	Output	real
Imodule	Current module [A]	Output	real

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Example

See Example Power Converter Envelope Simulation

Top

References

Envelope Simulation

Complex Passive Elements

- Complex Capacitor (CCapacitor)
- Complex Inductor (CInductance)
- Complex Resistor (CResistor)

Complex Rectifiers

- Complex Full Wave Rectifier (CFullRectifier)
- Complex Half Wave Rectifier (CHallRectifier)

Complex Sources

- Complex Current Source (CCurrentSource)
- Complex Voltage Source (CVoltageSource)

Complex Transformers

- Complex Ideal Transformer (CIdealTransformer)

Complex Ideal Transformer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

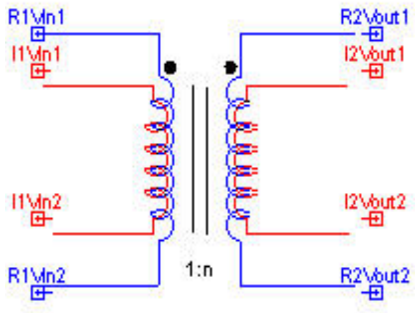

Figure 1. Component symbol

Description

This block models an ideal complex transformer.

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Assumptions and Limitations

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Mathematical Description

The relation between complex primary and secondary voltages and currents is given by:

$$\vec{v}_2 = n \cdot \vec{v}_1$$

$$\vec{i}_1 = n \cdot \vec{i}_2$$

Where the symbol → indicates a complex variable. This relation is implemented in terms of their real and imaginary parts as follows:

$$V_{2R} = n \cdot V_{1R}$$

$$V_{2I} = n \cdot V_{1I}$$

$$I_{1R} = n \cdot I_{2R}$$

$$I_{1I} = n \cdot I_{2I}$$

Top

Netlist Syntax

MODEL CIdealTransformer ?InstanceName(@InstanceName):(@(Refbase)@(ID)) I1Vin1:= %0, I1Vin2:= %1, I2Vout1:= %2, I2Vout2:= %3, R1Vin1:= %4, R1Vin2:= %5, R2Vout2:= %6, R2Vout1:= %7 (n:= @n) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
R1vin1	Primary Side Real Node vin1	Electrical terminal
R2vin2	Primary Side Real Node vin2	Electrical terminal
I1vin1	Primary Side Imaginary Node vin1	Electrical terminal
I2vin2	Primary Side Imaginary Node vin2	Electrical terminal
R1vout1	Secondary Side Real Node vout1	Electrical terminal
R2vout2	Secondary Side Real Node vout2	Electrical terminal
I1vout1	Secondary Side Imaginary Node vout1	Electrical terminal
I2vout2	Secondary Side Imaginary Node vout2	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
n	Number of Secondary Turns	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
U1module	Primary Side Voltage module [V]	Output	real
I1module	Primary Side Current module [A]	Output	real
U2module	Secondary Side Voltage module [V]	Output	real
I2module	Secondary Side Current module [A]	Output	real

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Example

See Example Complex Power Converter Envelope Simulation

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References

Multiphase Converters

2 Phase Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

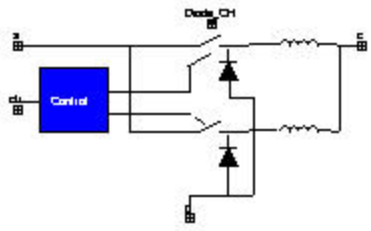

Figure 1. Component symbol

Description

This block represents the switch level model of a 2 Phases Buck converter. It accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to program the phase of each phase independently.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

MODEL BUCK_2PH_SW ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, c:= %1, ctr:= %2, p:= %3 (Phase1_DEG:= @Phase1_DEG, Phase2_DEG:= @Phase2_DEG, Rw:= @Rw, L2_IC:= @L2_IC, Diode_CH:= @Diode_CH, L1_IC:= @L1_IC, L:= @L, Fs:= @Fs, Rsa:= @Rsa) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	Active Node	Electrical terminal
p	Passive Node	Electrical terminal
c	Common Node	Electrical terminal
ctrl	Control Node	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
F_s	Switching Frequency	real	1e+5 [Hz]
Phase1_DEG	Delay of Phase 1	real	0 [Deg]
Phase2_DEG	Delay of Phase 2	real	180 [Deg]
L	Inductance per Phase	real	1e-5 [H]
R_w	Inductance Resistance of each Phase	real	.001 [Ohm]
L1_IC	Initial Current of Phase 1 Inductance	real	0 [A]
L2_IC	Initial Current of Phase 2 Inductance	real	0 [A]
R_{sa}	Active Switch Conduction Resistance	real	0.01 [Ohm]
Diode_CH	Diode Characteristics	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
iL1	Phase 1 Inductor Current [A]	Output	real
iL2	Phase 2 Inductor Current [A]	Output	real

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Example

In this example, a 2 Phase Buck converter is used to switch a source to a complex load. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

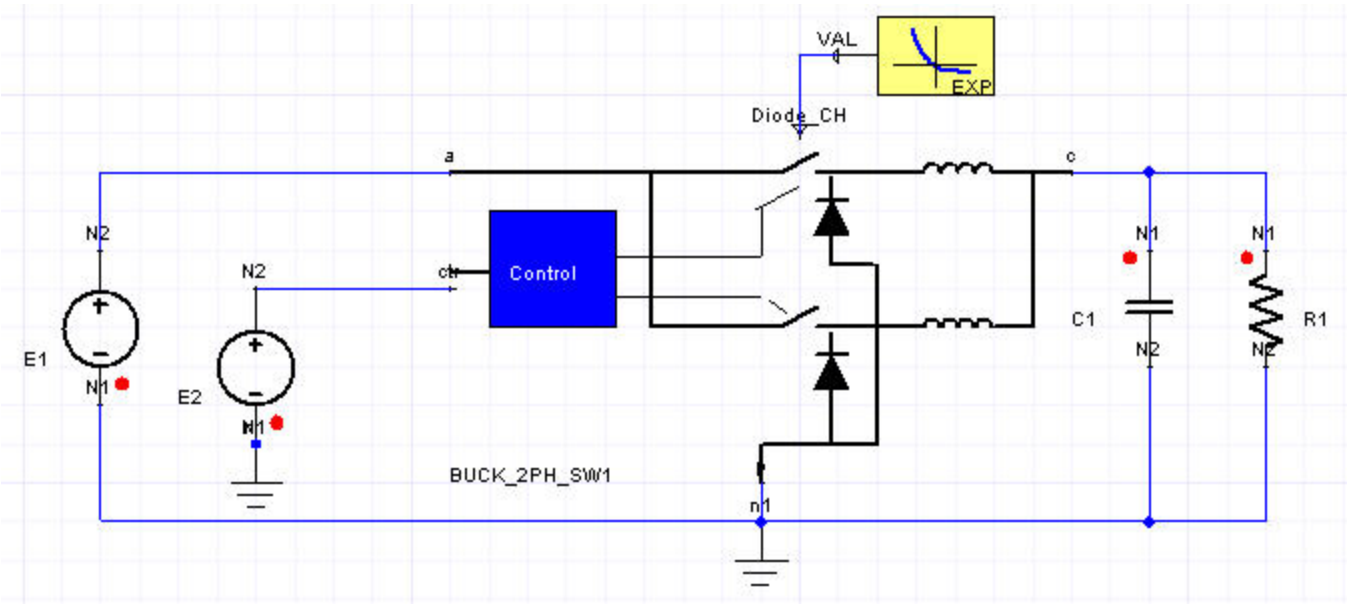

Figure 3. Application example of the 2 Phase Buck Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
2 Phase Buck Converter Buck_2PH_SW1	L	3e-5 [H]
	Diode_CH	EXP.VAL
Voltage Source E1	EMF Value	42 [V]
	TPERIO	T_{end}-1

Voltage Source E2	EMF Value	12/42 [V]
	TPERIO	T_{end}-1
Capacitor C1	Capacitance	7.5e-5 [F]
Resistor R1	Resistance	0.24 [Ohm]
Exponential Function EXP	VT	0.035 [V]
	ISAT	1e-12 [A]
	RR	100000 [Ohm]

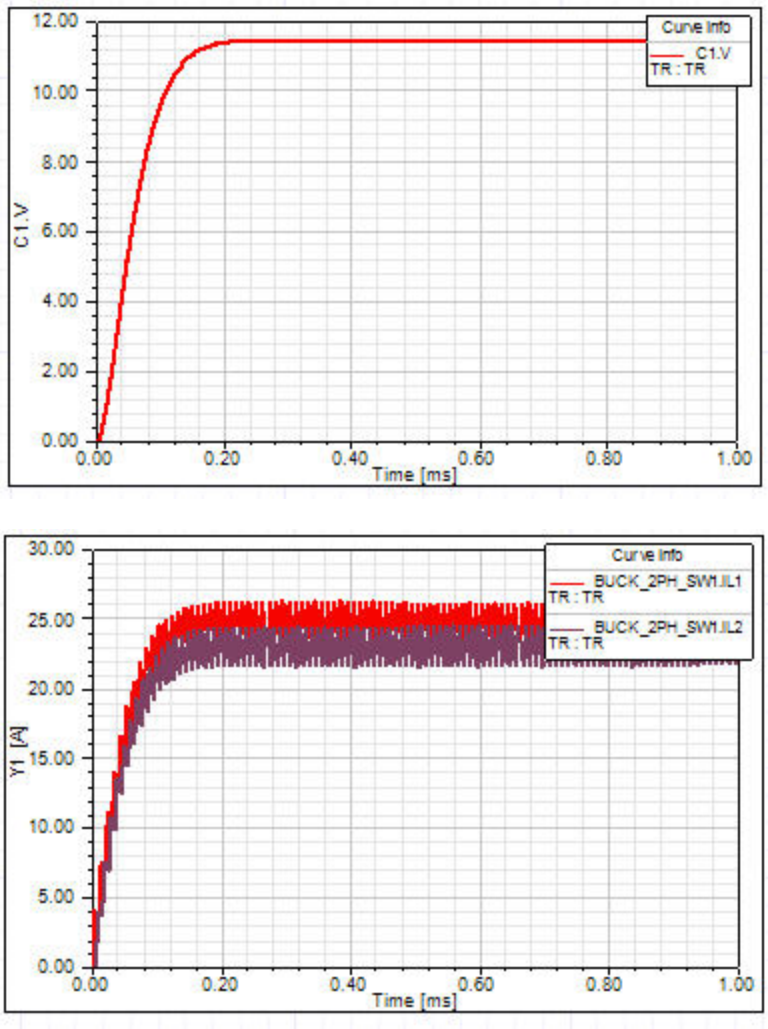

Figure 4. Simulation results – Output Voltage and Phase Currents of the 2 Phase Buck Converter

Top

References

2 Phase Synchronous Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

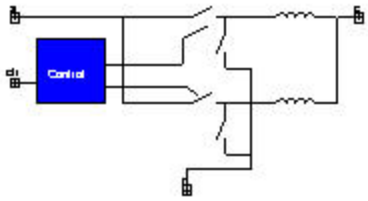

Figure 1. Component symbol

Description

This block represents the switch level model of a 2 Phases Synchronous Buck converter. It accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to program the phase of each phase independently.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

MODEL BUCK_SYNC_2PH_SW ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, c:= %1, ctr:= %2, p:= %3 (Fs:= @Fs, L:= @L, L1_IC:= @L1_IC, Rsa:= @Rsa, Phase1_DEG:= @Phase1_DEG, Phase2_DEG:= @Phase2_DEG, Rw:= @Rw, L2_IC:= @L2_IC) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	Active Node	Electrical terminal
p	Passive Node	Electrical terminal
c	Common Node	Electrical terminal
ctrl	Control Node	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
F_s	Switching Frequency	real	1e+005 [Hz]
Phase1_DEG	Delay of Phase 1	real	0 [Deg]
Phase2_DEG	Delay of Phase 2	real	180 [Deg]
L	Inductance per Phase	real	1e-005 [H]
R_w	Inductance Resistance of each Phase	real	0.001 [Ohm]
L1_IC	Initial Current of Phase 1 Inductance	real	0 [A]
L2_IC	Initial Current of Phase 2 Inductance	real	0 [A]
R_{sa}	Active Switch Conduction Resistance	real	0.01 [Ohm]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
iL1	Phase 1 Inductor Current [A]	Output	real
iL2	Phase 2 Inductor Current [A]	Output	real

Top

Example

In this example, a 2 Phase Synchronous Buck Converter is used to switch a source voltage to a complex load. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

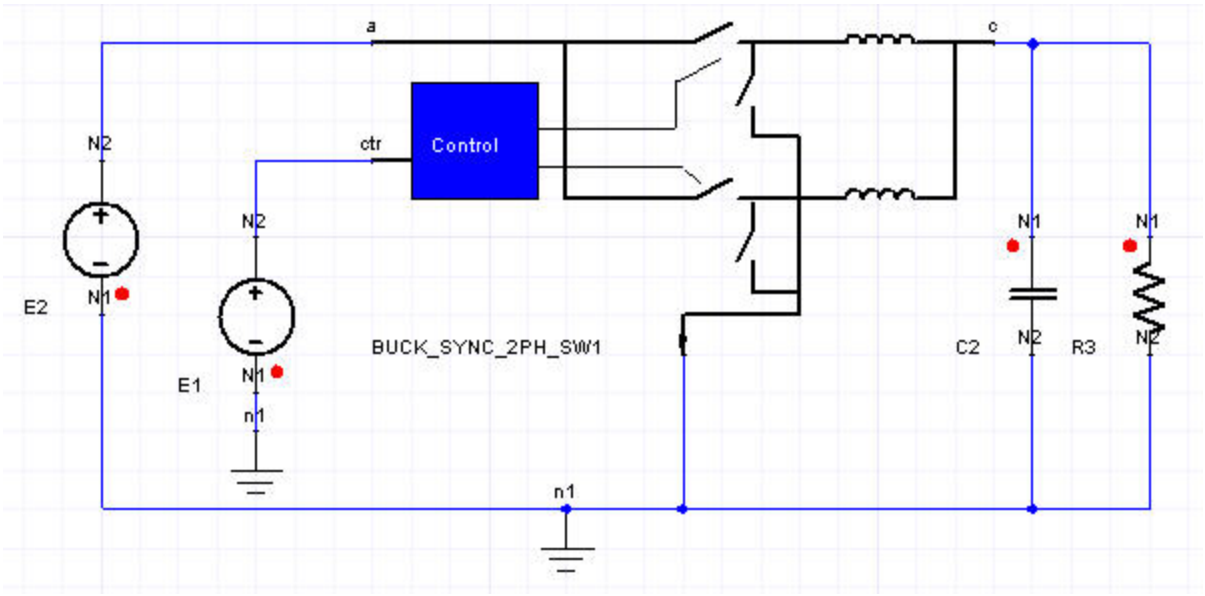
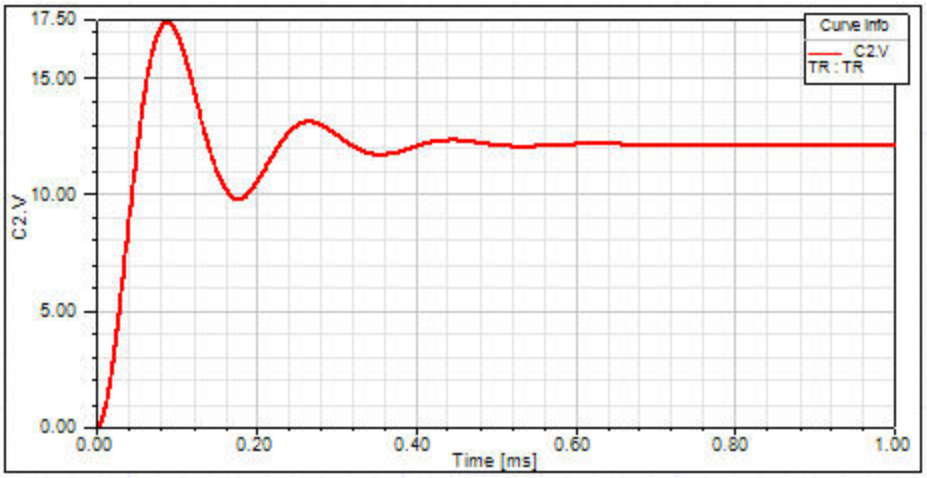


Figure 3. Application example of 2 Phase Synchronous Buck Converter

Table 4. System Parameters

Component	Parameter	Value [unit]

2 Phase Synchronous Buck Converter BUCK_SYNC_2PH_SW1	L	3e-5 [H]
	Rsa	0.01 [Ohm]
	Phase_DEG1	0 [Deg]
	Phase_DEG2	180 [Deg]
	Fs	100000 [Hz]
	L1_IC	0.1 [A]
	L2_IC	0 [A]
Voltage Source E1	EMF Value	0.5 [V]
	TPERIO	T_{end}-1
Voltage Source E2	EMF Value	25 [V]
	TPERIO	T_{end}-1
Capacitor C1	Capacitance	5e-5 [F]
Resistor R1	Resistance	1.1 [Ohm]



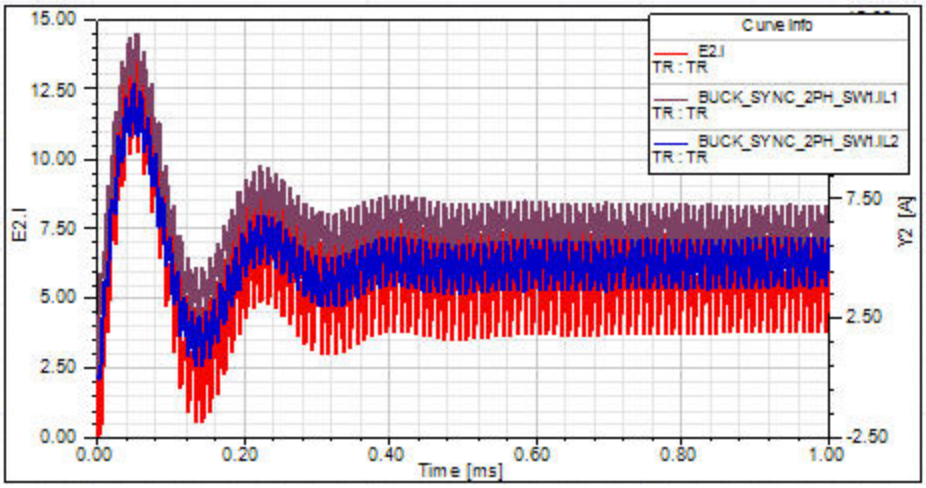


Figure 4. Simulation results – Output voltage and Phase currents of the 2 Phase Synchronous Buck Converter

Top

References

3 Phase Synchronous Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

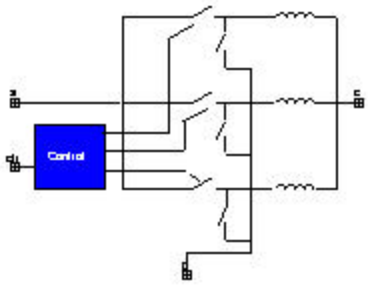


Figure 1. Component symbol

Description

This block represents the switch level model of a 3 Phases Synchronous Buck converter. It accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to program the phase of each phase independently.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

MODEL BUCK_SYNC_3PH_SW ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, c:= %1, ctr:= %2, p:= %3 (Phase2_DEG:= @Phase2_DEG, Rw:= @Rw, L2_IC:= @L2_IC, Phase3_DEG:= @Phase3_DEG, L3_IC:= @L3_IC, L:= @L, Fs:= @Fs, L1_IC:= @L1_IC, Rsa:= @Rsa, Phase1_DEG:= @Phase1_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	Active Node	Electrical terminal
p	Passive Node	Electrical terminal
c	Common Node	Electrical terminal
ctrl	Control Node	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
F_s	Switching Frequency	real	1e+005 [Hz]
Phase1_DEG	Delay of Phase 1	real	0 [Deg]
Phase2_DEG	Delay of Phase 2	real	120 [Deg]
Phase3_DEG	Delay of Phase 3	real	-120 [Deg]
L	Inductance per Phase	real	1e-005 [H]
R_w	Inductance Resistance of each Phase	real	0.001 [Ohm]
L1_IC	Initial Current of Phase 1 Inductance	real	0 [A]
L2_IC	Initial Current of Phase 2 Inductance	real	0 [A]
L3_IC	Initial Current of Phase 3 Inductance	real	0 [A]
R_{sa}	Active Switch Conduction Resistance	real	0.01 [Ohm]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
iL1	Phase 1 Inductor Current [A]	Output	real
iL2	Phase 2 Inductor Current [A]	Output	real
iL3	Phase 3 Inductor Current [A]	Output	real

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Example

In this example, a 3 Phase Synchronous Buck Converter is used to switch a source voltage to a complex load. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

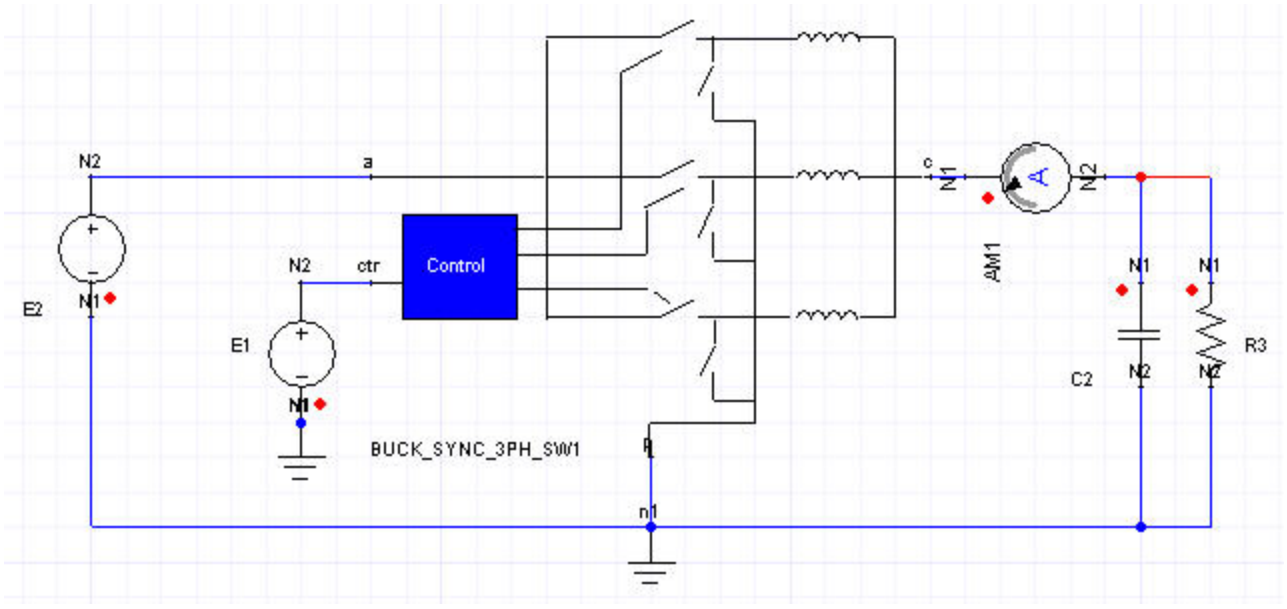
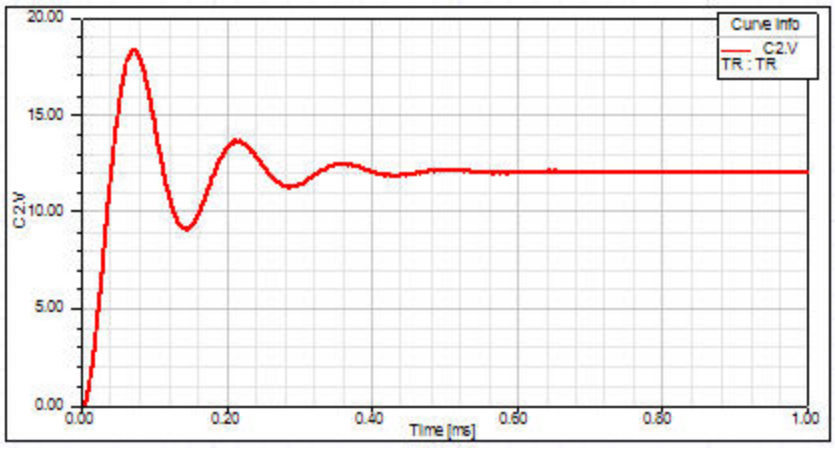


Figure 3. Application example of the 3 Phase Synchronous Buck Converter

Table 4. System Parameters

Component	Parameter	Value [unit]

3 Phase Synchronous Buck Converter BUCK_SYNC_3PH_SW1	L	3e-5 [H]
	Rsa	0.01 [Ohm]
	Rw	0.01 [Ohm]
	Phase_DEG1	0 [Deg]
	Phase_DEG2	180 [Deg]
	Fs	100000 [Hz]
	L1_IC	0.1 [A]
	L2_IC	0 [A]
Voltage Source E1	EMF Value	0.5 [V]
	TPERIO	T_{end}-1
Voltage Source E2	EMF Value	25 [V]
	TPERIO	T_{end}-1
Capacitor C1	Capacitance	5e-5 [F]
Resistor R1	Resistance	1.1 [Ohm]



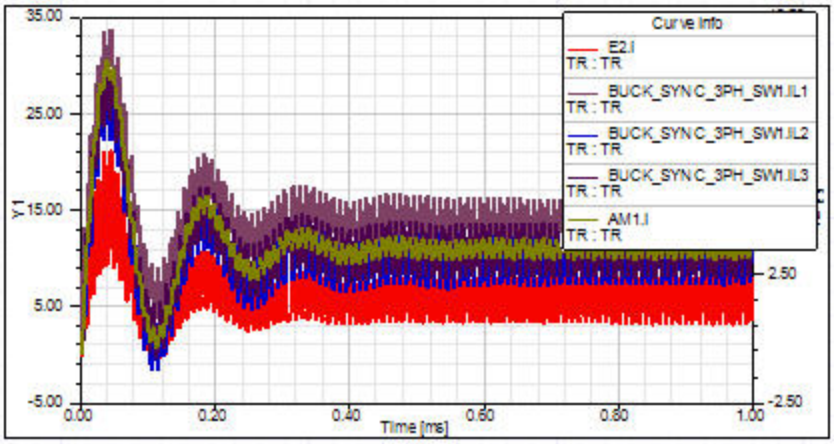


Figure 4. Simulation results – Output voltage and Phase currents of the 3 Phase Synchronous Buck Converter

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References

4 Phase Synchronous Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

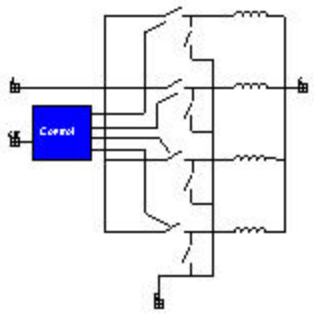

Figure 1. Component symbol

Description

This block represents the switch level model of a 4 Phases Synchronous Buck converter. It accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to program the phase of each phase independently.

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Netlist Syntax

MODEL BUCK_SYNC_4PH_SW ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, c:= %1, ctr:= %2, p:= %3 (Phase2_DEG:= @Phase2_DEG, Rw:= @Rw, L2_IC:= @L2_IC, Phase3_DEG:= @Phase3_DEG, L3_IC:= @L3_IC, L:= @L, Fs:= @Fs, L1_IC:= @L1_IC, Rsa:= @Rsa, Phase1_DEG:= @Phase1_DEG, L4_IC:= @L4_IC, Phase4_DEG:= @Phase4_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	Active Node	Electrical terminal
p	Passive Node	Electrical terminal
c	Common Node	Electrical terminal
ctrl	Control Node	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
F_s	Switching Frequency	real	1e+005 [Hz]
Phase1_DEG	Delay of Phase 1	real	0 [Deg]
Phase2_DEG	Delay of Phase 2	real	90 [Deg]
Phase3_DEG	Delay of Phase 3	real	180 [Deg]
Phase4_DEG	Delay of Phase 4	real	270 [Deg]
L	Inductance per Phase	real	1e-005 [H]
R_w	Inductance Resistance of each Phase	real	0.001 [Ohm]
L1_IC	Initial Current of Phase 1 Inductance	real	0 [A]
L2_IC	Initial Current of Phase 2 Inductance	real	0 [A]
L3_IC	Initial Current of Phase 3 Inductance	real	0 [A]
L4_IC	Initial Current of Phase 4	real	0 [A]

	Inductance		
R_{sa}	Active Switch Conduction Resistance	real	0.01 [Ohm]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
iL1	Phase 1 Inductor Current [A]	Output	real
iL2	Phase 2 Inductor Current [A]	Output	real
iL3	Phase 3 Inductor Current [A]	Output	real
iL4	Phase 4 Inductor Current [A]	Output	real

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Example

In this example, a 4 Phase Synchronous Buck Converter is used to switch a source voltage to a complex load. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

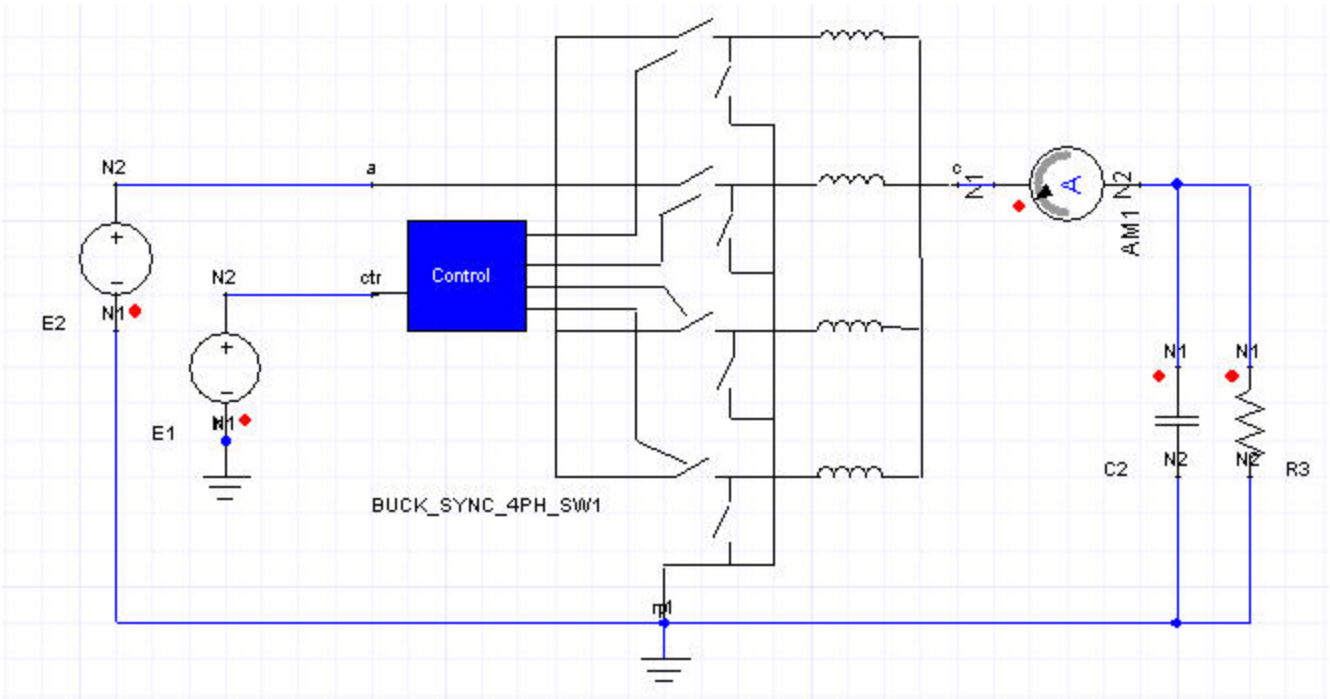
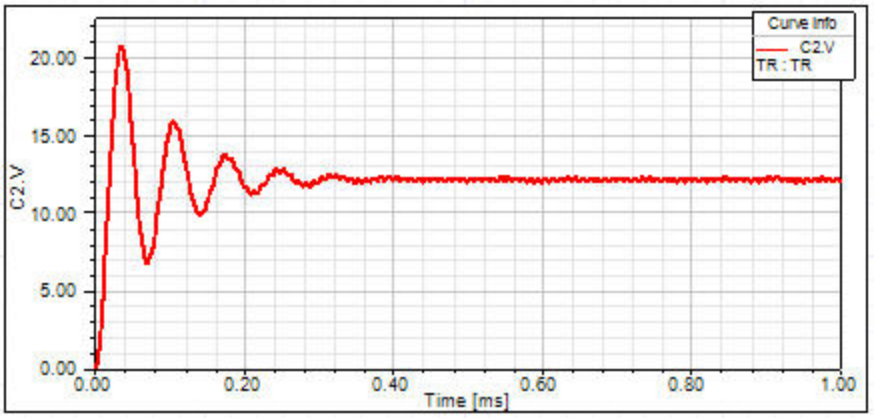


Figure 3. Application example of the 4 Phase Synchronous Buck Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
4 Phase Synchronous Buck Converter BUCK_SYNC_4PH_SW1	L	1e-5 [H]
	Rsa	0.01 [Ohm]
	Rw	0.001 [Ohm]
	Phase_DEG1	0 [Deg]
	Phase_DEG2	90 [Deg]
	Phase_DEG3	180 [Deg]
	Phase_DEG4	270 [Deg]
	Fs	100000 [Hz]
	L1_IC/L2_IC/L3_IC/L4_IC	0 [A]
Voltage Source E1	EMF Value	0.5 [V]
	TPERIO	T_{end}-1
Voltage Source E2	EMF Value	25 [V]
	TPERIO	T_{end}-1
Capacitor C1	Capacitance	5e-5 [F]
Resistor R1	Resistance	1.1 [Ohm]



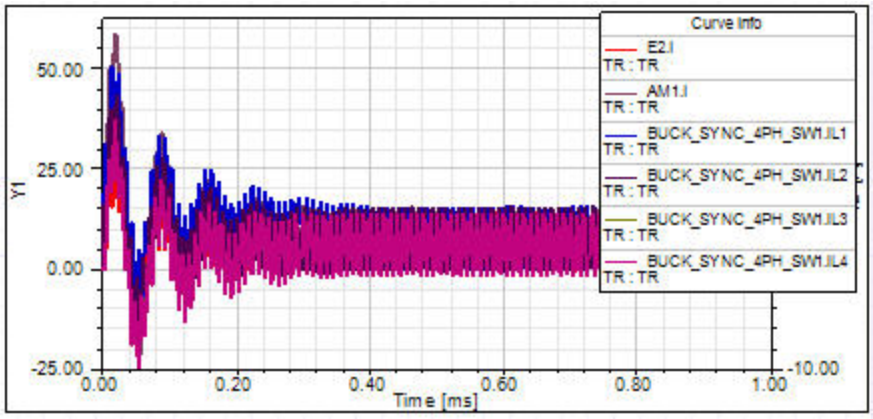


Figure 4. Simulation results – Output voltage and Phase currents of the 4 Phase Synchronous Buck Converter

Top

References

3 Phase Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

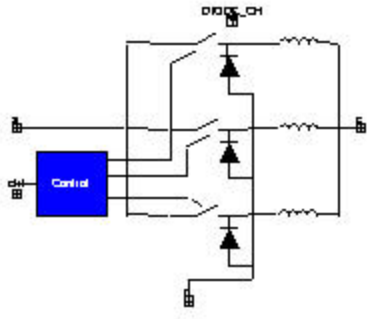


Figure 1. Component symbol

Description

This block represents the switch level model of a 3 Phase Buck converter. It accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to program the phase of each phase independently.

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Netlist Syntax

MODEL Buck3 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, c:= %1, p:= %2, ctrl:= %3 (Rsa:= @Rsa, Phase_DEG1:= @Phase_DEG1, Phase_DEG2:= @Phase_DEG2, Phase_DEG3:= @Phase_DEG3, Fs:= @Fs, L:= @L, L_IC:= @L_IC, DIODE_CH:= @DIODE_CH, Rw:= @Rw) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	Active Node	Electrical terminal
p	Passive Node	Electrical terminal
c	Common Node	Electrical terminal
ctrl	Control Node	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
F_s	Switching Frequency	real	1e+5 [Hz]
Phase1_DEG	Delay of Phase 1	real	0 [Deg]
Phase2_DEG	Delay of Phase 2	real	120 [Deg]
Phase3_DEG	Delay of Phase 3	real	-120 [Deg]
L	Inductance per Phase	real	1e-5 [H]
R_w	Inductance Resistance of each Phase	real	.001 [Ohm]
L1_IC	Initial Current of Phase 1 Inductance	real	0 [A]
L2_IC	Initial Current of Phase 2 Inductance	real	0 [A]
L3_IC	Initial Current of Phase 3 Inductance	real	0 [A]
R_{sa}	Active Switch Conduction Resistance	real	0.01 [Ohm]
Diode_CH	Diode Characteristics	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
iL1	Phase 1 Inductor Current [A]	Output	real
iL2	Phase 2 Inductor Current [A]	Output	real
iL3	Phase 3 Inductor Current [A]	Output	real

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Example

In this example, a 3 Phase Buck Converter is used to switch a source voltage to a complex load. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

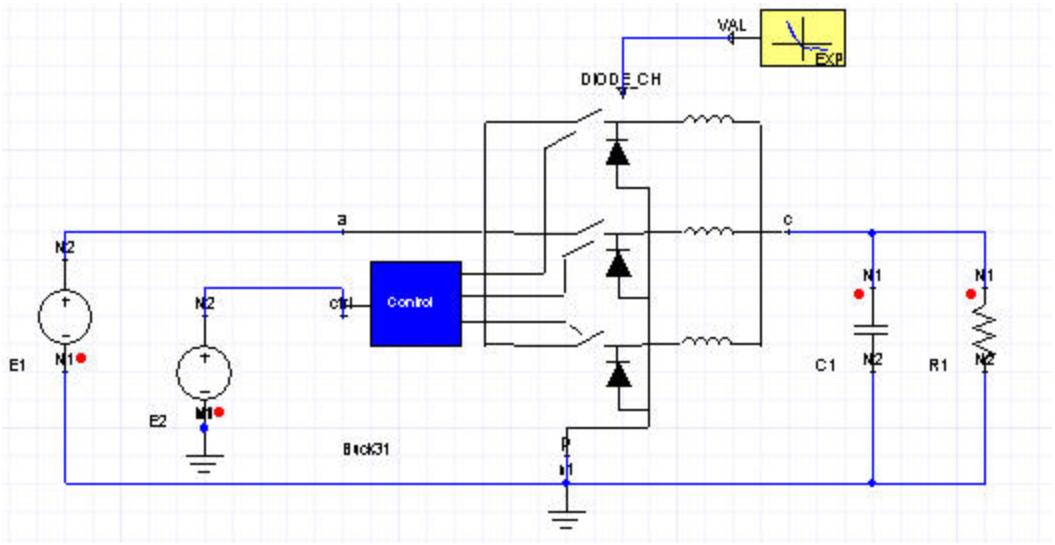
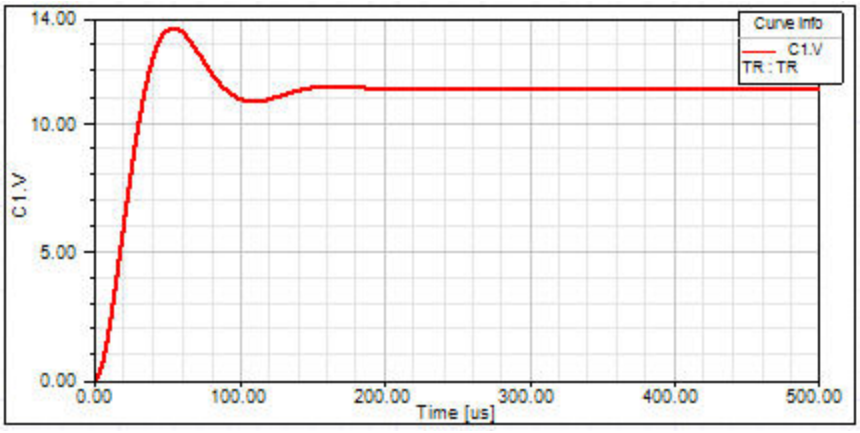


Figure 3. Application example of the 3 Phase Buck Converter

Table 4. System Parameters

Component	Parameter	Value [unit]

3 Phase Buck Converter Buck31	L	1e-5 [H]
	Rsa	0.01 [Ohm]
	Phase_DEG1	0
	Phase_DEG2	120
	Phase_DEG3	-120
	Fs	100000
	L_IC	0.1
	Diode_CH	EXP.VAL
Voltage Source E1	EMF Value	42 [V]
	TPERIO	T_{end}-1
Voltage Source E2	EMF Value	12/42 [V]
	TPERIO	T_{end}-1
Capacitor C1	Capacitance	7.5e-5 [F]
Resistor R1	Resistance	0.24 [Ohm]
Exponential Function EXP	VT	0.035 [V]
	ISAT	1e-12 [A]
	RR	100000 [Ohm]



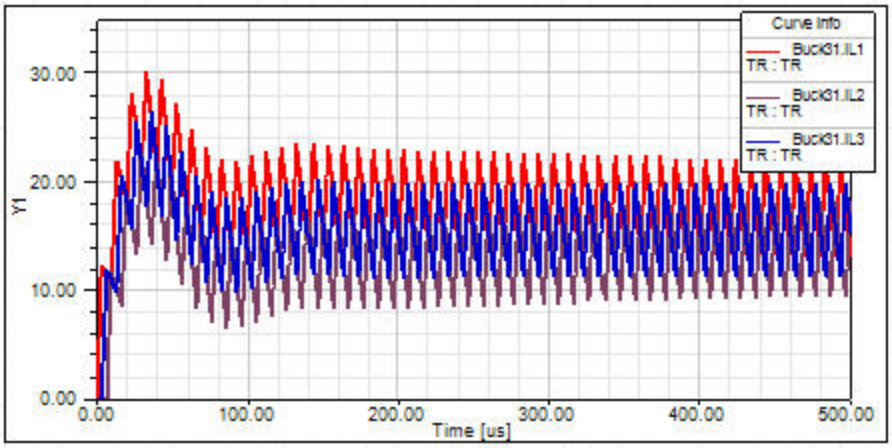


Figure 4. Simulation results – Output Voltage and Phase Currents of the 3 Phase Buck Converter

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References

4 Phase Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

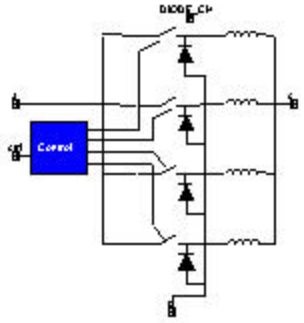

Figure 1. Component symbol

Description

This block represents the switch level model of a 4 Phases Buck converter. It accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to program the phase of each phase independently.

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Netlist Syntax

MODEL Buck4 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, c:= %1, p:= %2, ctrl:= %3 (Rsa:= @Rsa, Phase_DEG1:= @Phase_DEG1, Phase_DEG2:= @Phase_DEG2, Phase_DEG3:= @Phase_DEG3, Fs:= @Fs, L:= @L, L_IC:= @L_IC, DIODE_CH:= @DIODE_CH, Phase_DEG4:= @Phase_DEG4, Rw:= @Rw) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	Active Node	Electrical terminal
p	Passive Node	Electrical terminal
c	Common Node	Electrical terminal
ctrl	Control Node	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
F_s	Switching Frequency	real	1e+005 [Hz]
Phase1_DEG	Delay of Phase 1	real	0 [Deg]
Phase2_DEG	Delay of Phase 2	real	90 [Deg]
Phase3_DEG	Delay of Phase 3	real	180 [Deg]
Phase4_DEG	Delay of Phase 4	real	270 [Deg]
L	Inductance per Phase	real	1e-005 [H]
R_w	Inductance Resistance of each Phase	real	0.001 [Ohm]
L1_IC	Initial Current of Phase 1 Inductance	real	0 [A]
L2_IC	Initial Current of Phase 2 Inductance	real	0 [A]
L3_IC	Initial Current of Phase 3 Inductance	real	0 [A]
L4_IC	Initial Current of Phase 4 Inductance	real	0 [A]

R_{sa}	Active Switch Conduction Resistance	real	0.01 [Ohm]
Diode_CH	Diode Characteristics	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
iL1	Phase 1 Inductor Current [A]	Output	real
iL2	Phase 2 Inductor Current [A]	Output	real
iL3	Phase 3 Inductor Current [A]	Output	real
iL4	Phase 4 Inductor Current [A]	Output	real

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Example

In this example, a 4 Phase Buck Converter is used to switch a source voltage to a complex load. The schematic of the example is shown in Figure 3, system parameters are listed in the table 4, and the simulation results are shown in Figure 4.

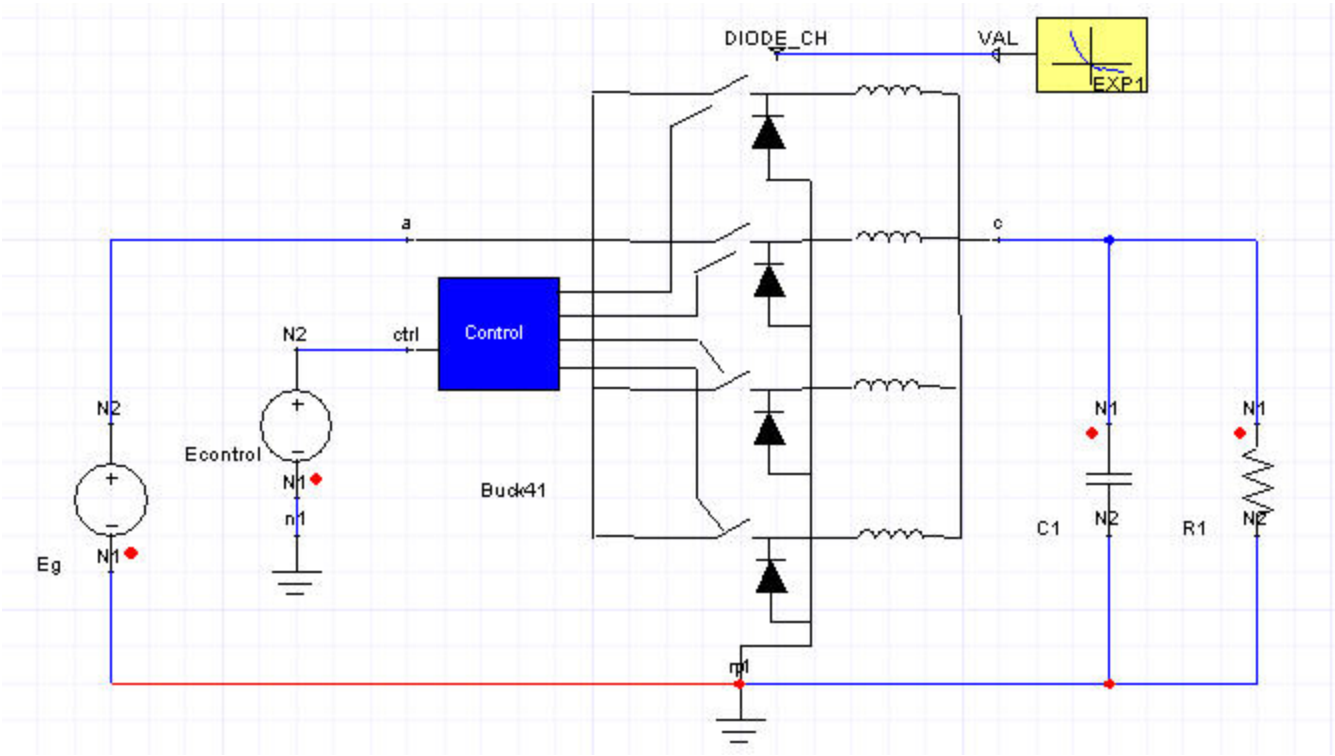

Figure 3. Application example of the 4 Phase Buck Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
3 Phase Buck Converter Buck31	L	1e-5 [H]
	Rsa	0.01 [Ohm]
	Phase_DEG1	0
	Phase_DEG2	90
	Phase_DEG3	180
	Fs	100000
	L_IC	0.1
	Diode_CH	EXP.VAL
Voltage Source Eg	EMF Value	42 [V]
	TPERIO	T_{end}-1
Voltage Source Econtrol	EMF Value	12/42 [V]
	TPERIO	T_{end}-1
Capacitor C1	Capacitance	7.5e-5 [F]

Resistor R1	Resistance	0.24 [Ohm]
Exponential Function EXP	VT	0.035 [V]
	ISAT	1e-12 [A]
	RR	100000 [Ohm]

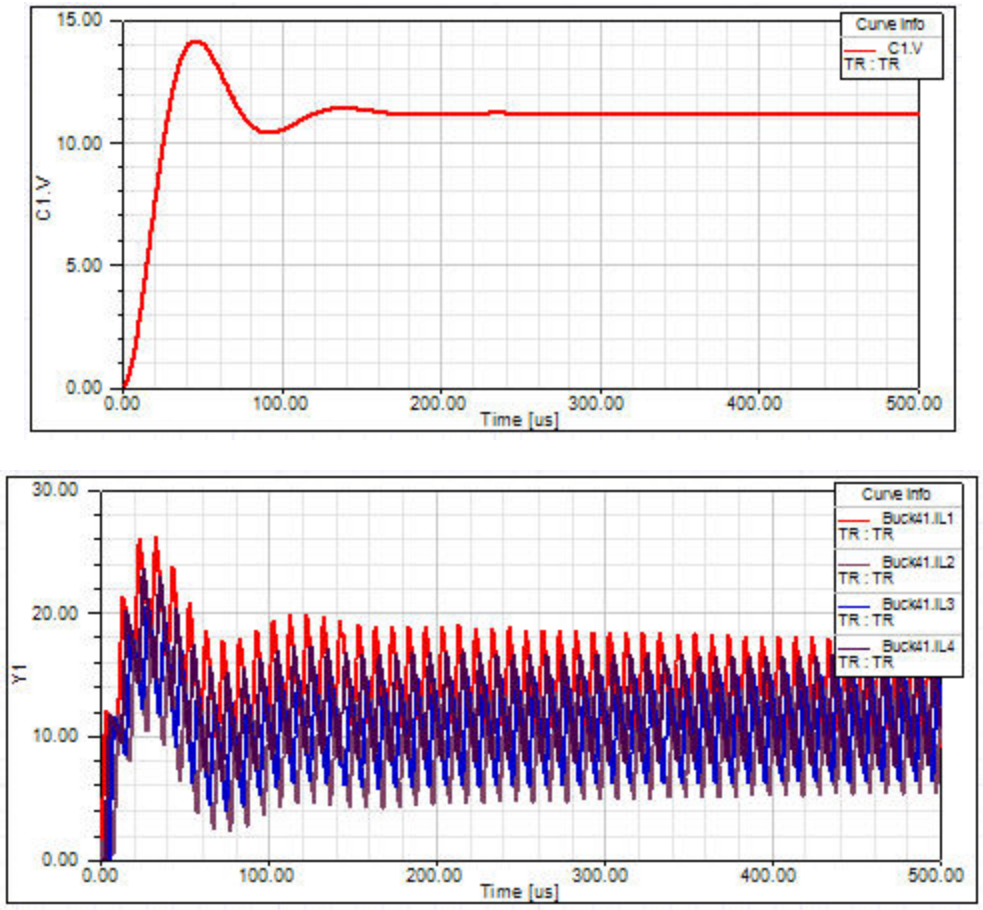

Figure 4. Simulation results – Output voltage and Phase currents of the 4 Phase Buck Converter

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References

Piezoelectric

Piezoelectricity implies the interaction between the electrical and mechanical energy of the medium. A first approximation involves a linear relation between the mechanical and electrical variables:

$$S = s^E T + dE$$

$$D = dT + \varepsilon^T E$$

Where S is the mechanical strain, T is the mechanical stress applied, E is the electrical field strength and D is the dielectric displacement. The choice of the electrical variables is arbitrary. Other possible relations are as follows:

$$S = s^D T + gD$$

$$E = -gT + \beta^T D$$

$$T = c^D S - hD$$

$$E = -hS + \beta^S D$$

It is possible to establish some relations between constants (actually tensors) The coupling factor is defined as:

$$k^2 = \frac{d^2}{\varepsilon^T s^E}$$

$$k_{33}{}^2 = \frac{d_{33}{}^2}{\varepsilon_{33}{}^T s_{33}{}^E}$$

$$k_{31}{}^2 = \frac{d_{31}{}^2}{\varepsilon_{33}{}^T s_{11}{}^E}$$

$$s^D = s^E\left(1-k^2\right)$$

$$s_{33}{}^D = s_{33}{}^E\left(1-k_{33}{}^2\right)$$

$$s_{11}{}^D = s_{11}{}^E\left(1-k_{31}{}^2\right)$$

$$\varepsilon_{33}{}^S = \varepsilon_{33}{}^T\left(1-k_{33}{}^2\right)$$

The following two types of Piezoelectric transformers are supported.

- Rosen
- Thickness

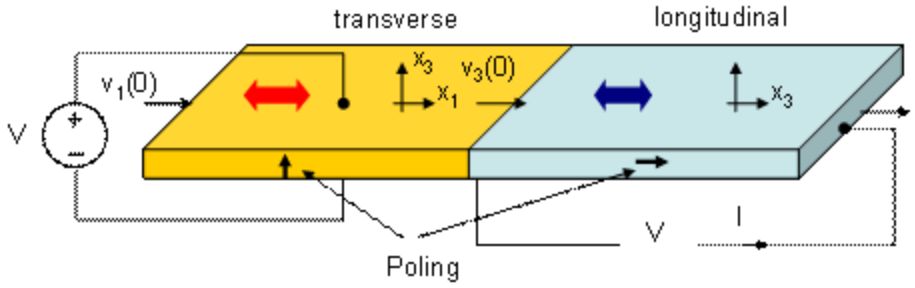
References

[1] W.P. Mason, "Electromechanical Transducers and Wave Filters", Princeton, NJ, Van Nostrand 1948.

[2] M. Redwood, "Transient Performance of a Piezoelectric Transducer", J. Acoust. Soc. Am., Vol. 33, no. 4, pp. 527-536, April 1961.

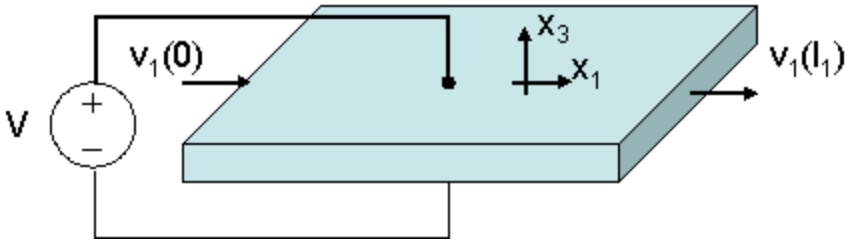
[3] Oliver, J.A.; Prieto, R.; Sanz, M.; Cobos, J.A.; Uceda, J., "1D modeling of multi-layer piezo-electric transformers," Power Electronics Specialists Conference, PESC 2001, vol.4, pp.2097-2102

Rosen Type Piezoelectric Transformers



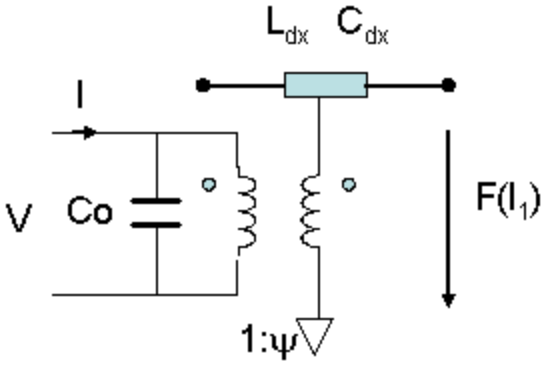
- Longitudinal Rosen
- Monolayer Rosen
- Transverse Rosen
- Transverse Multilayer Rosen

Transverse Mode Equivalent Circuit



$$S_1 = s_{11}{}^{E} T_1 + d_{31} E_3$$

$$D_3 = d_{31} T_1 + \varepsilon_{33}{}^{T} E_3$$



$$L_{dx} = \rho \cdot A_1$$

$$C_{dx} = \frac{s_{11}^{E}}{A_1}$$

$$\psi = W \frac{d_{31}}{s_{11}^{E}}$$

$$Co = \varepsilon_{33}^{T} \left(1 - k_{31}^{2}\right) \frac{W \cdot l_1}{l_3}$$

$$k_{31}^{2} = \frac{d_{31}^{2}}{\varepsilon_{33}^{T} s_{11}^{E}}$$

Longitudinal Rosen

LD110 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

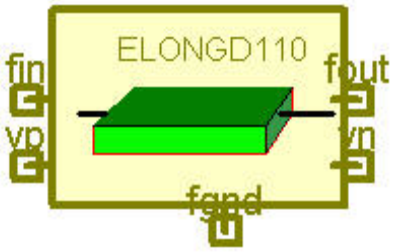


Figure 1. Component symbol

Description

This block represents a D110 Longitudinal Rosen Piezoelectric layer.

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Assumptions and Limitations

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Mathematical Description

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Netlist Syntax

MODEL LD110 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, th:= @th) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.0001 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]

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Example

This example a Rosen type transformer is comprised of a primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

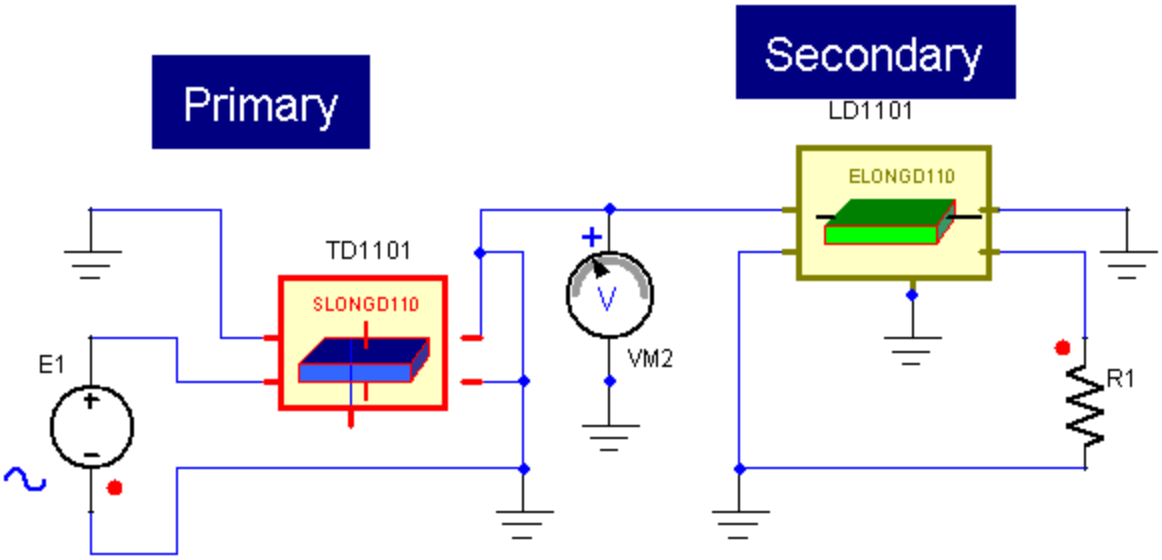

Figure 2. Application example of the Rosen Longitudinal D110 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal D110 LD1101	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen Primary Layer Transverse D110 TD1101	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]

	Freq	50 [Hz]

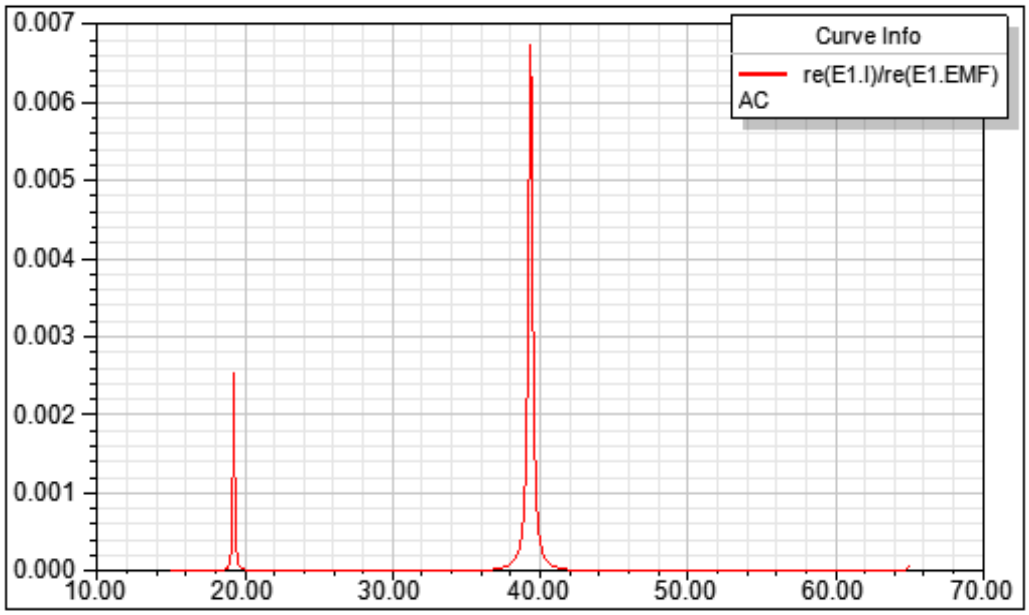

Figure 3. Simulation results-Input Conductance.

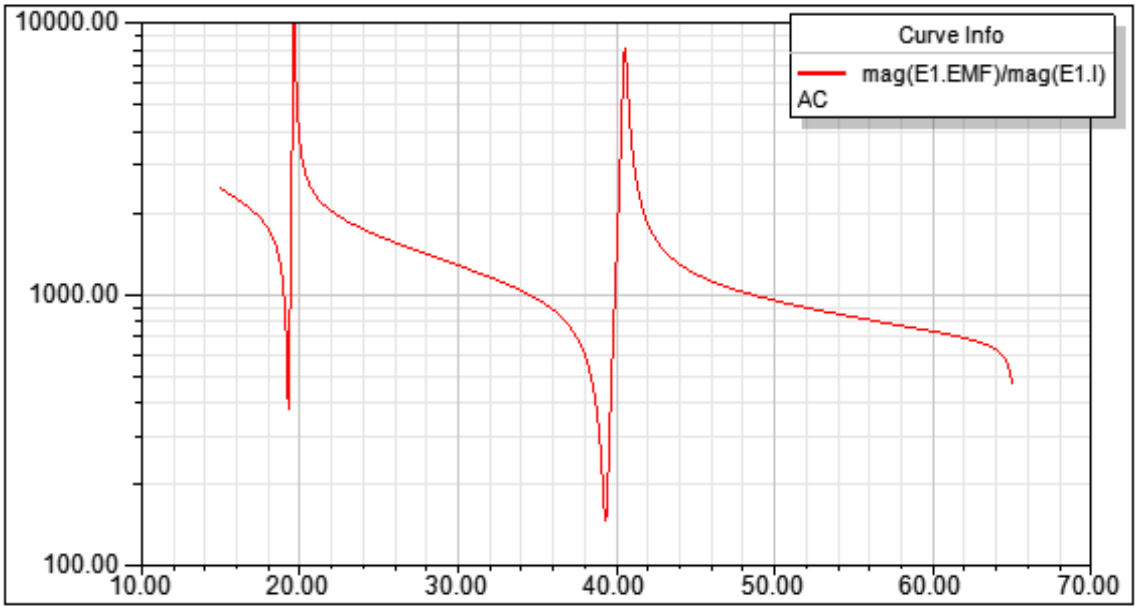

Figure 4. Simulation results-Input Impedance.

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References

LD140 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

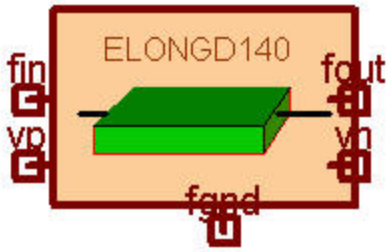

Figure 1. Component symbol

Description

This block represents a D140 Longitudinal Rosen Piezoelectric layer.

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Assumptions and Limitations

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Mathematical Description

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Netlist Syntax

MODEL LD140 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, th:= @th) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.005 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]

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Example

This example a Rosen type transformer is comprised of a primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

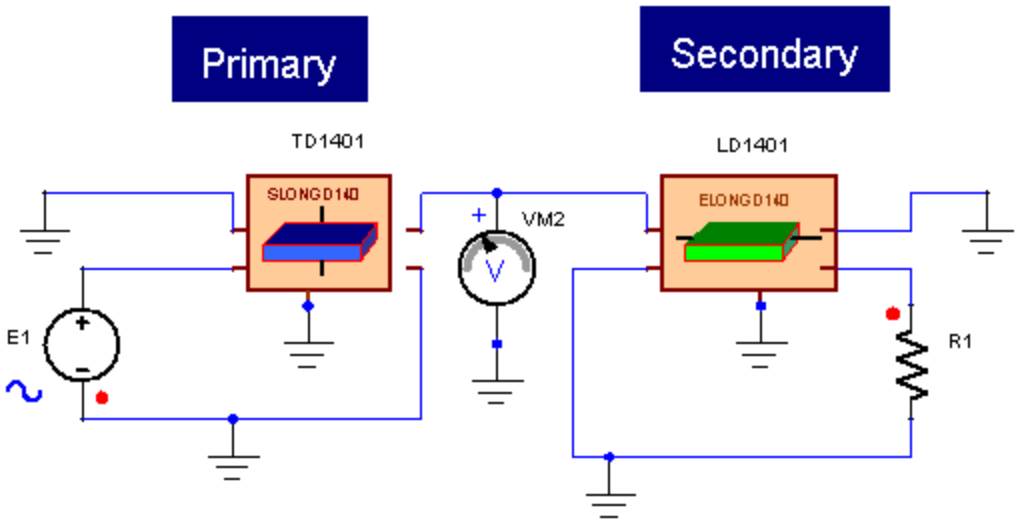

Figure 2. Application example of the Rosen Longitudinal D140 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal D140 LD1401	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen Primary Layer Transverse D140 TD1401	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

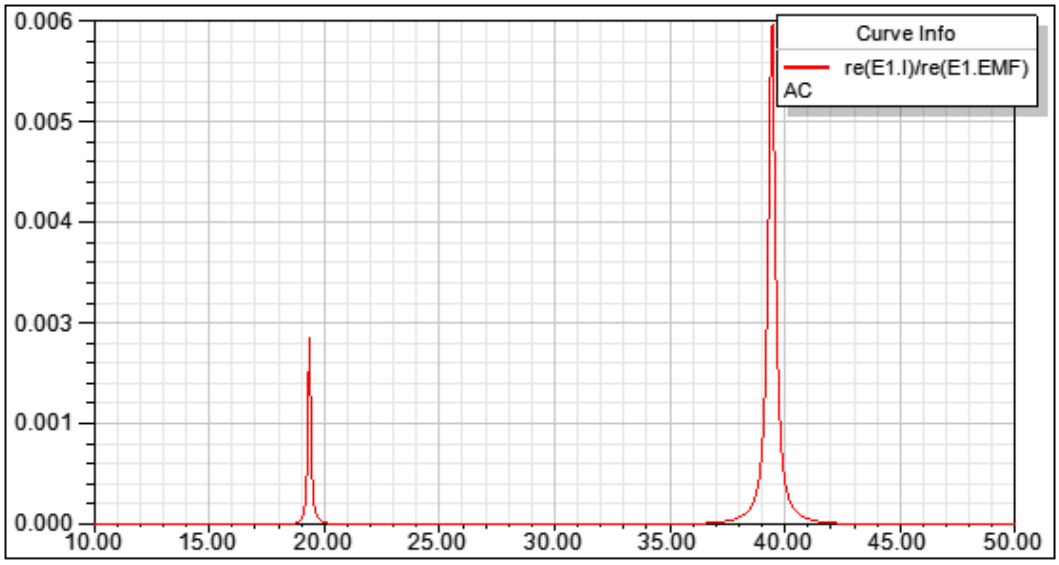

Figure 3. Simulation results-Input Conductance.

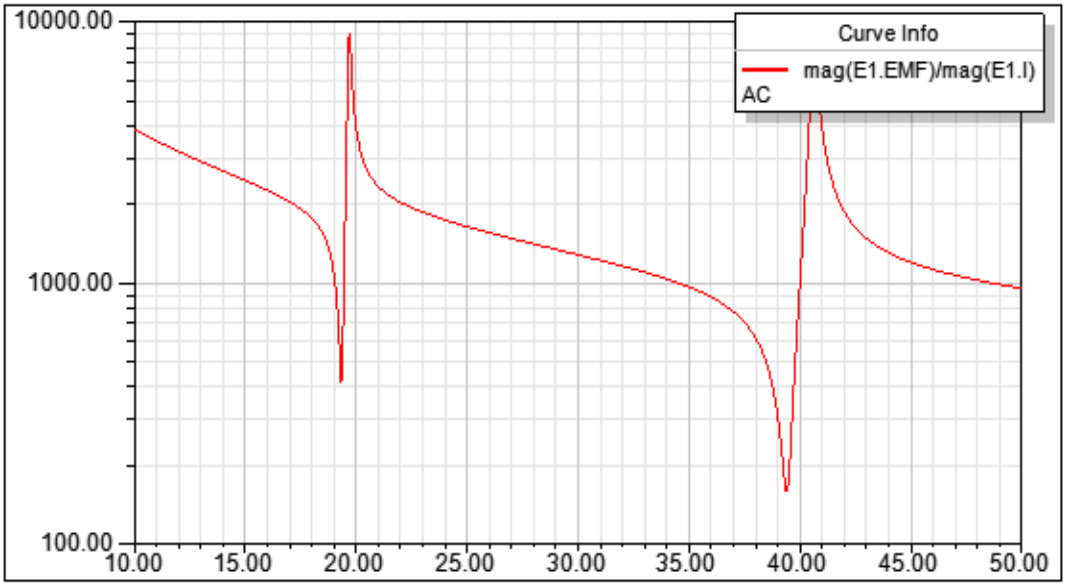

Figure 4. Simulation results-Input Impedance.

Top

References

LONG Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

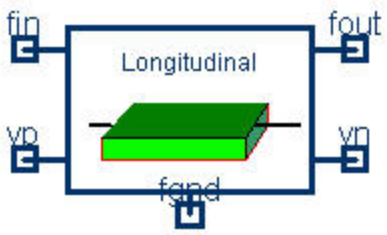

Figure 1. Component symbol

Description

This block represents a General Longitudinal Rosen Piezoelectric layer.

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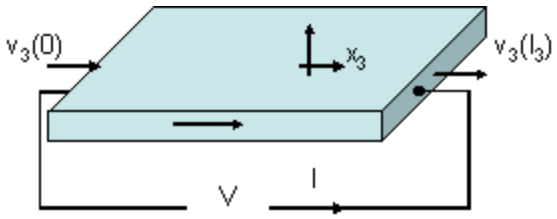
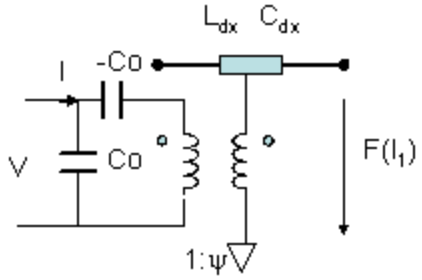


$$S_3 = s_{33}{}^{E} T_3 + d_{33} E_3$$

where S_3 is the mechanical strain, T_3 is the mechanical stress, and E_3 is Electric Field strength. $s_{33}{}^{E}$ is the mechanical compliance with constant Electric Field, and d_{33} is the piezoelectric constant, named strain constant, relating the mechanical strain produced by an applied electric field.

$$D_3 = d_{33} T_3 + \varepsilon_{33}{}^{T} E_3$$

Where D_3 is the electric charge density displacement (electric displacement), $\varepsilon_{33}{}^{T}$ is permittivity with constant mechanical stress.



$$L_{dx} = \rho \cdot A_3$$

$$C_{dx} = \frac{s_{33}{}^{D}}{A_3}$$

$$\psi = \frac{A_3}{l_3} \frac{d_{33}}{{s_{33}}^E}$$

$$Co = \frac{A_3}{l_3} {\varepsilon_{33}}^T \left(1 - {k_{33}}^2\right)$$

The equivalent circuit that represents the behavior of the piezoelectric layer is shown in the figure, where the mechanical behavior is described by a transmission line. The voltages in the transmission line represent the mechanical force and the current in the transmission line the mechanical velocity. L_{dx} and C_{dx} are the equivalent inductance and capacitance per unit length of the transmission line.

The mechanical-electrical coupling is represented by the ideal transformer, and the turn ratio of the transformer is given by the parameter ψ.

Co represents the electrode capacitance.

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Netlist Syntax

MODEL LONG ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, Qm:= @Qm, rho:= @rho, s33_E:= @s33_E, E33_Tr:= @E33_Tr, Qe:= @Qe, k33:= @k33, th:= @th) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thickness	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.0001 [m]
th	Piezoelectric Layer Thickness	real	0.001 [m]
Qm	Mechanical Quality Factor	real	2000
Qe	Electrical Quality Factor	real	333
rho	Density	real	7700 [Kg/m^3]
s33_E	Mechanical Compliance with Constant Electric Field	real	1.96e-11
E33_Tr	Relative Permittivity with Constant Stress	real	1330
k33	Electromechanical Coupling Factor	real	0.684

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Example

This example is a Rosen type transformer composed of a primary layer vibrating in thickness mode and a secondary layer vibrating in transverse mode.

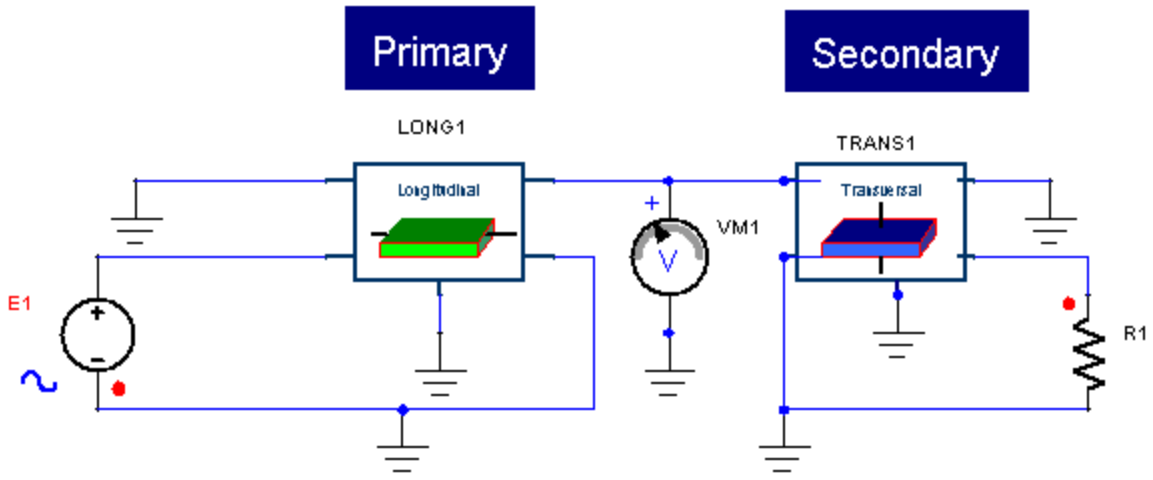

Figure 2. Application example of the Rosen Longitudinal LONG model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen General Secondary Layer Longitudinal LONG1	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen General Primary Layer Transverse TRANS TRANS1	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

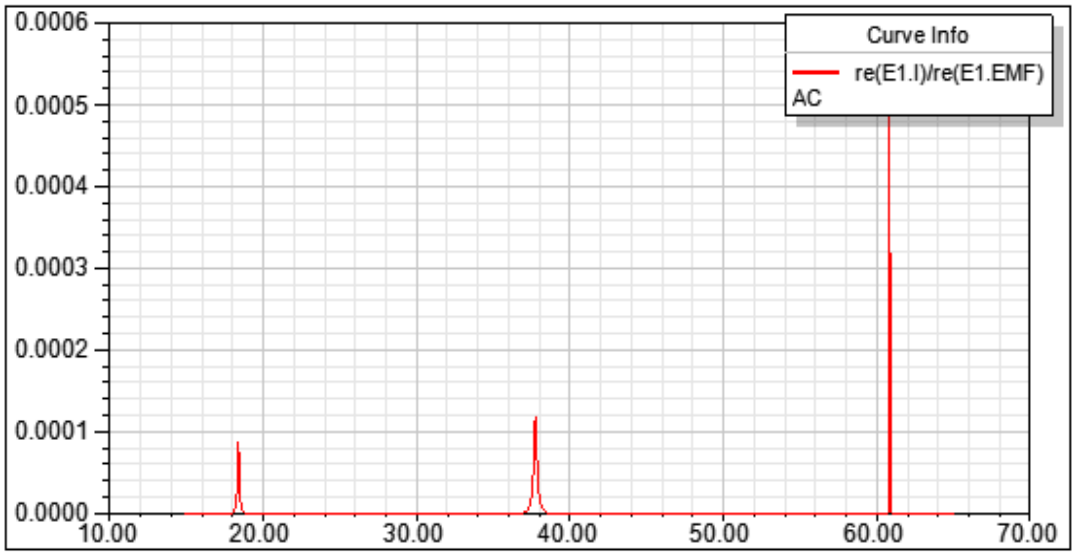

Figure 3. Simulation results-Input Conductance.

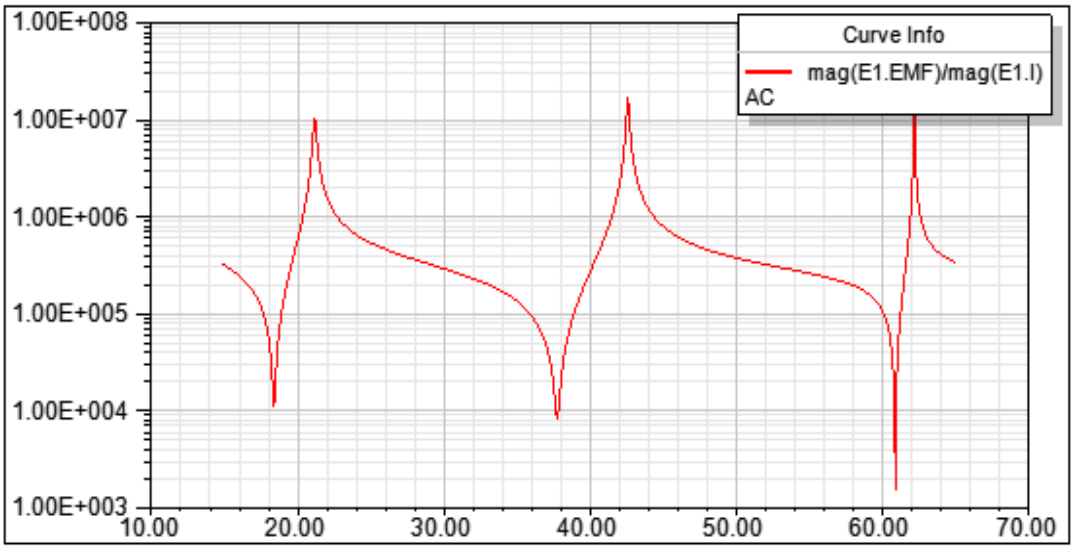

Figure 4. Simulation results-Input Impedance.

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References

LPZ26 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

Figure 1. Component symbol

Description

This block represents a LPZ26 Longitudinal Rosen Piezoelectric layer.

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Netlist Syntax

MODEL LPZ26 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, th:= @th) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.0001 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]

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Example

This example a Rosen type transformer is comprised of a primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

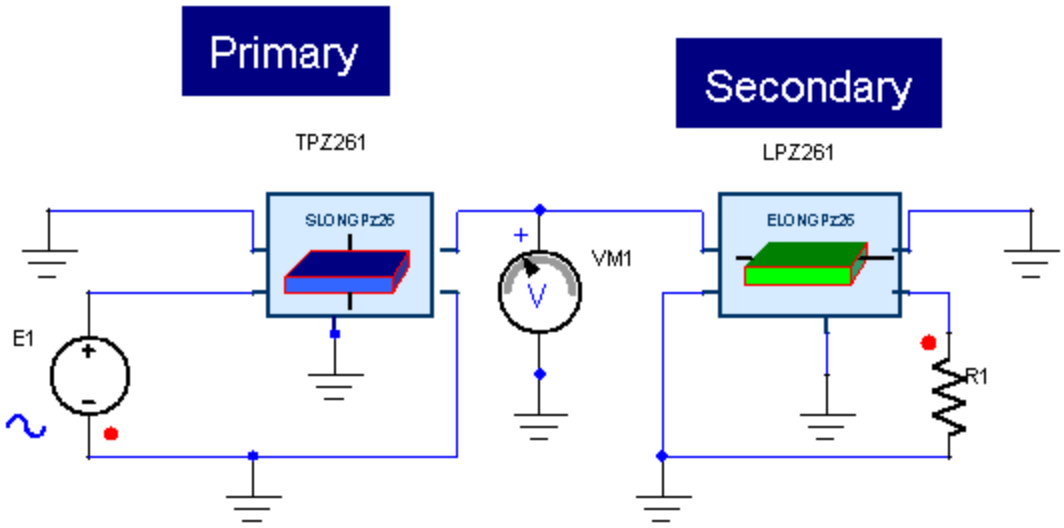

Figure 2. Application example of the Rosen Longitudinal Pz26 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal Pz26 LPZ261	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen Primary Layer Transverse PZ26 TPZ261	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

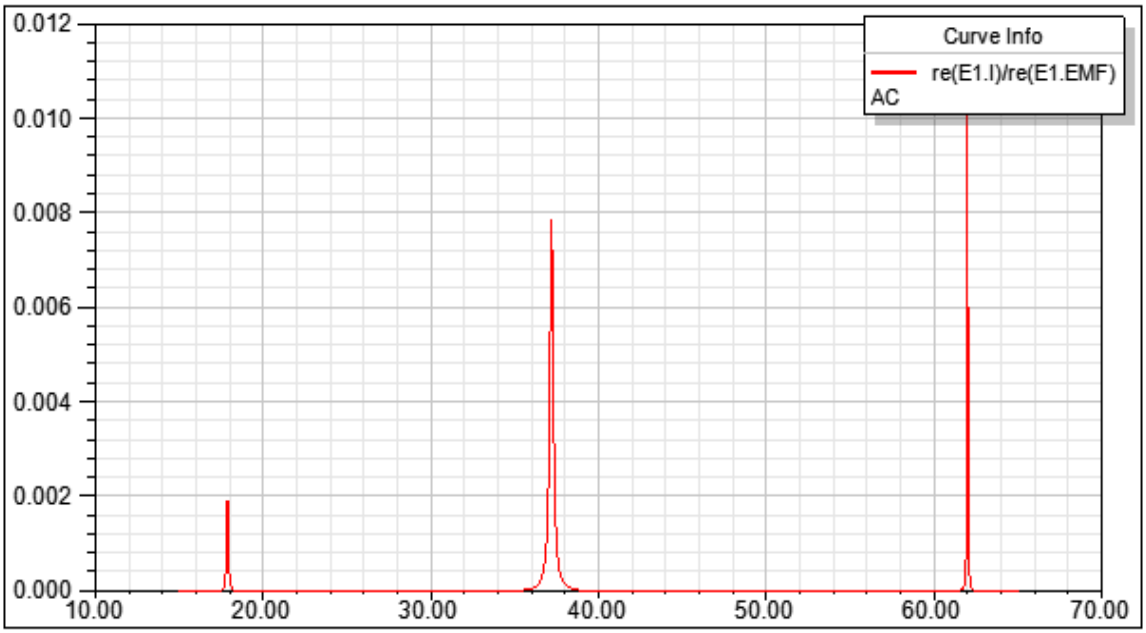

Figure 3. Simulation results-Input Conductance.

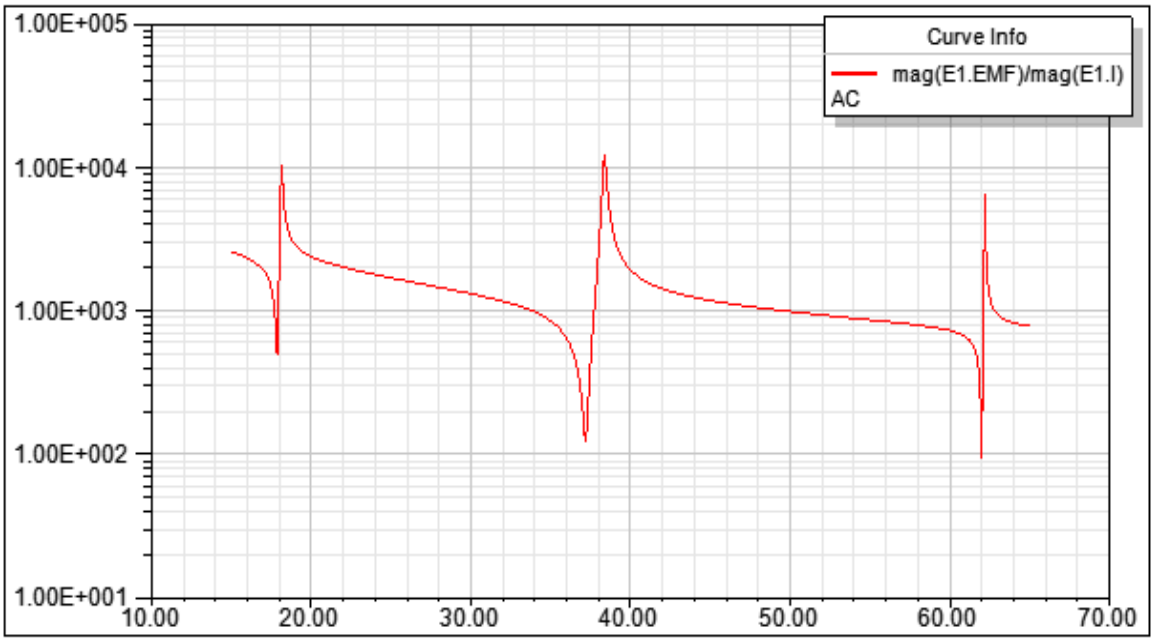

Figure 4. Simulation results-Input Impedance.

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References

Monolayer Rosen

- R1L_D110: Block representing a monolayer Rosen PT of material D110
- R1L_D140: Block representing a monolayer Rosen PT of material D140
- R1L_PZ26: Block representing a monolayer Rosen PT of material Pz26
- R1LG: General Rosen Model

R1L_D110 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

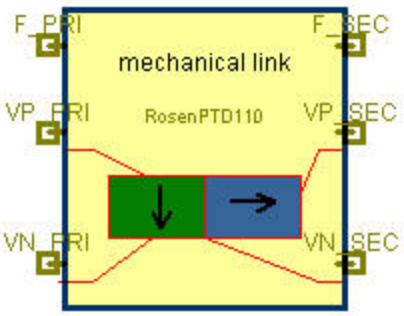

Figure 1. Component symbol

Description

This block represents a D110 Rosen Monolayer Piezoelectric layer.

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Netlist Syntax

MODEL R1L_D110 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) F_PRI:= %0, VP_PRI:= %1, VN_PRI:= %2, F_SEC:= %3, VN_SEC:= %4, VP_SEC:= %5 (W:= @W, Lp:= @Lp, th:= @th, Ls:= @Ls) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
F_PRI	Mechanical Force Pin(primary side)	Electrical terminal
F_SEC	Mechanical Force Pin(secondary side)	Electrical terminal
VP_PRI	Electrical Pin(primary side)	Electrical terminal
VN_PRI	Electrical Pin(primary side)	Electrical terminal
VP_SEC	Electrical Pin(secondary side)	Electrical terminal
VN_SEC	Electrical Pin(secondary side)	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Lp	Primary Side Length	real	0.01 [m]
Ls	Secondary Side Length	real	0.01 [m]
W	Layer Width	real	0.005 [m]
th	Layer Thickness	real	0.001 [m]

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Example

This example a Rosen monolayer type piezoelectric transformer.

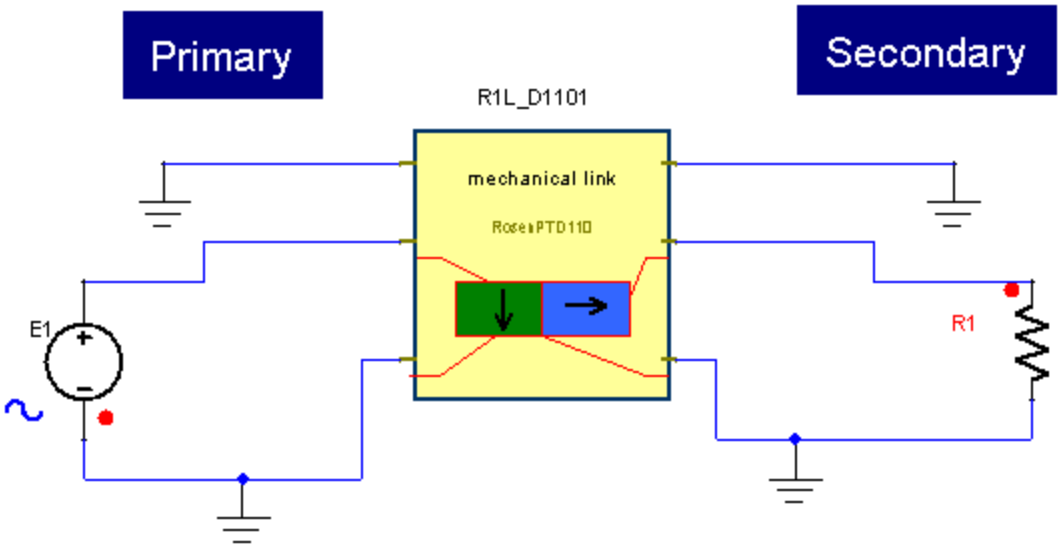

Figure 2. Application example of the Rosen Monolayer R1L_D110 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Monolayer of material D110 R1L_D1101	Ls	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
	Lp	0.03837 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

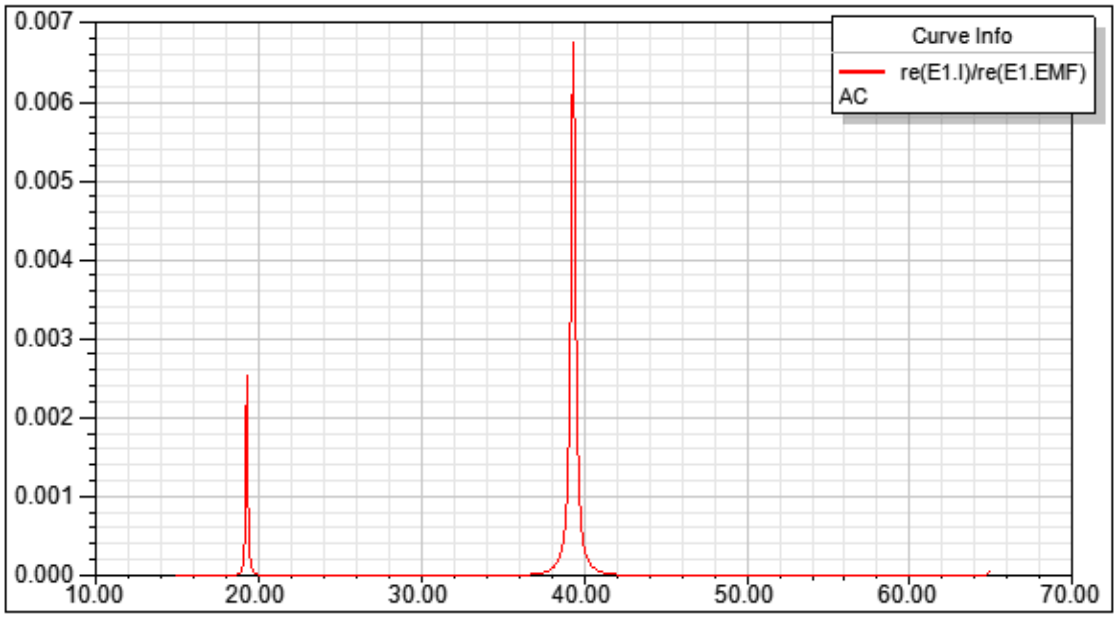

Figure 3. Simulation results-Input Conductance.

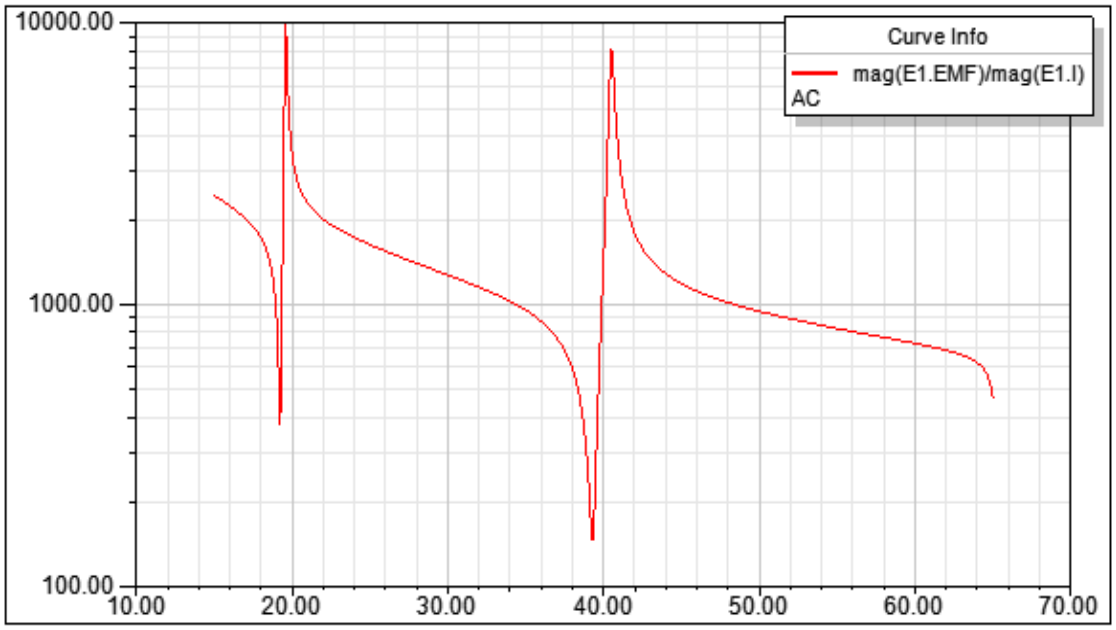

Figure 4. Simulation results-Input Impedance.

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References

R1L_D140 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

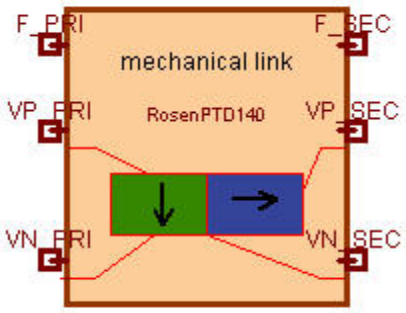

Figure 1. Component symbol

Description

This block represents a D140 Rosen Monolayer Piezoelectric layer.

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Netlist Syntax

MODEL R1L_D140 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) F_PRI:= %0, VP_PRI:= %1, VN_PRI:= %2, F_SEC:= %3, VN_SEC:= %4, VP_SEC:= %5 (W:= @W, Lp:= @Lp, th:= @th, Ls:= @Ls) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
F_PRI	Mechanical Force Pin(primary side)	Electrical terminal
F_SEC	Mechanical Force Pin(secondary side)	Electrical terminal
VP_PRI	Electrical Pin(primary side)	Electrical terminal
VN_PRI	Electrical Pin(primary side)	Electrical terminal
VP_SEC	Electrical Pin(secondary side)	Electrical terminal
VN_SEC	Electrical Pin(secondary side)	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Lp	Primary Side Length	real	0.01 [m]
Ls	Secondary Side Length	real	0.01 [m]
W	Layer Width	real	0.005 [m]
th	Layer Thickness	real	0.001 [m]

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Example

This example a Rosen monolayer type piezoelectric transformer.

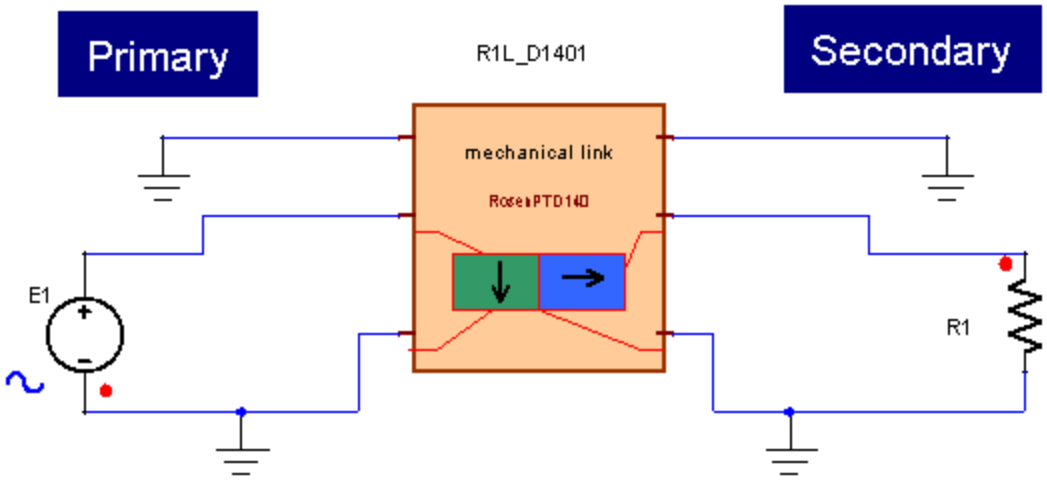

Figure 2. Application example of the Rosen Monolayer R1L_D140 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Monolayer of material D140 R1L_D1401	Ls	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
	Lp	0.03837 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

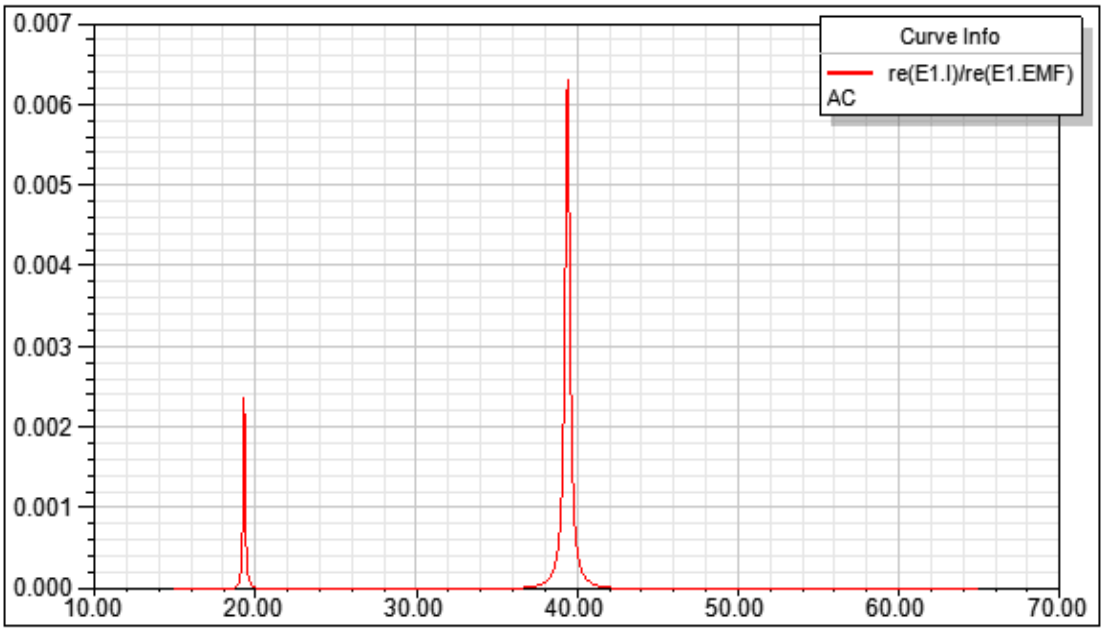

Figure 3. Simulation results-Input Conductance.

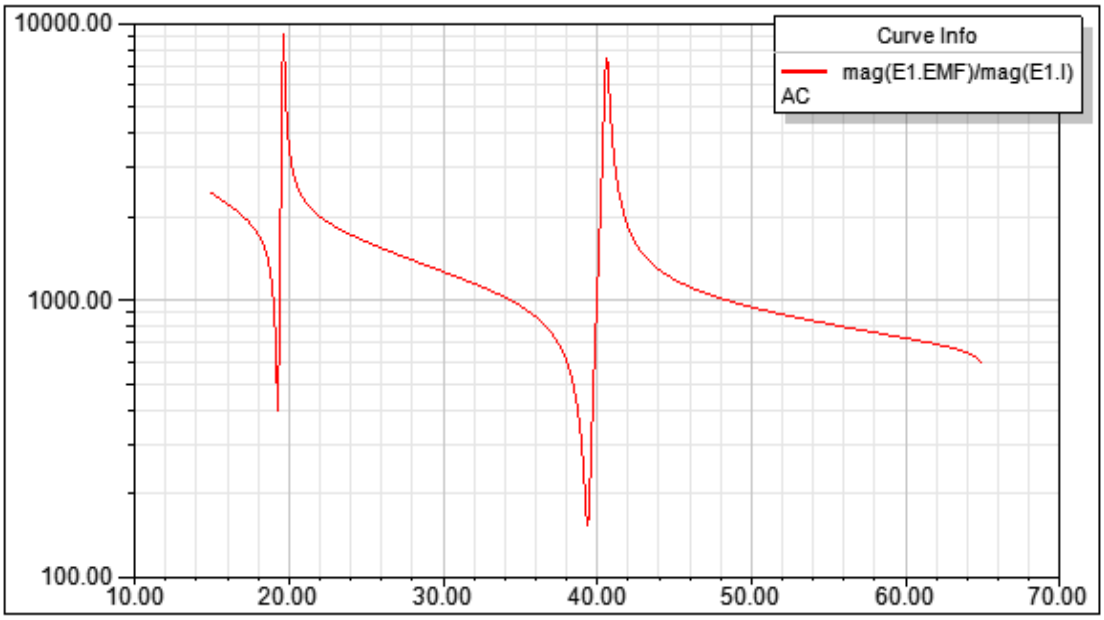

Figure 4. Simulation results-Input Impedance.

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References

R1L_PZ26 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

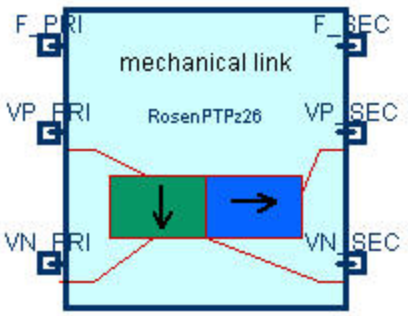

Figure 1. Component symbol

Description

This block represents a PZ26 Rosen Monolayer Piezoelectric layer.

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Netlist Syntax

MODEL R1L_PZ26 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) F_PRI:= %0, VP_PRI:= %1, VN_PRI:= %2, F_SEC:= %3, VN_SEC:= %4, VP_SEC:= %5 (W:= @W, Lp:= @Lp, th:= @th, Ls:= @Ls) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
F_PRI	Mechanical Force Pin(primary side)	Electrical terminal
F_SEC	Mechanical Force Pin(secondary side)	Electrical terminal
VP_PRI	Electrical Pin(primary side)	Electrical terminal
VN_PRI	Electrical Pin(primary side)	Electrical terminal
VP_SEC	Electrical Pin(secondary side)	Electrical terminal
VN_SEC	Electrical Pin(secondary side)	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Lp	Primary Side Length	real	0.01 [m]
Ls	Secondary Side Length	real	0.01 [m]
W	Layer Width	real	0.005 [m]
th	Layer Thickness	real	0.001 [m]

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Example

This example a Rosen monolayer type piezoelectric transformer.

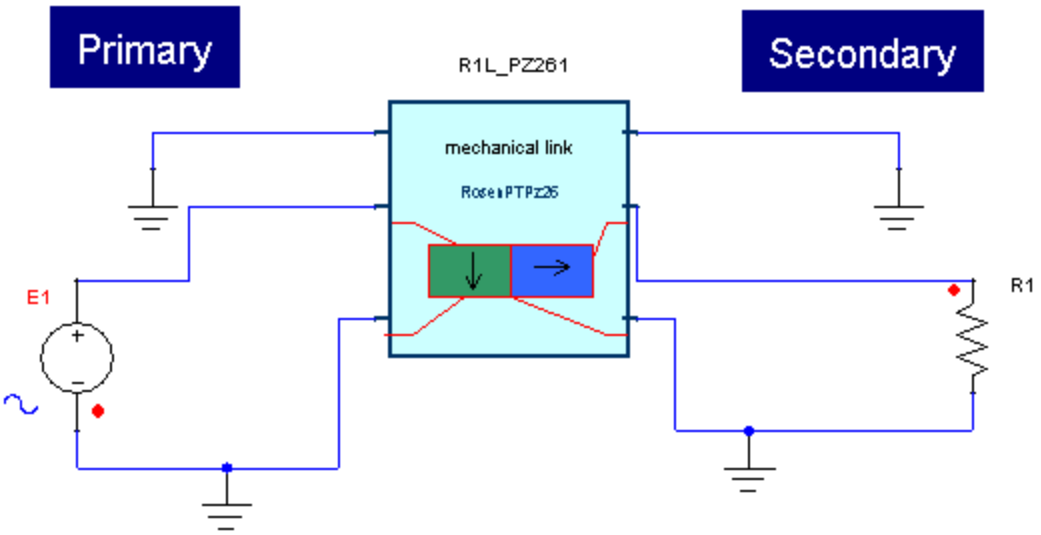

Figure 2. Application example of the Rosen Monolayer R1L_PZ26 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Monolayer of material PZ26 R1L_PZ261	Ls	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
	Lp	0.03837 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

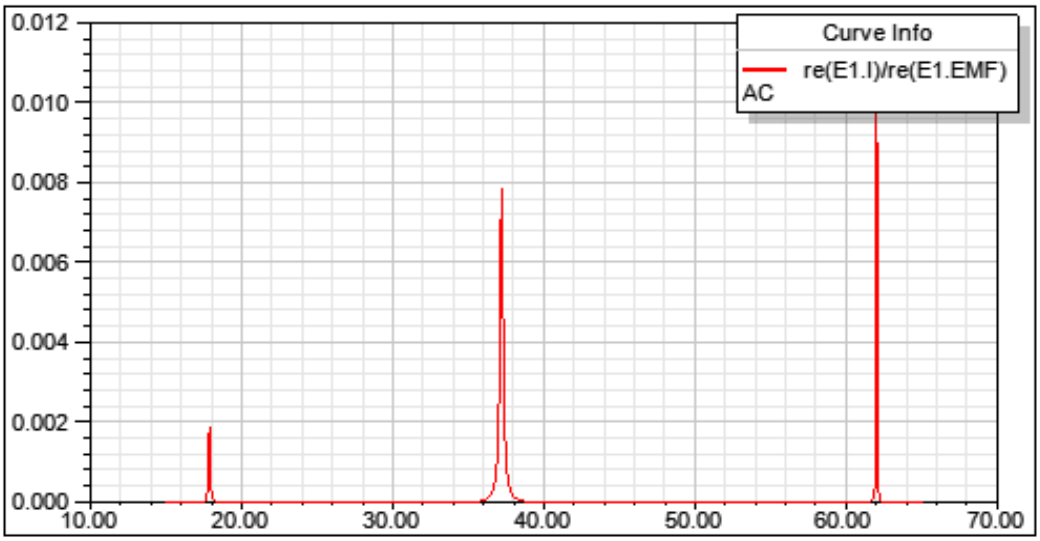

Figure 3. Simulation results-Input Conductance.

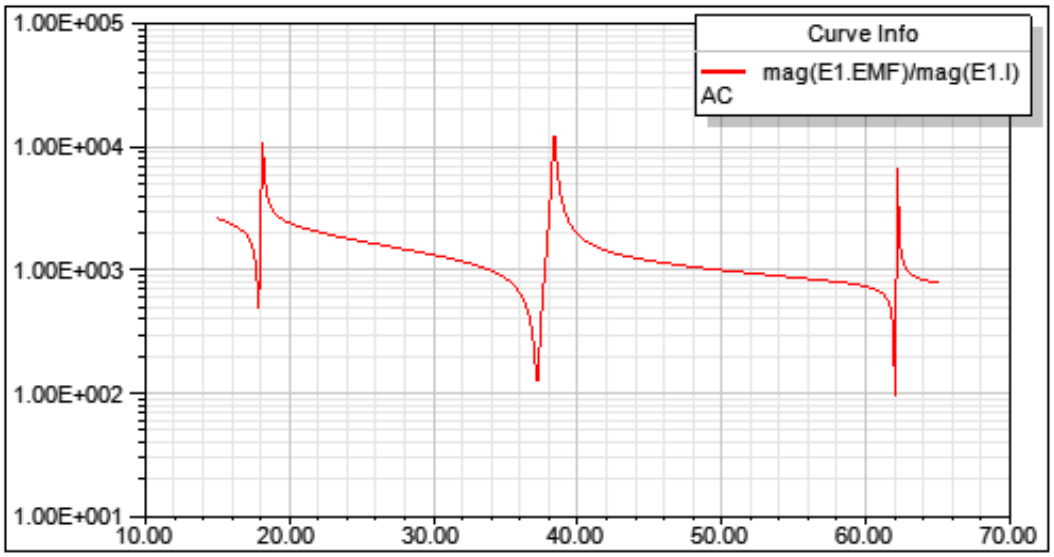

Figure 4. Simulation results-Input Impedance.

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References

R1LG Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

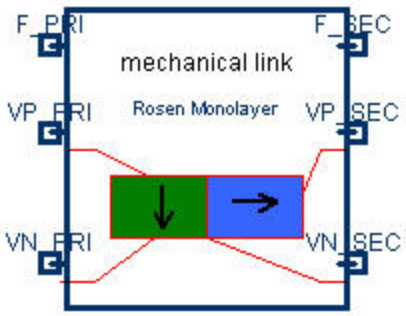

Figure 1. Component symbol

Description

This block represents a General Monolayer Rosen Piezoelectric layer.

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Netlist Syntax

MODEL R1LG ?InstanceName(@InstanceName):(@(Refbase)@(ID)) F_PRI:= %0, VP_PRI:= %1, VN_PRI:= %2, F_SEC:= %3, VN_SEC:= %4, VP_SEC:= %5 (W:= @W, Lp:= @Lp, th:= @th, Ls:= @Ls, E33_Tr:= @E33_Tr, s33_E:= @s33_E, s11_E:= @s11_E, k31:= @k31, k33:= @k33, rho:= @rho, Qe:= @Qe, Qm:= @Qm) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
F_PRI	Mechanical Force Pin(primary side)	Electrical terminal
F_SEC	Mechanical Force Pin(secondary side)	Electrical terminal
VP_PRI	Electrical Pin(primary side)	Electrical terminal
VN_PRI	Electrical Pin(primary side)	Electrical terminal
VP_SEC	Electrical Pin(secondary side)	Electrical terminal
VN_SEC	Electrical Pin(secondary side)	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Lp	Primary Side Length	real	0.01 [m]
Ls	Secondary Side Length	real	0.01 [m]
W	Layer Width	real	0.005 [m]
th	Layer Thickness	real	0.001 [m]
Qm	Mechanical Quality Factor	real	2000
Qe	Electrical Quality Factor	real	1000
rho	Density	real	7700 [Kg/m^3]
s33_E	Mechanical Compliance with Constant Electric Field	real	1.61e-11

s11_E	Mechanical Compliance with Constant Electric Field	real	1.3e-11
E33_Tr	Relative Permittivity with Constant Stress	real	1000
k33	Thickness Electromechanical Coupling Factor	real	0.7
k11	Thickness Electromechanical Coupling Factor	real	0.4

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Example

This example a Rosen monolayer type piezoelectric transformer.

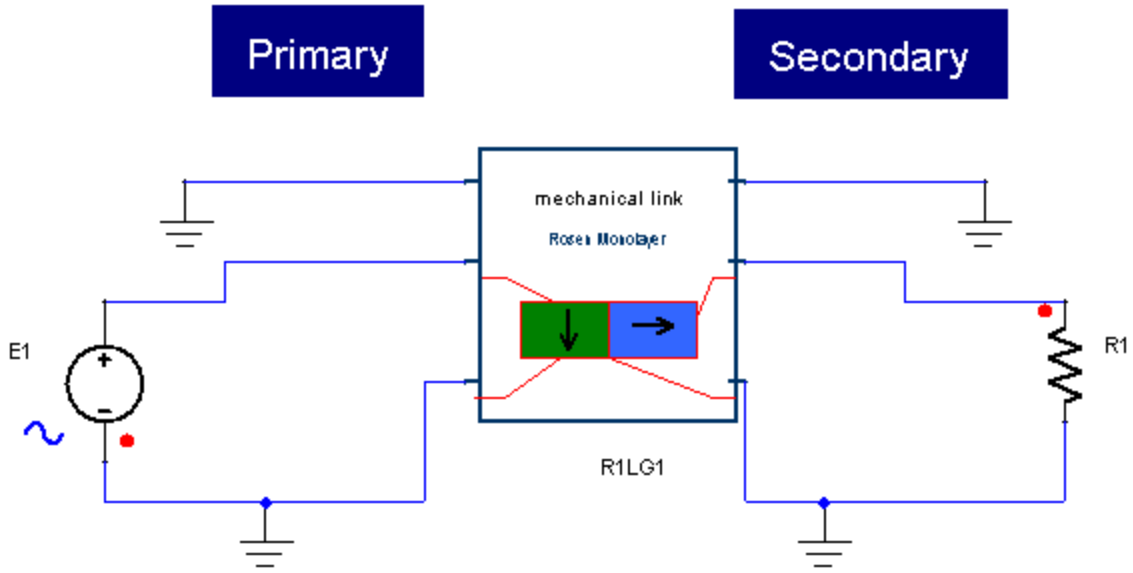

Figure 2. Application example of the Rosen Monolayer R1LG model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen General Monolayer R1LG1	Ls	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]

	Lp	0.03837 [m]
	E33_Tr	1300
	s33_E	1.96e-011
	k31	0.327
	k33	0.684
	Qe	333
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

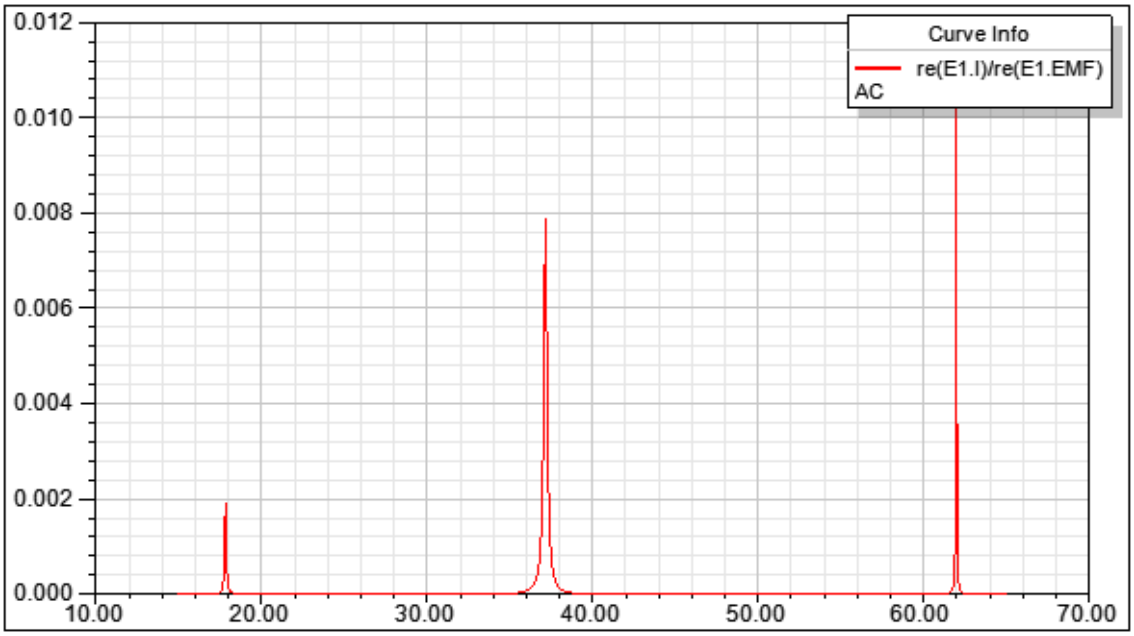

Figure 3. Simulation results-Input Conductance.

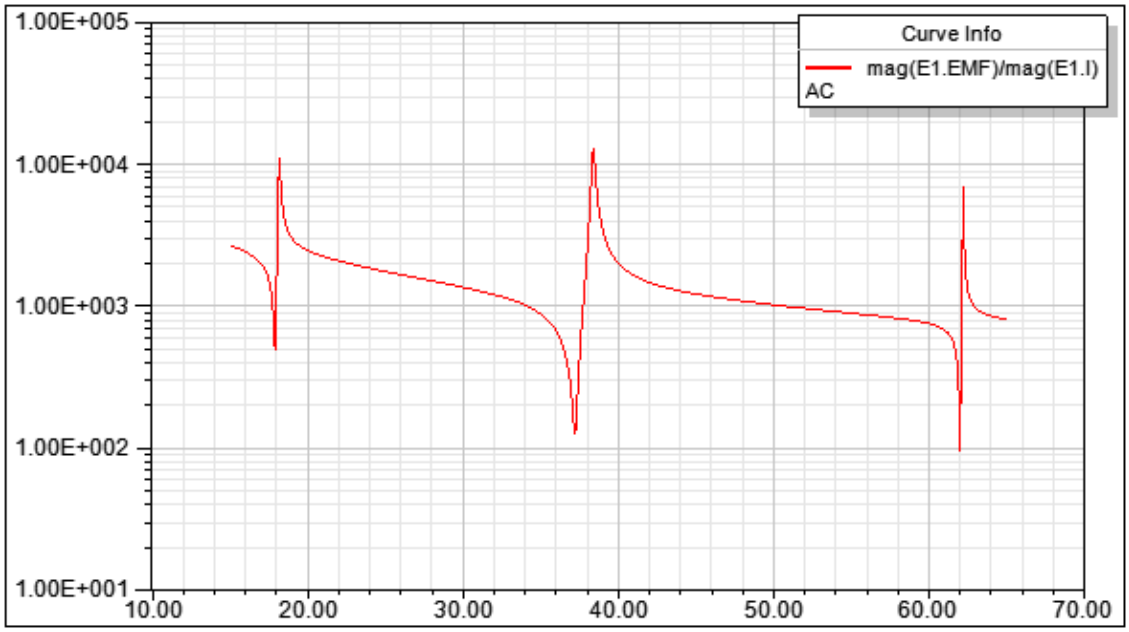

Figure 4. Simulation results-Input Impedance.

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References

Transverse Rosen

- TD110: Primary layer of Rosen PT of material D110
- TD140: Primary layer of Rosen PT of material D140
- TPZ26: Primary layer of Rosen PT of material Pz26
- TRANS: General Transverse Model

TD110 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

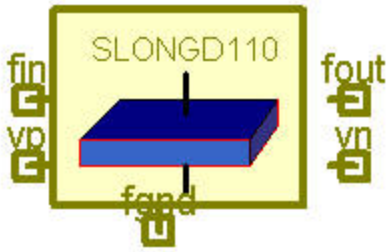

Figure 1. Component symbol

Description

This block represents a D110 Rosen Transverse Piezoelectric layer.

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Netlist Syntax

MODEL TD110 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, th:= @th) SRC: DB(Lib:- :=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.01 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]

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Example

This example a Rosen type transformer is comprised of a primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

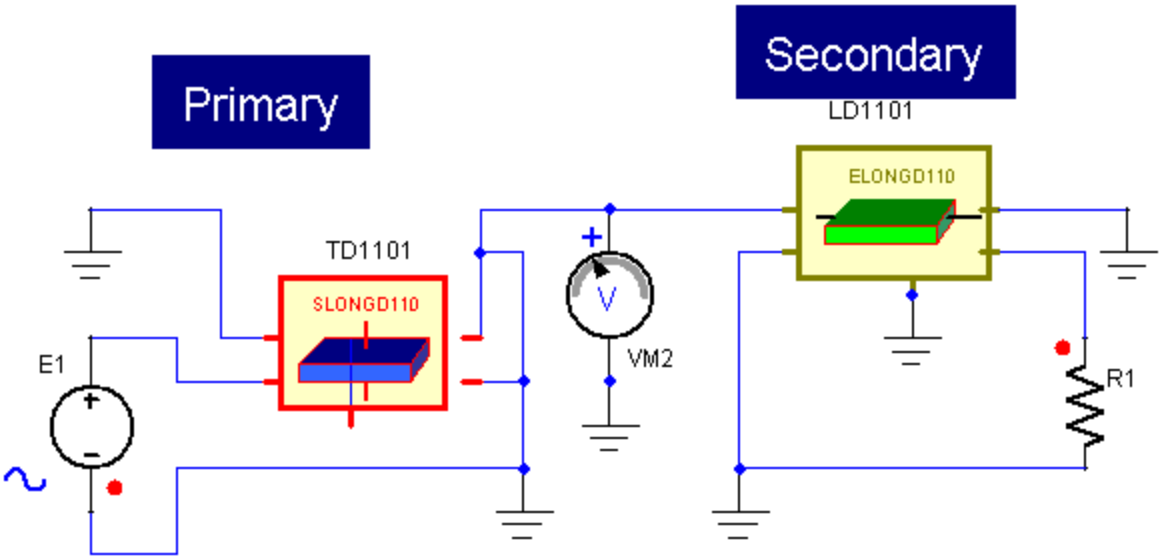

Figure 2. Application example of the Rosen Transverse D110 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal D110 LD1101	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen Primary Layer Transverse D110 TD1101	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]

	Freq	50 [Hz]

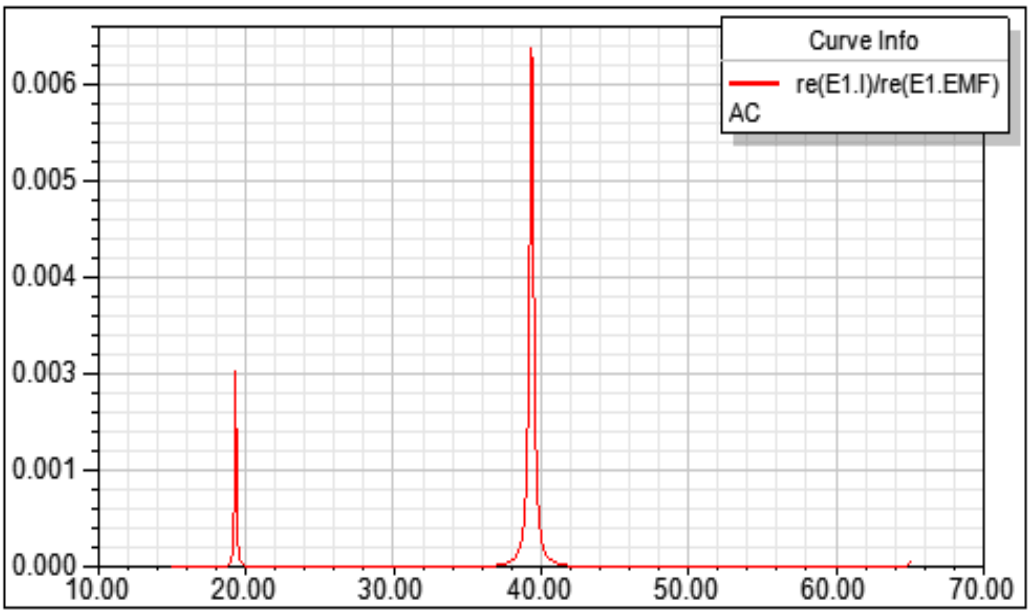

Figure 3. Simulation results-Input Conductance.

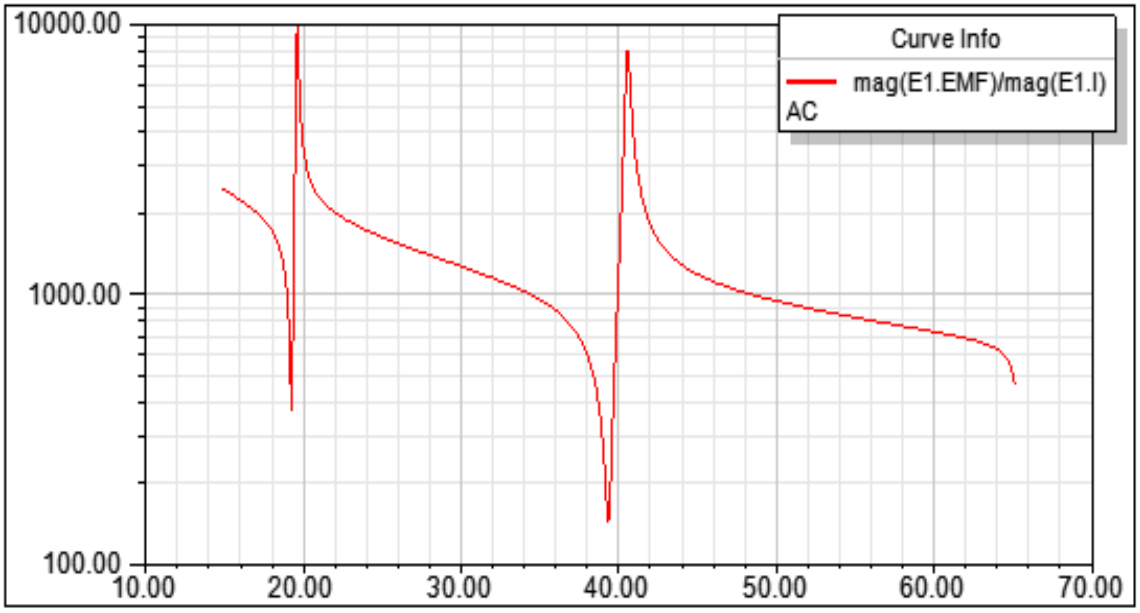

Figure 4. Simulation results-Input Impedance.

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References

TD140 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

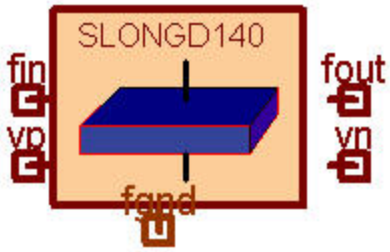

Figure 1. Component symbol

Description

This block represents a D140 Rosen Transverse Piezoelectric layer.

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Netlist Syntax

MODEL TD140 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, th:= @th) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.01 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]

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Example

This example a Rosen type transformer is comprised of a primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

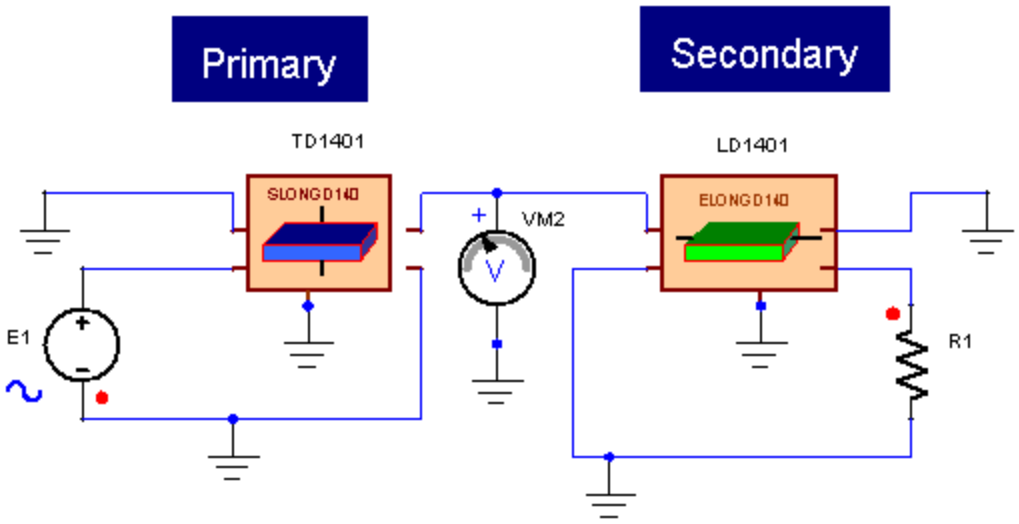

Figure 2. Application example of the Rosen Transverse D140 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal D140 LD1401	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen Primary Layer Transverse D140 TD1401	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

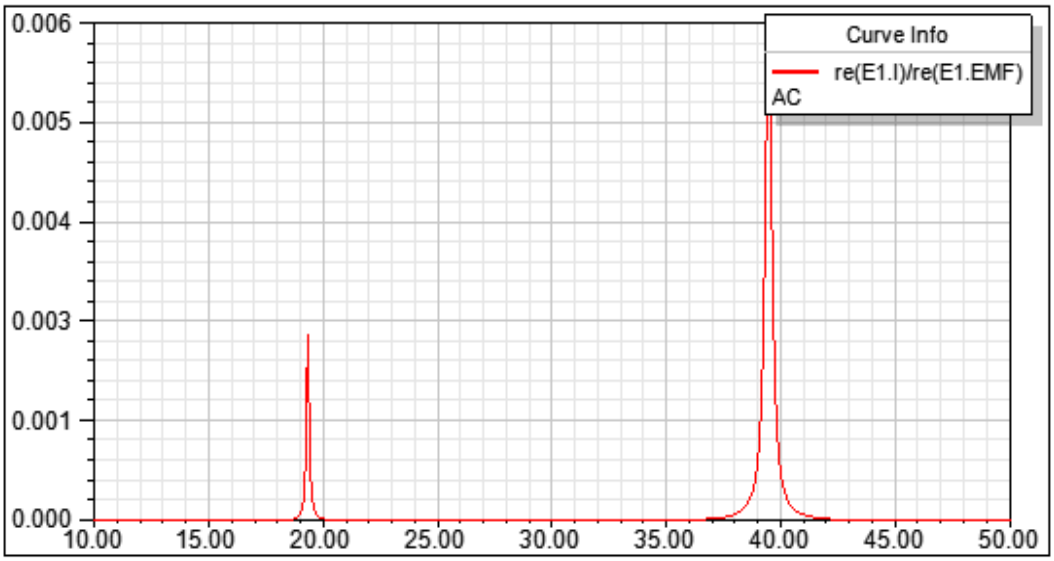

Figure 3. Simulation results-Input Conductance.

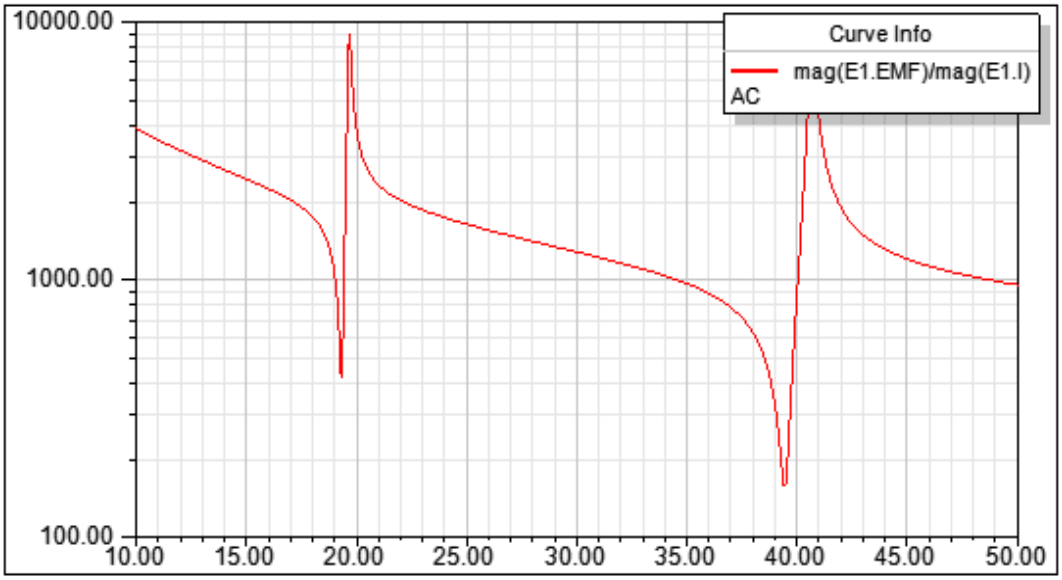

Figure 4. Simulation results-Input Impedance.

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References

TPZ26 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

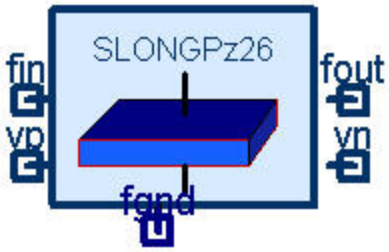

Figure 1. Component symbol

Description

This block represents a PZ26 Rosen Transverse Piezoelectric layer.

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Netlist Syntax

MODEL TPZ26 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, th:= @th) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.01 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]

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Example

This example a Rosen type transformer is comprised of a multilayer primary vibrating in thick-ness mode (SLONG) and a secondary vibrating in longitudinal mode (ELONG).

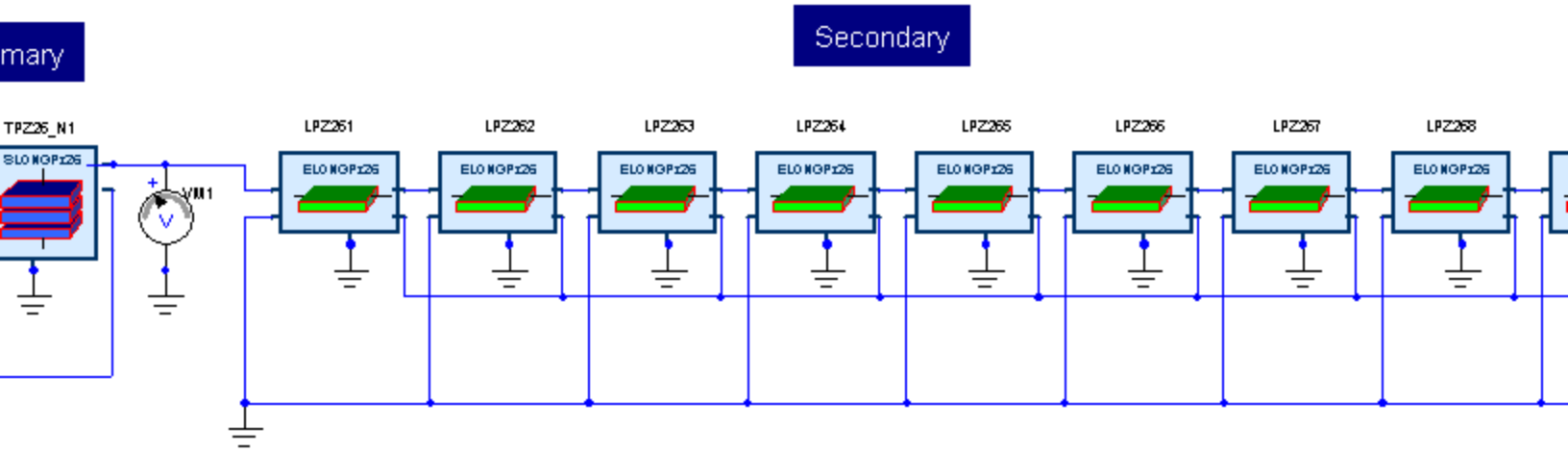

Figure 2. Application example of the Rosen Transverse Pz26 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal Pz26 LPZ261 - LPZ269	len	16.9m/9 [m]
	W	0.015 [m]
	th	0.001 [m]
Rosen Primary Layer Transverse PZ26 TPZ261	len	0.0141 [m]
	W	0.015 [m]
	th	0.001 [m]
	Nlayer	18
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

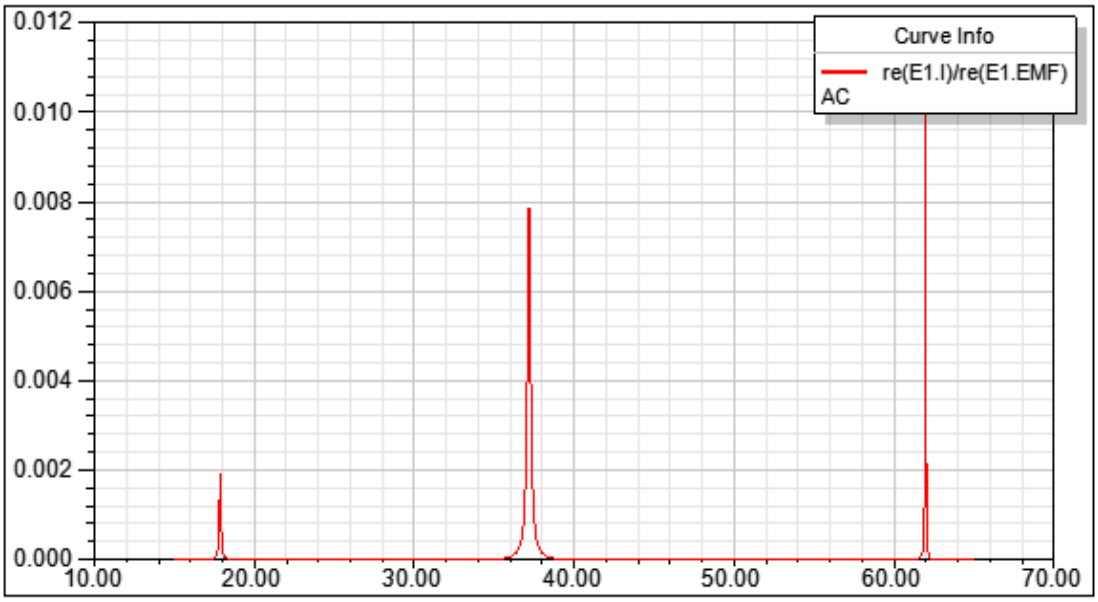

Figure 3. Simulation results-Input Conductance.

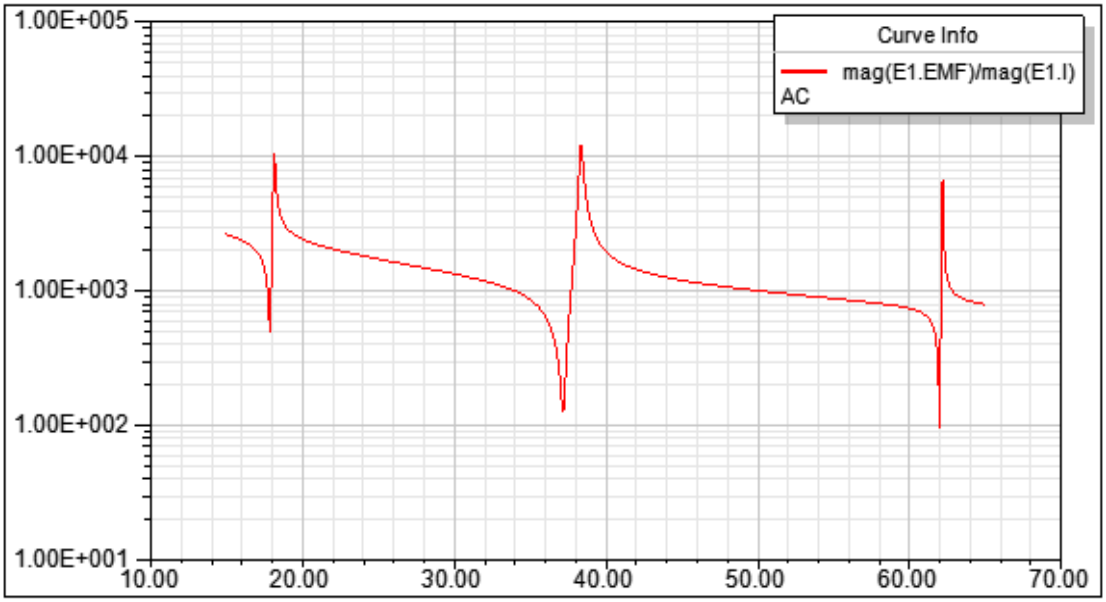

Figure 4. Simulation results-Input Impedance.

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References

TRANS Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

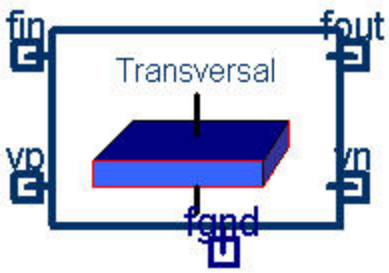

Figure 1. Component symbol

Description

This block represents a General Rosen Transverse Piezoelectric layer.

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Netlist Syntax

MODEL TRANS ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, W:= @W, Qm:= @Qm, rho:= @rho, s11_E:= @s11_E, E33_Tr:= @E33_Tr, Qe:= @Qe, k31:= @k31, th:= @th) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
rho	Density	real	7700 [kg/m^3]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.01 [m]
th	Piezoelectric Layer Thickness	real	0.001 [m]
Qm	Mechanical Quality Factor	real	2000
Qe	Electrical Quality Factor	real	333
k31	Electromechanical Coupling Factor	real	0.327
s11_E	Mechanical Compliance with Constant Electric Field	real	1.3e-11 [m^2/N]
E33_Tr	Relative Permittivity with Constant Stress	real	1330

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Example

This example a Rosen type transformer is comprised of a primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

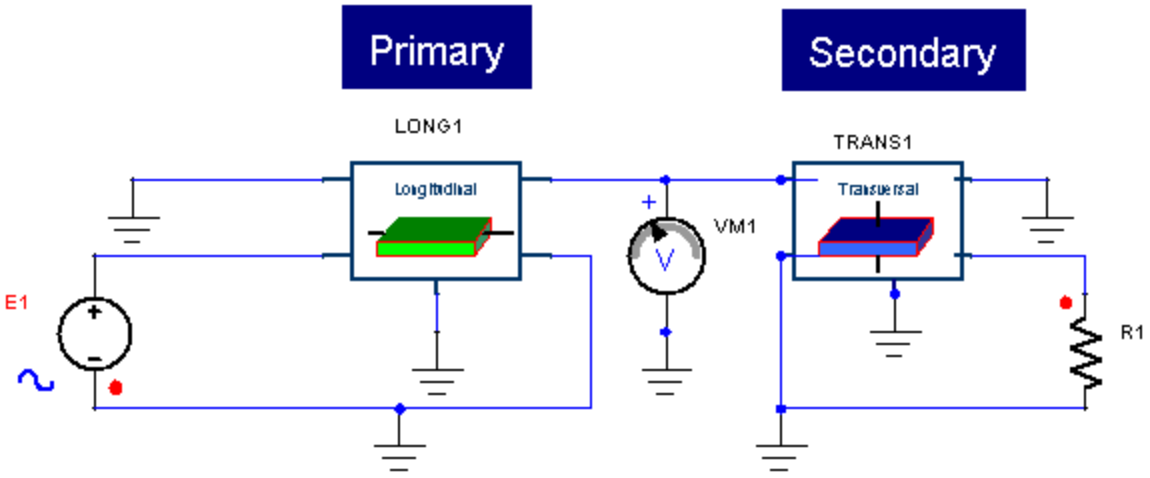

Figure 2. Application example of the Rosen General Transverse model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen General Secondary Layer Longitudinal LONG1	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen General Primary Layer Transverse TRANS TRANS1	len	0.04163 [m]
	W	0.024 [m]

	th	0.0029 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

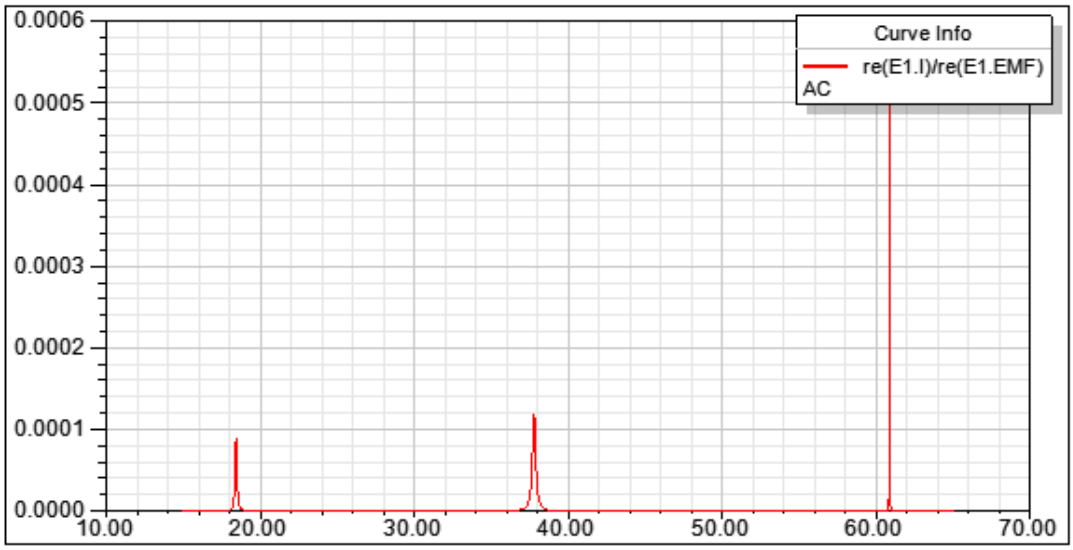

Figure 3. Simulation results-Input Conductance.

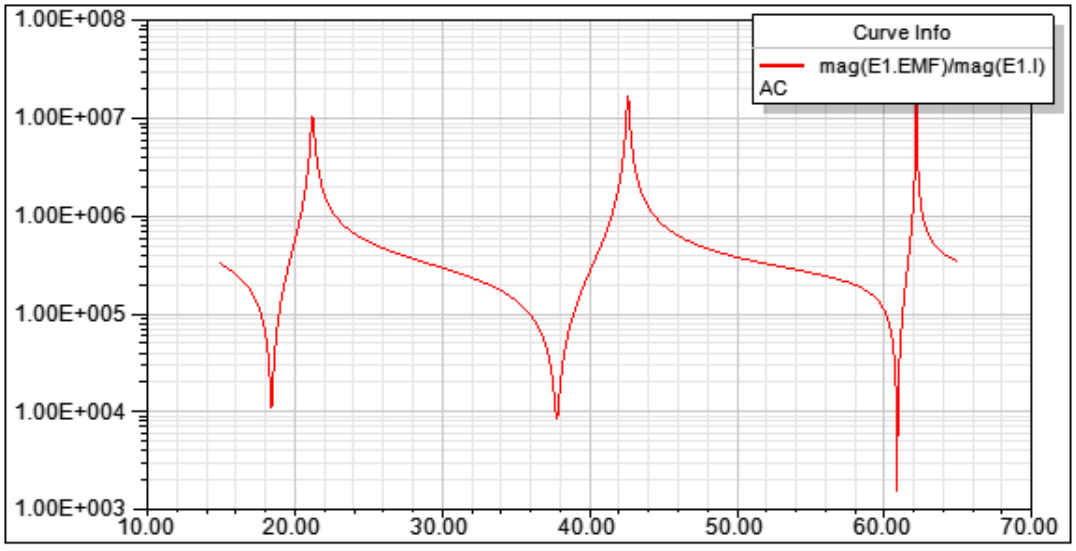

Figure 4. Simulation results-Input Impedance.

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References

Transverse Multilayer Rosen

- TD110_N: Primary layer of Rosen PT of material D110
- TD140_N: Primary layer of Rosen PT of material D140
- TPZ26_N: Primary layer of Rosen PT of material Pz26
- TRANS_N: General Transverse Multilayer

TD110_N Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

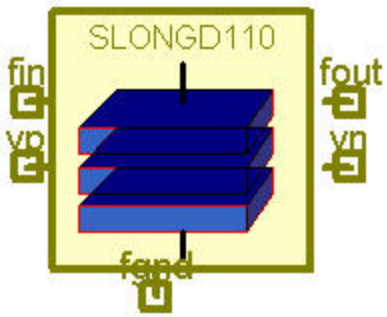

Figure 1. Component symbol

Description

This block represents a D110 Rosen Transverse Multilayer Piezoelectric layer.

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Netlist Syntax

MODEL TD110_N ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (W:= @W, len:= @len, th:= @th, Nlayer:= @Nlayer) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.005 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]
Nlayer	Number of Layers	real	1

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Example

This example a Rosen type transformer is comprised of a multilayer primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

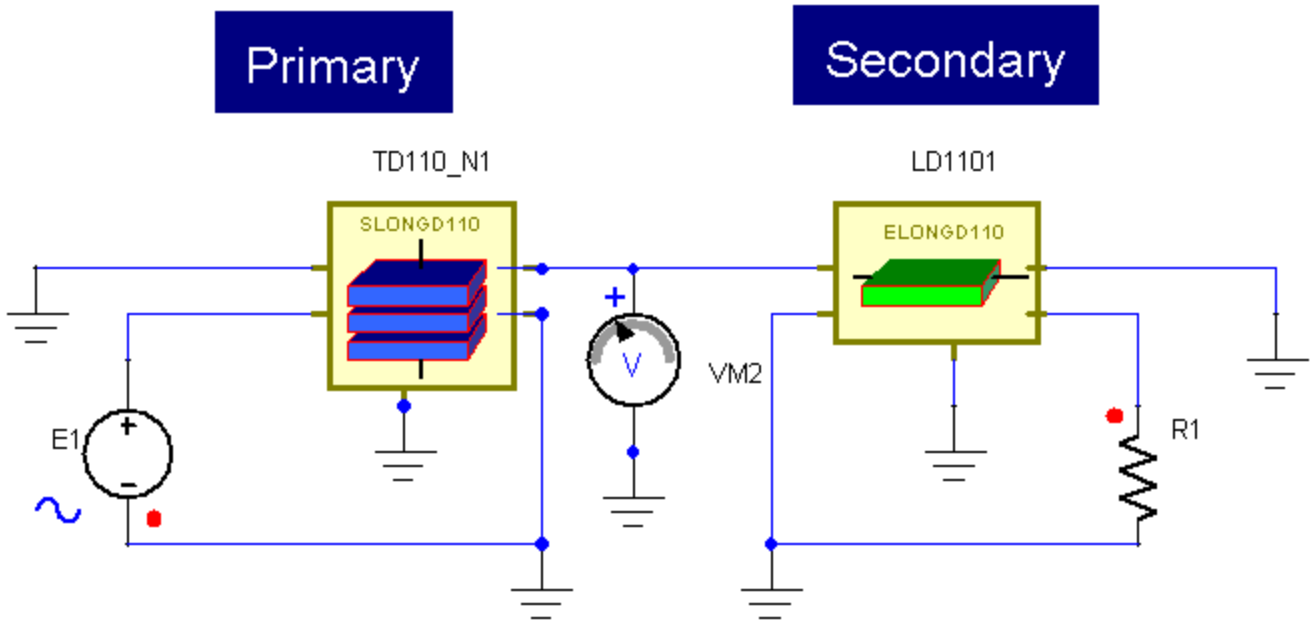

Figure 2. Application example of the Rosen Transverse Multilayer D110 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal D110 LD1101	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen Primary Layer Transverse D110 TD1101	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
	Nlayer	3

Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

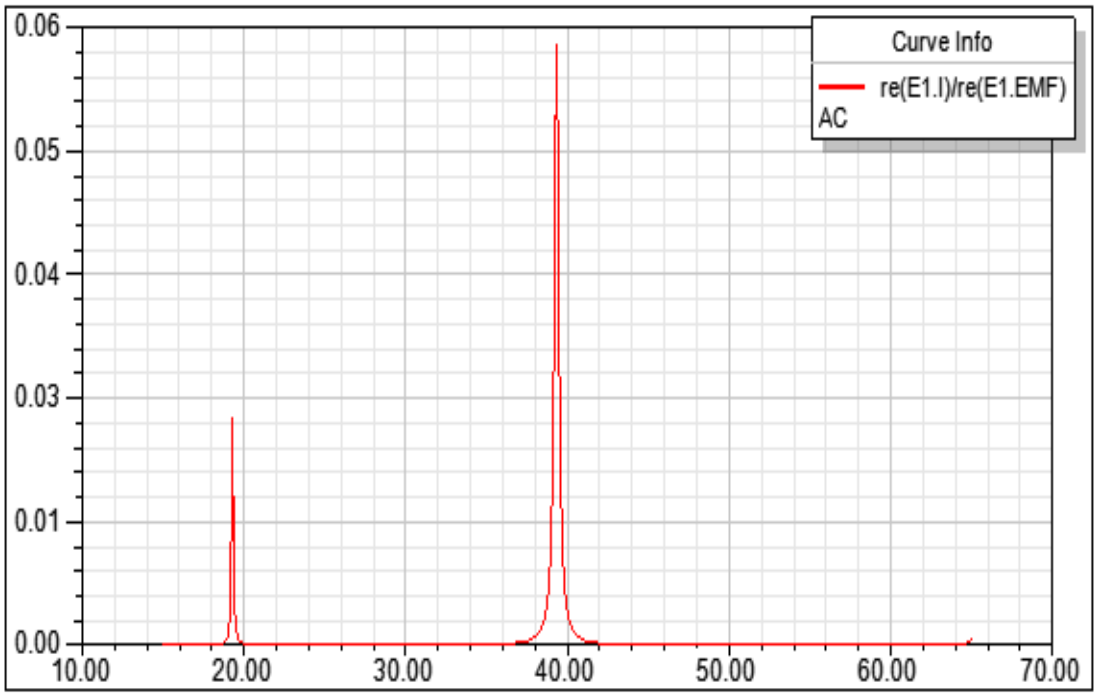

Figure 3. Simulation results-Input Conductance.

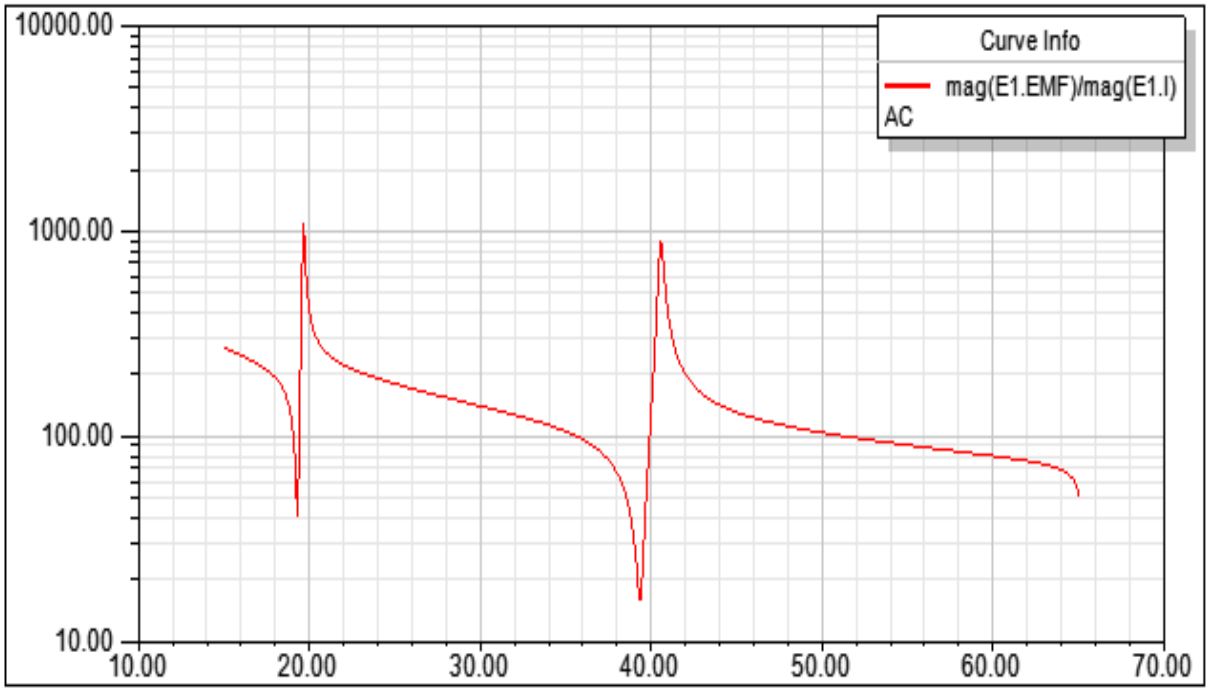

Figure 4. Simulation results-Input Impedance.

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References

TD140_N Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

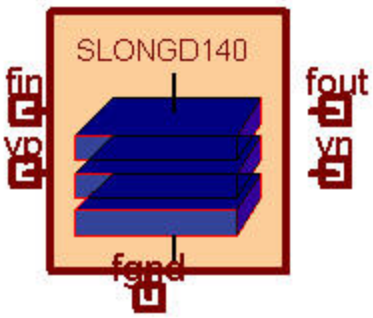

Figure 1. Component symbol

Description

This block represents a D140 Rosen Transverse Multilayer Piezoelectric layer.

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Netlist Syntax

MODEL TD140_N ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (W:= @W, len:= @len, th:= @th, Nlayer:= @Nlayer) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.005 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]
Nlayer	Number of Layers	real	1

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Example

This example a Rosen type transformer is comprised of a multilayer primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

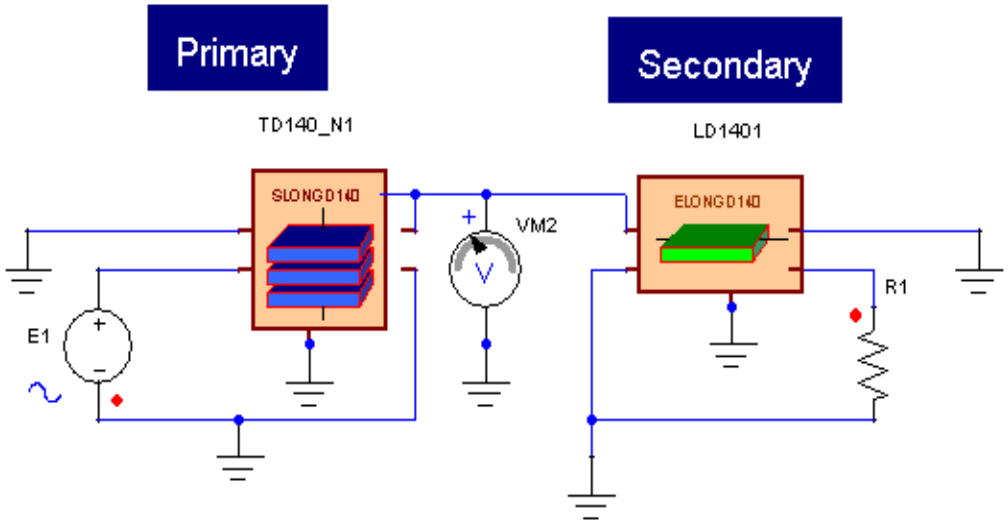

Figure 2. Application example of the Rosen Transverse Multilayer D140 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal D140 LD1401	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen Primary MultiLayer Transverse TD140_N1	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
	Nlayer	3
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

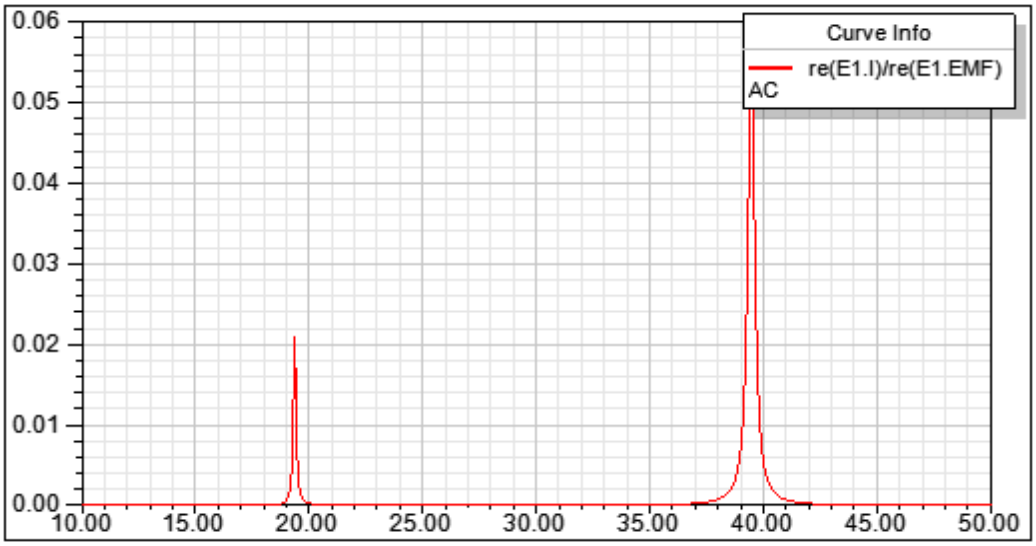

Figure 3. Simulation results-Input Conductance.

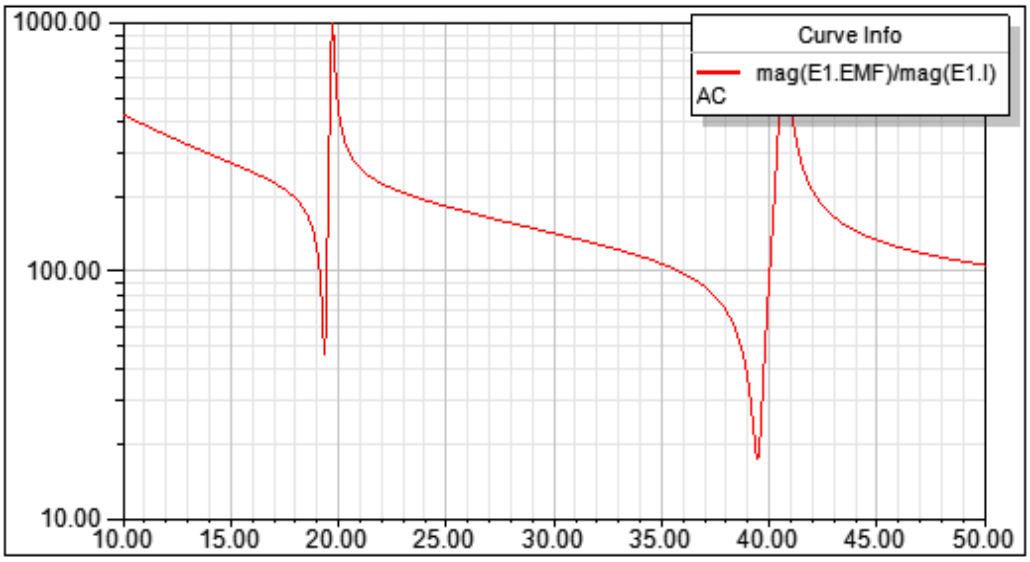

Figure 4. Simulation results-Input Impedance.

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References

TPZ26_N Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

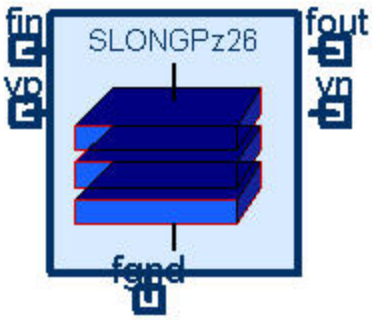

Figure 1. Component symbol

Description

This block represents a PZ26 Rosen Transverse Multilayer Piezoelectric layer.

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Netlist Syntax

MODEL TPZ26_N ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (W:= @W, len:= @len, th:= @th, Nlayer:= @Nlayer) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.005 [m]
th	Piezoelectric Layer Thick-ness	real	0.001 [m]
Nlayer	Number of Layers	real	1

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Example

This example a Rosen type transformer is comprised of a multilayer primary vibrating in thick-ness mode (SLONG) and a secondary vibrating in longitudinal mode (ELONG).

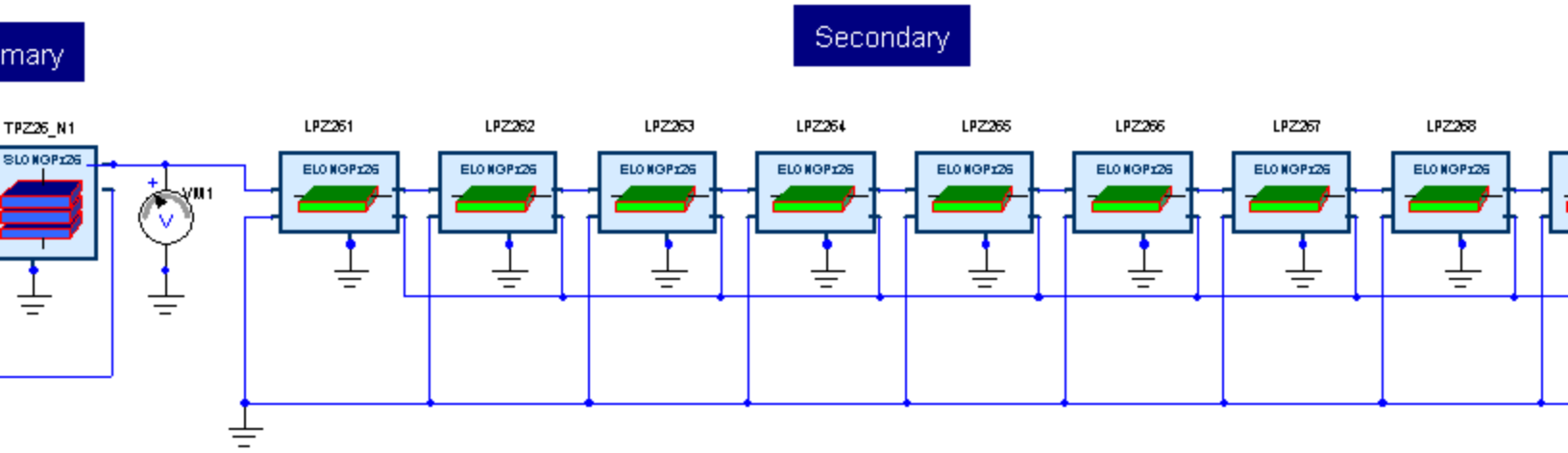

Figure 2. Application example of the Rosen Multilayer Transverse Pz26 model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen Secondary Layer Longitudinal Pz26 LPZ261 - LPZ269	len	16.9m/9 [m]
	W	0.015 [m]
	th	0.001 [m]
Rosen Primary Layer Transverse PZ26 TPZ261	len	0.0141 [m]
	W	0.015 [m]
	th	0.001 [m]
	Nlayer	18
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

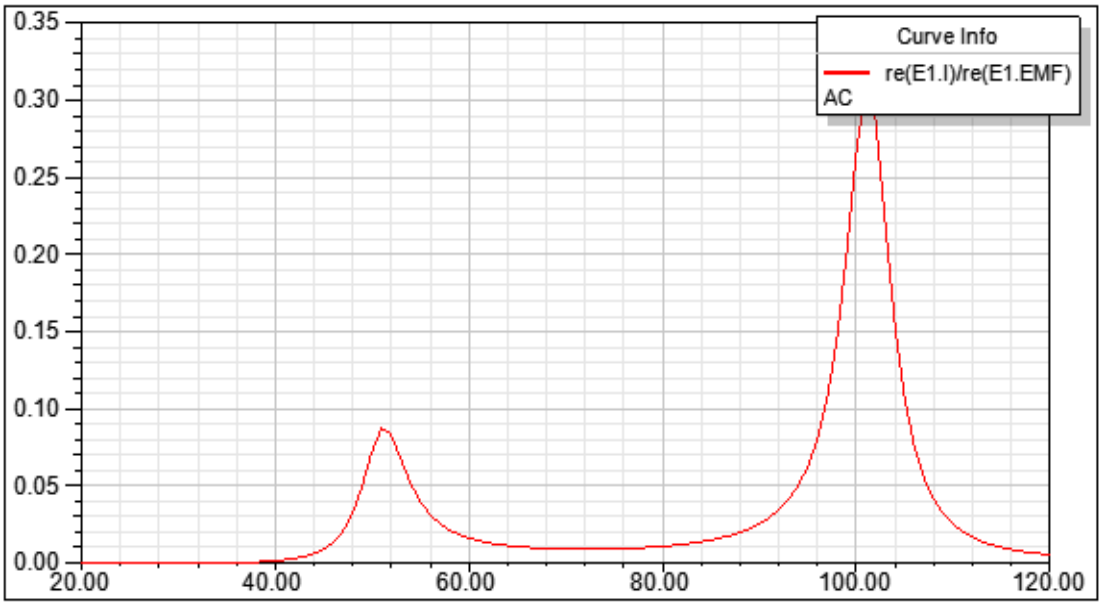

Figure 3. Simulation results-Input Conductance.

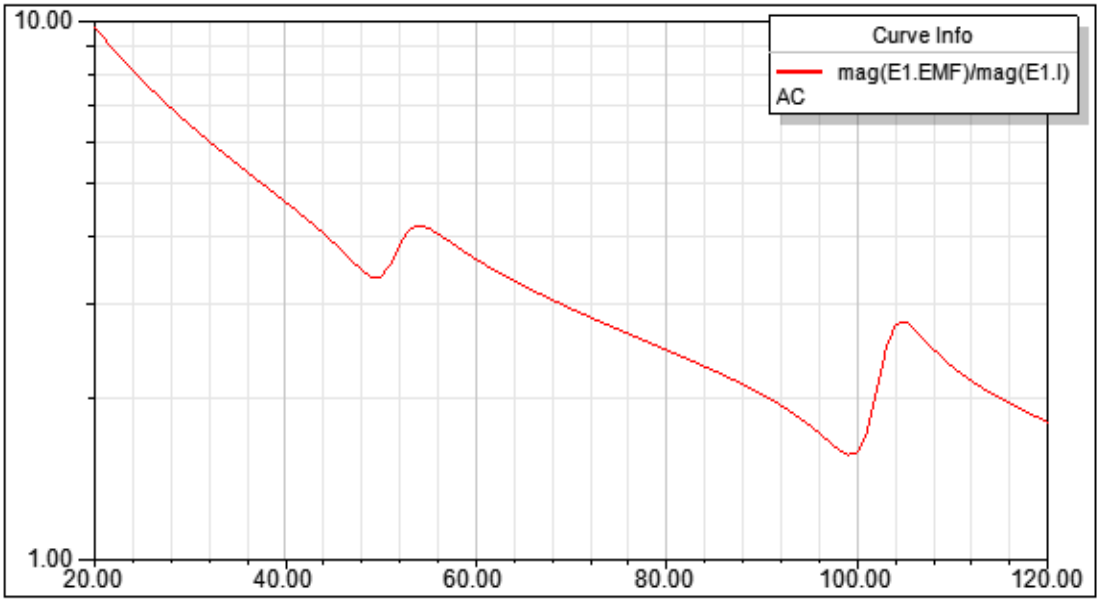

Figure 4. Simulation results-Input Impedance.

Top

References

TRANS_N Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

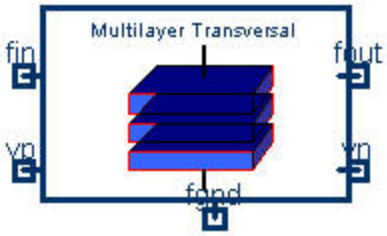

Figure 1. Component symbol

Description

This block represents a General Rosen Transverse Multilayer Piezoelectric layer. The multilayer structure can be modeled as a single transverse mode piezoelectric layer taking into account that the force will be multiplied by the number of layers and the input current is also multiplied by the number of layers in parallel.

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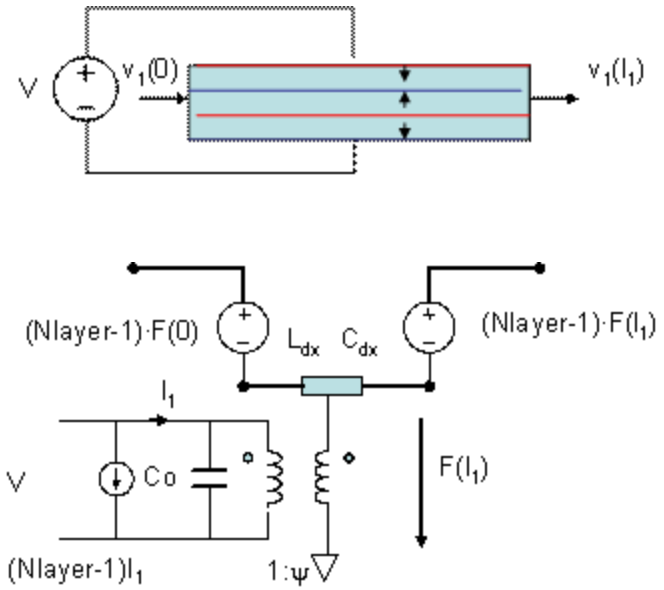
Mathematical Description



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Netlist Syntax

MODEL TRANS_N ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (W:= @W, len:= @len, th:= @th, Nlayer:= @Nlayer, E33_Tr:= @E33_Tr, rho:= @rho, k31:= @k31, s11_E:= @s11_E, Qe:= @Qe, Qm:= @Qm) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
rho	Density	real	7700 [kg/m^3]
len	Piezoelectric Layer Length	real	0.01 [m]
W	Piezoelectric Layer Width	real	0.005 [m]
th	Piezoelectric Layer Thickness	real	0.001 [m]
Qm	Mechanical Quality Factor	real	2000
Qe	Electrical Quality Factor	real	333
k31	Electromechanical Coupling Factor	real	0.327
s11_E	Mechanical Compliance with Constant Electric Field	real	1.3e-11 [m^2/N]
E33_Tr	Relative Permittivity with Constant Stress	real	1330
Nlayer	Number of Layers	real	1

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Example

This example a Rosen type transformer is comprised of a primary layer vibrating in thickness mode (SLONG) and a secondary layer vibrating in longitudinal mode (ELONG).

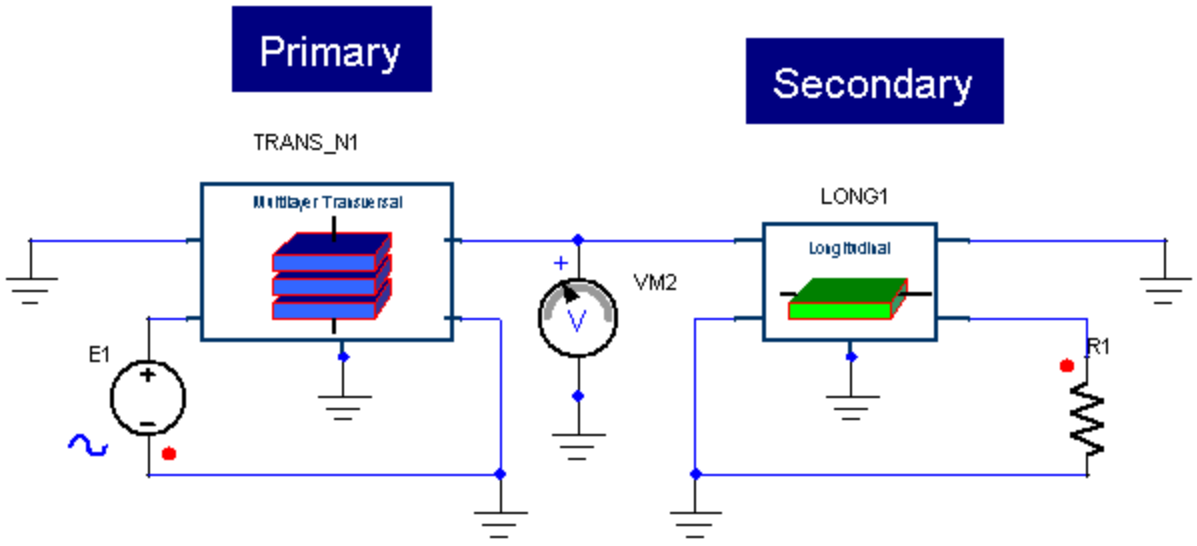

Figure 2. Application example of the Rosen General Transverse Multilayer model

Table 3. System Parameters

Component	Parameter	Value [unit]
Rosen General Secondary Layer Longitudinal LONG1	len	0.04163 [m]
	W	0.024 [m]
	th	0.0029 [m]
Rosen General Primary MultiLayer Transverse TRANS_N1	len	0.03837 [m]
	W	0.024 [m]
	th	0.0029 [m]
	Nlayer	3
Resistor R1	R	10000 [Ohm]

Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

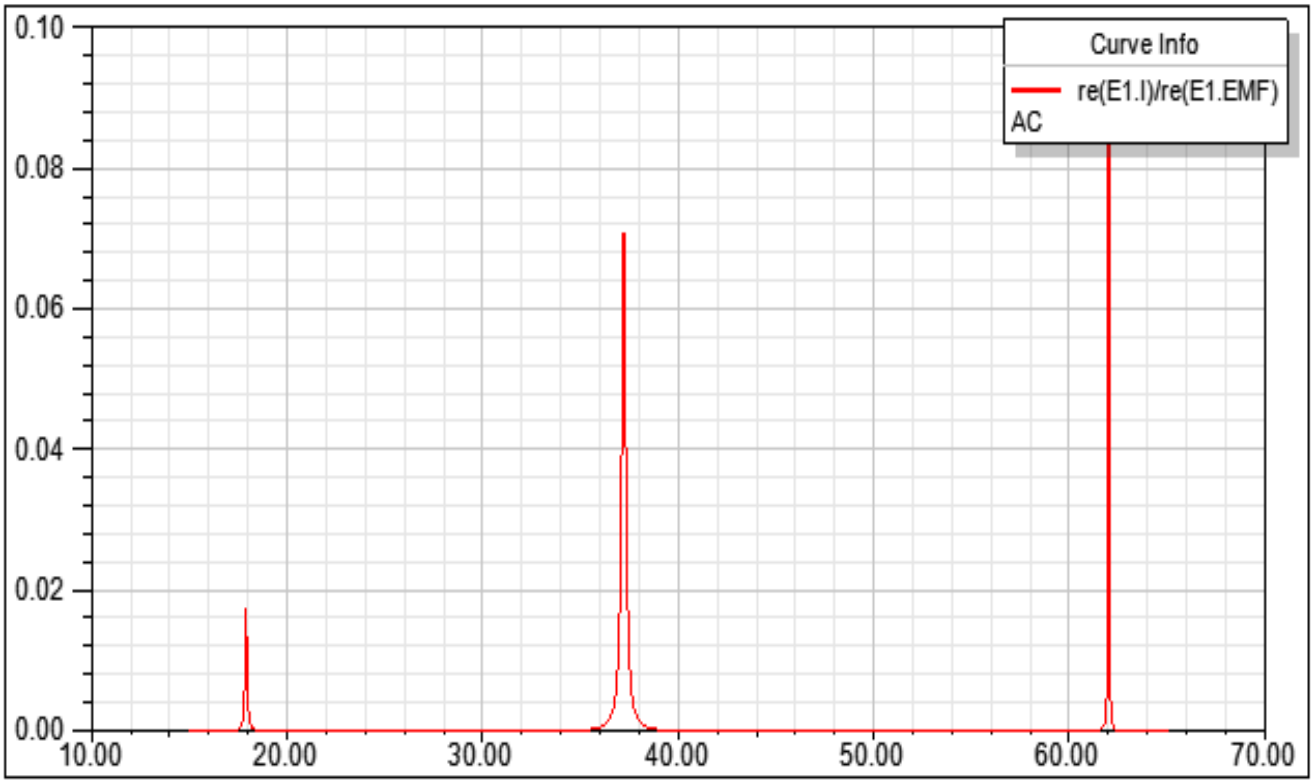

Figure 3. Simulation results-Input Conductance.

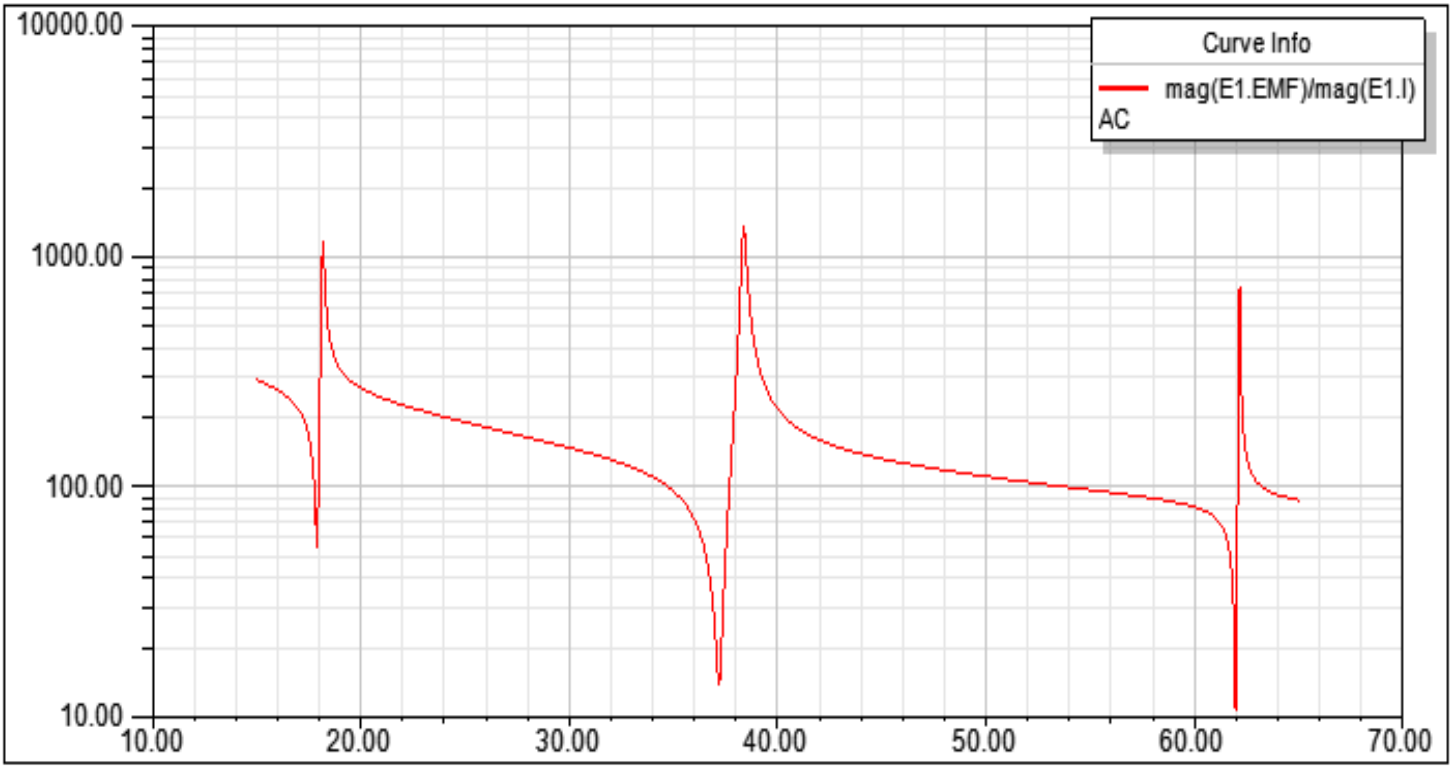

Figure 4. Simulation results-Input Impedance.

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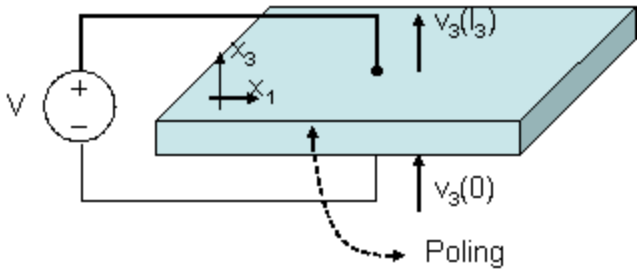
References

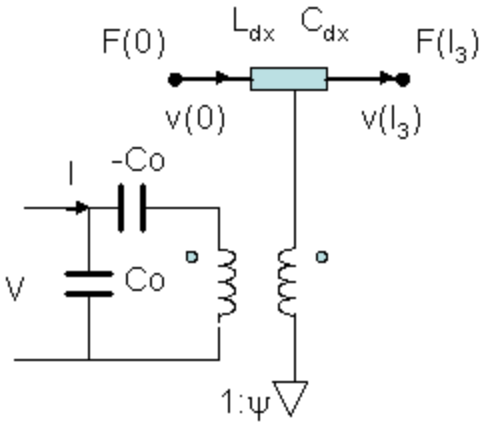
Piezoelectric - Thickness

- BulkG: General Thickness Bulk
- bulkPz26: Block of non polarized material PZ26
- bulkPz27: Block of non polarized material Pz27
- bulkPz34: Block of non polarized material Pz34
- PZ26n: Layer of material Pz26n vibrating in thickness mode and polarized directly
- PZ26p: Layer of material Pz26p vibrating in thickness mode and polarized directly
- PZ27n: Layer of material Pz27n vibrating in thickness mode and polarized directly
- PZ27p: Layer of material Pz27p vibrating in thickness mode and polarized directly
- PZ34n: Layer of material Pz34n vibrating in thickness mode and polarized directly
- PZ34p: Layer of material Pz34p vibrating in thickness mode and polarized directly
- PZL: General Thickness Model p
- PZL1: General Thickness Model n

Thickness Mode of Vibration

In this mode of vibration the electric field is applied in the poling direction, x3, and the movement takes places also in this direction. Applying Newton's law, Maxwell's equations and piezoelectric relations it is possible to obtain an electrical equivalent circuit in which force is represented by voltage and velocity is represented by current.





$$L_{dx} = \rho \cdot A_3$$

$$C_{dx} = \frac{s_{33}^{D}}{A_3}$$

$$\psi = \frac{A_3}{l_3} \frac{d_{33}}{s_{33}^{E}}$$

$$Co = \frac{A_3}{l_3} \varepsilon_{33}^{T} \left(1 - k_{33}^{2}\right)$$

$$s_{33}^{D} = s_{33}^{E} \left(1 - k_{33}^{2}\right)$$

Generic Bulk Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

Figure 1. Component symbol

Description

This block represents a generic bulk layer.

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Netlist Syntax

MODEL BulkG ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1 (len:= @len, Area:= @Area, Qm:= @Qm, rho:= @rho, s33:= @s33) SRC: DB(Lib:- :=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	.0001 [m^2]
Qm	Mechanical Quality Factor	real	2000
rho	Density	real	7700 [kg/m^3]
s33	Mechanical Compliance	real	8.13e-12

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

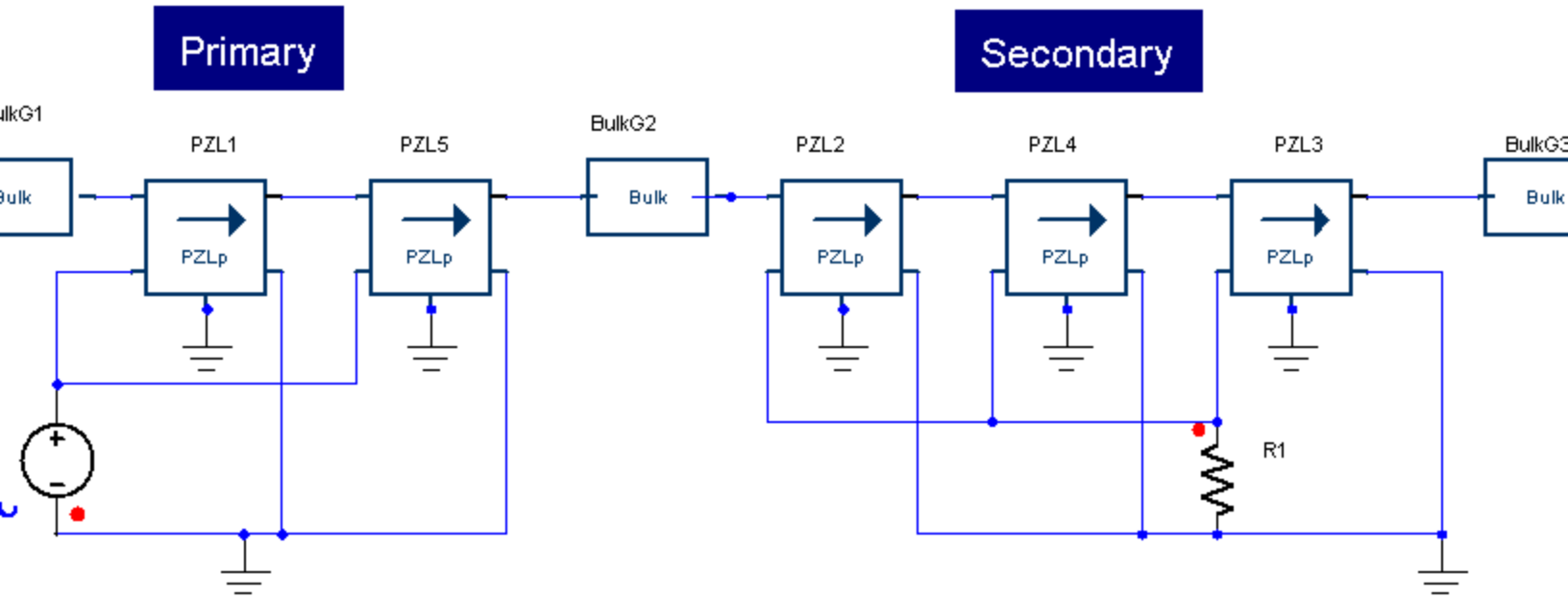

Figure 2. Application example of the BulkG piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
General Bulk material BulkG1/BulkG3	len	0.0001 [m]
General Bulk material BulkG2	len	0.001 [m]
Material Layer vibrating in thickness mode PZL1/PZL2/PZL3/PZL4/PZL5	len	0.001 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

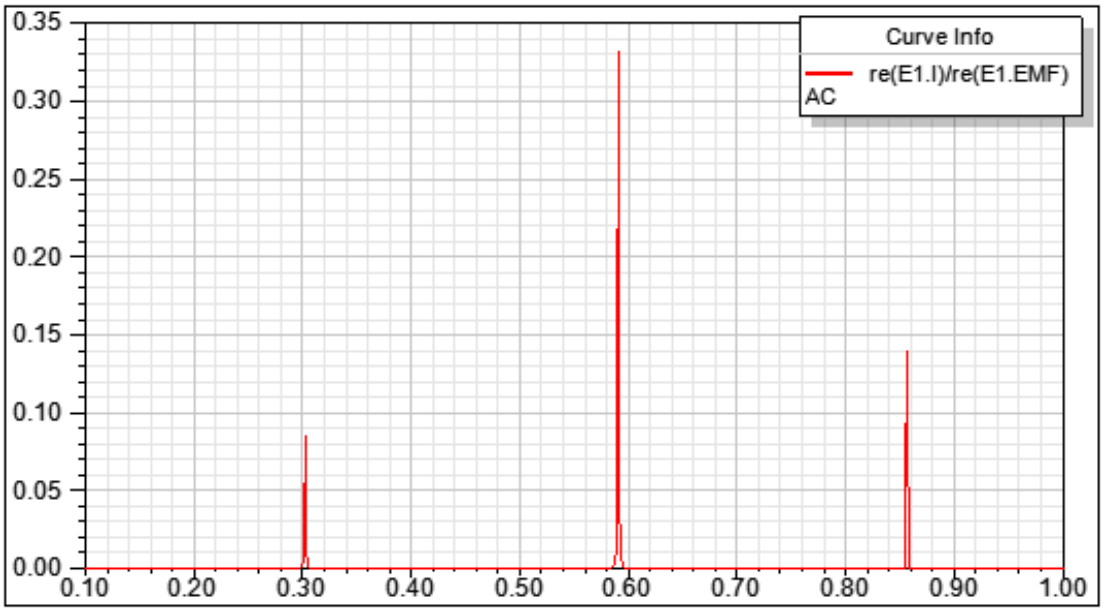

Figure 3. Simulation results-Input Conductance.

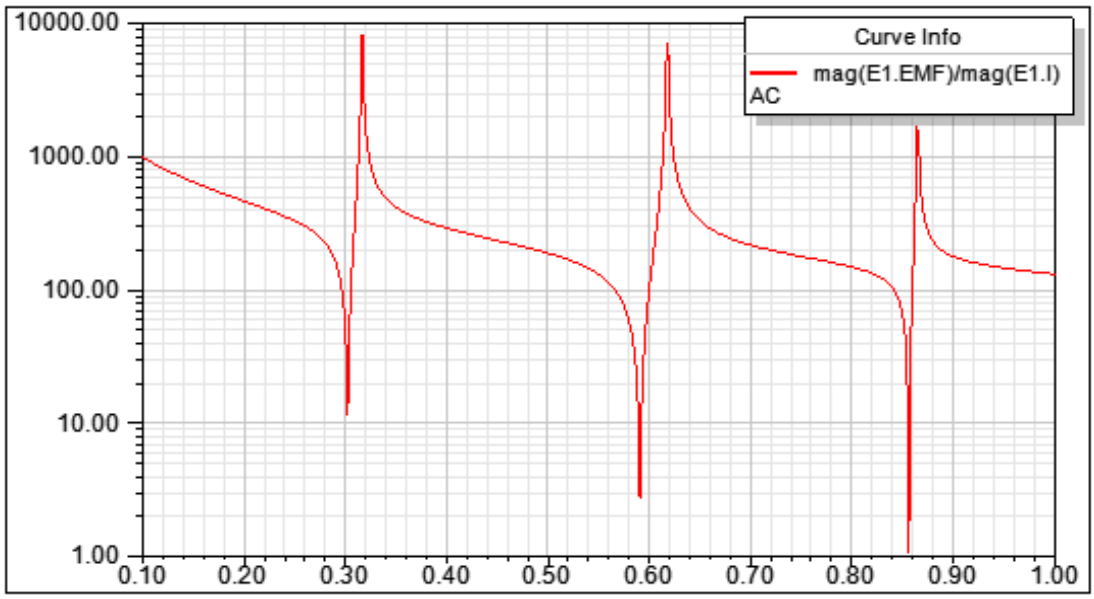

Figure 4. Simulation results-Input Impedance.

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References

PZ26 Bulk Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

Figure 1. Component symbol

Description

This block represents a PZ26 bulk layer.

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Netlist Syntax

MODEL bulkPz26 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) f1:= %0, f2:= %1 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
f1	Mechanical Force Pin	Electrical terminal
f2	Mechanical Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0
Area	Piezoelectric Layer Area	real	0

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

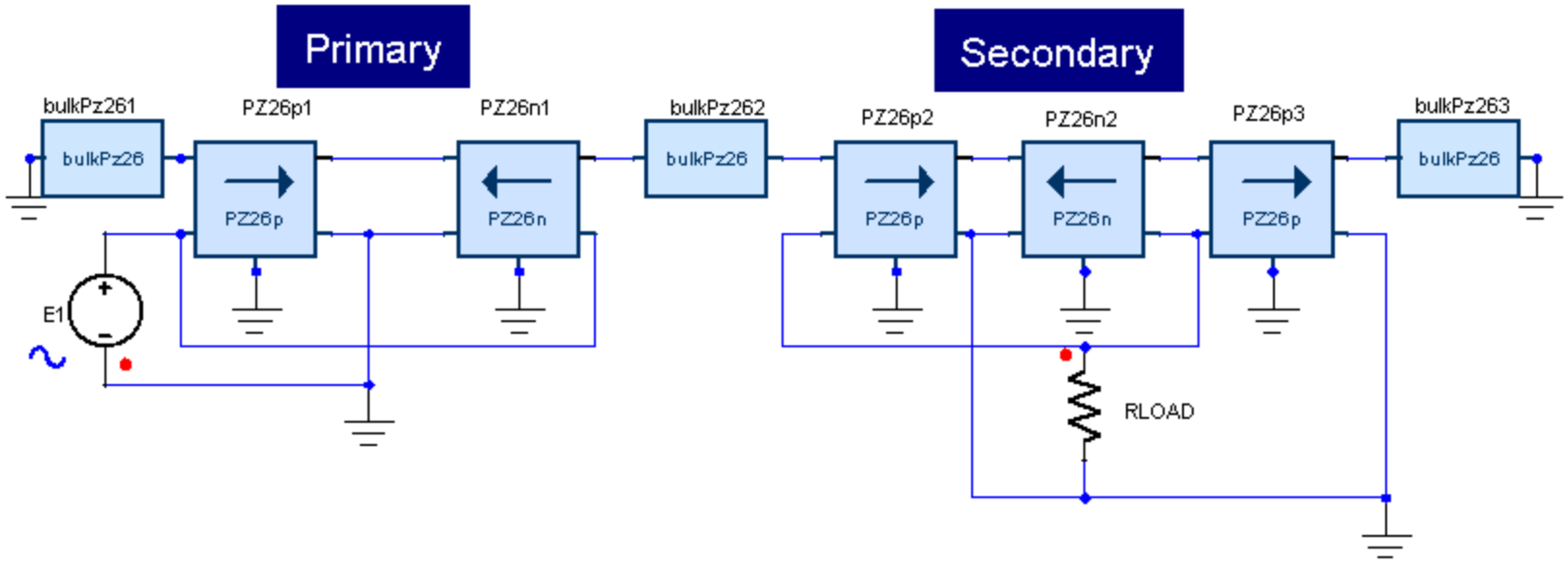

Figure 2. Application example of the BulkPZ26 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ261/BulkPZ263	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ262	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ26p1/PZ26p2/PZ26p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ26n1/PZ26n2	len	0.001 [m]
Resistor RLOAD	R	10000

		[Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

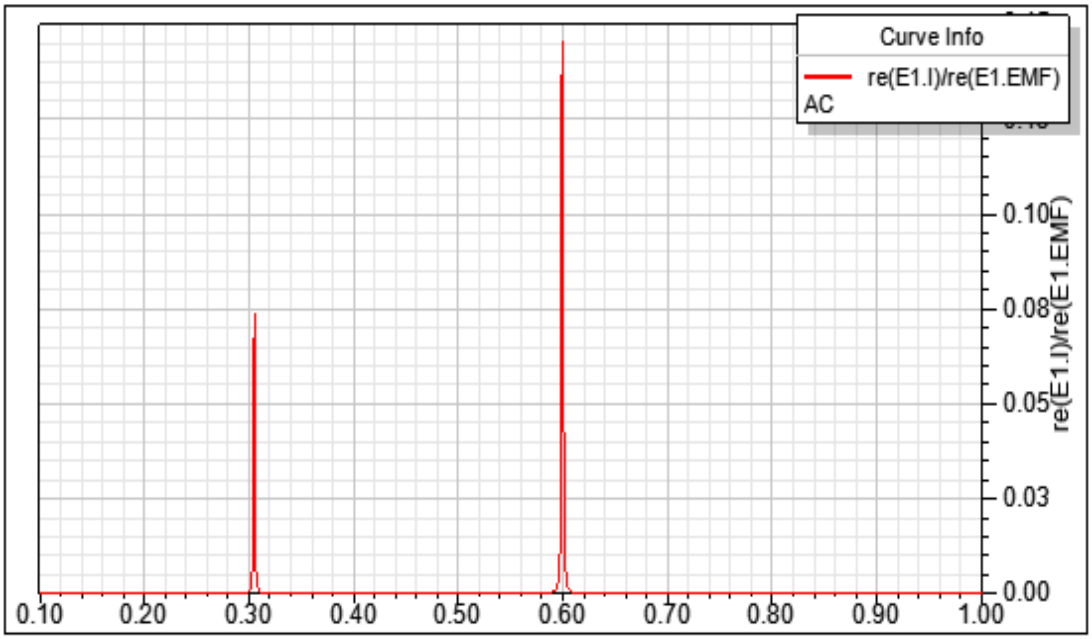

Figure 3. Simulation results-Input Conductance.

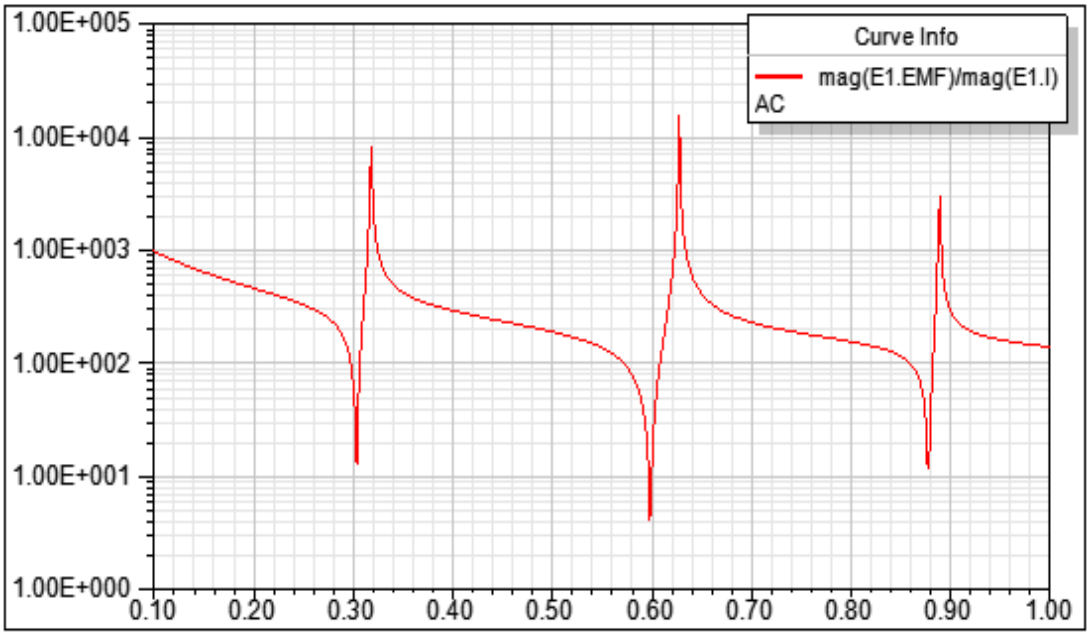

Figure 4. Simulation results-Input Impedance.

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References

PZ27 Bulk Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

Figure 1. Component symbol

Description

This block represents a PZ27 bulk layer.

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Netlist Syntax

MODEL bulkPz27 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) f1:= %0, f2:= %1 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
f1	Mechanical Force Pin	Electrical terminal
f2	Mechanical Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0 [m]
Area	Piezoelectric Layer Area	real	0 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

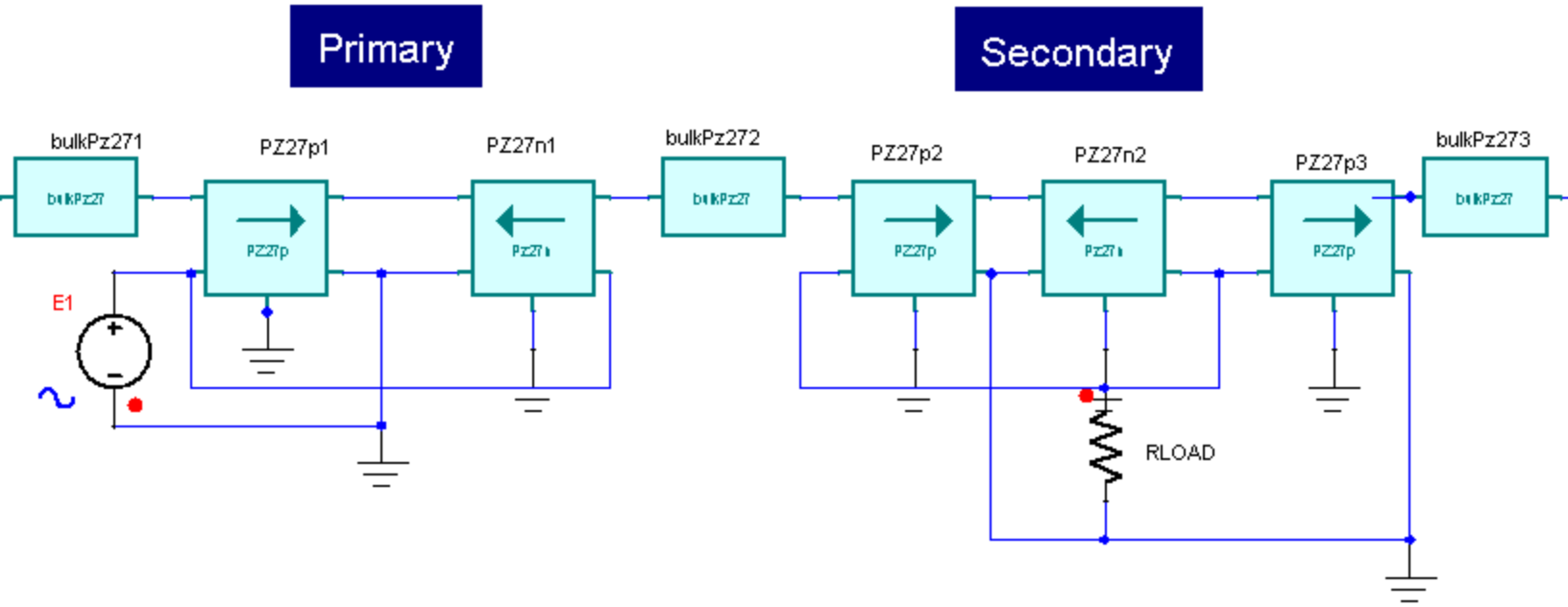

Figure 2. Application example of the BulkPZ27 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ271/BulkPZ273	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ272	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ27p1/PZ27p2/PZ27p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ27n1/PZ27n2	len	0.001 [m]
Resistor RLOAD	R	10000

		[Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

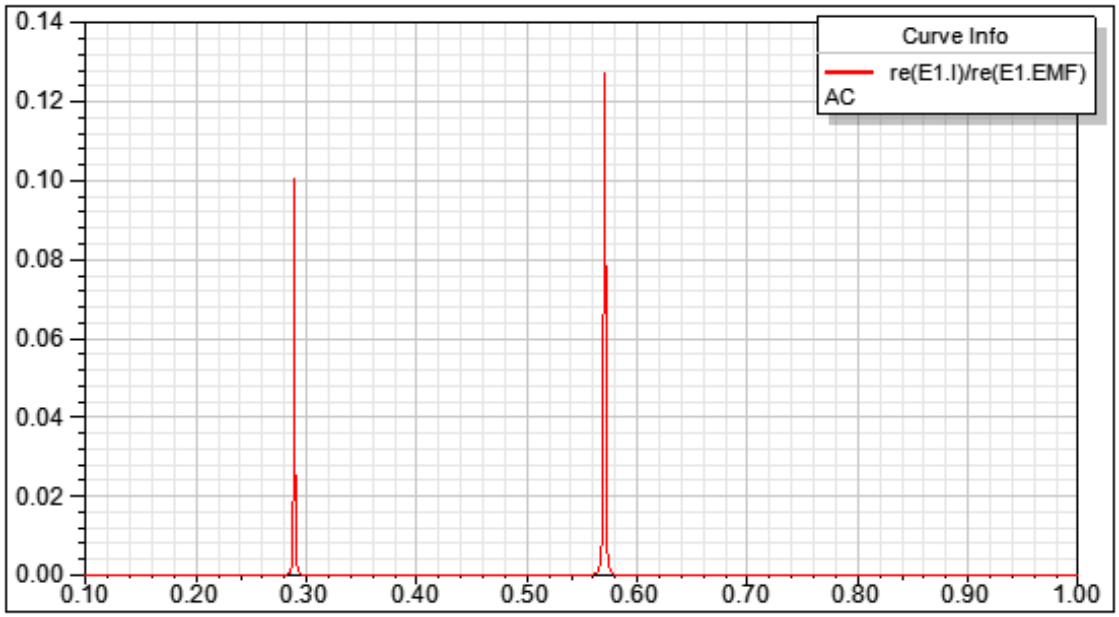

Figure 3. Simulation results-Input Conductance.

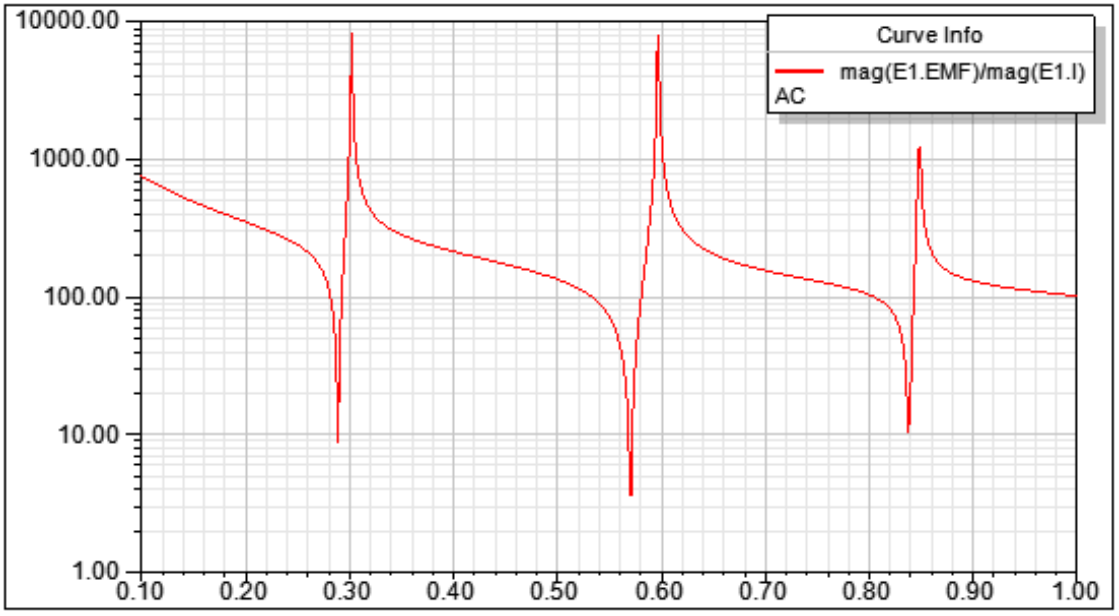

Figure 4. Simulation results-Input Impedance.

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References

PZ34 Bulk Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

Figure 1. Component symbol

Description

This block represents a PZ34 bulk layer.

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Netlist Syntax

MODEL bulkPz34 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) f1:= %0, f2:= %1 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
f1	Mechanical Force Pin	Electrical terminal
f2	Mechanical Force Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0 [m]
Area	Piezoelectric Layer Area	real	0 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

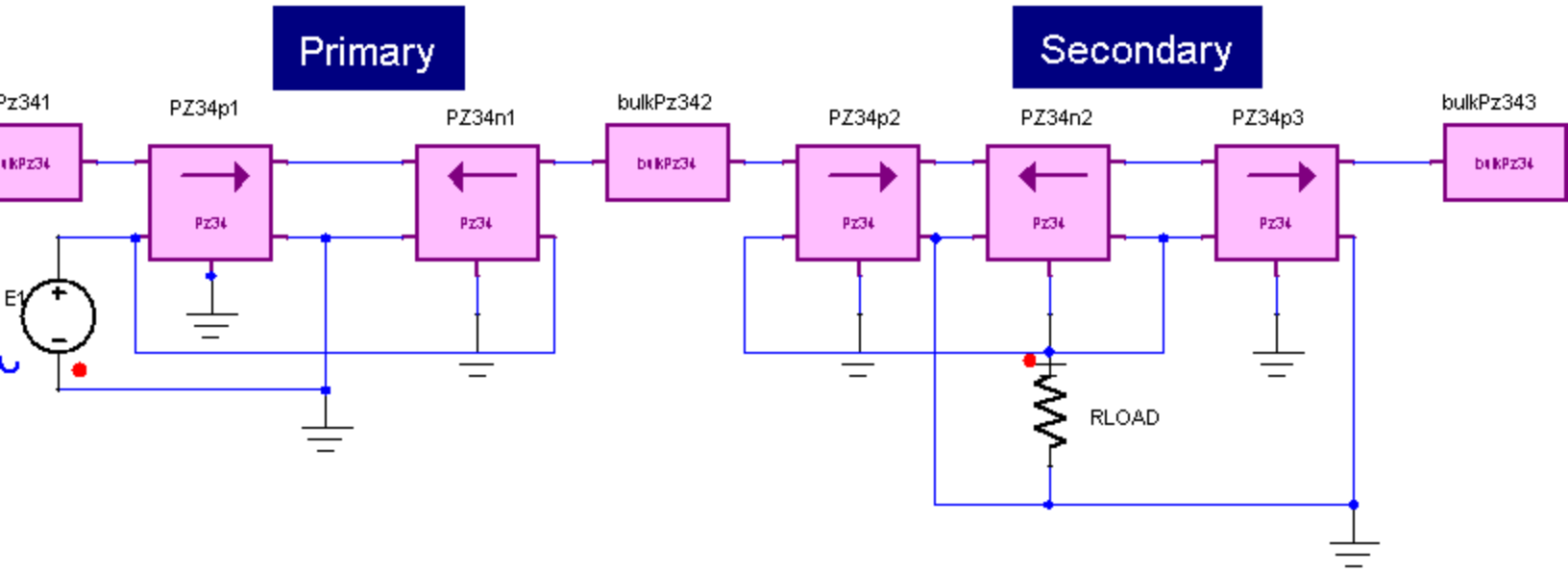

Figure 2. Application example of the BulkPZ34 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ341/BulkPZ343	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ342	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ34p1/PZ34p2/PZ34p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ34n1/PZ34n2	len	0.001 [m]
Resistor RLOAD	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

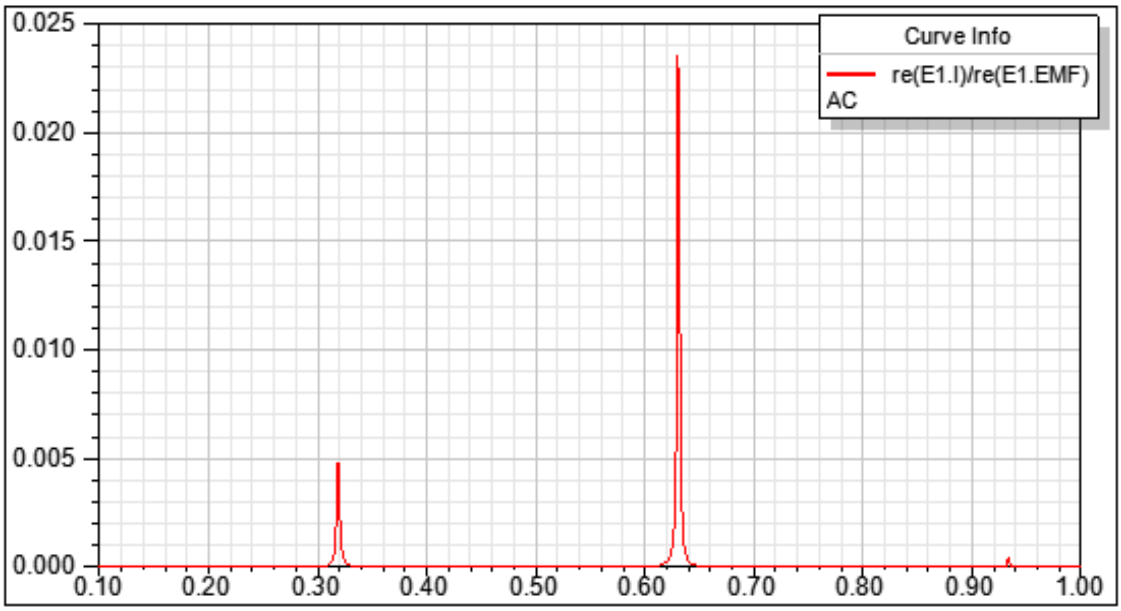

Figure 3. Simulation results-Input Conductance.

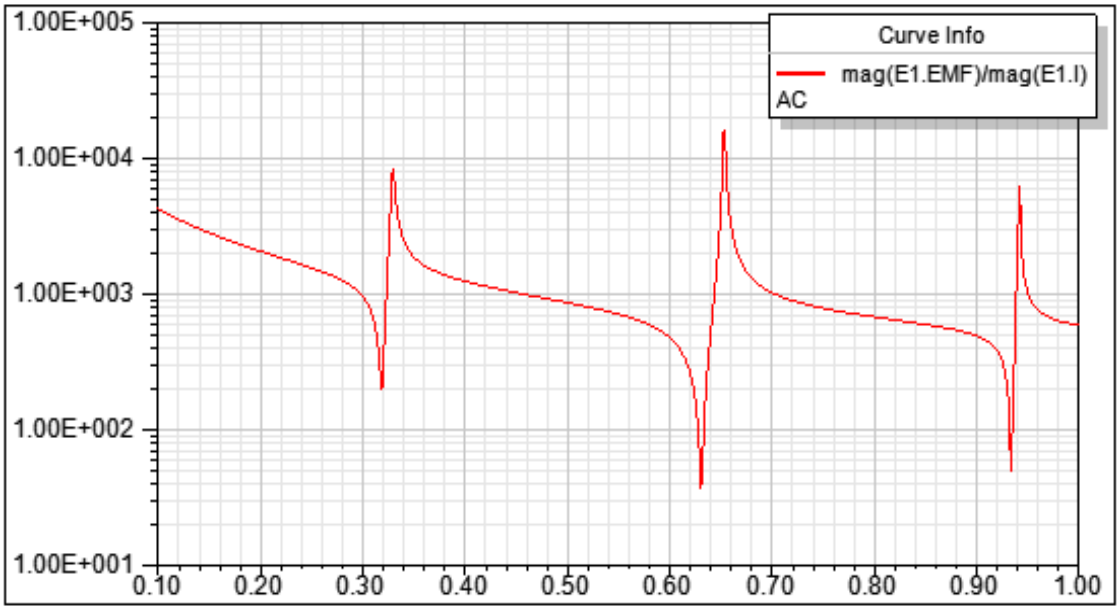

Figure 4. Simulation results-Input Impedance.

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References

PZ26n Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

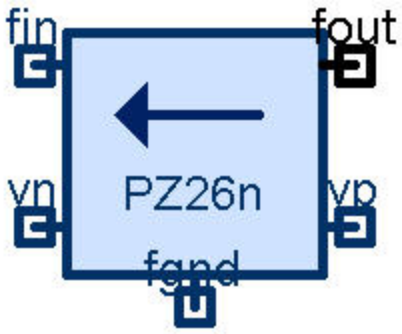

Figure 1. Component symbol

Description

This block represents a PZ26 Piezoelectric layer.

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Netlist Syntax

MODEL PZ26n ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

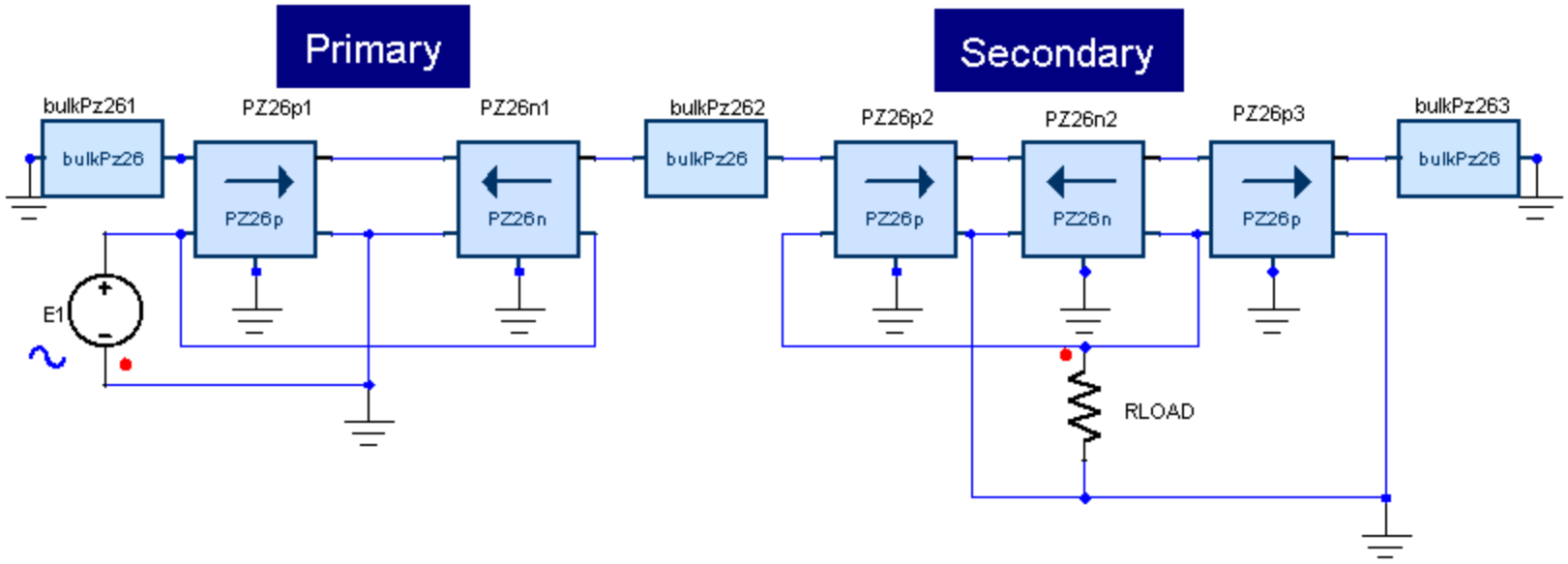

Figure 2. Application example of the BulkPZ26 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ261/BulkPZ263	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ262	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ26p1/PZ26p2/PZ26p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ26n1/PZ26n2	len	0.001 [m]
Resistor RLOAD	R	10000

		[Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

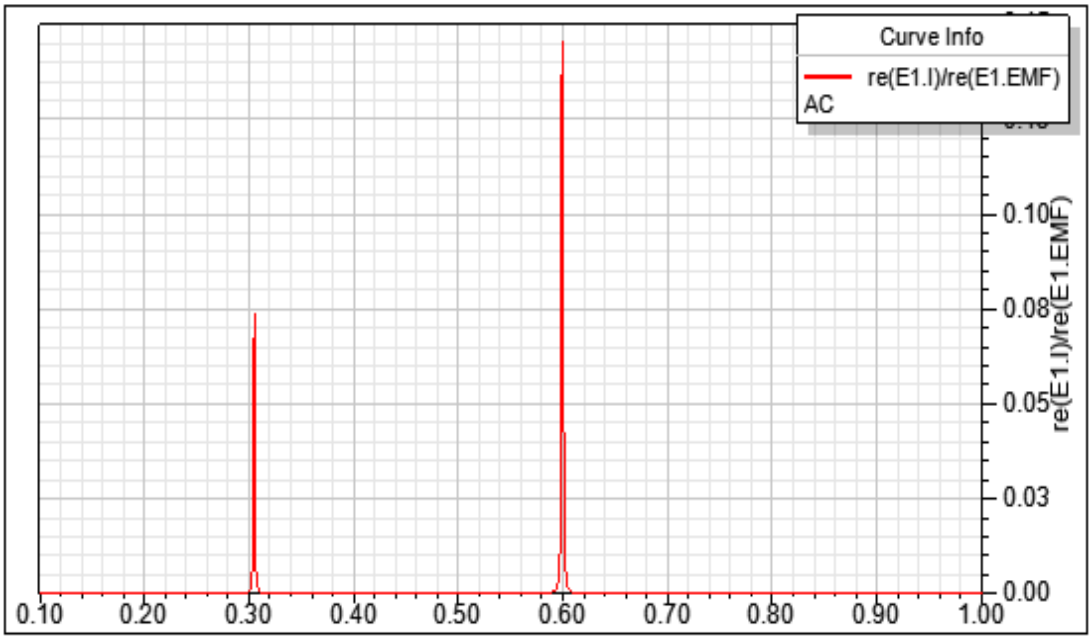

Figure 3. Simulation results-Input Conductance.

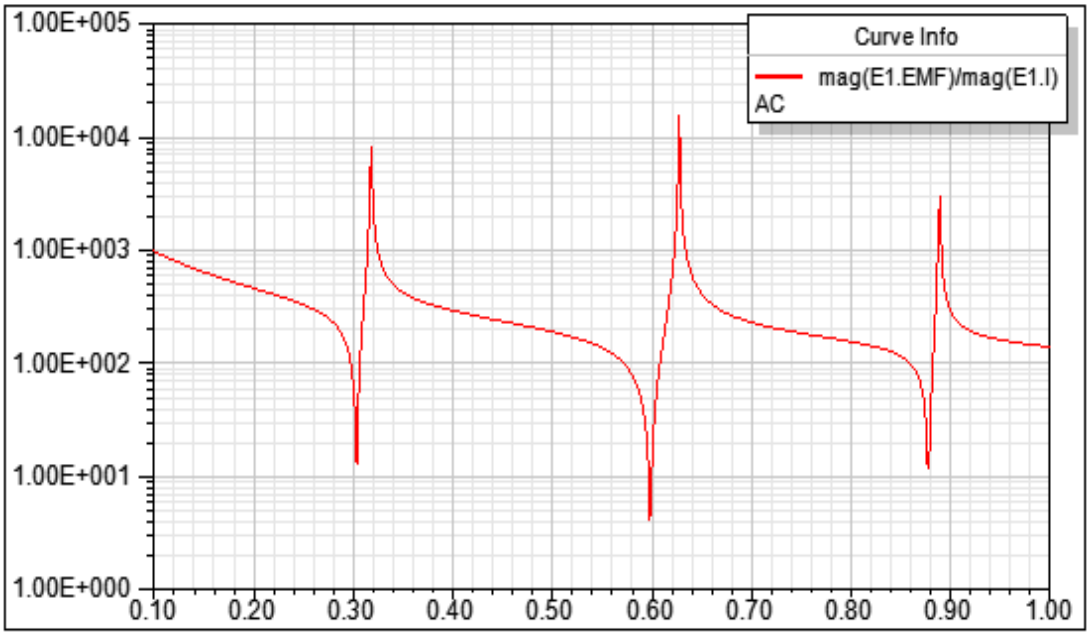

Figure 4. Simulation results-Input Impedance.

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References

PZ26p Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

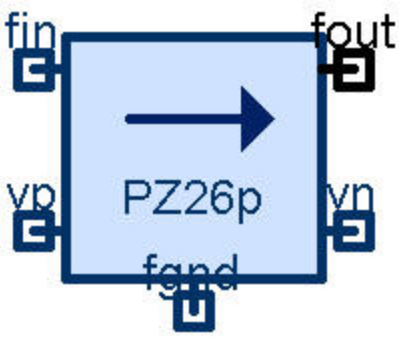

Figure 1. Component symbol

Description

This block represents a PZ26 Piezoelectric layer.

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Netlist Syntax

MODEL PZ26p ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

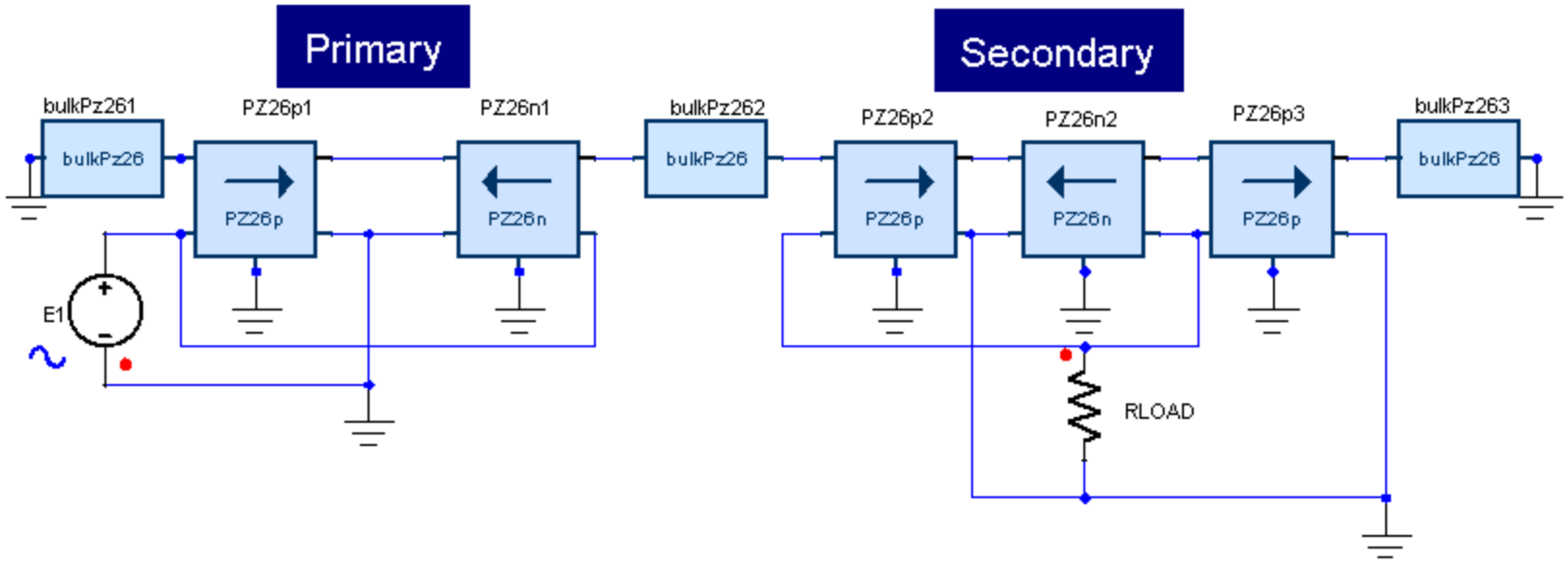

Figure 2. Application example of the BulkPZ26 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ261/BulkPZ263	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ262	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ26p1/PZ26p2/PZ26p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ26n1/PZ26n2	len	0.001 [m]
Resistor RLOAD	R	10000

		[Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

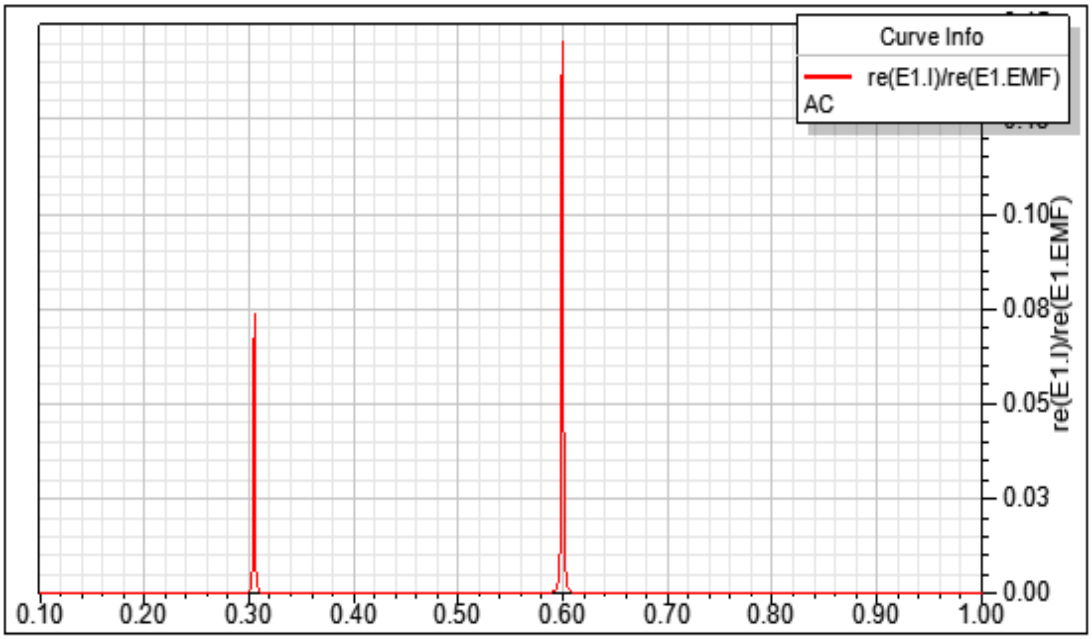

Figure 3. Simulation results-Input Conductance.

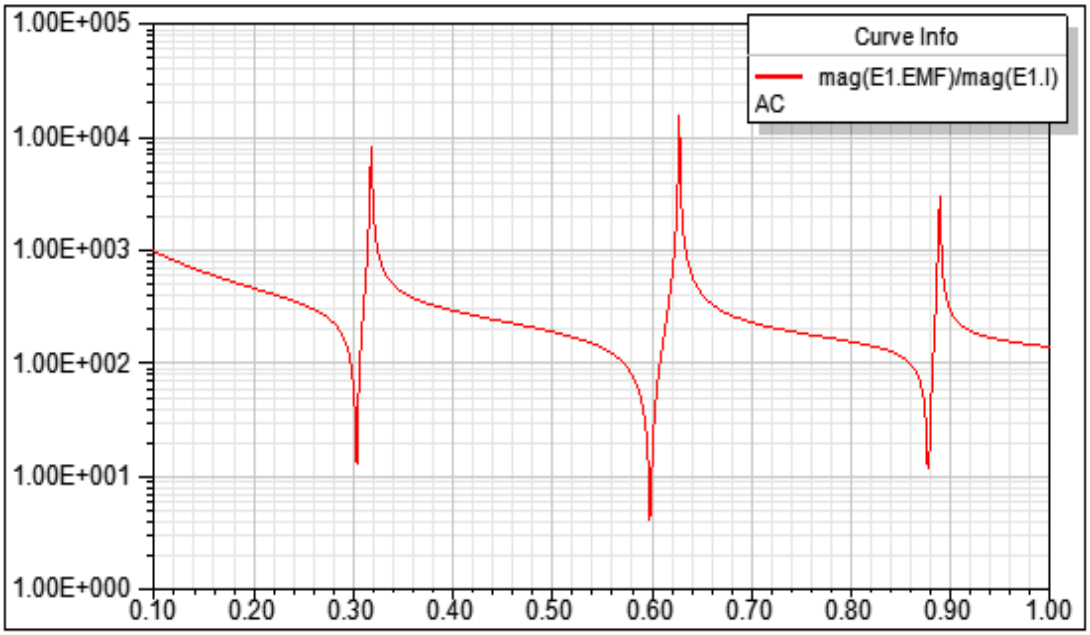

Figure 4. Simulation results-Input Impedance.

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References

PZ27n Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

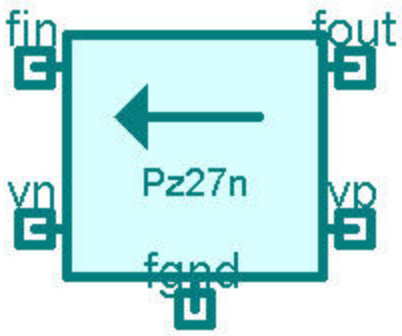

Figure 1. Component symbol

Description

This block represents a PZ27 Piezoelectric layer.

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Netlist Syntax

MODEL PZ27n ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

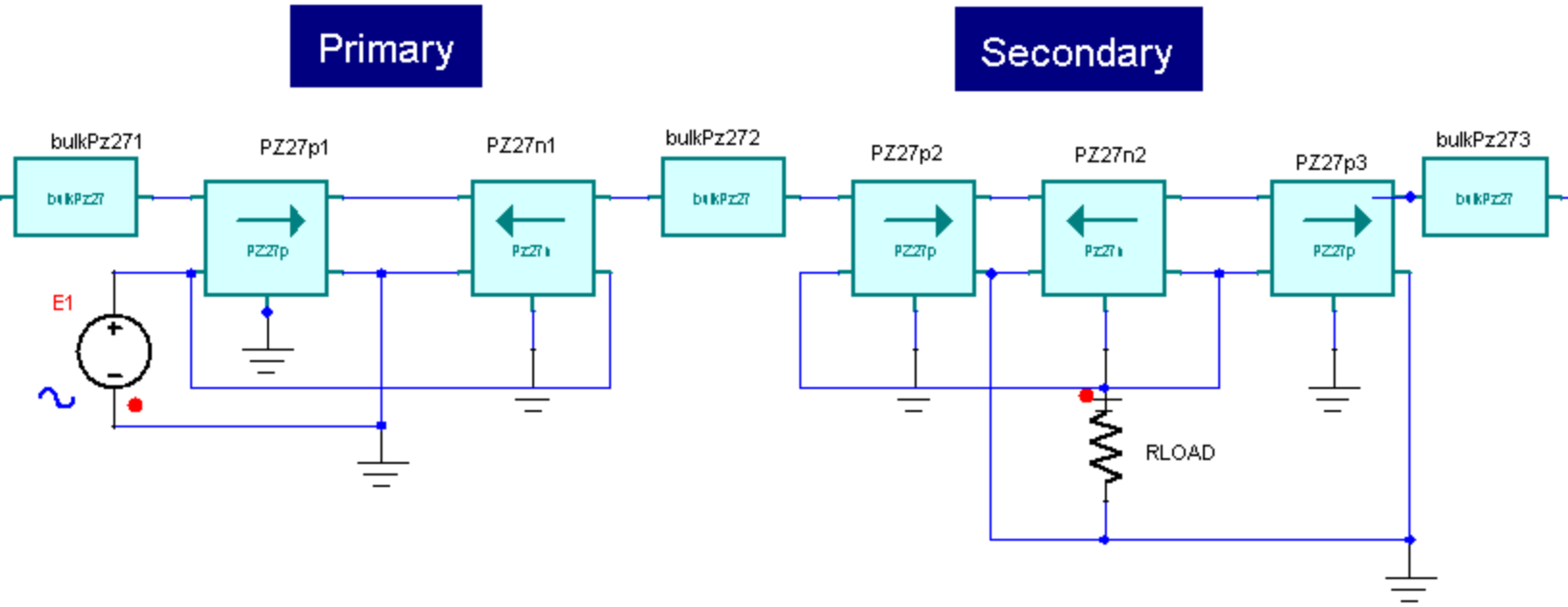

Figure 2. Application example of the BulkPZ27 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ271/BulkPZ273	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ272	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ27p1/PZ27p2/PZ27p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ27n1/PZ27n2	len	0.001 [m]
Resistor RLOAD	R	10000

		[Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

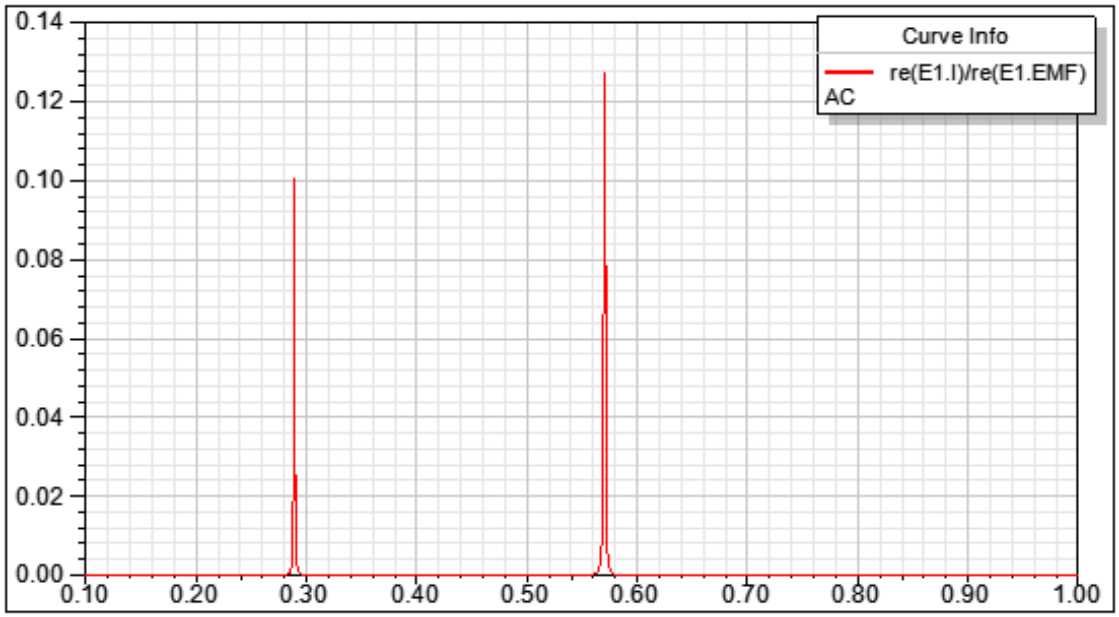

Figure 3. Simulation results-Input Conductance.

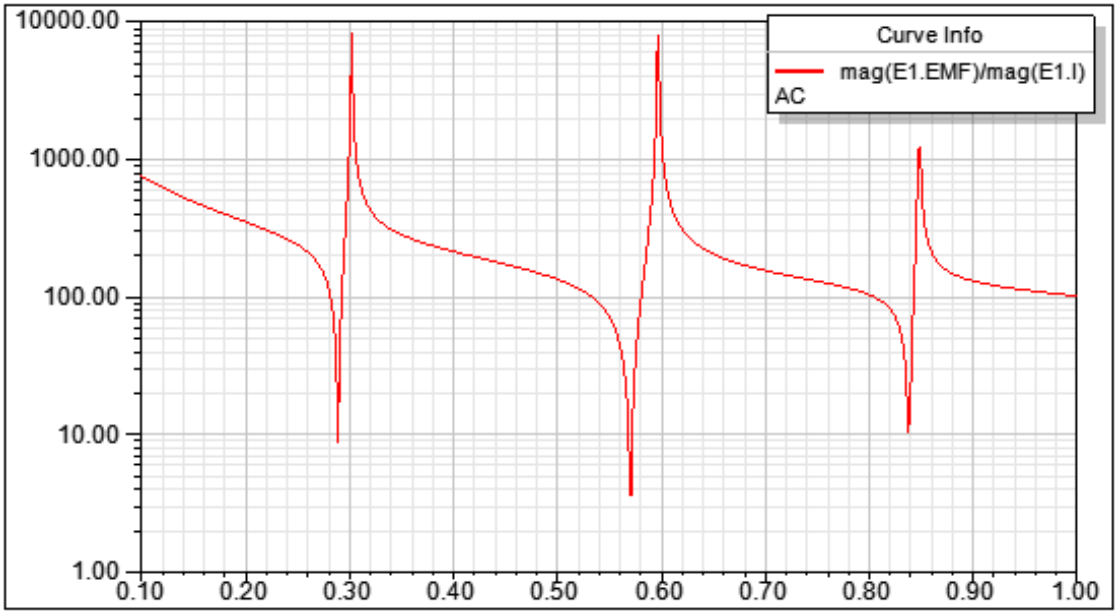

Figure 4. Simulation results-Input Impedance.

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References

PZ27p Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

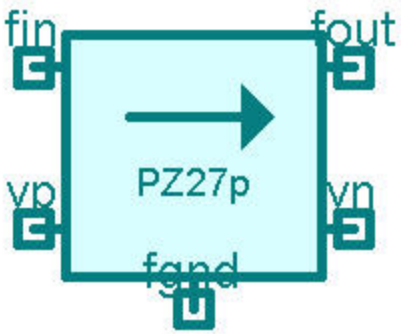

Figure 1. Component symbol

Description

This block represents a PZ27 Piezoelectric layer.

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Netlist Syntax

MODEL PZ27p ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

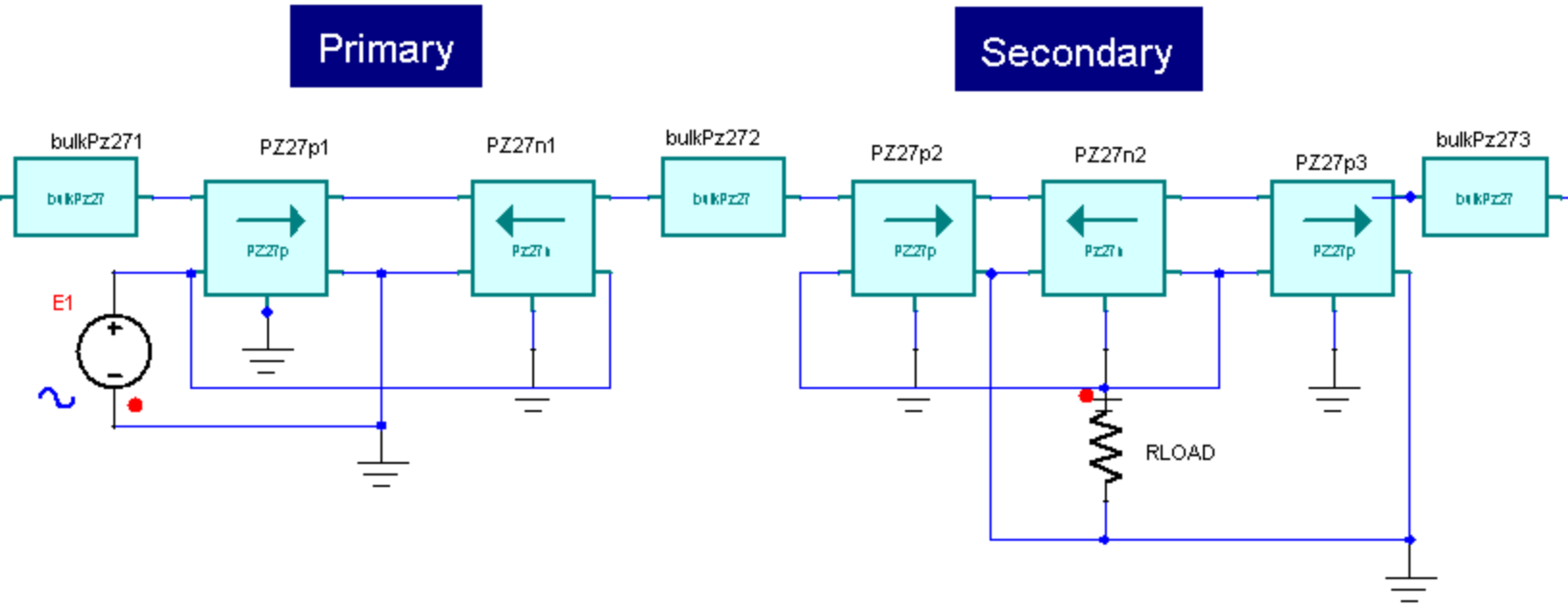

Figure 2. Application example of the BulkPZ27 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ271/BulkPZ273	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ272	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ27p1/PZ27p2/PZ27p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ27n1/PZ27n2	len	0.001 [m]
Resistor RLOAD	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

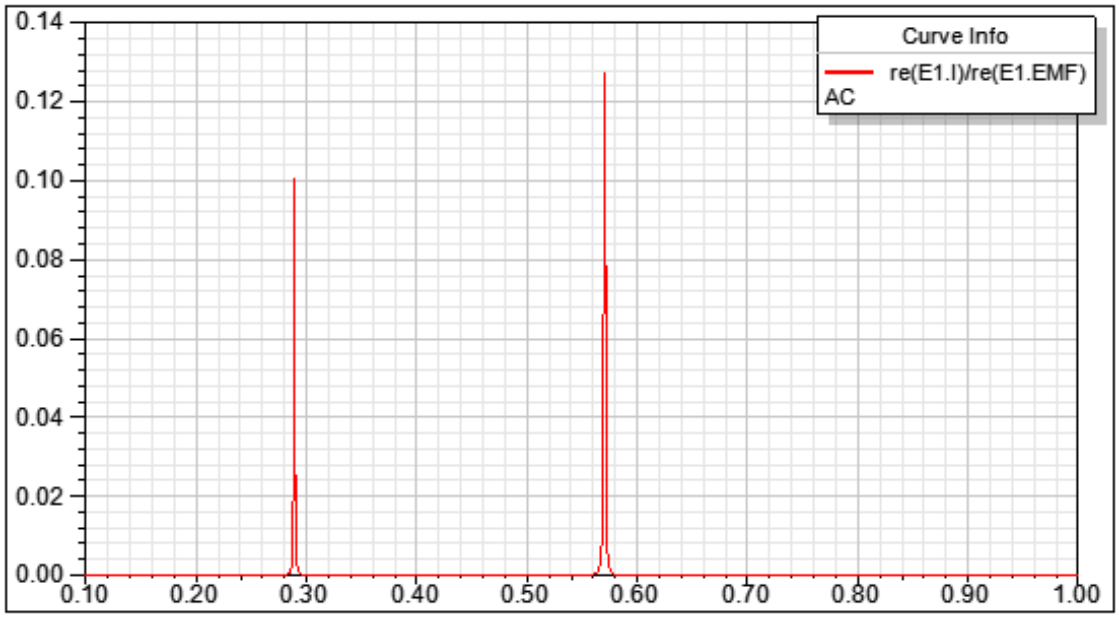

Figure 3. Simulation results-Input Conductance.

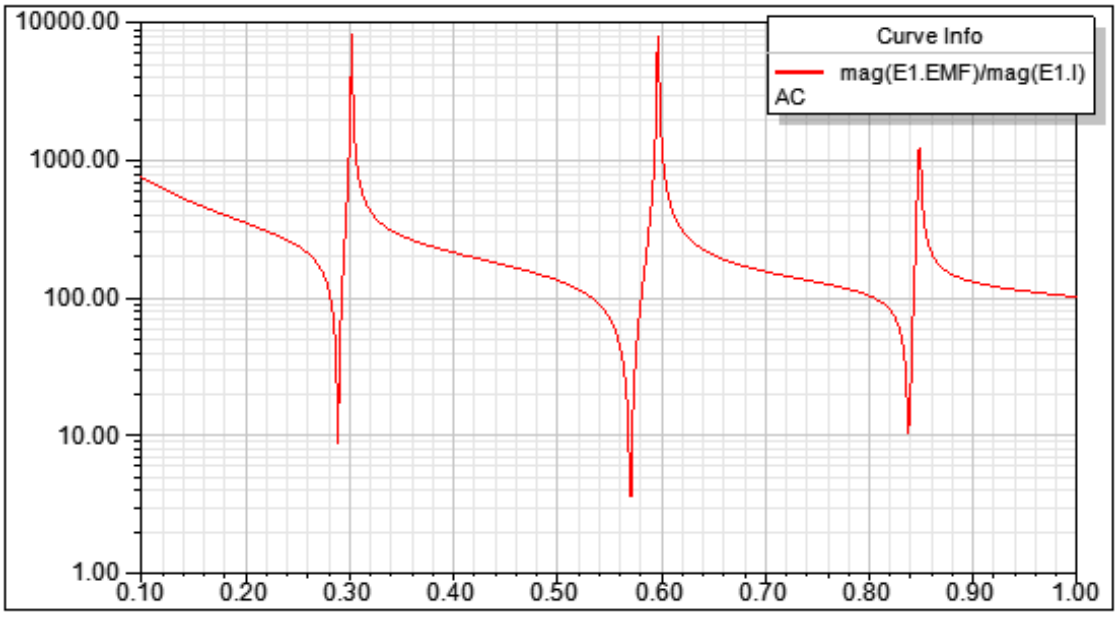

Figure 4. Simulation results-Input Impedance.

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References

PZ34n Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

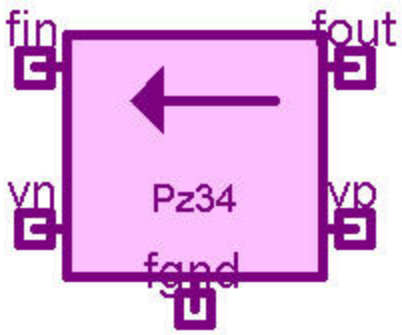

Figure 1. Component symbol

Description

This block represents a PZ34 Piezoelectric layer.

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Netlist Syntax

MODEL PZ34n ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

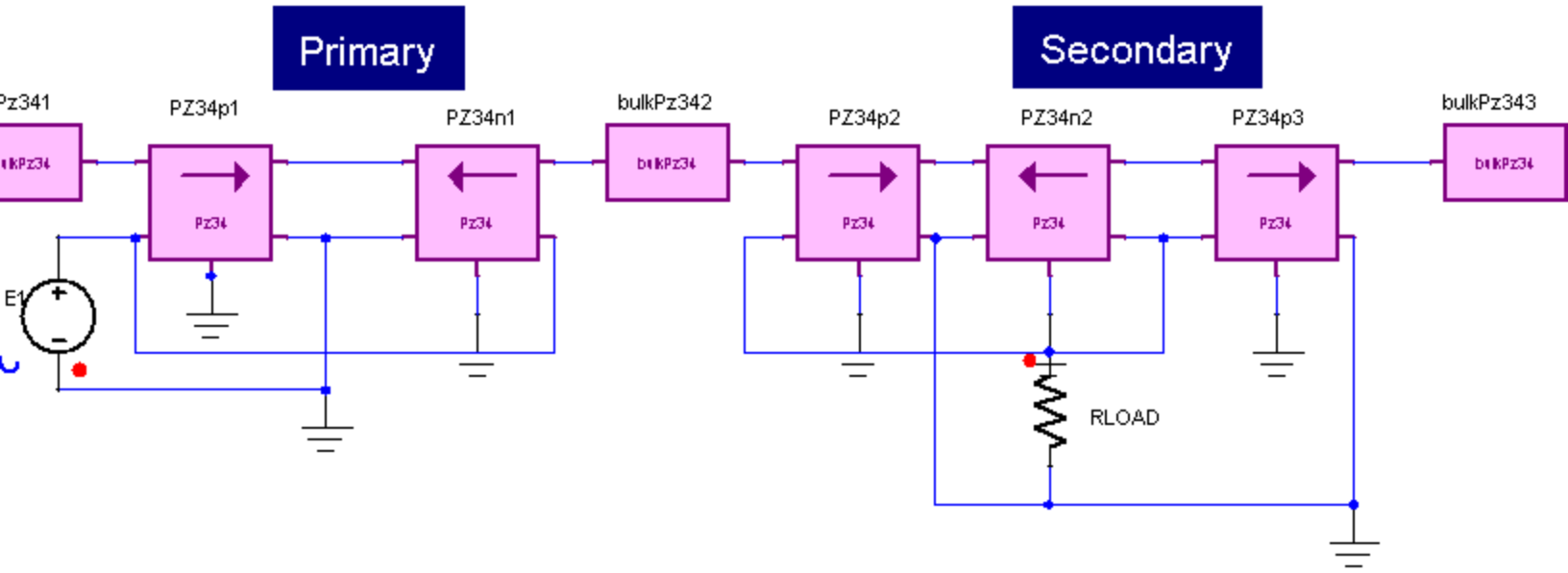

Figure 2. Application example of the BulkPZ34 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ341/BulkPZ343	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ342	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ34p1/PZ34p2/PZ34p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ34n1/PZ34n2	len	0.001 [m]
Resistor RLOAD	R	10000 [Ohm]

Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

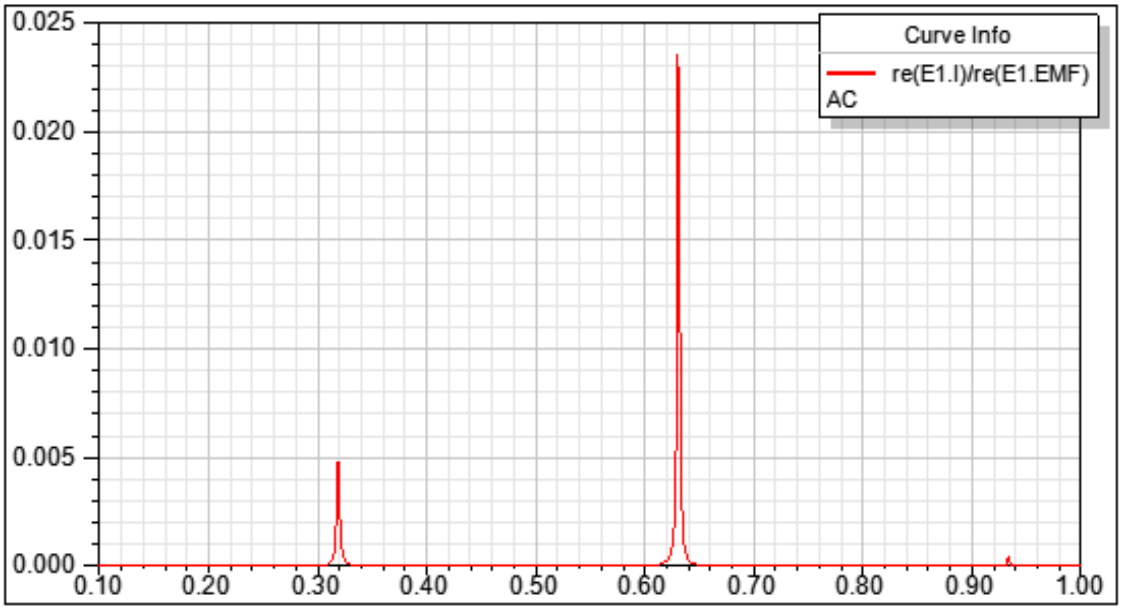

Figure 3. Simulation results-Input Conductance.

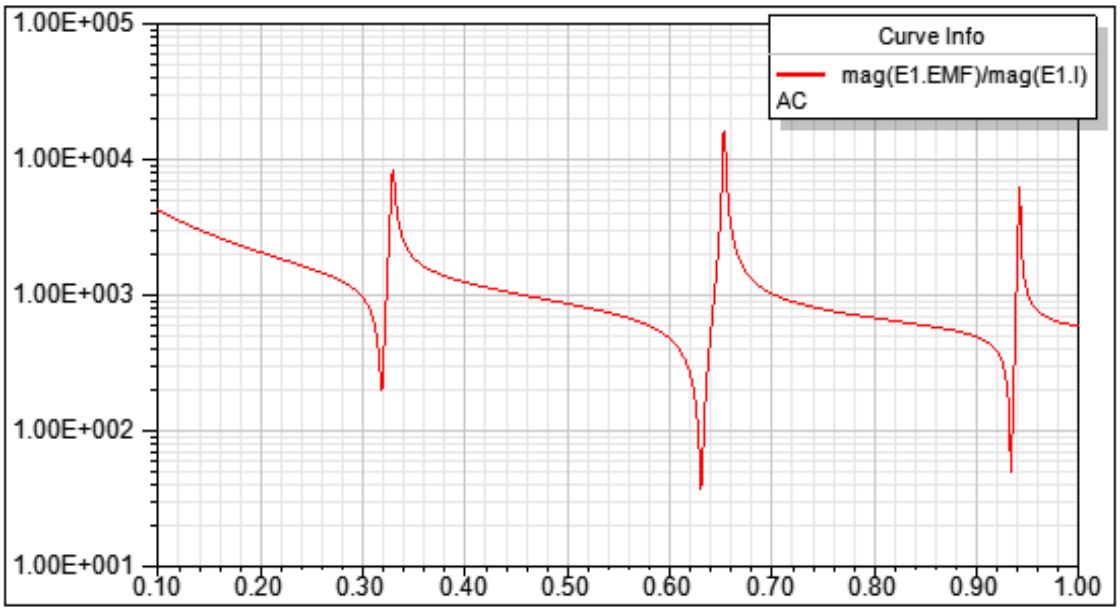

Figure 4. Simulation results-Input Impedance.

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References

PZ34p Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

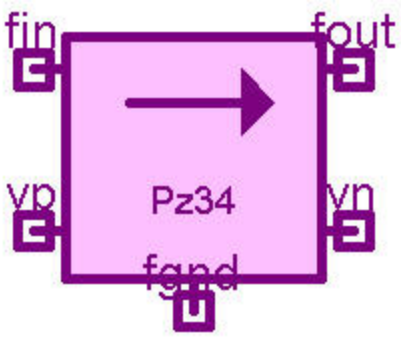

Figure 1. Component symbol

Description

This block represents a PZ34 Piezoelectric layer.

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Netlist Syntax

MODEL PZ34p ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thick-ness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2]

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

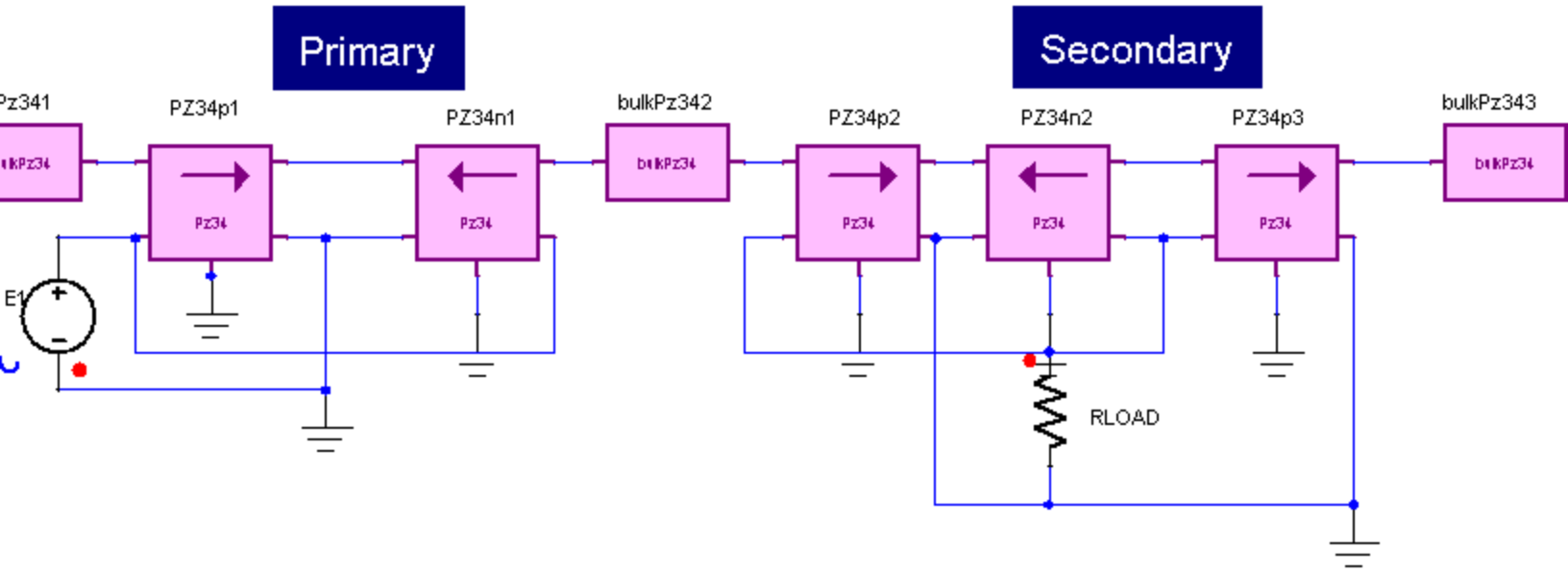

Figure 2. Application example of the BulkPZ34 piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
PZ26 Bulk material BulkPZ341/BulkPZ343	len	0.001 [m]
	Area	0.0001 [m^2]
PZ26 Bulk material BulkPZ342	len	0.0001 [m]
	Area	0.0001 [m^2]
Material Layer vibrating in thickness mode PZ34p1/PZ34p2/PZ34p3	len	0.001 [m]
Material Layer vibrating in thickness mode PZ34n1/PZ34n2	len	0.001 [m]
Resistor RLOAD	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

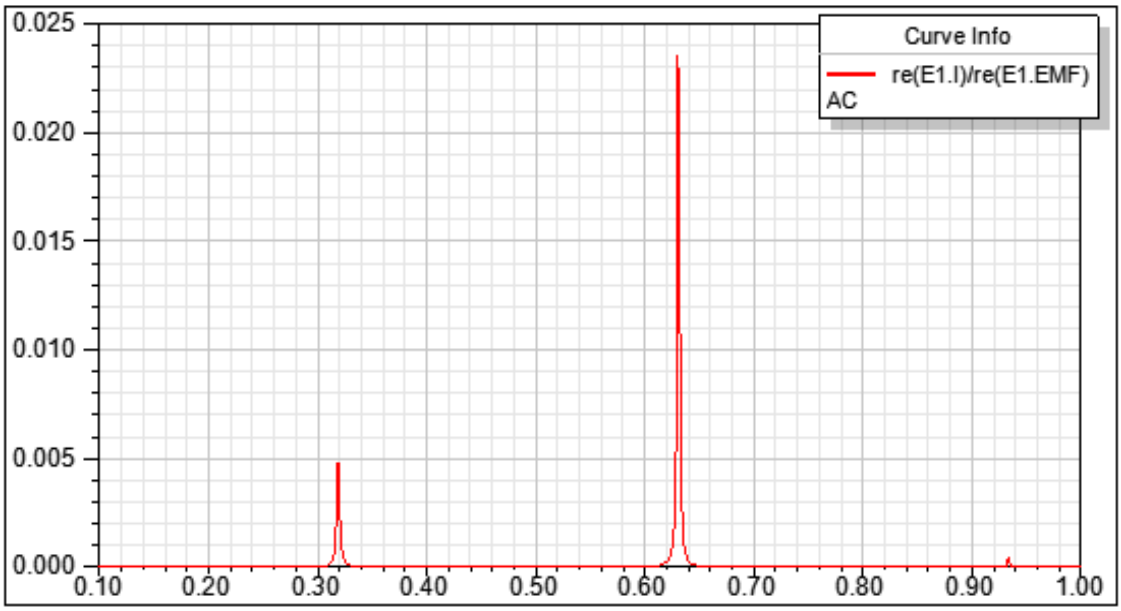

Figure 3. Simulation results-Input Conductance.

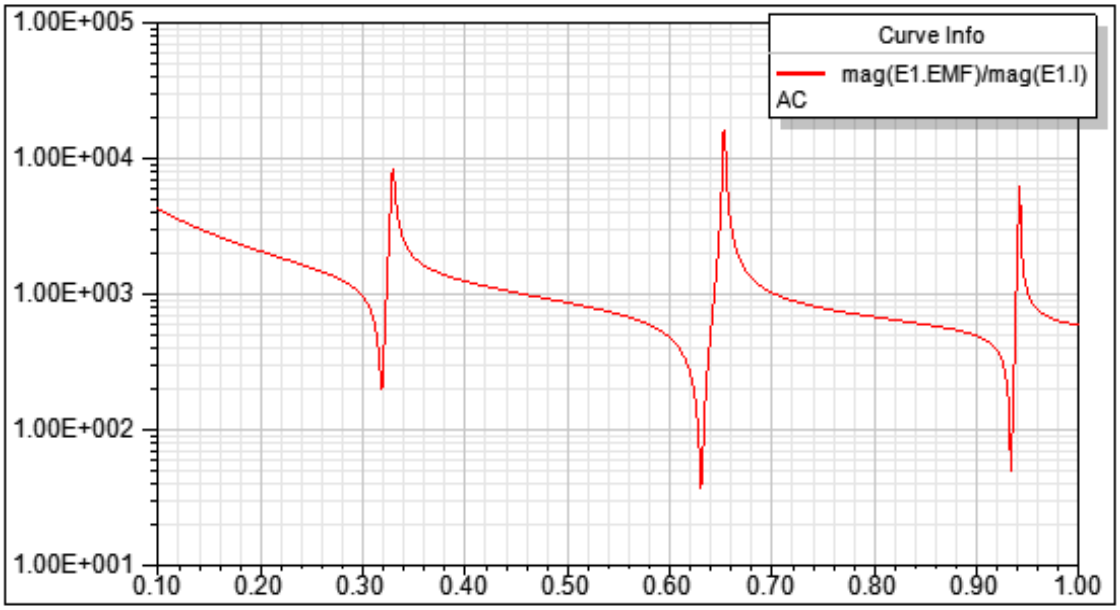

Figure 4. Simulation results-Input Impedance.

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References

PZL Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

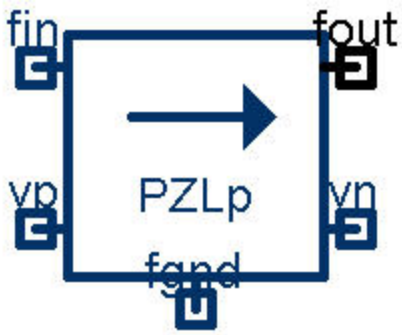

Figure 1. Component symbol

Description

This block represents a generic Piezoelectric layer.

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Netlist Syntax

MODEL PZL ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area, Qm:= @Qm, rho:= @rho, s33_E:= @s33_E, E33_Tr:= @E33_Tr, Qe:= @Qe, kt:= @kt) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thickness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2]
Qm	Mechanical Quality Factor	real	2000
kt	Thickness electromechanical coupling factor	real	0.48
rho	Density	real	7700 [kg/m^3]
s33_E	Mechanical Compliance	real	8.1e-12
E33_Tr	Relative Permittivity(free stress)	real	900
Qe	Electrical Quality Factor	real	333

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

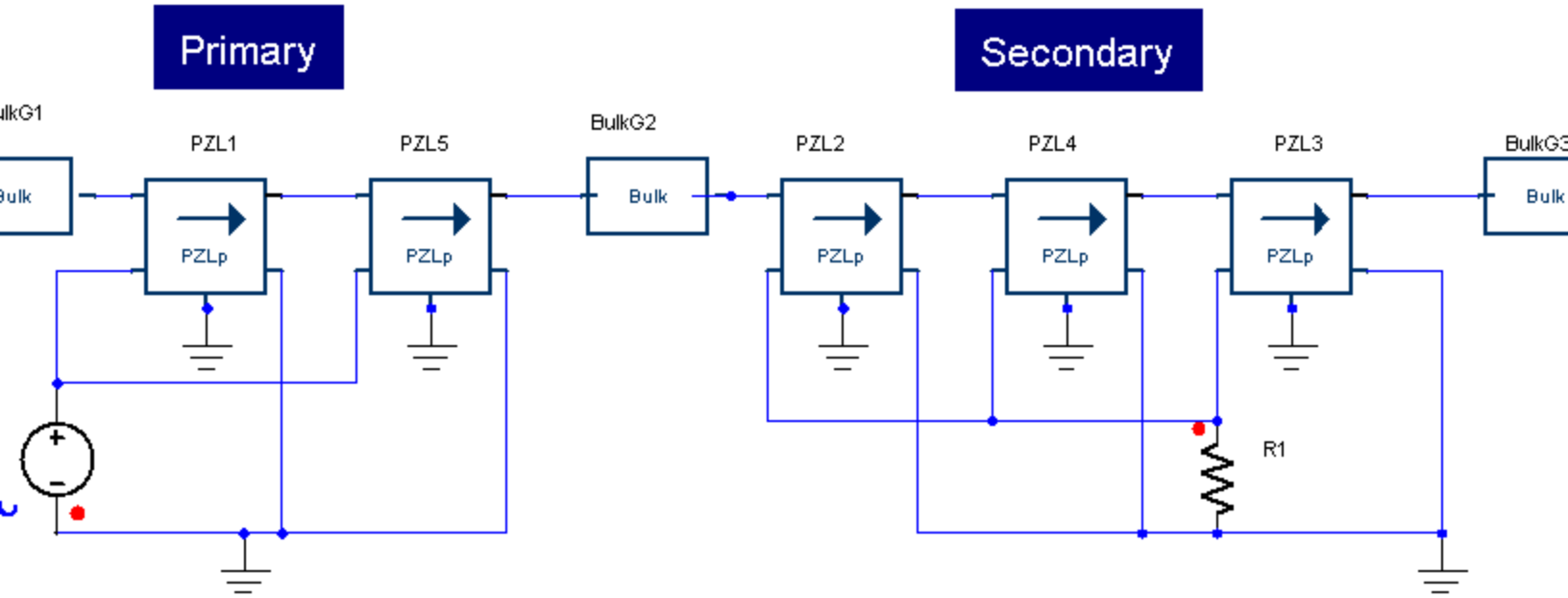

Figure 2. Application example of the BulkG piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
General Bulk material BulkG1/BulkG3	len	0.0001 [m]
General Bulk material BulkG2	len	0.001 [m]
Material Layer vibrating in thickness mode PZL1/PZL2/PZL3/PZL4/PZL5	len	0.001 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

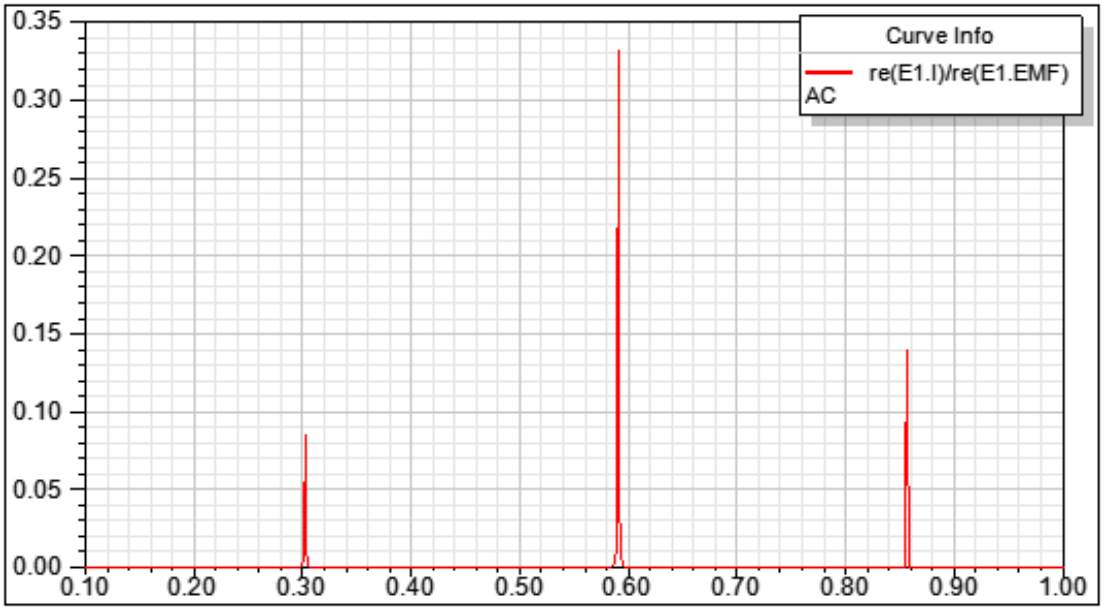

Figure 3. Simulation results-Input Conductance.

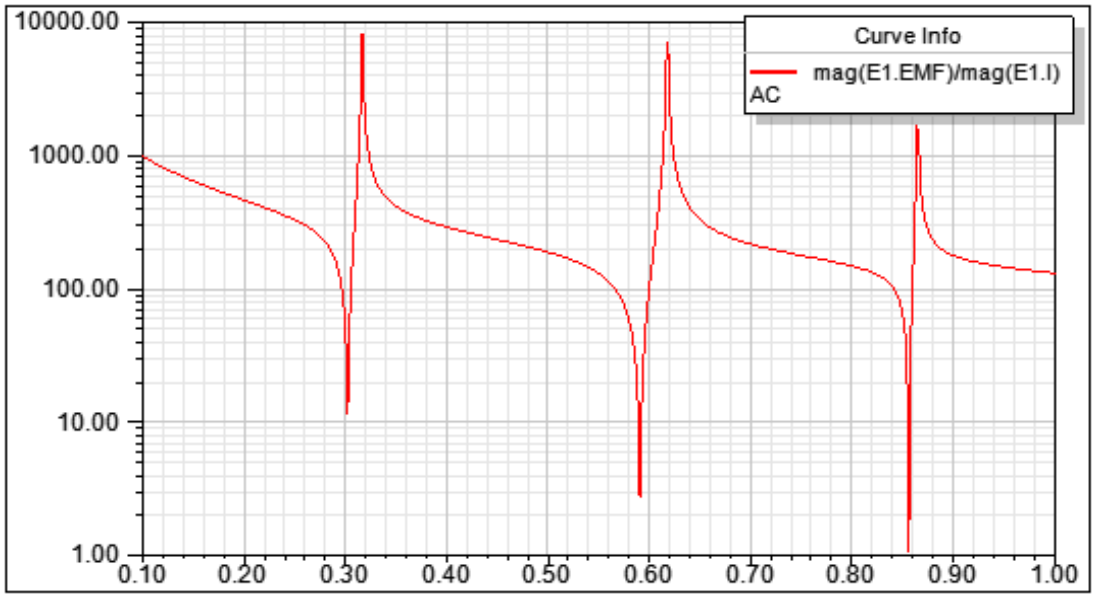

Figure 4. Simulation results-Input Impedance.

Top

References

PZL1 Piezoelectric Layer

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

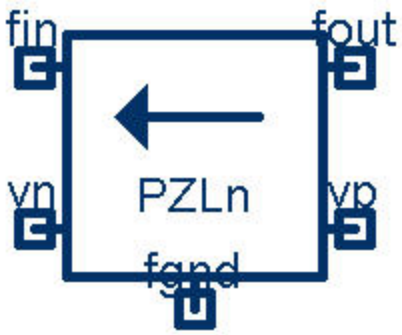

Figure 1. Component symbol

Description

This block represents a generic Piezoelectric layer.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

MODEL PZL1 ?InstanceName(@InstanceName):(@(Refbase)@(ID)) fin:= %0, fout:= %1, vp:= %2, vn:= %3, fgnd:= %4 (len:= @len, Area:= @Area, Qm:= @Qm, rho:= @rho, s33_E:= @s33_E, E33_Tr:= @E33_Tr, Qe:= @Qe, kt:= @kt) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
fin	Mechanical Force Pin	Electrical terminal
fout	Mechanical Force Pin	Electrical terminal
vp	Electrical Pin	Electrical terminal
vn	Electrical Pin	Electrical terminal
fgnd	Mechanical Reference Pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
len	Piezoelectric Layer Thickness	real	0.01 [m]
Area	Piezoelectric Layer Area	real	0.0001 [m^2wire]
Qm	Mechanical Quality Factor	real	2000
kt	Thickness electromechanical coupling factor	real	0.48
rho	Density	real	7700 [kg/m^3]
s33_E	Mechanical Compliance	real	8.1e-12
E33_Tr	Relative Permittivity(free stress)	real	900
Qe	Electrical Quality Factor	real	333

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Example

This example is a Multilayer piezoelectric transformer vibrating in thickness mode.

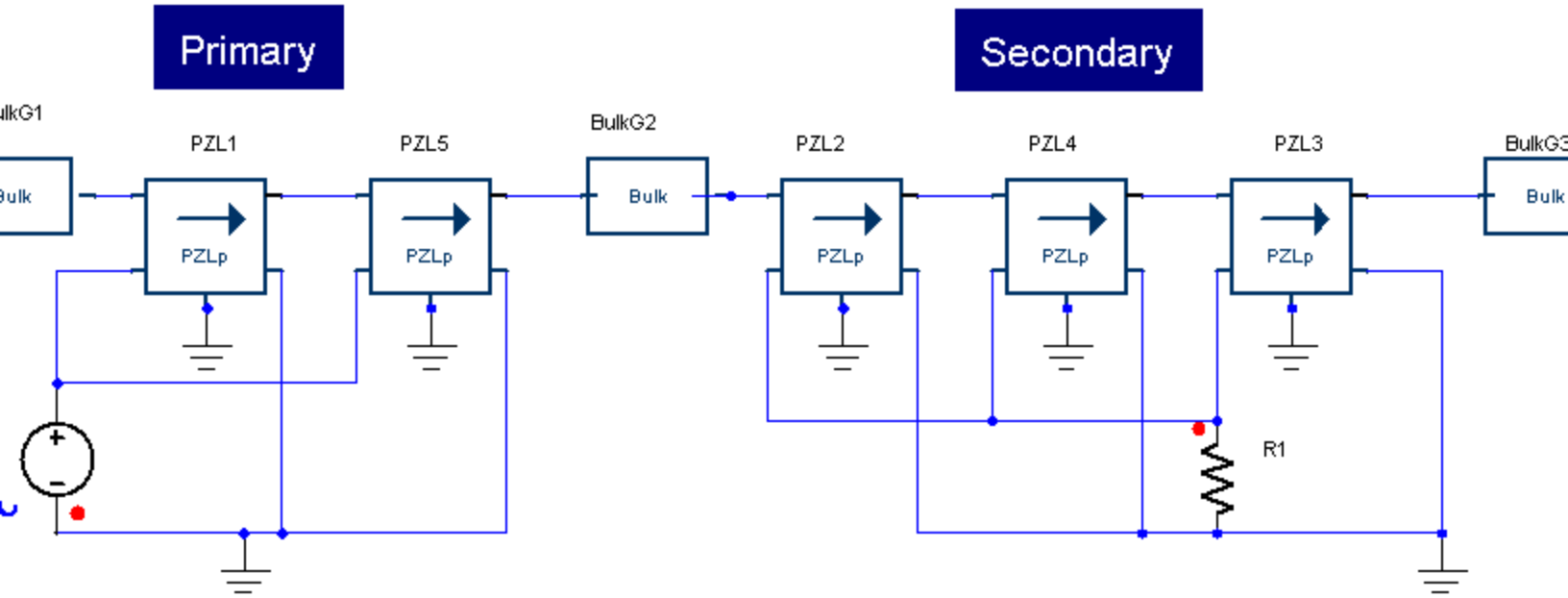

Figure 2. Application example of the BulkG piezoelectric thickness model

Table 3. System Parameters

Component	Parameter	Value [unit]
General Bulk material BulkG1/BulkG3	len	0.0001 [m]
General Bulk material BulkG2	len	0.001 [m]
Material Layer vibrating in thickness mode PZL1/PZL2/PZL3/PZL4/PZL5	len	0.001 [m]
Resistor R1	R	10000 [Ohm]
Voltage Source (Sinusoidal) E1	AMPL	1 [V]
	Freq	50 [Hz]

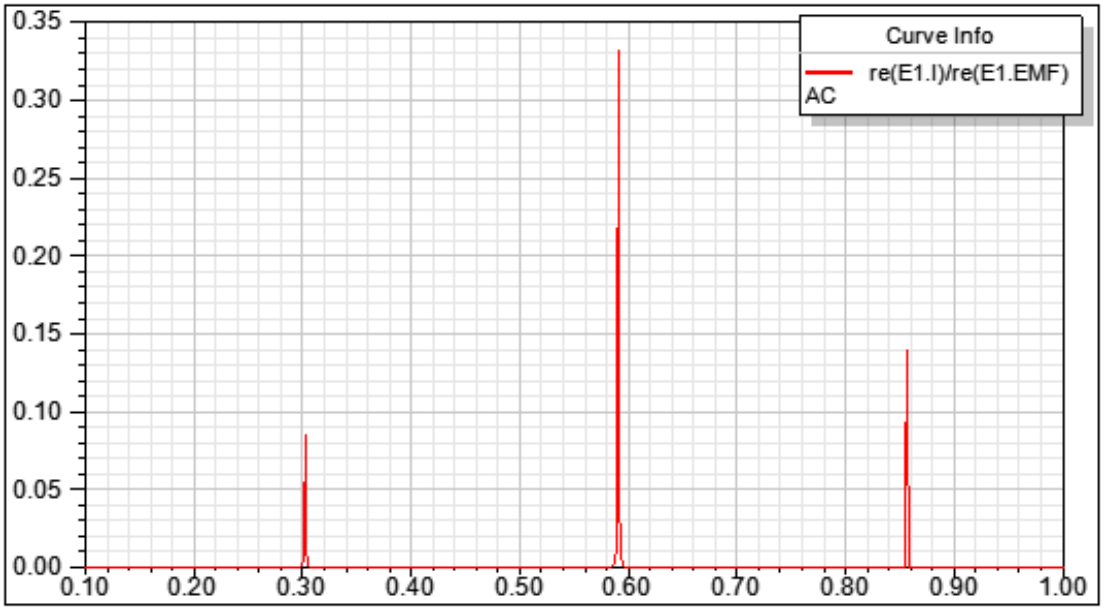

Figure 3. Simulation results-Input Conductance.

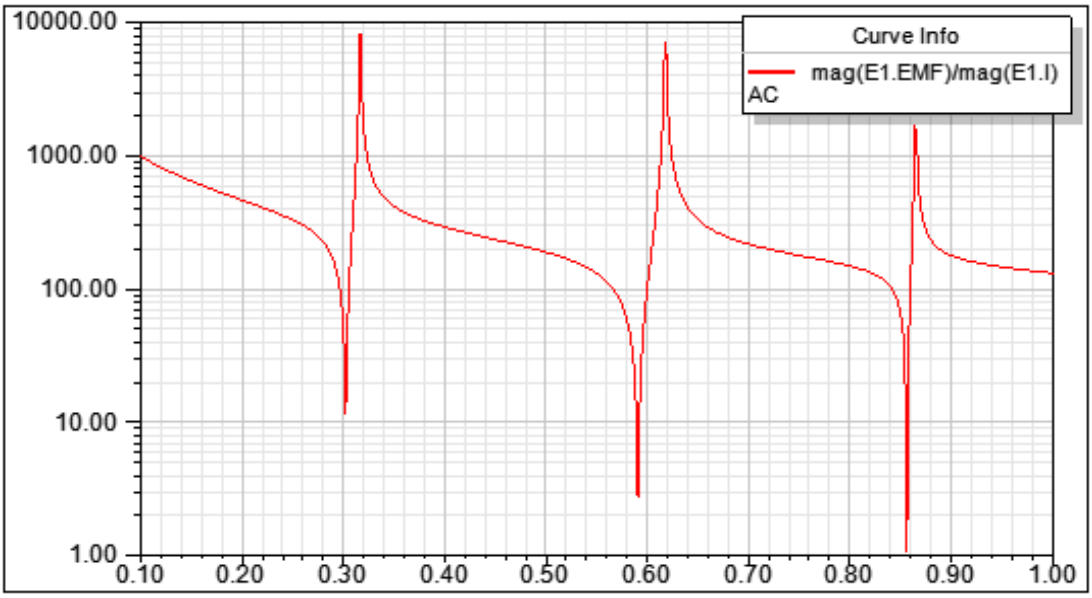

Figure 4. Simulation results-Input Impedance.

Top

References

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal	Boost with Internal Inductor (BOOST_A_II)

	Inductor (BUCK_AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal	Boost with Internal Inductor (BOOST_A_II)

	Inductor (BUCK_AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Averaged Forward Converter With Active Clamp

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

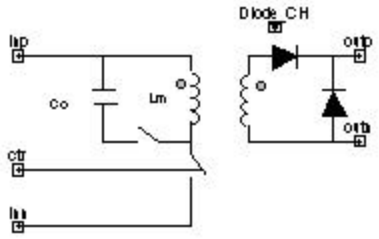

Figure 1. Component symbol

Description

This block represents the averaged model of the Forward with Active Clamp converter.

Top

Assumptions and Limitations

The model is valid for both conduction modes of operation. It accounts for conduction losses in the switches. It automatically detects the change in the mode of operation. The model also includes the clamp capacitor and the magnetizing inductance of the transformer referred to primary.

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Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

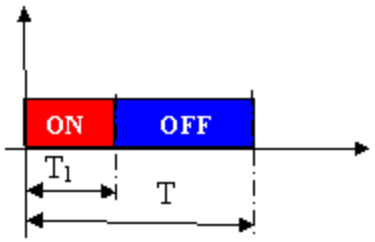

Figure 2. Duty Cycle Calculation

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Netlist Syntax

MODEL FAC_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, ctr:= %3, outn:= %4 (Fs:= @Fs, L:= @L, n1:= @n1, n2:= @n2, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Lm:= @Lm, Lm_IC:= @Lm_IC, Co:= @Co, Co_IC:= @Co_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	positive input pin	Electrical terminal
inn	negative input pin	Electrical terminal
outp	positive output pin	Electrical terminal
outn	negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
L	Output Filter Inductance	real	1e-4 [H]
n1	Primary Number of Turns	real	1
n2	Secondary Number of Turns	real	1
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]
Co	Clamping Capacitance	real	1e-4 [F]
Co_IC	Clamping Capacitor Initial Condition	real	0 [V]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

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Example

This example shows an averaged model of a Forward Converter with active clamp for use in transient, AC or DC analysis.

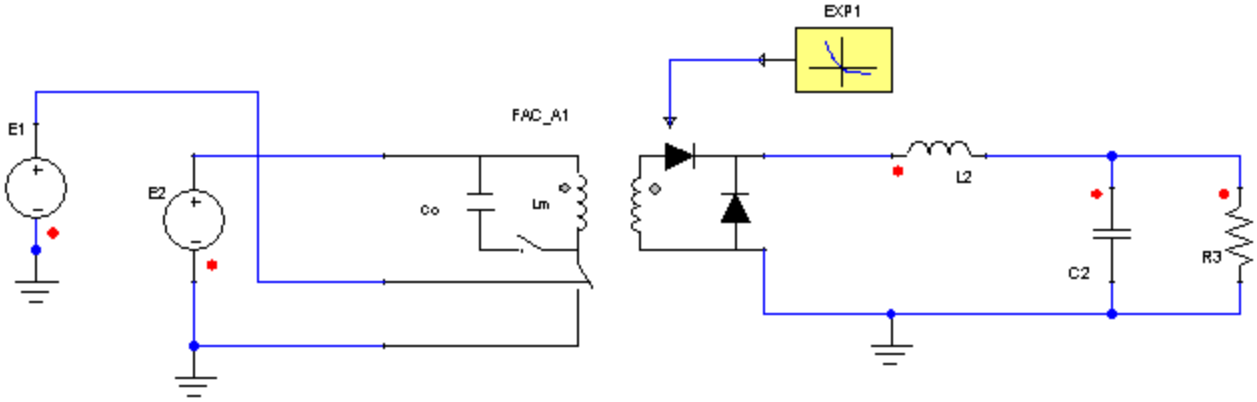

Figure 3. Application example of the Isolated Average Forward Converter with Active Clamp.

Table 3. System Parameters

Component	Parameter	Value [unit]
Isolated Averaged Forward Converter with Active Clamp FAC_A1	L	3e-005 [H]
	n1	1
	n2	1
	Rsa	0.01 [Ohm]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

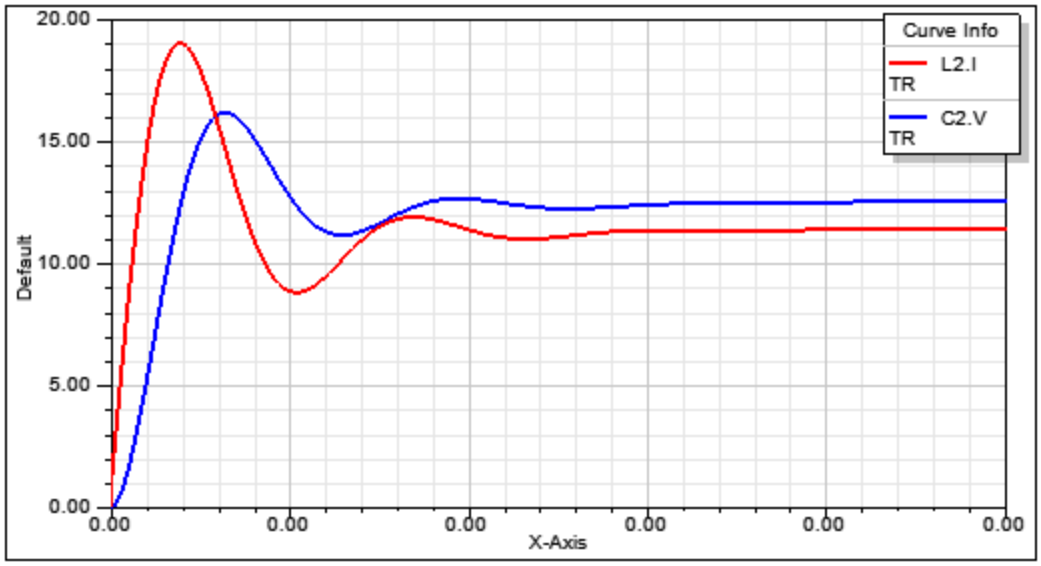

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

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References

Averaged Forward Converter With Active Clamp and Two Outputs

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

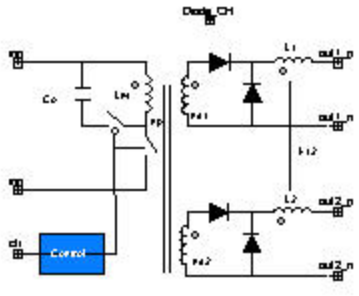

Figure 1. Component symbol

Description

This block represents the averaged model of the Forward with Active Clamp converter with two outputs.

Top

Assumptions and Limitations

The model is valid for both conduction modes of operation. It accounts for conduction losses in the switches. It automatically detects the change in the mode of operation. The model also includes the clamp capacitor, the magnetizing inductance of the transformer referred to primary and the output filter coupled inductors. This model is also valid for non coupled output filter inductors setting the coupling coefficient, k12, to zero.

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Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

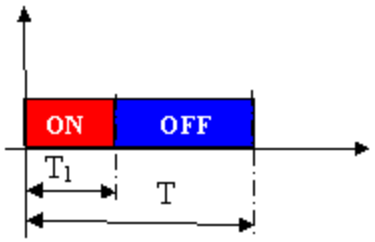

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL FAC2o_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, ctr:= %2, out1_p:= %3, out1_n:= %4, out2_p:= %5, out2_n:= %6 (Fs:= @Fs, np:= @np, ns1:= @ns1, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Lm:= @Lm, Lm_IC:= @Lm_IC, Co:= @Co, Co_IC:= @Co_IC, ns2:= @ns2, L1:= @L1, L2:= @L2, k12:= @k12, L1_IC:= @L1_IC, L2_IC:= @L2_IC) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	positive input pin	Electrical terminal
inn	negative input pin	Electrical terminal
out1_p	positive output 1 pin	Electrical terminal
out1_n	negative output 1 pin	Electrical terminal
out2_p	positive output 2 pin	Electrical terminal
out2_n	negative output 2 pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
L1	Output Filter 1 Inductance	real	1e-5 [H]
L2	Output Filter 2 Inductance	real	1e-5 [H]
L1_IC	Output Filter 1 Inductance Initial Condition	real	0 [A]
L2_IC	Output Filter 2 Inductance Initial Condition	real	0 [A]
k12	Output Filter Inductances Coupling Coefficient	real	0.99999
np	Primary Number of Turns	real	1
ns1	Secondary 1 Number of Turns	real	1
ns2	Secondary 2 Number of Turns	real	1
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]
Co	Clamping Capacitance	real	1e-4 [F]
Co_IC	Clamping Capacitor Initial Condition	real	0 [V]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Lf1_I	Output Filter 1 Current [A]	Output	real
Lf2_I	Output Filter 2 Current [A]	Output	real

Top

Example

This example shows an averaged model of a Forward Converter with active clamp and two outputs for use in transient, AC or DC analysis.

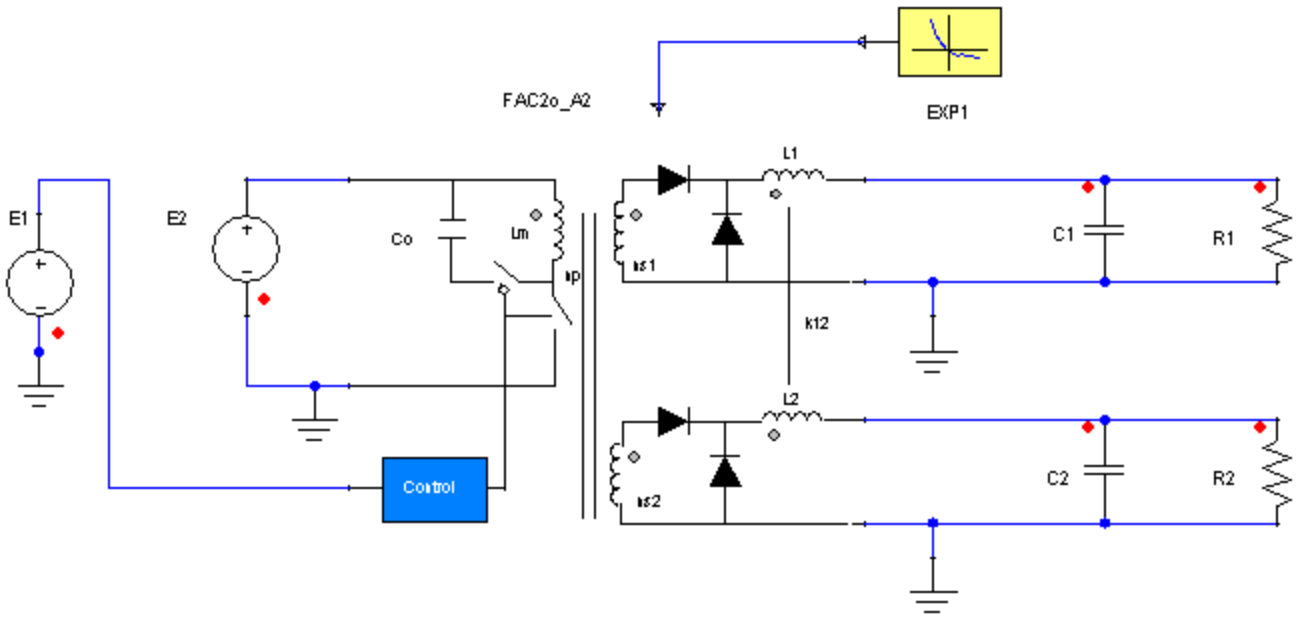

Figure 3. Application example of the Isolated Average Forward Converter with Active Clamp and two outputs.

Table 4. System Parameters

Component	Parameter	Value [unit]
Isolated Averaged Forward Converter with Active Clamp and two outputs FAC2o_A2	np	1
	ns1	1
	ns2	0.5
	Rsa	0.01 [Ohm]
	Diode_CH	EXP1.VAL
	Co_IC	25 [V]

	L1	0.0001 [H]
	L2	2.5e-005 [H]
	k12	0
	L1_IC	0.1
	L2_IC	0.1
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R1	R	1 [Ohm]
Resistor R2	R	0.5 [Ohm]
Capacitor C1	C	5e-005 [F]
Capacitor C2	C	0.0002 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

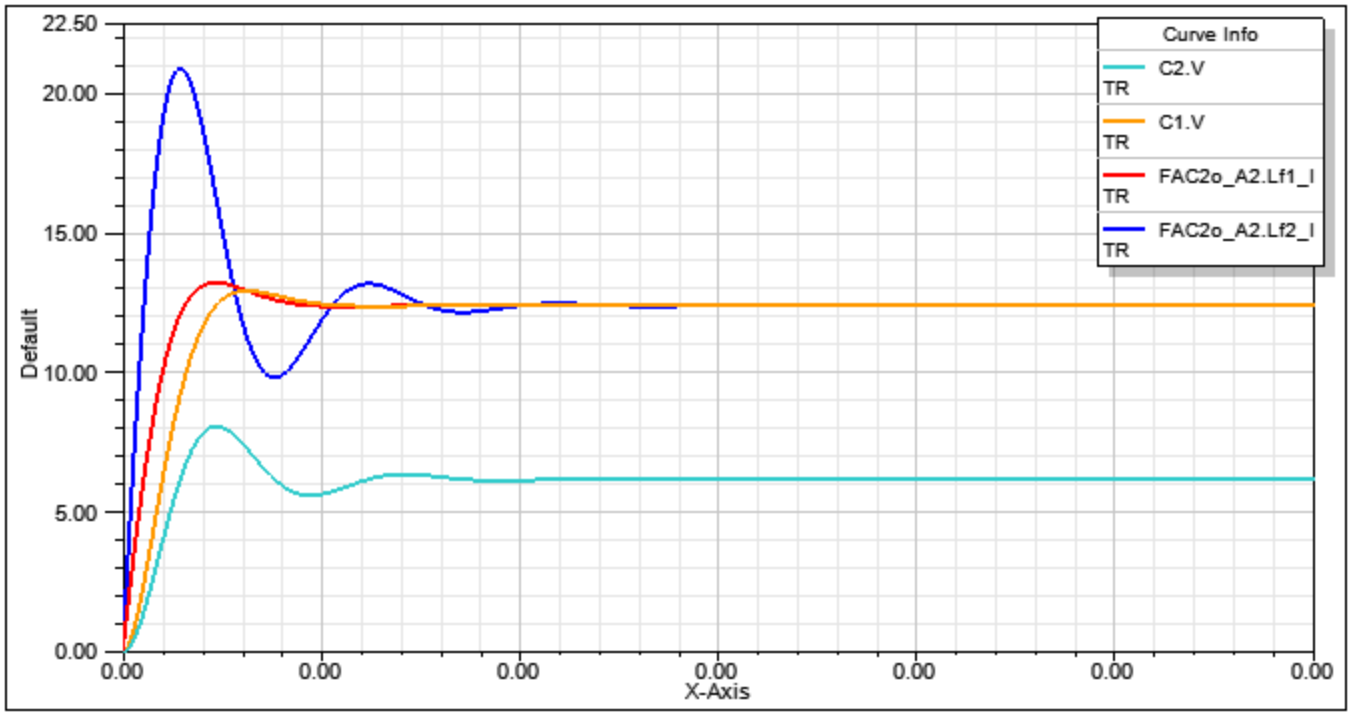

Figure 4. Simulation results-Output currents (FAC2o_A2.Lf1_I, FAC2o_A2.Lf2_I) and Output Voltages (C1.V, C2.V).

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References

Averaged Flyback Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

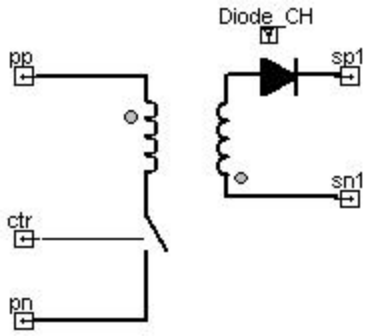

Figure 1. Component symbol

Description

This block represents the averaged model of the Flyback converter.

Top

Assumptions and Limitations

The model is valid for both conduction modes of operation. It accounts for conduction losses in the switches. It automatically detects the change in the mode of operation. The model also includes the magnetizing inductance of the transformer.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

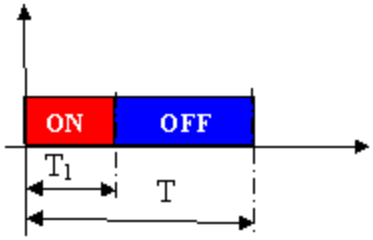

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL FLYBACK_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) pp:= %0, pn:= %1, sp1:= %2, sn1:= %3, ctr:= %4 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, np:= @np, ns1:= @ns1) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
pp	positive input pin	Electrical terminal
pn	negative input pin	Electrical terminal
sp1	positive output pin	Electrical terminal
sn1	negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
np	Primary Number of Turns	real	1

ns1	Secondary Number of Turns	real	1
L	Magnetizing Inductance (Primary)	real	0.0001 [H]
L_IC	Magnetizing Inductance Initial Condition	real	0.001 [A]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Imag	Magnetizing Current [A]	Output	real

Top

Example

This example shows an averaged model of a Flyback Converter for use in transient, AC or DC analysis.

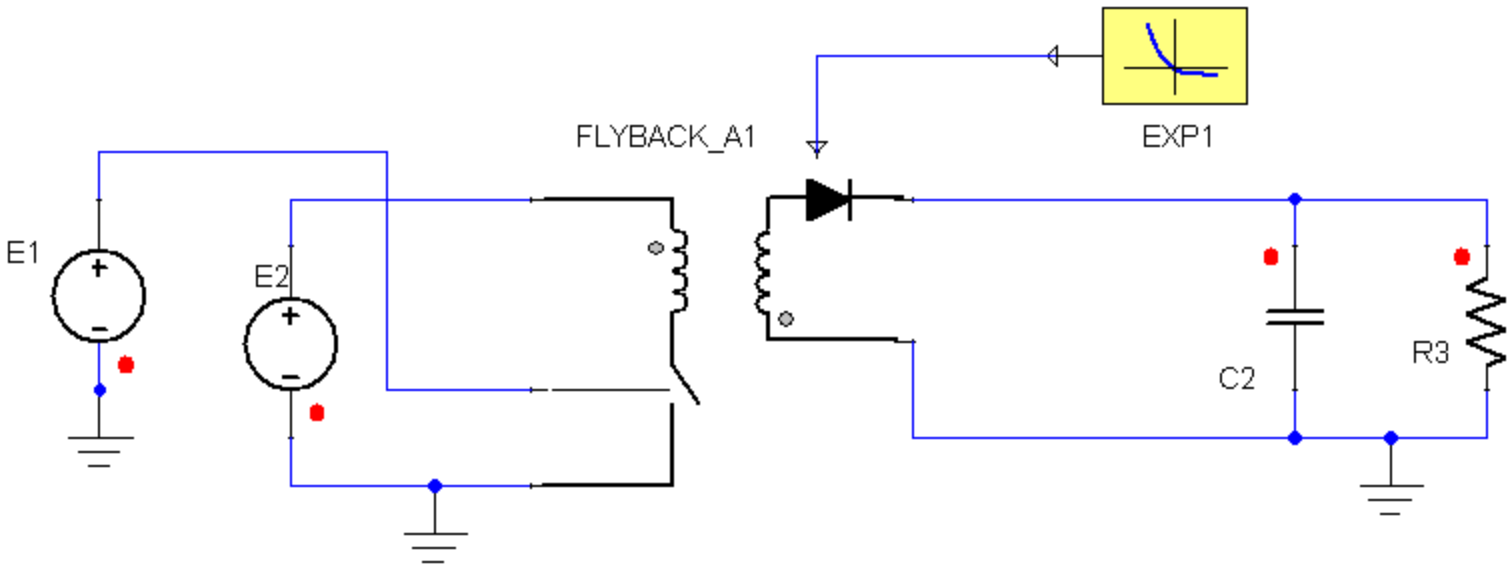

Figure 3. Application example of the Isolated Average Flyback Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]
Isolated Averaged Flyback Converter FLYBACK_A1	L	3e-005 [H]
	L_IC	0.001 [A]
	Diode_CH	EXP1.VAL
	Rsa	0.01 [Ohm]
	np	2
	ns1	1
Exponential Function EXP1	VT	0.025 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	2 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

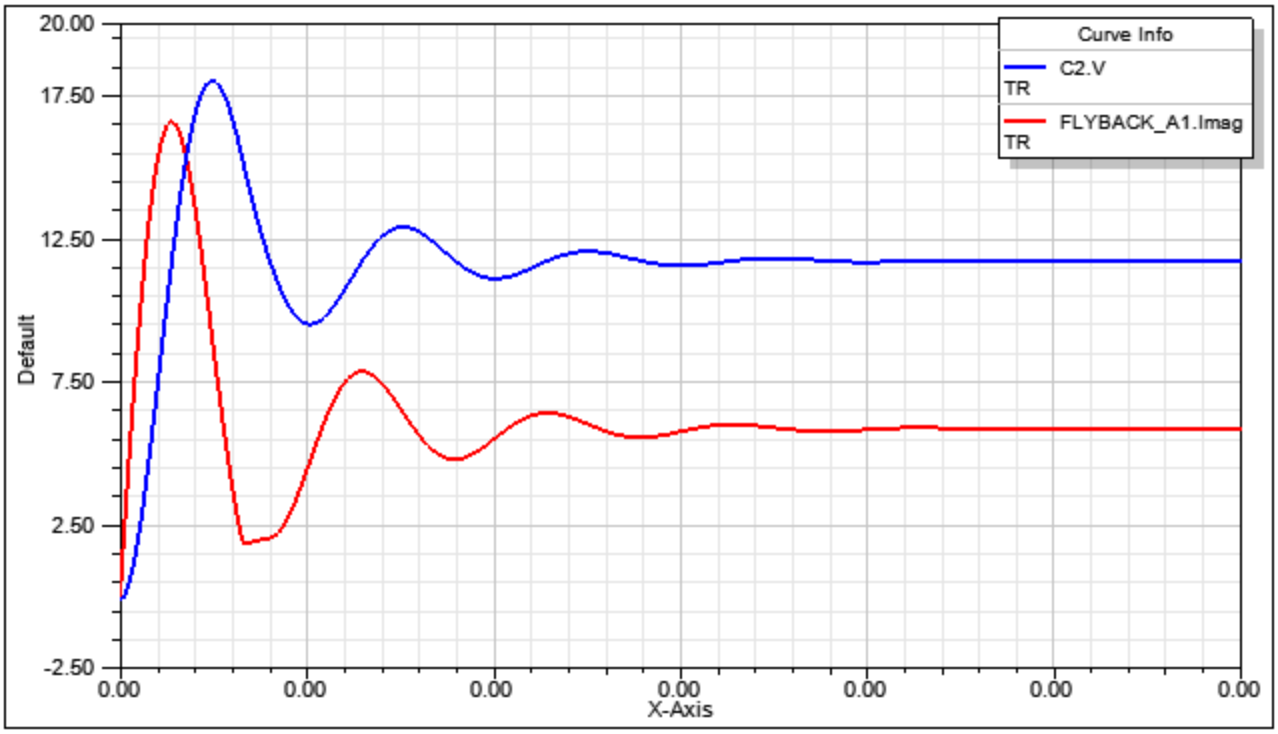

Figure 4. Simulation results-Magnetizing current (FLYBACK_A1.Imag) and Output Voltage (C2.V).

Top

References

Averaged Forward Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

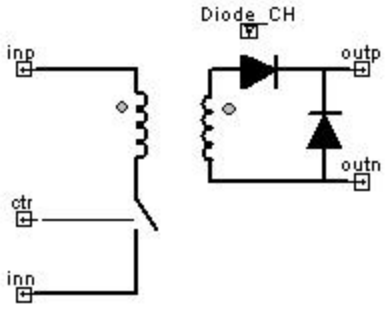

Figure 1. Component symbol

Description

This block represents the averaged model of the Forward converter.

Top

Assumptions and Limitations

The model is valid for both conduction modes of operation. It accounts for conduction losses in the switches. It automatically detects the change in the mode of operation. The model assumes demagnetization of the magnetizing inductance through some mechanism that does not affect its dynamics. It is not necessary to add any external demagnetizing circuit.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

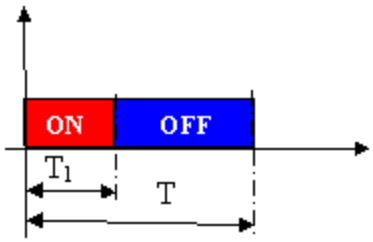

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL FORWARD_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, ctr:= %3, outn:= %4 (Fs:= @Fs, L:= @L, n1:= @n1, n2:= @n2, Diode_CH:= @Diode_CH, Rsa:= @Rsa) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	positive input pin	Electrical terminal
inn	negative input pin	Electrical terminal
outp	positive output pin	Electrical terminal
outn	negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
L	Output Filter Inductance	real	1e-4 [H]
n1	Primary Number of Turns	real	1
n2	Secondary Number of Turns	real	1
Rsa	Active Switch ON Resist-ance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

Top

Example

This example shows an averaged model of a Forward Converter for use in transient, AC or DC analysis.

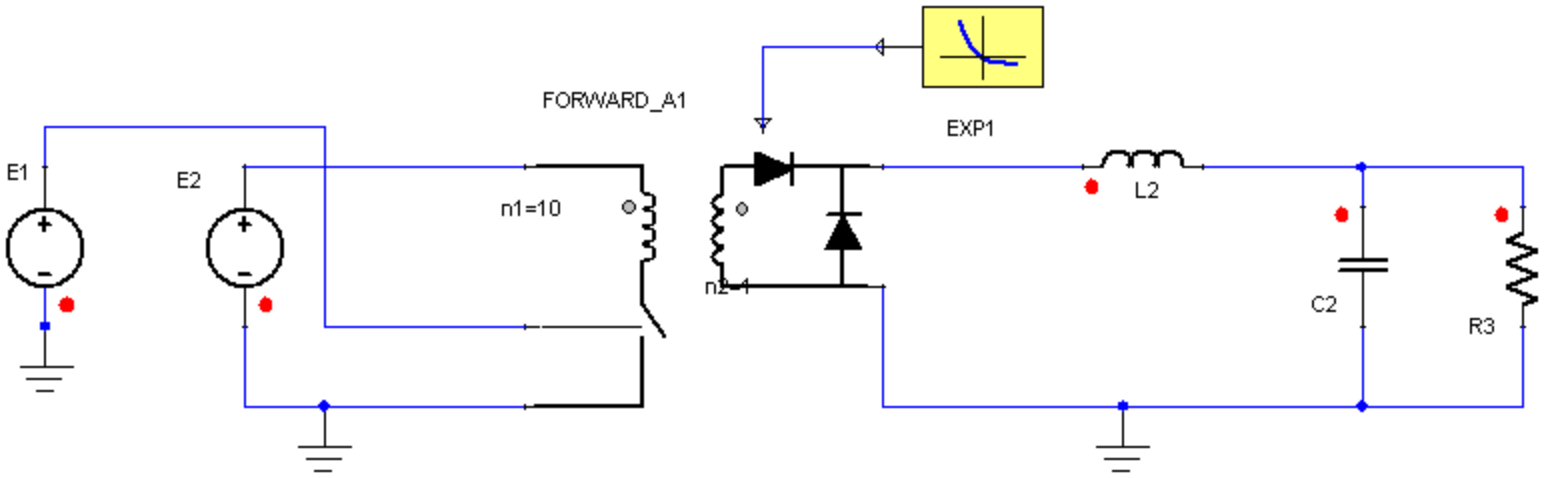

Figure 3. Application example of the Isolated Average Forward Converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Isolated Averaged Forward Converter FORWARD_A1	L	0.0001 [H]
	n1	10
	Diode_CH	EXP1.VAL
	Rsa	0.01 [Ohm]
	n2	1
	F3	100000 [Hz]
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	0.0001 [H]
Voltage Source E1	EMF Value	0.25 [V]
Voltage Source E2	EMF Value	400 [V]

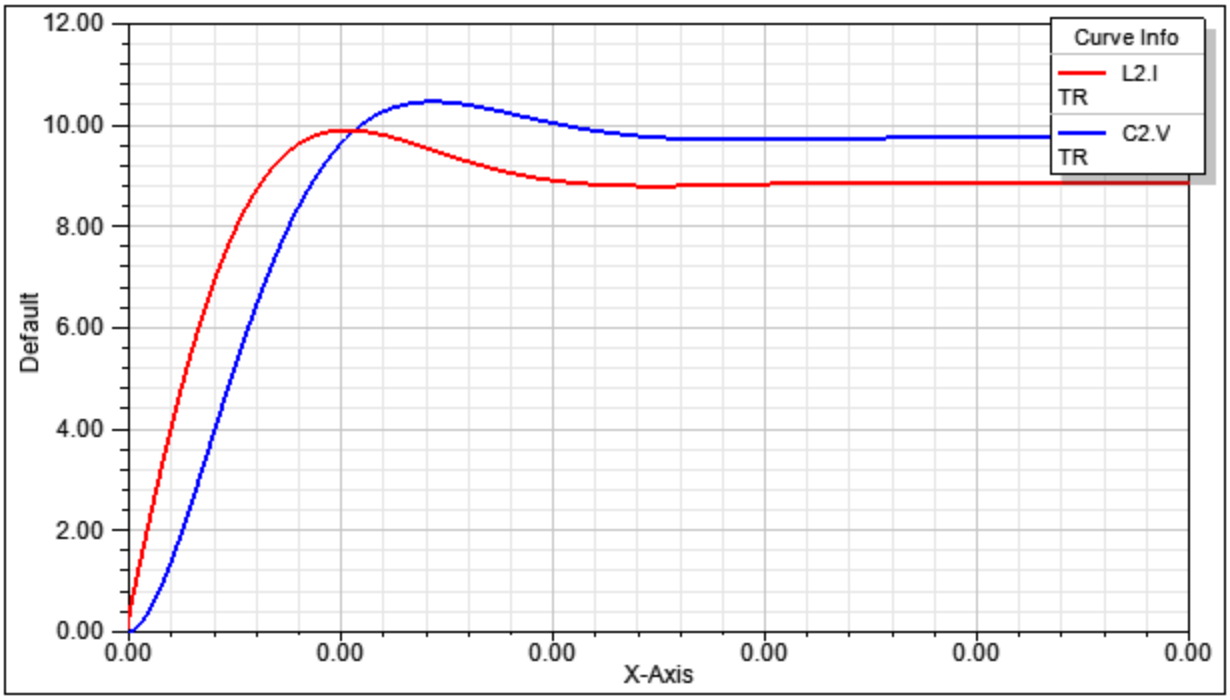

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

Averaged Full-Bridge Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

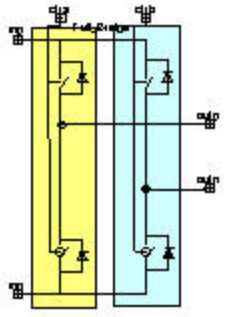

Figure 1. Component symbol

Description

This block represents the averaged model of the Full Bridge converter.

Top

Assumptions and Limitations

The model accounts for conduction losses in the switches, assuming that all of them have the same ON Resistance (Rsa).

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

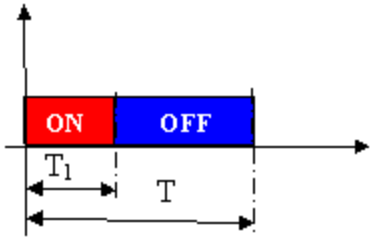

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL Full_Bridge ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, ctra:= %3, outn:= %4, ctrb:= %5 (Rsa:= @Rsa) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	positive input pin	Electrical terminal
inn	negative input pin	Electrical terminal
outp	positive output pin	Electrical terminal
outn	negative output pin	Electrical terminal
ctra	control pin: input for the duty cycle of leg A	Electrical terminal
ctrb	control pin: input for the duty cycle of leg B	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]

Top

Example

This example shows an averaged model of a Full Bridge Converter for use in transient, AC or DC analysis.

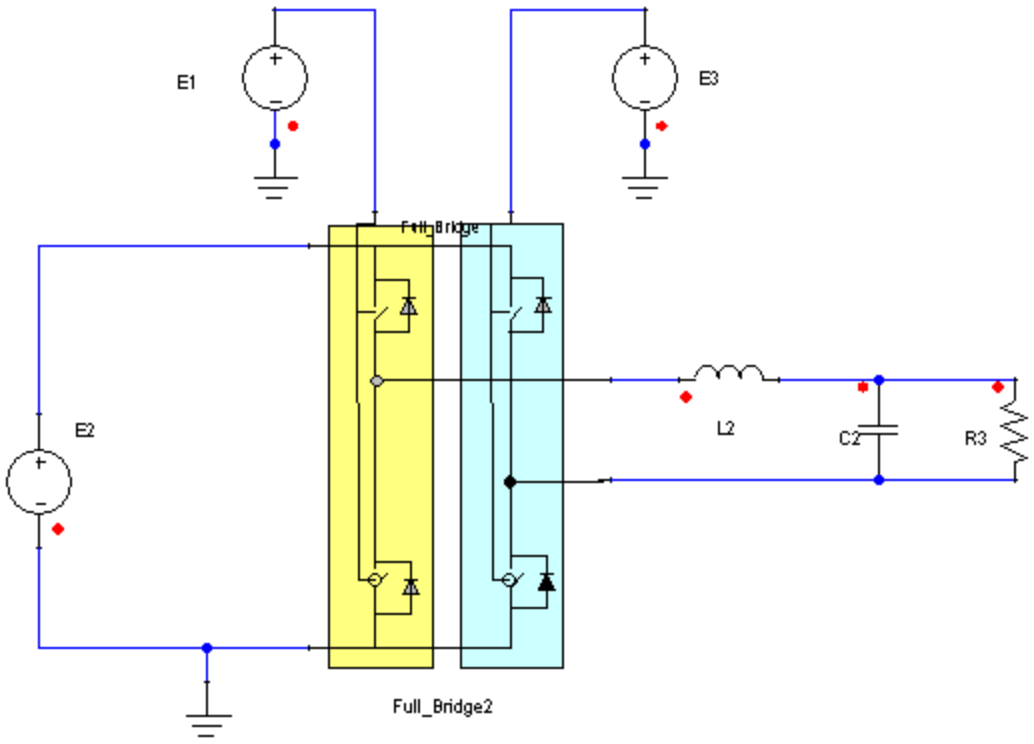

Figure 3. Application example of the Isolated Average Full Bridge Converter.

Table 3. System Parameters

Component	Parameter	Value [unit]

Isolated Averaged Full Bridge Converter Full_Bridge2	Rsa	0.01 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.75 [V]
Voltage Source E3	EMF Value	0.25 [V]
Voltage Source E2	EMF Value	25 [V]

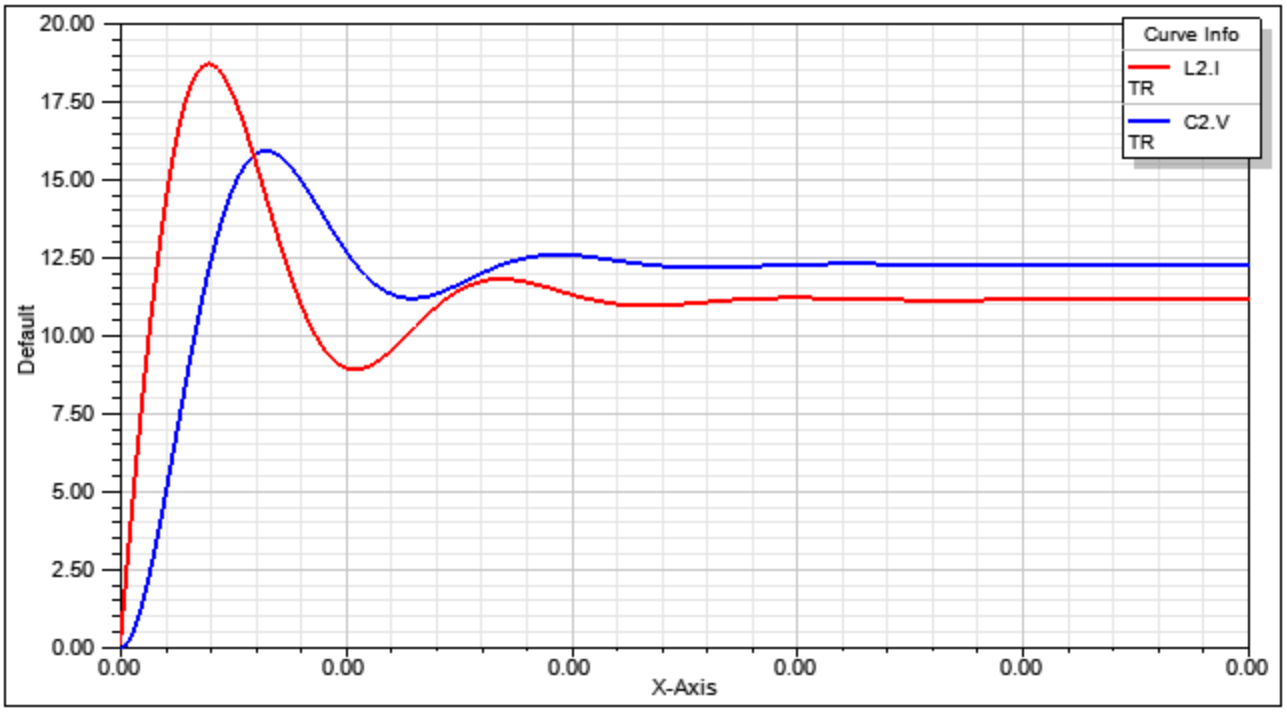

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

Averaged Half-Bridge Converter with Complementary Control

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

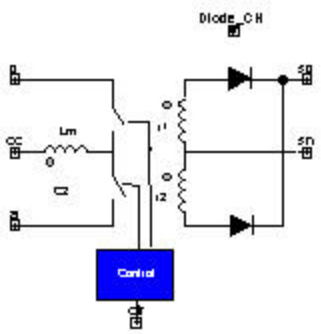

Figure 1. Component symbol

Description

This block represents the averaged model of the Half Bridge with Complementary Control converter.

Top

Assumptions and Limitations

The model is valid for both conduction modes of operation. It accounts for conduction losses in the switches. It automatically detects the change in the mode of operation. It is assumed that the duty cycle is referred to the lower switch. The other switch is operated in a complementary way. The model also includes magnetizing inductance of the transformer referred to primary.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

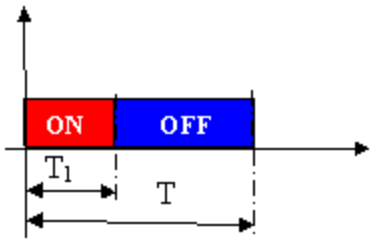

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL HBCC_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) p:= %0, sp:= %1, sn:= %2, a:= %3, cc:= %4, ctr:= %5 (Rsa:= @Rsa, L:= @L, r1:= @r1, r2:= @r2, Rsp:= @Rsp, Diode_CH:= @Diode_CH, Fs:= @Fs, Lm:= @Lm, Lm_IC:= @Lm_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
p	positive input pin	Electrical terminal
cc	middle input pin	Electrical terminal
a	negative input pin	Electrical terminal
sp	positive output pin	Electrical terminal
sn	negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Primary High Side Switch ON Resistance	real	0.01 [Ohm]
L	Output Filter Inductance	real	0.0001 [H]
r1	Transformation Ratio of upper secondary/primary	real	1
r2	Transformation Ratio of lower secondary/primary	real	1
Rsp	Primary Low Side Switch ON Resistance	real	0.01 [Ohm]
Diode_ CH	Diode Characteristic	real	
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]

Top

Example

This example shows an averaged model of a Half Bridge Converter with Complementary Control for use in transient, AC or DC analysis.

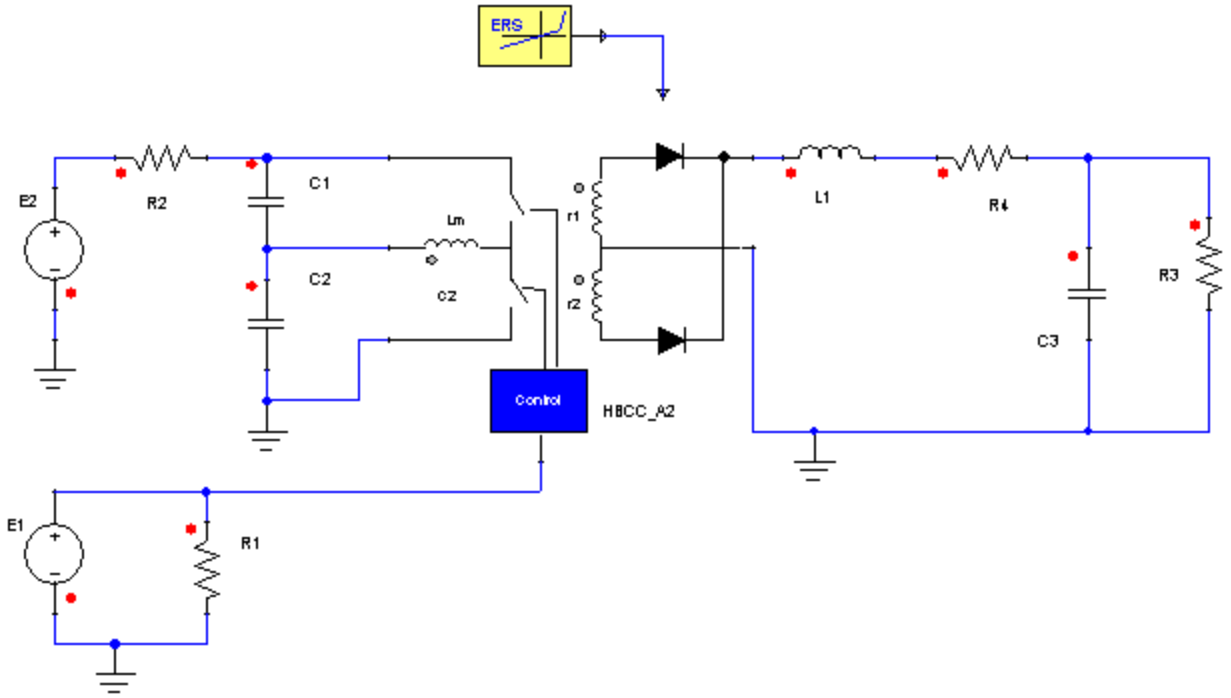

Figure 3. Application example of the Isolated Average Half Bridge Converter with Complementary Control.

Table 3. System Parameters

Component	Parameter	Value [unit]
Isolated Averaged Half Bridge Converter with Complementary Control HBCC_A2	Rsa	0.01 [Ohm]
	r1	0.3
	r2	0.3
	Diode_CH	EQUL1.VAL
Equivalent Line EQUL1	VF	0.6 [V]
	RB	0.001 [Ohm]
	RR	100000 [Ohm]
Resistor R1	R	1000 [Ohm]
Resistor R2	R	0.1 [Ohm]
Resistor R3	R	1 [Ohm]
Resistor R4	R	0.01 [Ohm]
Capacitor C1	C	3e-005 [F]
Capacitor C2	C	3e-005 [F]
Capacitor C3	C	0.0001 [F]
Inductor L1	L	3e-005 [H]
Voltage Source E1	EMF Value	0.45 [V]
Voltage Source E2	EMF Value	25 [V]

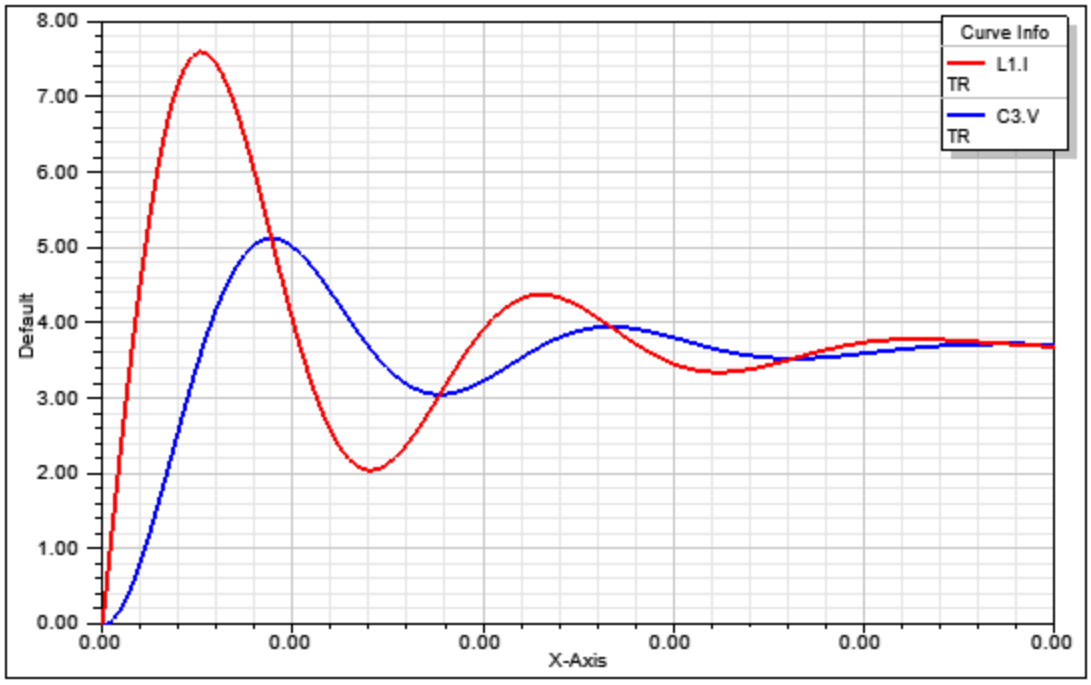

Figure 4. Simulation results-Output current (L1.I) and Output Voltage (C3.V).

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References

Averaged Synchronous Half-Bridge Converter with Complementary Control

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

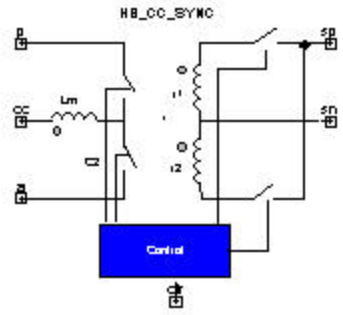

Figure 1. Component symbol

Description

This block represents the averaged model of the Half Bridge with Complementary Control converter with synchronous rectification.

Top

Assumptions and Limitations

The model accounts for conduction losses in the switches. It is assumed that the duty cycle is referred to the lower switch. The other switch is operated in a complementary way. The model also includes magnetizing inductance of the transformer referred to primary.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

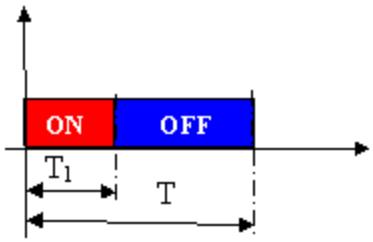

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL HBCCS_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) p:= %0, sp:= %1, sn:= %2, a:= %3, cc:= %4, ctr:= %5 (Rsa:= @Rsa, Lm:= @Lm, r1:= @r1, r2:= @r2, Rsp:= @Rsp, Rsync:= @Rsync, Lm_IC:= @Lm_IC) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
p	positive input pin	Electrical terminal
cc	middle input pin	Electrical terminal
a	negative input pin	Electrical terminal
sp	positive output pin	Electrical terminal
sn	negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Rsa	Primary High Side Switch ON Resistance	real	0.01 [Ohm]
Rsync	Synchronous Rectification Switches ON Resistance	real	0.01 [Ohm]
r1	Turns Ratio of Upper secondary/primary	real	1
r2	Turns Ratio of Lower secondary/primary	real	1
Rsp	Primary Low Side Switch ON Resistance	real	0.01 [Ohm]
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]

Top

Example

This example shows an averaged model of a Half Bridge Converter with Complementary Control and Synchronous Rectification for use in transient, AC or DC analysis.

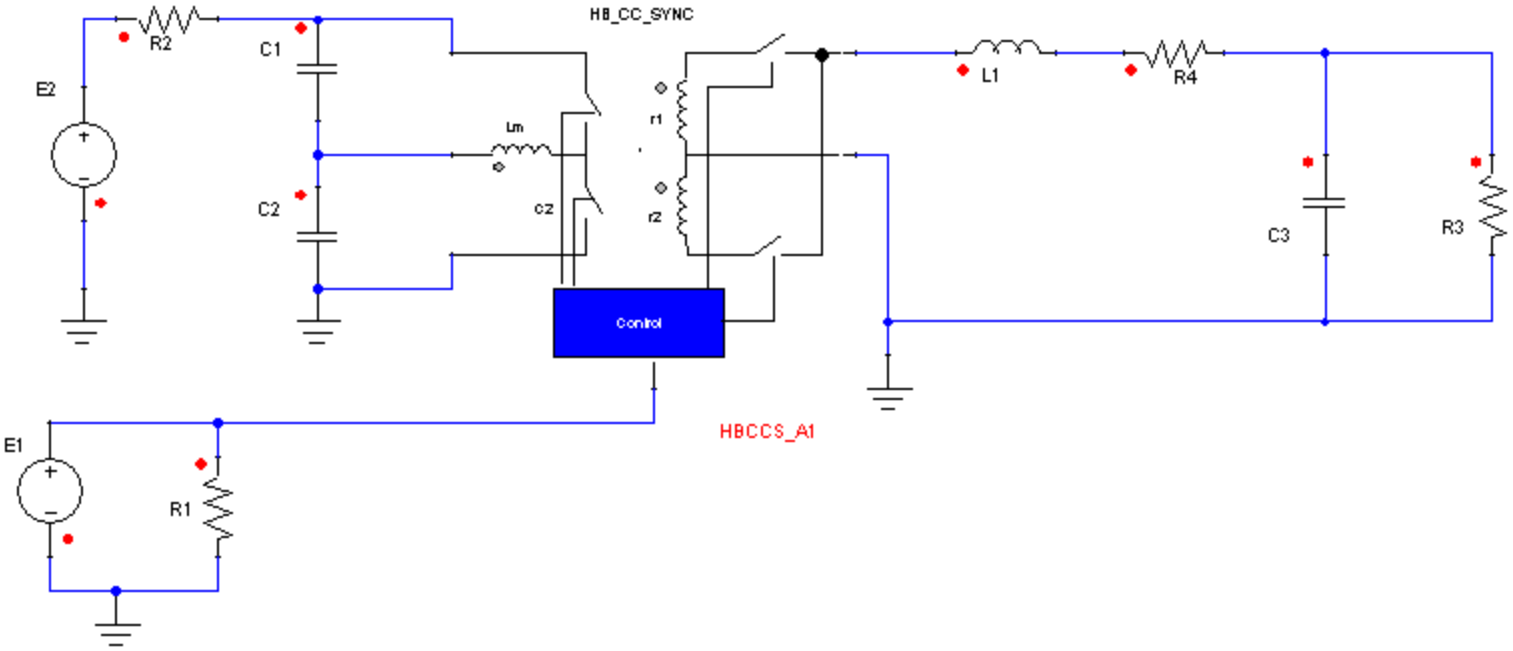

Figure 3. Application example of the Isolated Average Half Bridge Converter with Complementary Control and Synchronous Rectification.

Table 3. System Parameters

Component	Parameter	Value [unit]
Isolated Averaged Half Bridge Converter with Complementary Control and Synchronous Rectification HBCCS_A1	Rsa	0.01 [Ohm]
	r1	0.3
	r2	0.3
Resistor R1	R	1000 [Ohm]
Resistor R2	R	0.1 [Ohm]
Resistor R3	R	1 [Ohm]
Resistor R4	R	0.01

		[Ohm]
Capacitor C1	C	3e-005 [F]
Capacitor C2	C	3e-005 [F]
Capacitor C3	C	0.0001 [F]
Inductor L1	L	3e-005 [H]
Voltage Source E1	EMF Value	0.45 [V]
Voltage Source E2	EMF Value	25 [V]

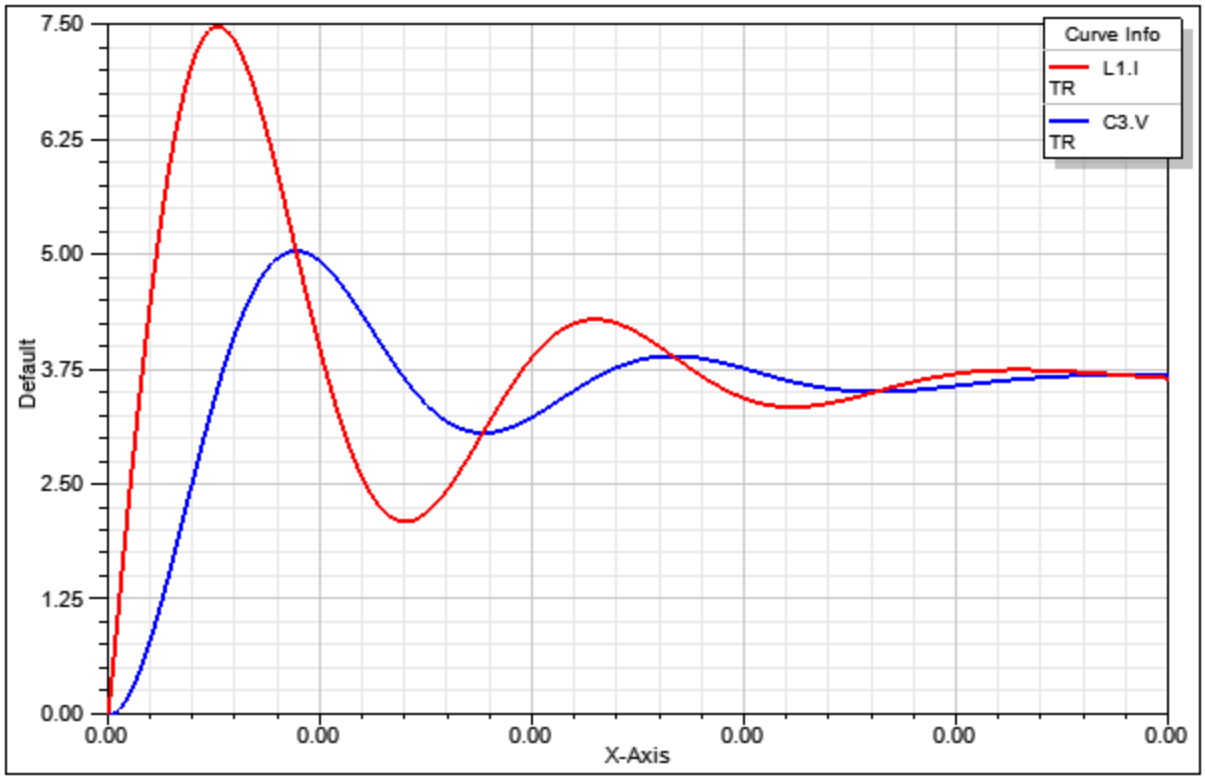

Figure 4. Simulation results-Output current (L1.I) and Output Voltage (C3.V).

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References

Averaged Half Bridge Current Doubler Rectifier

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

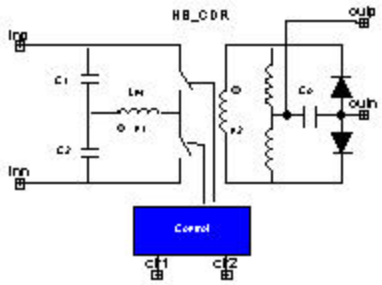

Figure 1. Component symbol

Description

This block represents the averaged model of the Half Bridge with Current Doubler Rectifier Converter.

Top

Assumptions and Limitations

The model accounts for conduction losses in the switches primary switches. This model is valid only for Continuous Conduction Mode of operation. The model also includes magnetizing inductance of the transformer referred to primary, the input capacitors and the current doubler rectifier of the output.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

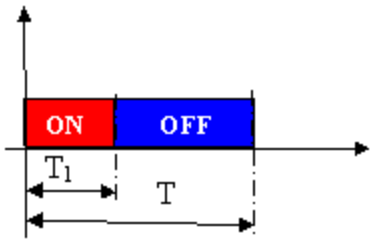

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL HBCDR_A ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, outn:= %3, ctr1:= %4, ctr2:= %5 (n1:= @n1, n2:= @n2, Rsa:= @Rsa, Fs:= @Fs, Lm:= @Lm, Lm_IC:= @Lm_IC, Co:= @Co, Co_IC:= @Co_IC, L1:= @L1, L1_IC:= @L1_IC, L2:= @L2, L2_IC:= @L2_IC, C1:= @C1, C2:= @C2, C1_IC:= @C1_IC, C2_IC:= @C2_IC) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	positive input pin	Electrical terminal
inn	negative input pin	Electrical terminal
outp	positive output pin	Electrical terminal
outn	negative output pin	Electrical terminal
ctr1	control pin 1: duty cycle for the upper switch	Electrical terminal
ctr2	control pin 2: duty cycle for the lower switch	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
n1	Primary Number of Turns	real	1
n2	Secondary Number of Turns	real	1
Rsa	Primary Side Switch ON Resistance	real	0.01 [Ohm]
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]
Co	Output Capacitor Value	real	0.0001 [F]
Co_IC	Output Capacitor Initial Condition	real	0 [V]
L1	Secondary Upper Filter Inductor	real	1e-5 [H]
L1_IC	Secondary Upper Filter Inductor Initial Condition	real	0 [A]
L2	Secondary Lower Filter Inductor	real	1e-5 [H]
L2_IC	Secondary Lower Filter Inductor Initial Condition	real	0 [A]
C1	Primary Upper Side Capacitor Value	real	1e-5 [F]
C1_IC	Primary Upper Side Capacitor Initial Condition	real	0 [V]
C2	Primary Lower Side Capacitor Value	real	1e-5 [F]
C2_IC	Primary Lower Side Capacitor Initial Condition	real	0 [V]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
I_Lm	Magnetizing Current (Primary) [A]	Output	real
I_L1	Output 1 Inductor Current [A]	Output	real
I_L2	Output 2 Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of a Half Bridge Converter with Current Doubler Rectifier for use in transient, AC or DC analysis.

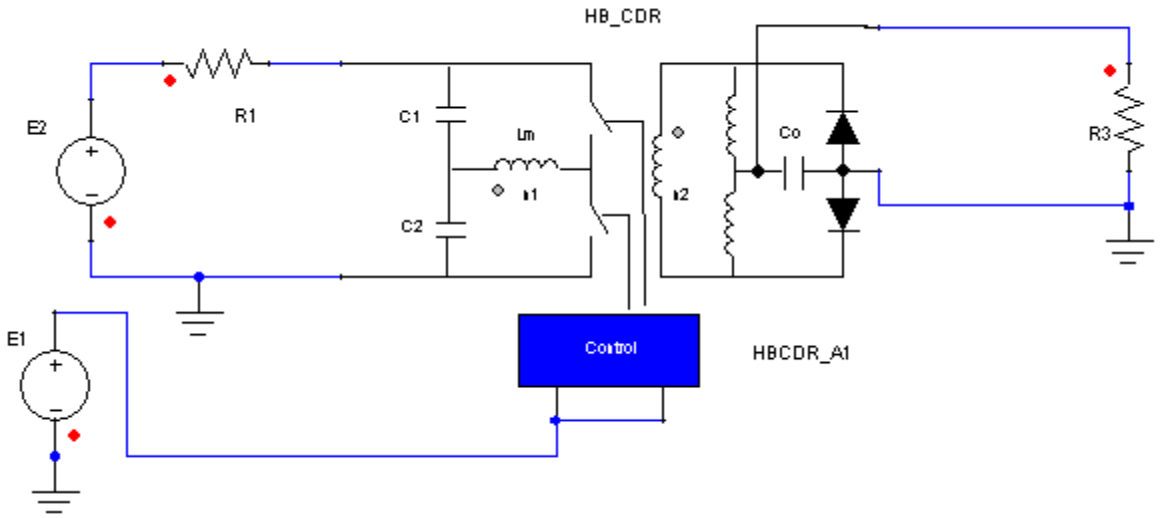

Figure 3. Application example of the Isolated Average Half Bridge Converter with Current Doubler Rectifier .

Table 4. System Parameters

Component	Parameter	Value [unit]
Isolated Averaged Half Bridge Converter with Current Doubler Rectifier HBCDR_A1	n1/n2	1

	L1	0.0001
	L2	0.0001
Resistor R1	R	0.001 [Ohm]
Resistor R3	R	1.1 [Ohm]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

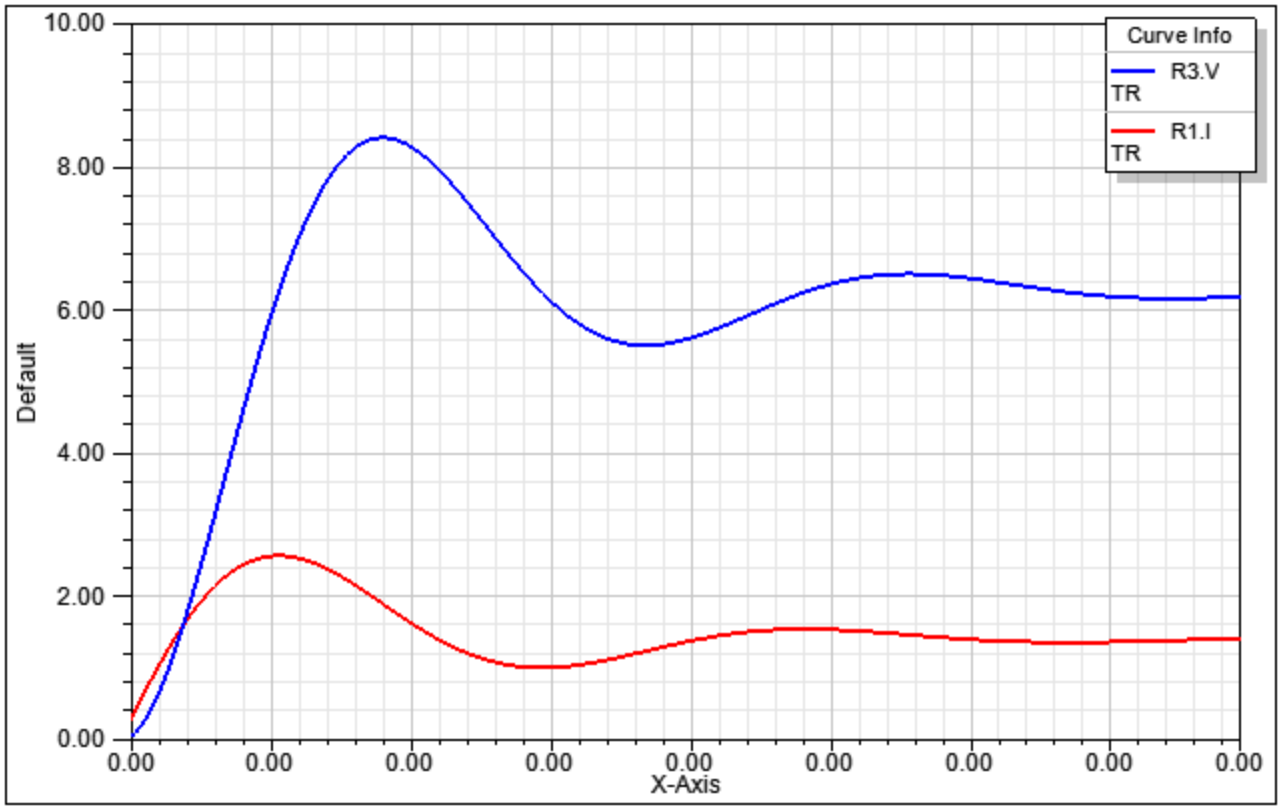

Figure 4. Simulation results-Input current (R1.I) and Output Voltage (R3.V).

Top

References

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Ideal Averaged Buck-Boost Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

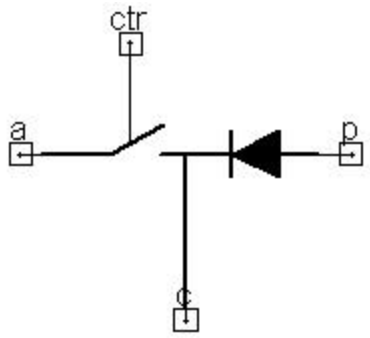

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck-Boost converter. It does not have an internal inductor.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

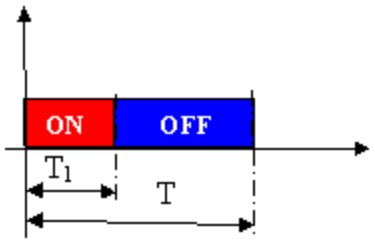

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BBOOST_AI_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L_EXT:= @L_EXT) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]

L_EXT	Inductance	real	1e-5 [H]
Fs	Switching Frequency	real	100000 [Hz]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current[A]	Output	real

Top

Example

This example shows an averaged model of an Ideal Buck-Boost Converter for transient, AC, or DC analysis.

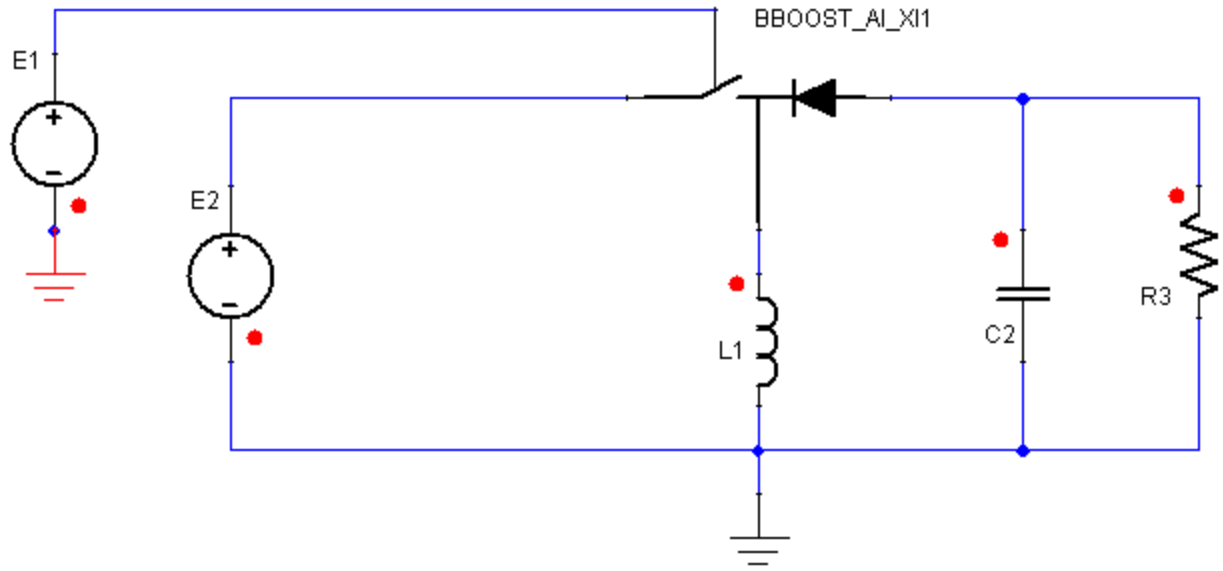

Figure 3. Application example of Ideal Averaged Buck-Boost Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]

Ideal Averaged Buck-Boost Converter BBOOST_AI_XI1	Fs	100000 [Hz]
	L_EXT	1e-005 [H]
Resistor R3	R	1 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L1	L	1e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

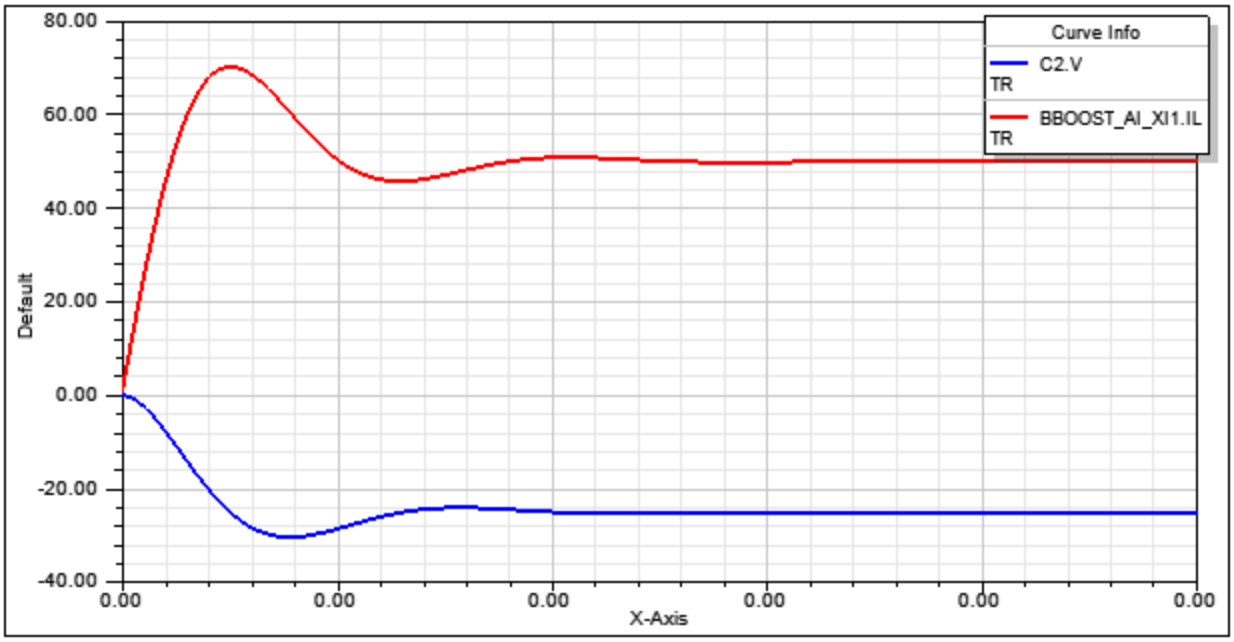

Figure 4. Simulation results-Output current (BBOOST_AI_XI1.IL) and Output Voltage (C2.V).

Top

References

Ideal Averaged Boost Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

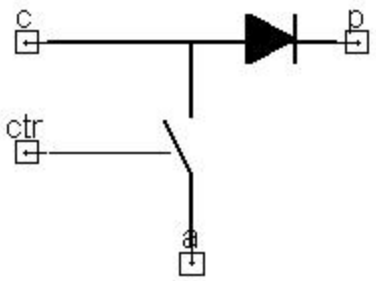

Figure 1. Component symbol

Description

This block represents the averaged model of the Boost converter. This component does not have an internal inductor.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

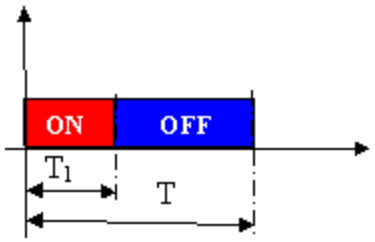

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BOOST_AI_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L_EXT:= @L_EXT) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]

L_EXT	Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current[A]	Output	real

Top

Example

This example shows an averaged model of an Ideal Boost Converter for transient, AC, or DC analysis.

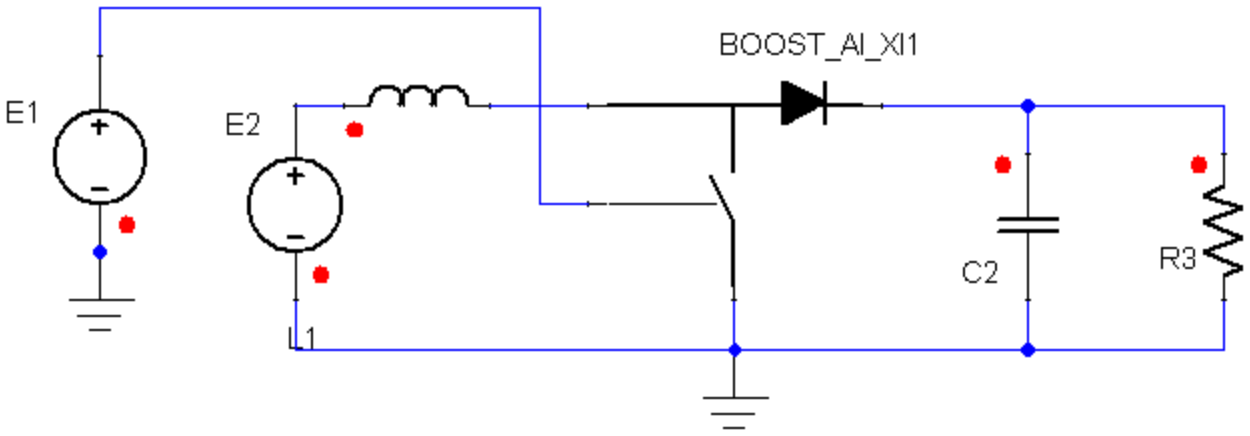

Figure 3. Application example of Ideal Averaged Boost Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]
Ideal Averaged Boost Converter BOOST_AI_XI1	Fs	100000 [Hz]
	L_EXT	0.0001 [H]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L1	L	0.0001 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

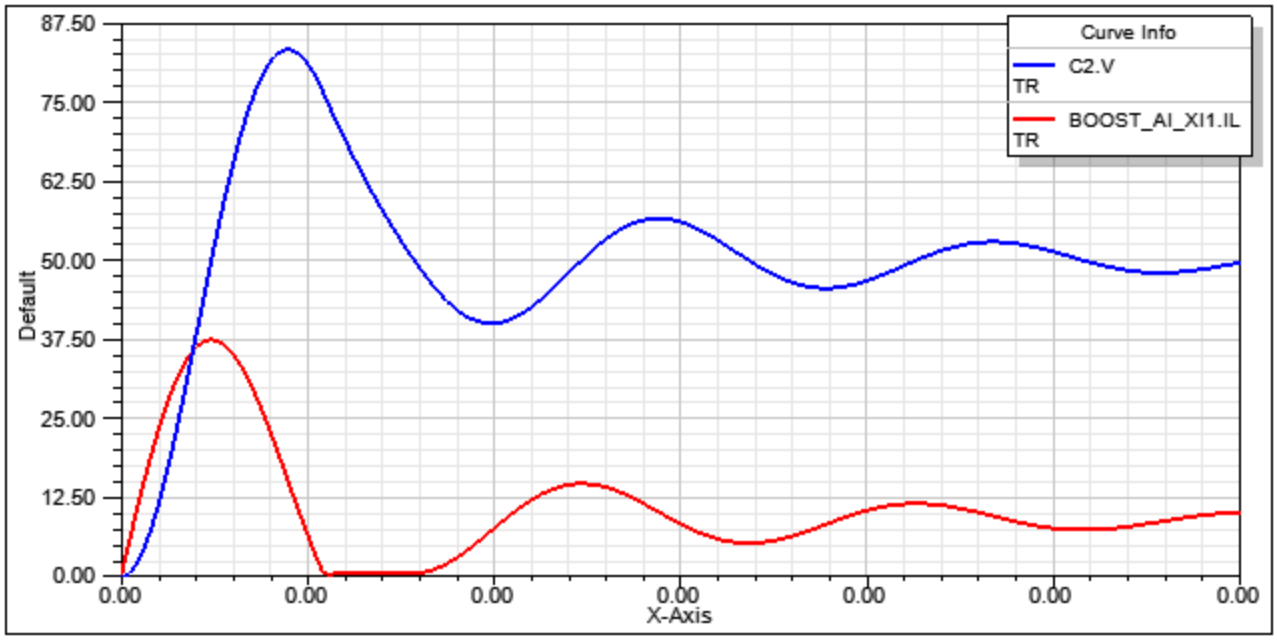

Figure 4. Simulation results-Output current (BOOST_AI_XI1.IL) and Output Voltage (C2.V).

Top

References

Ideal Averaged Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

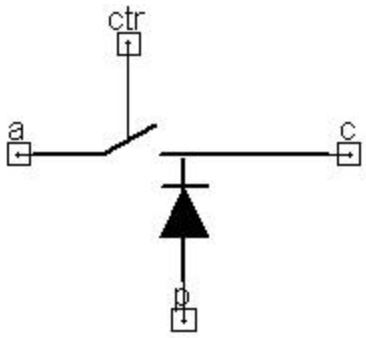

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter. It does not have an internal inductance.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

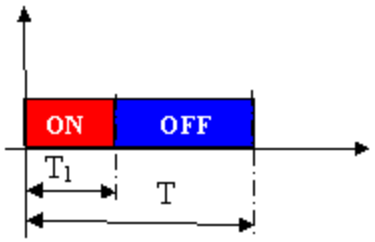

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCK_AI_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L_EXT:= @L_EXT) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]

L_EXT	Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]

Top

Example

This example shows an averaged model of an Ideal Buck Converter for transient, AC, or DC analysis.

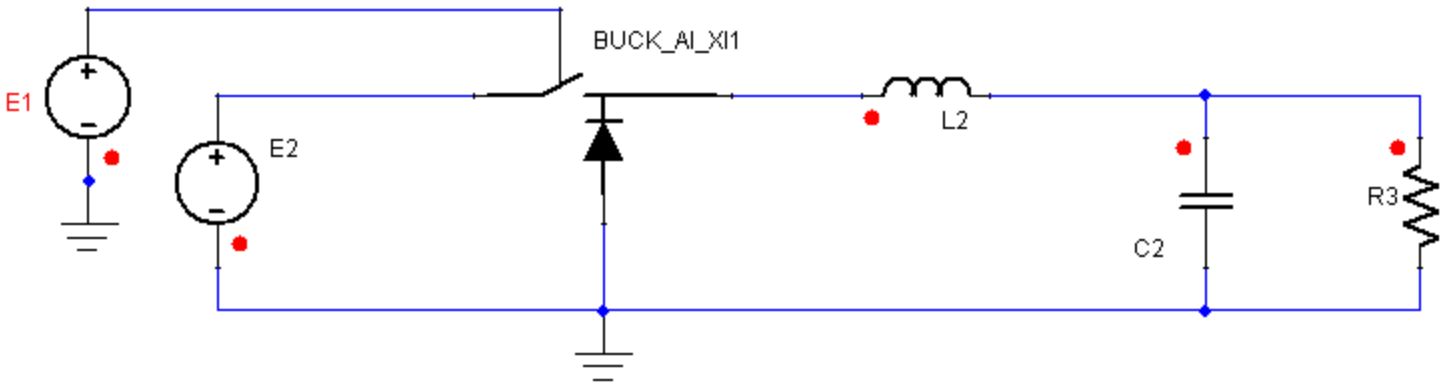

Figure 3. Application example of Ideal Averaged Buck Converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Averaged Ideal Buck Converter BUCK_AI_XI1	Fs	100000 [Hz]
	L_EXT	3e-005 [H]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]

Voltage Source E2	EMF Value	25 [V]

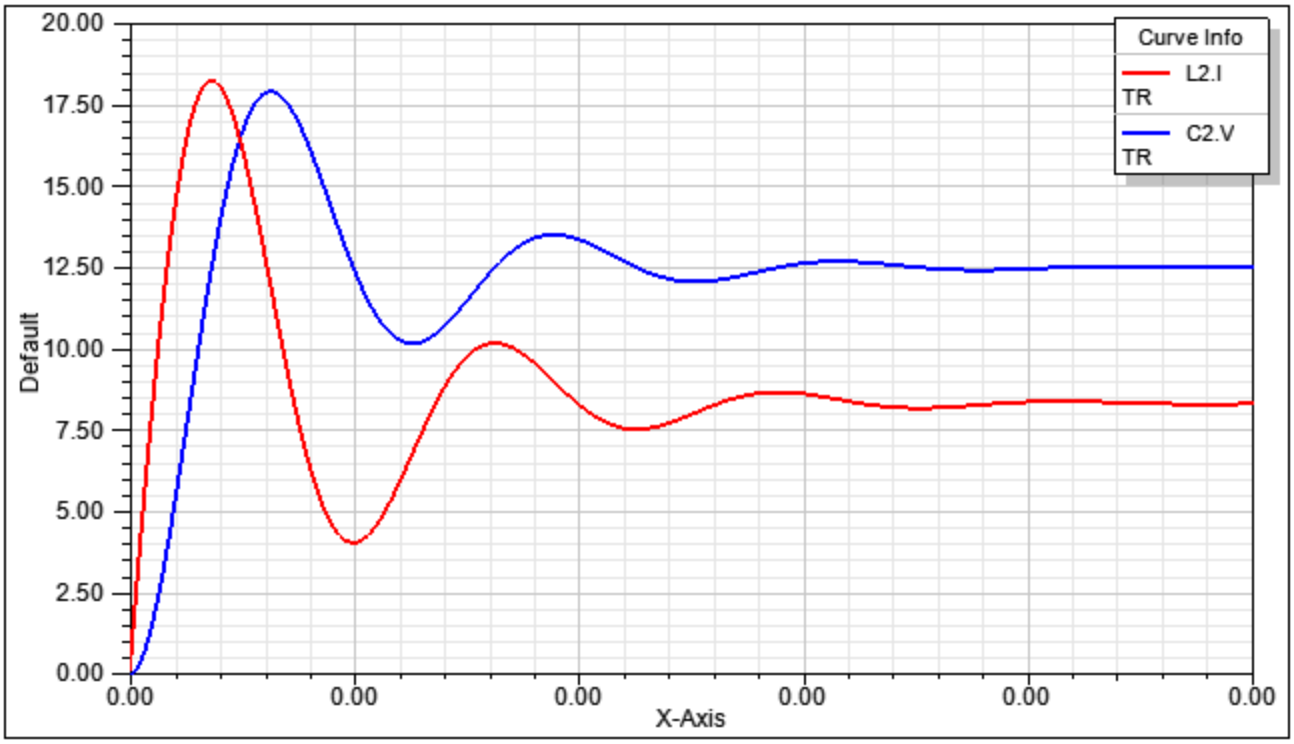

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

Ideal Averaged Buck Sync Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

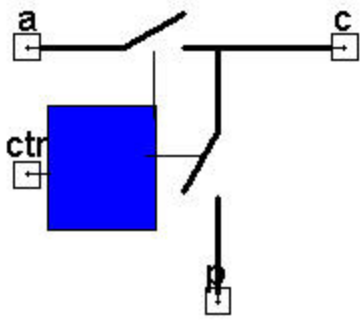

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter with synchronous rectification. It does not have an internal inductor.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

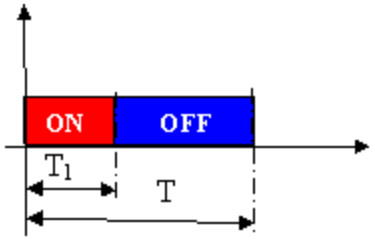

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCKS_AI_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 ( ) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Example

This example shows an averaged model of an Ideal Synchronous Buck Converter for transient, AC, or DC analysis.

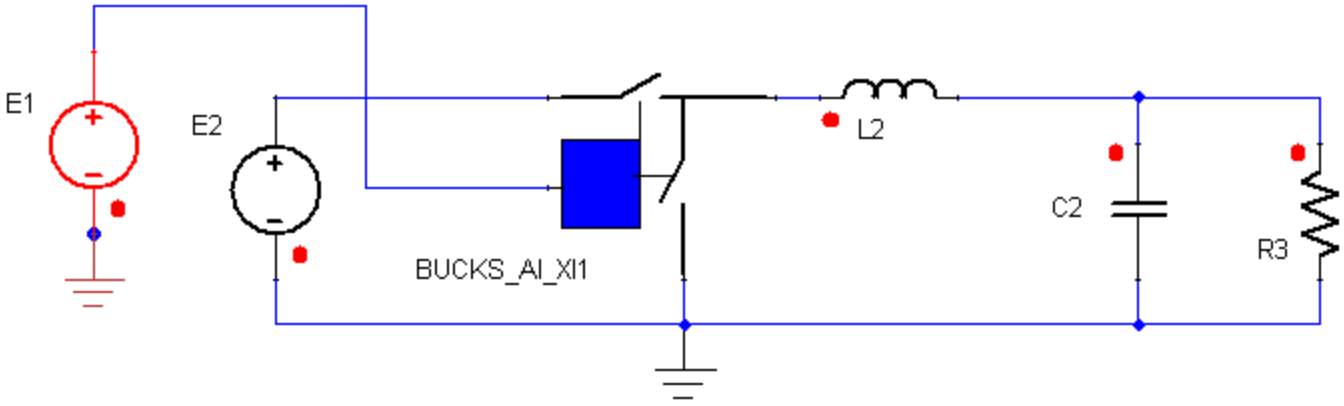

Figure 3. Application example of Ideal Averaged Synchronous Buck Converter.

Table 2. System Parameters

Component	Parameter	Value [unit]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

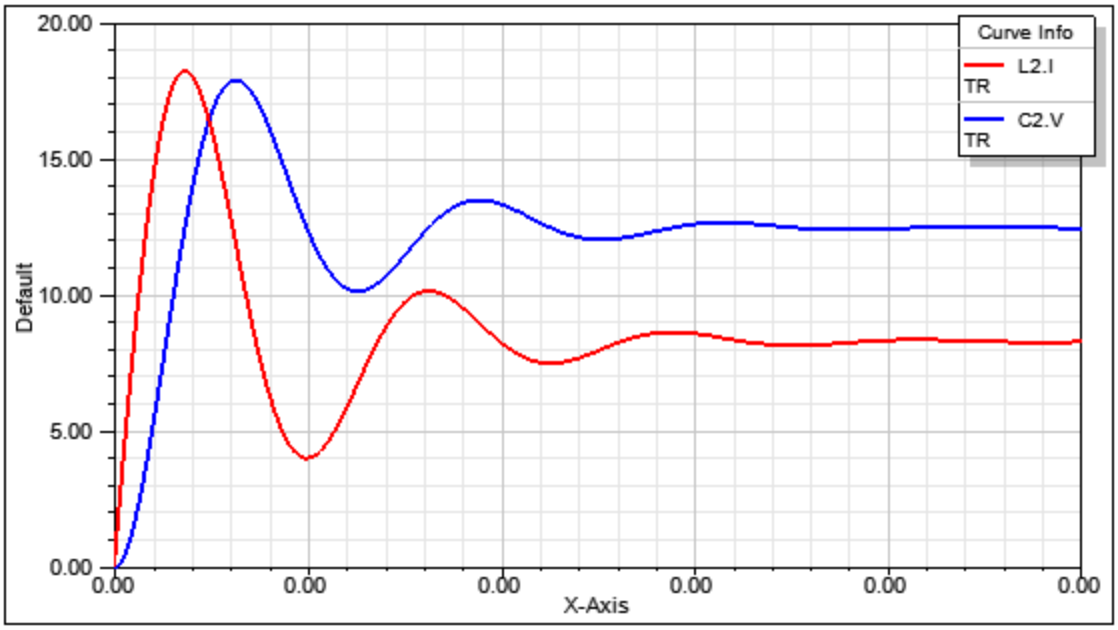

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

PWM-Switch

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

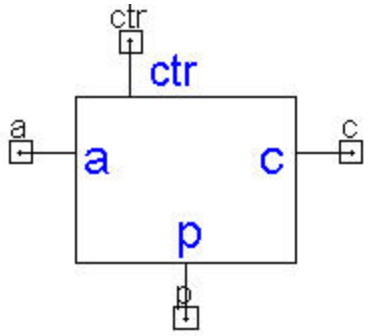

Figure 1. Component symbol

Description

This block represents the averaged model of a PWM Switch.

Top

Assumptions and Limitations

It assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

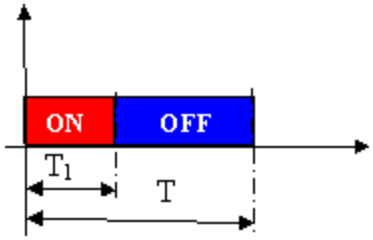

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL PWMS_AI_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) ctr:= %0, a:= %1, p:= %2, c:= %3 (L_EXT:= @L_EXT, Fs:= @Fs) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Equivalent inductance (usually connected to the common terminal)	real	1e-5 [H]
Fs	Switching Frequency	real	100000 [Hz]

Top

Example

This example shows a model of a PWM Switch applied to model a Buck Converter for transient, AC, or DC analysis.

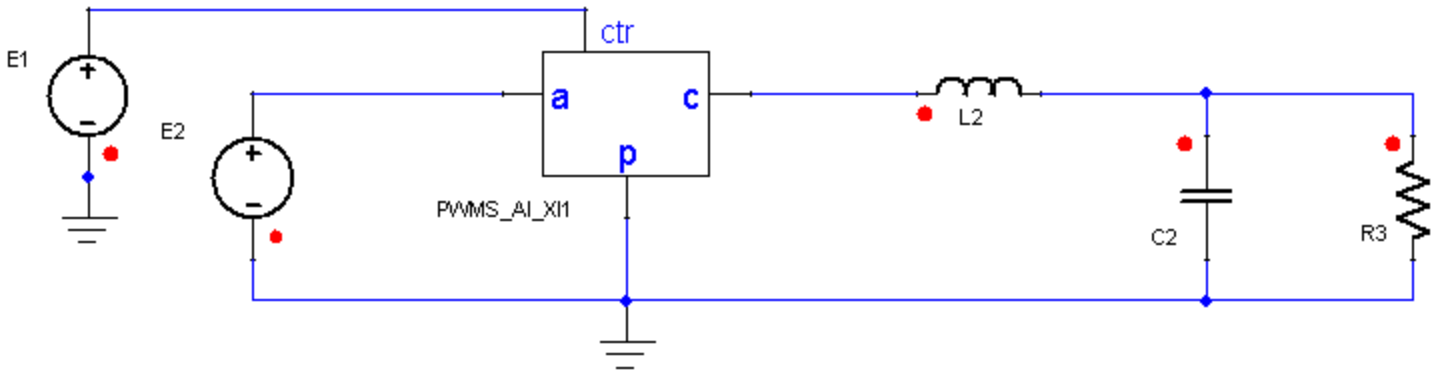

Figure 3. Application example of PWM Switch.

Table 3. System Parameters

Component	Parameter	Value [unit]
PWM Switch PWMS_AI_XI1	Fs	100000 [Hz]
	L_EXT	1e-005 [H]
Resistor R3	R	5 [Ohm]

Capacitor C2	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

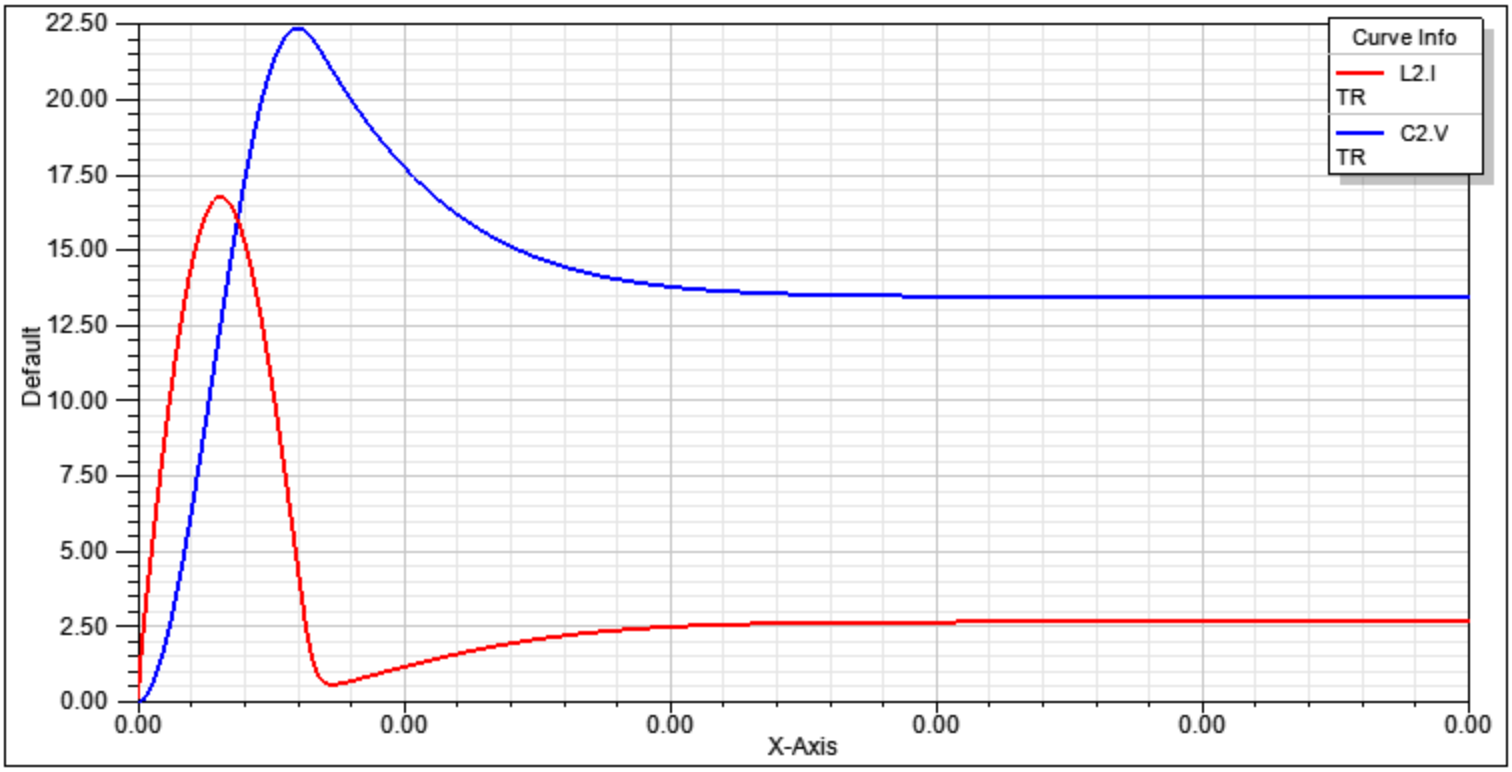

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Ideal Averaged Buck-Boost Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

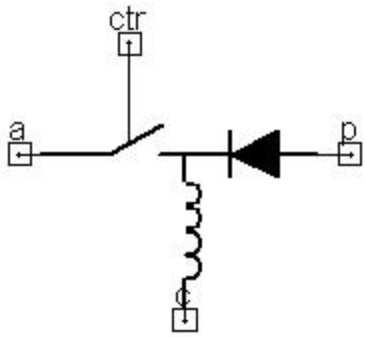

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck-Boost converter. This model includes an internal inductor.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

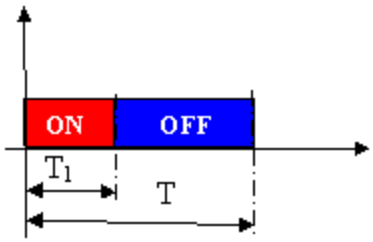

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BBOOST_AI_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Filter Inductance	real	1e-5 [H]
Fs	Switching Frequency	real	100000 [Hz]
L_IC	Inductor Initial Current	real	0 [A]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current[A]	Output	real

Top

Example

This example shows an averaged model of an Ideal Buck-Boost Converter with Internal Inductor for transient, AC, or DC analysis.

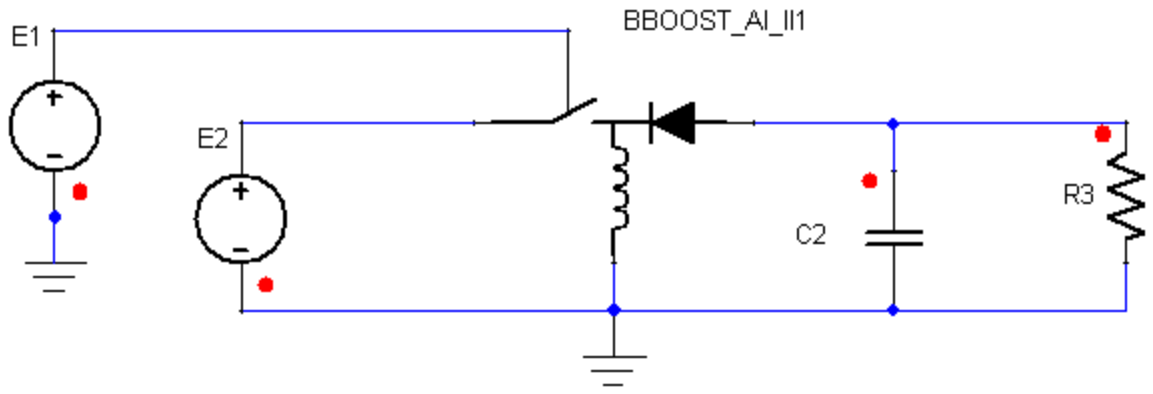

Figure 3. Application example of Ideal Averaged Buck-Boost Converter.

Table 4. System Parameters

Component	Parameter	Value

		[unit]
Ideal Averaged Buck-Boost Converter BBOOST_AI_II1	L	1e-005 [H]
	L_IC	0.001 [A]
Resistor R3	R	1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

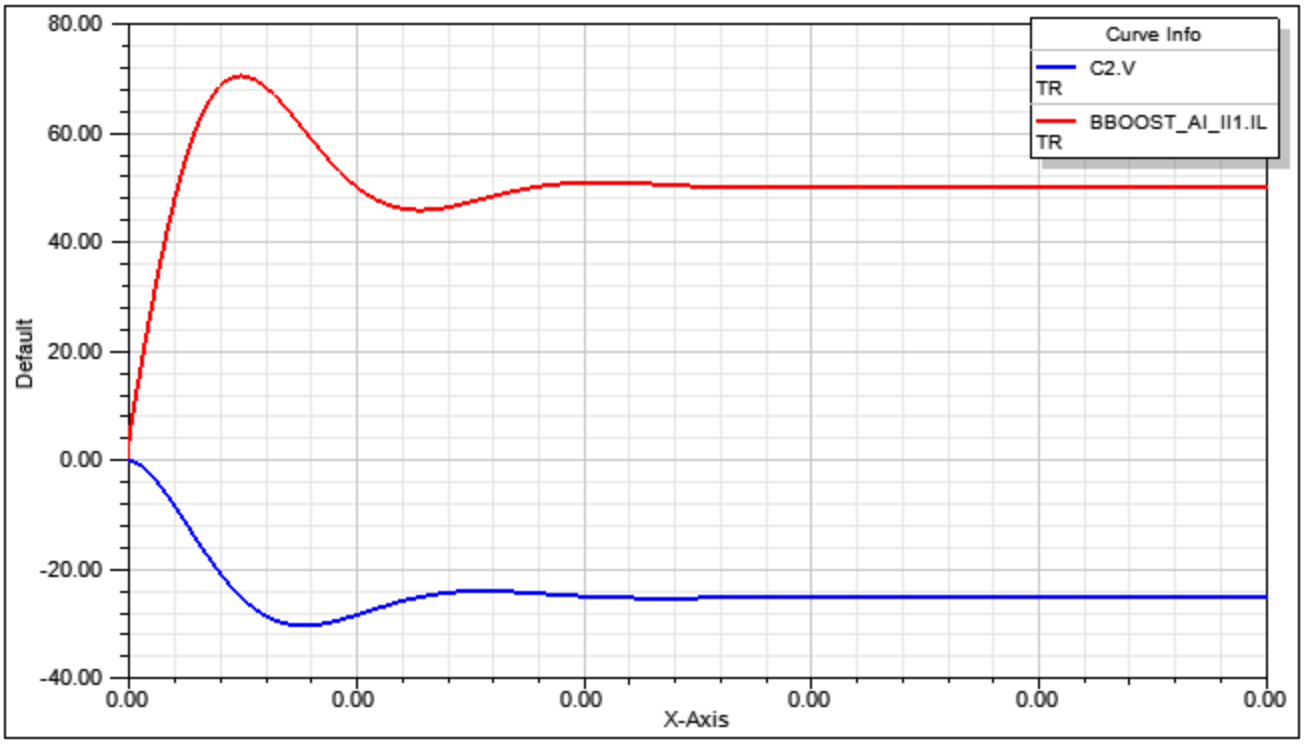

Figure 4. Simulation results-Output current (BBOOST_AI_II1.IL) and Output Voltage (C2.V).

Top

References

Ideal Averaged Boost Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

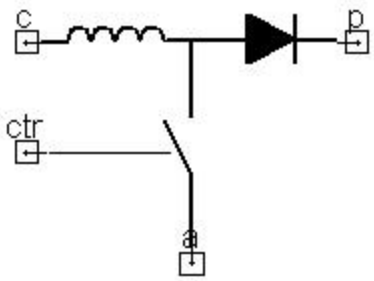

Figure 1. Component symbol

Description

This block represents the averaged model of the Boost converter. This model includes an internal inductor.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

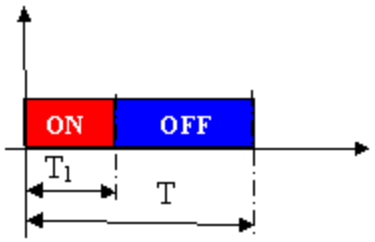

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BOOST_AI_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]

L	Filter Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]
L_IC	Inductor Initial Current	real	0.001 [A]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current[A]	Output	real

Top

Example

This example shows an averaged model of an Ideal Boost Converter with Internal Inductor for transient, AC, or DC analysis.

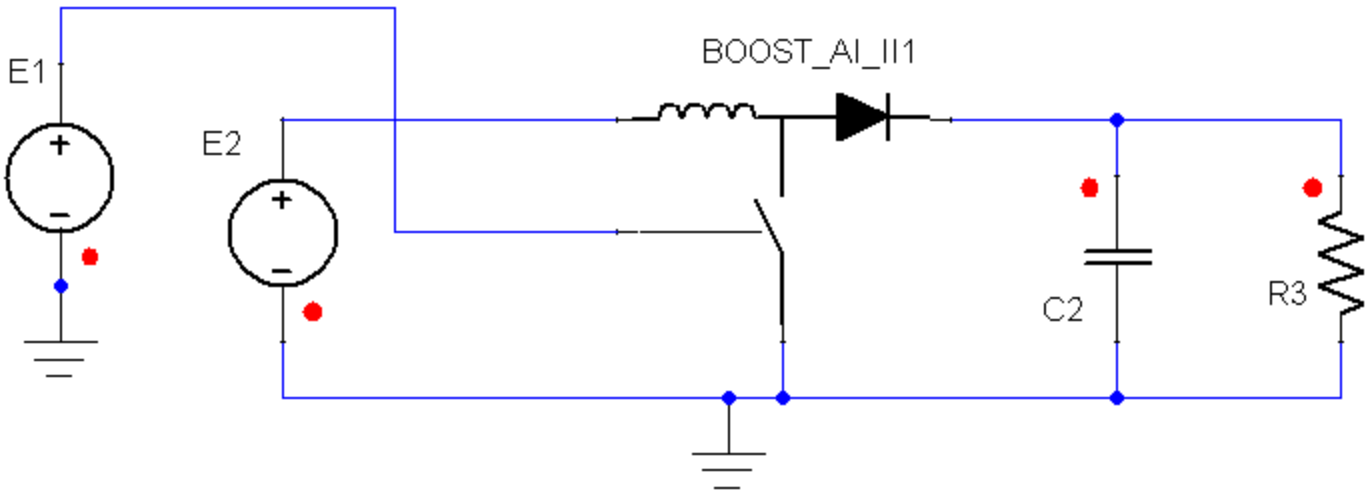

Figure 3. Application example of Ideal Averaged Boost Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]
Ideal Averaged Boost Converter BOOST_AI_II1	L	0.0001 [H]
	L_IC	0.001 [A]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

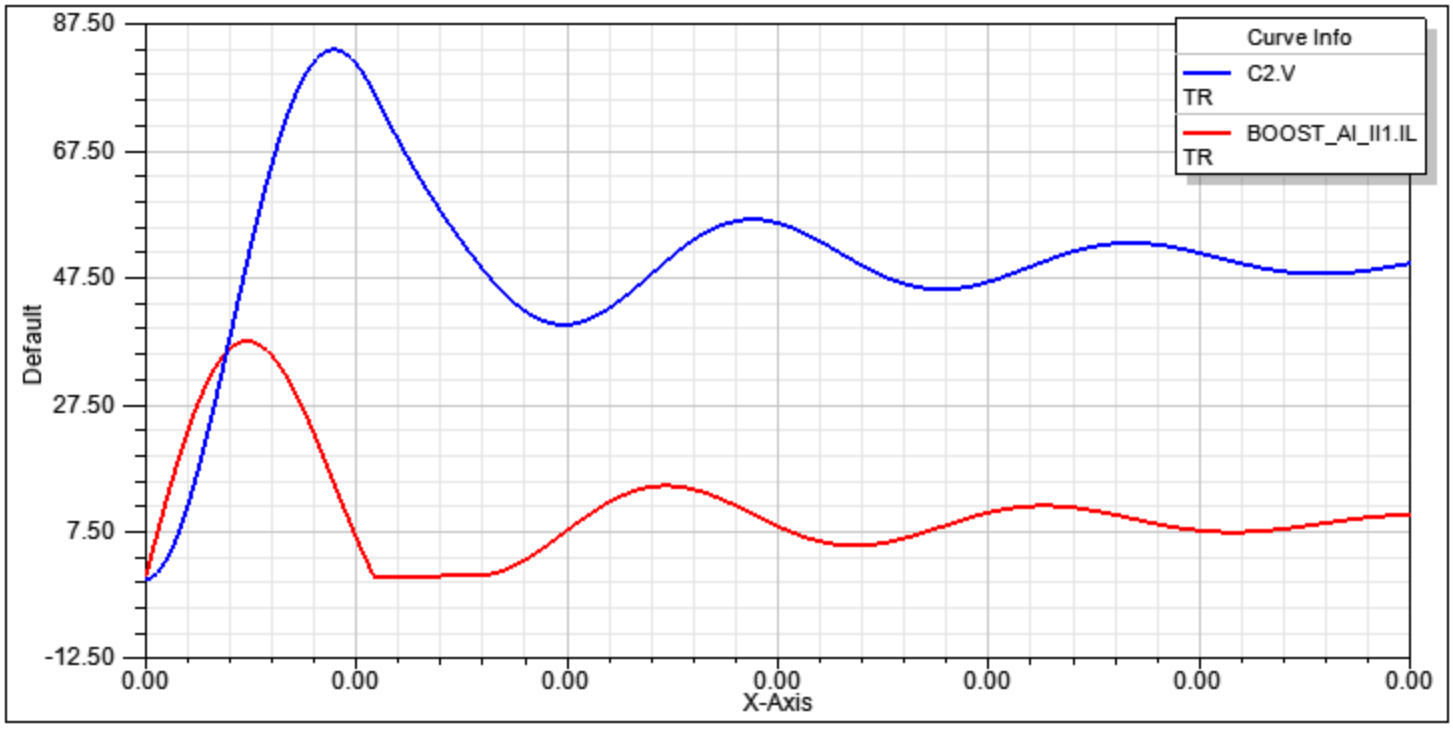

Figure 4. Simulation results-Output current (BOOST_AI_II1.IL) and Output Voltage (C2.V).

Top

References

Ideal Averaged Buck Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

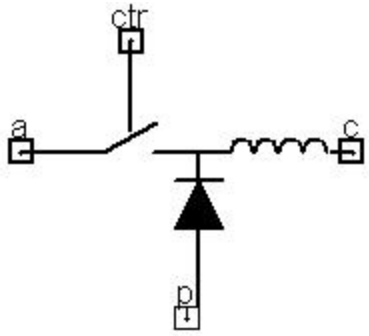

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter. This model includes an internal inductor.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

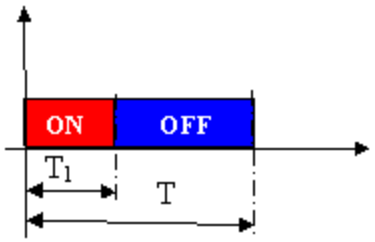

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCK_AI_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]

L	Filter Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]
L_IC	Inductor Initial Current	real	0 [A]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Ideal Buck Converter with Internal Inductor for transient, AC, or DC analysis.

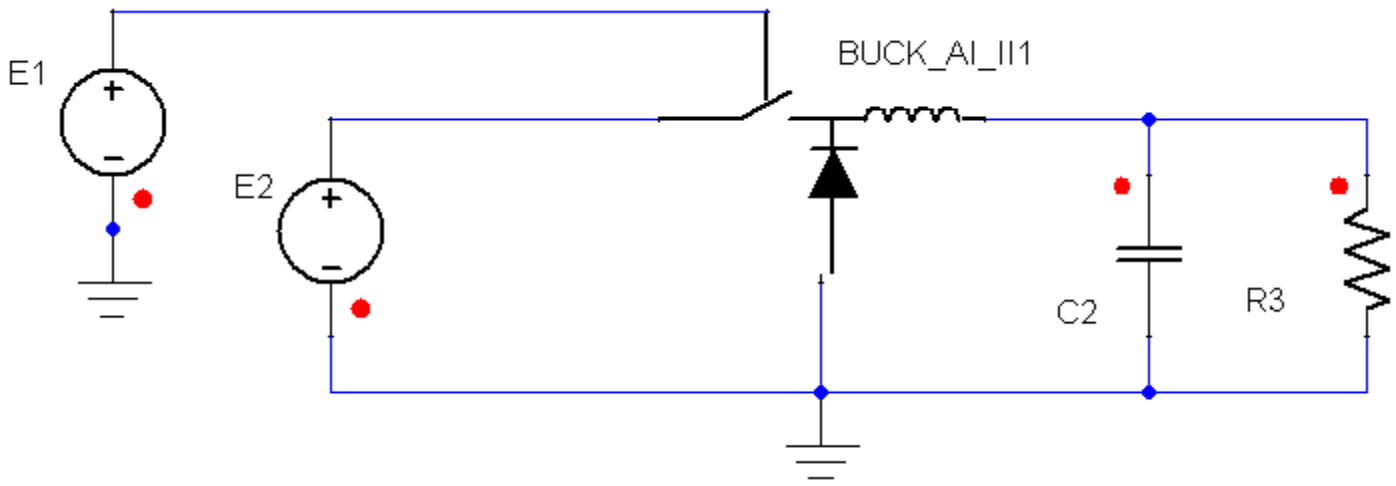

Figure 3. Application example of Ideal Averaged Buck Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]

Ideal Averaged Buck Converter BUCK_AI_II1	Fs	100000 [Hz]
	L	3e-005 [H]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

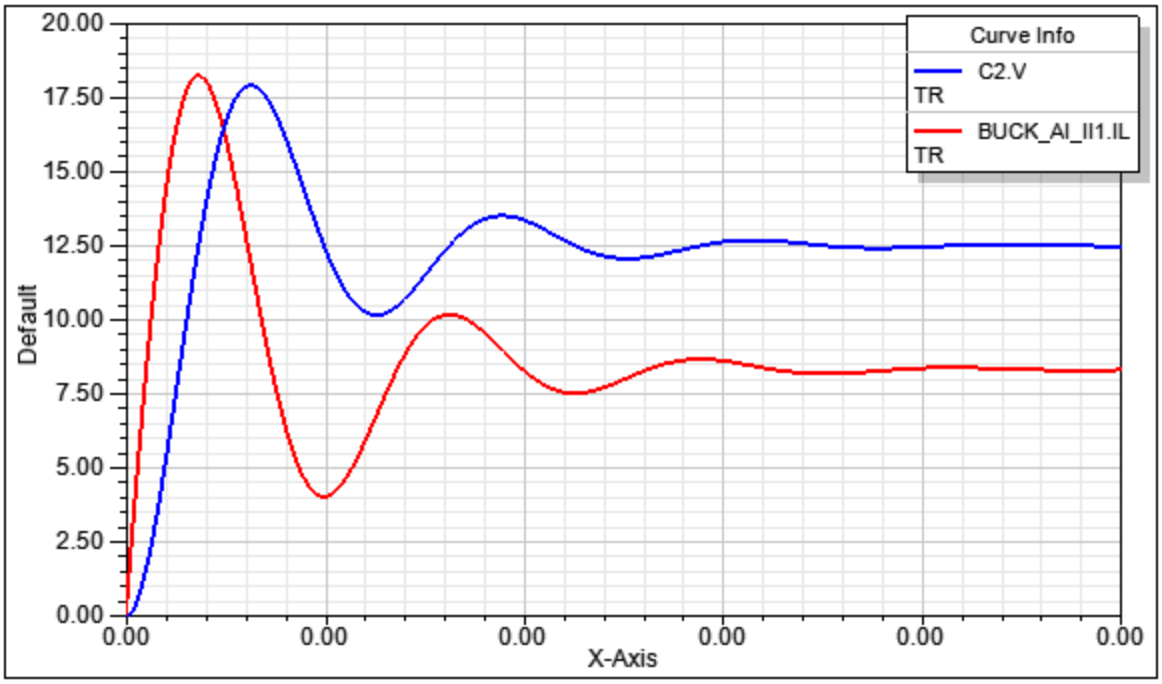

Figure 4. Simulation results-Output current (BUCK_AI_II1.IL) and Output Voltage (C2.V).

Top

References

Ideal Averaged Buck Sync Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

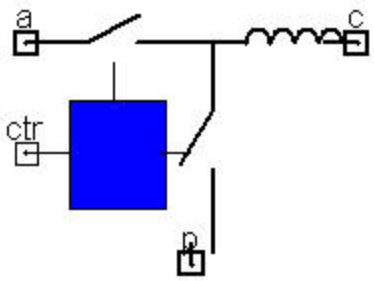

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter with synchronous rectification. This model includes an internal inductor.

Top

Assumptions and Limitations

This model assumes that the switches are ideal in the sense that the voltage drop across them when they are on is zero.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

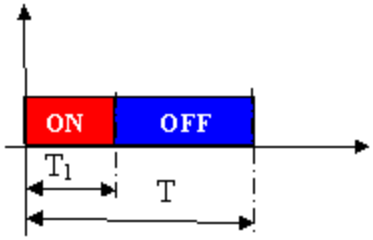

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCKS_AI_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (L:= @L, L_IC:= @L_IC) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Filter Inductance	real	1e-4 [H]
L_IC	Inductor Initial Current	real	0 [A]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Ideal Synchronous Buck Converter with Internal Inductor for transient, AC, or DC analysis.

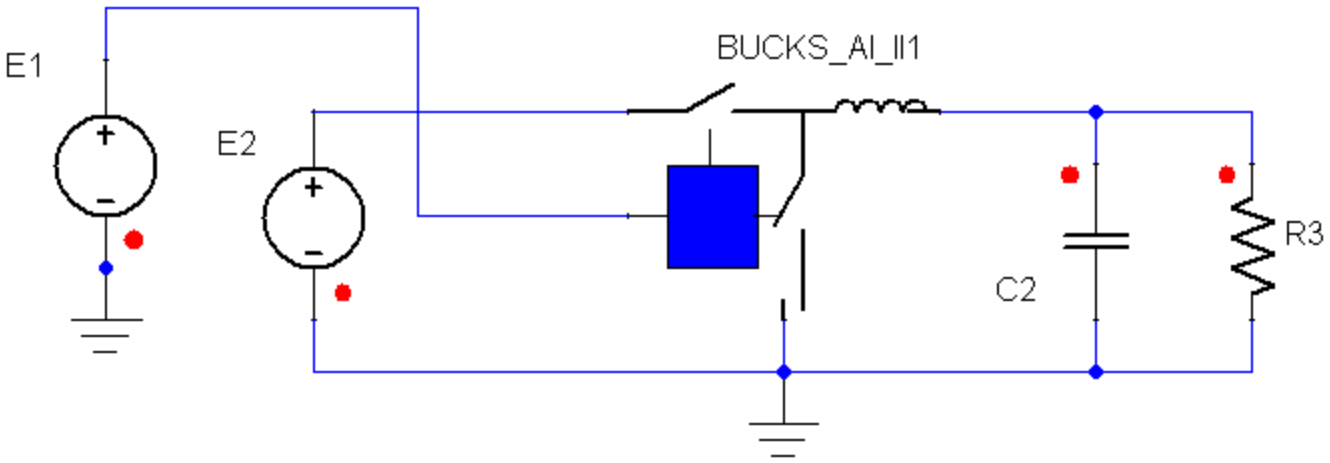

Figure 3. Application example of Ideal Averaged Synchronous Buck Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]
Ideal Averaged Buck Sync Converter BUCKS_AI_II1	L	3e-005 [H]
	L_IC	0 [A]
Resistor R3	R	1.5

		[Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

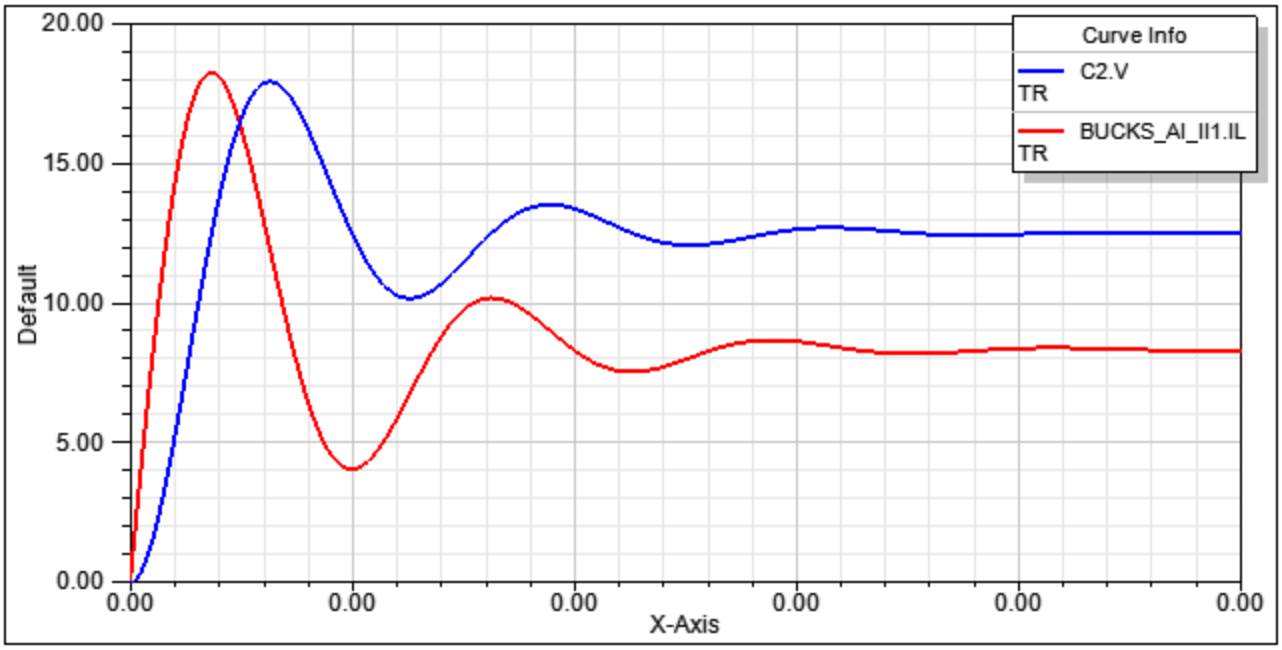

Figure 4. Simulation results-Output current (BUCKS_AI_II1.IL) and Output Voltage (C2.V).

Top

References

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Non-Ideal Averaged Buck-Boost Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

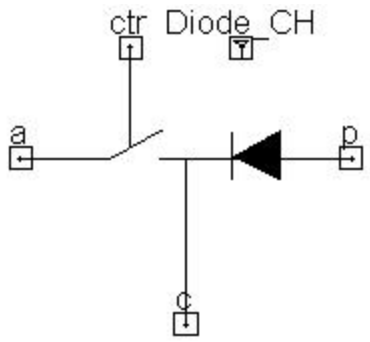

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck-Boost converter. It does not have an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

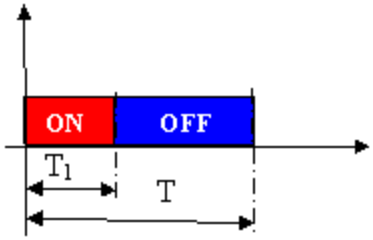

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BBOOST_A_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L_EXT:= @L_EXT, Diode_CH:= @Diode_CH, Rsa:= @Rsa) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L_EXT	Inductance	real	1e-5 [H]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Active Switch On Resist-ance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Buck-Boost Converter for transient, AC, or DC analysis.

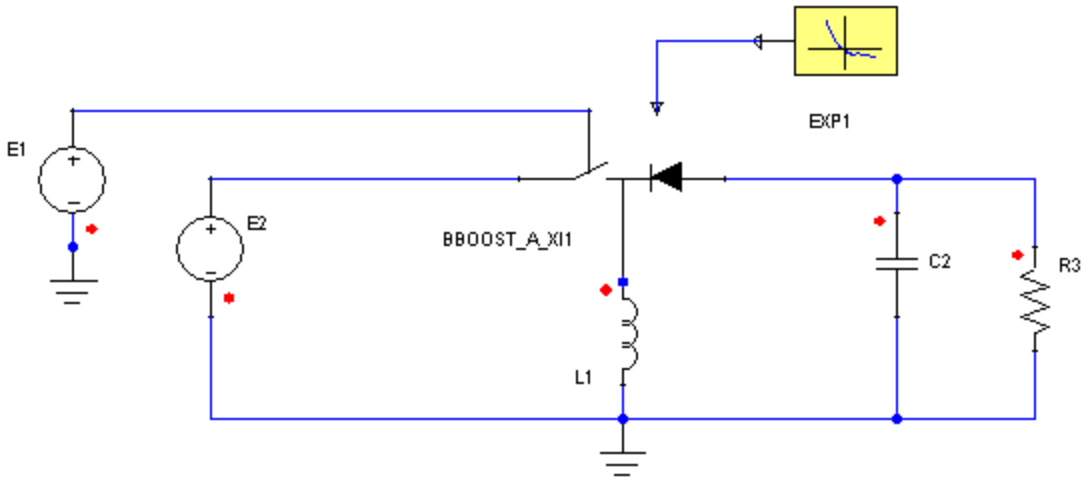

Figure 3. Application example of Non-Ideal Averaged Buck-Boost Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Buck-Boost Converter BBOOST_A_XI1	L_EXT	1e-005 [H]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L1	L	1e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

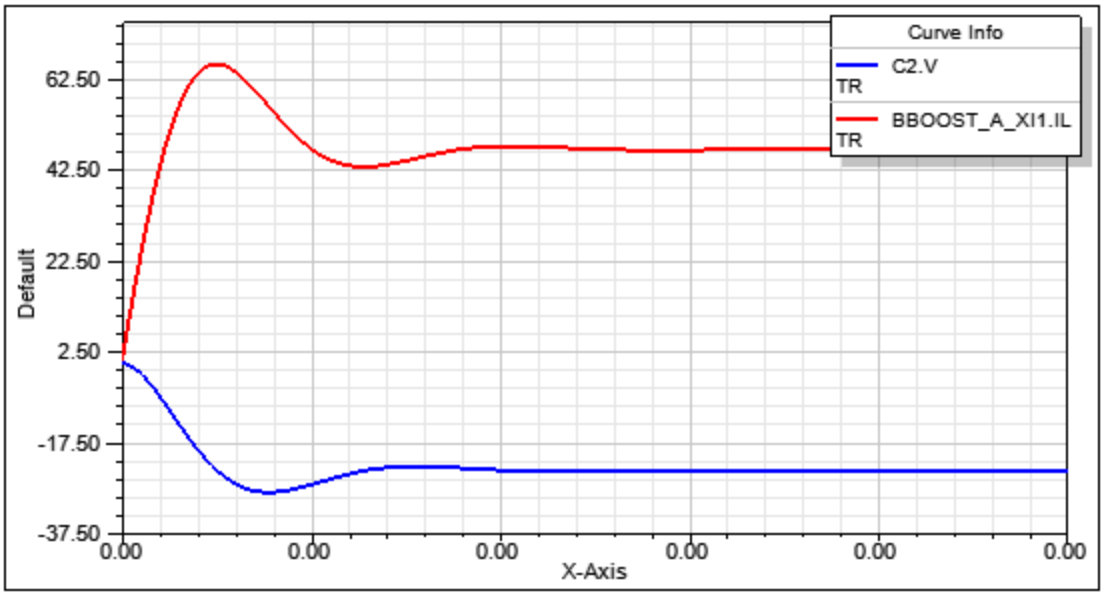

Figure 4. Simulation results-Output current (BBOOST_A_XI1.IL) and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Buck-Boost Converter with Synchronous Rectification

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

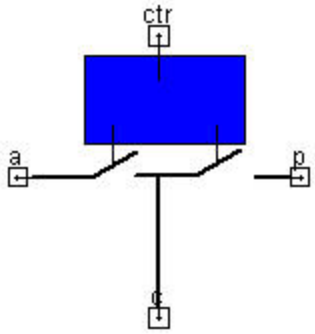

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck-Boost converter with synchronous rectification. It does not have an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

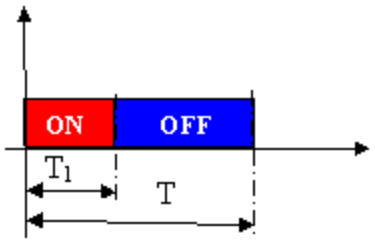

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BBOOSTS_A_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Rsa:= @Rsa, Rsp:= @Rsp) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]

Rsa	Active Switch On Resistance	real	0.01 [Ohm]
Rsp	Passive Switch On Resistance	real	0.01 [Ohm]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Buck-Boost Converter with Synchronous Rectification for transient, AC, or DC analysis.

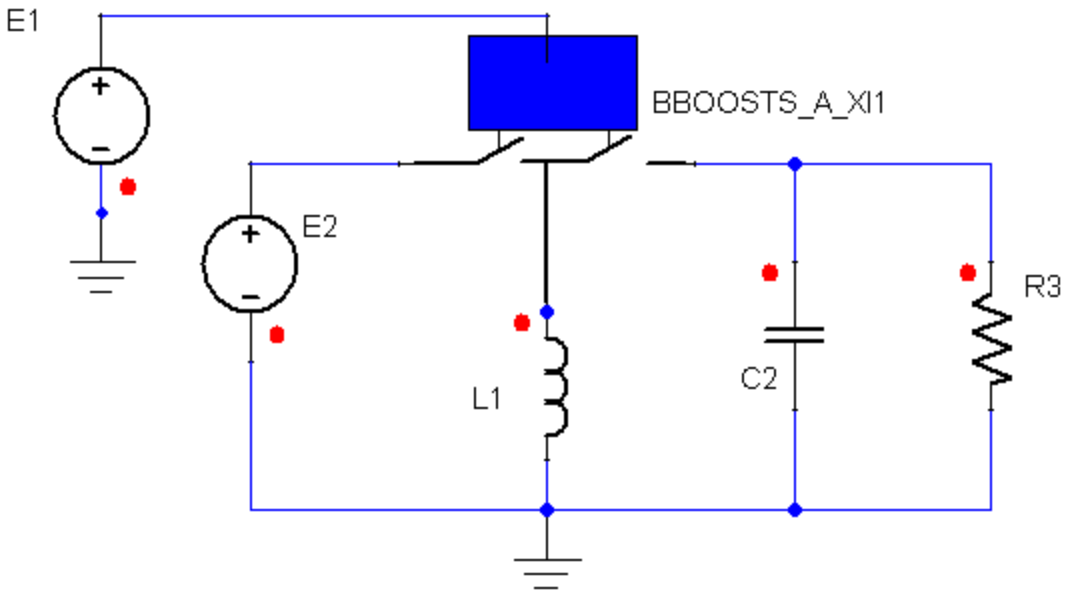

Figure 3. Application example of Non-Ideal Averaged Buck-Boost Converter with Synchronous Rectification.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Buck-Boost Converter with Synchronous Rectification BBOOSTS_A_XI1	Rsa	0.01 [Ohm]
	Rsp	0.01 [Ohm]
Resistor R3	R	1 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L1	L	1e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

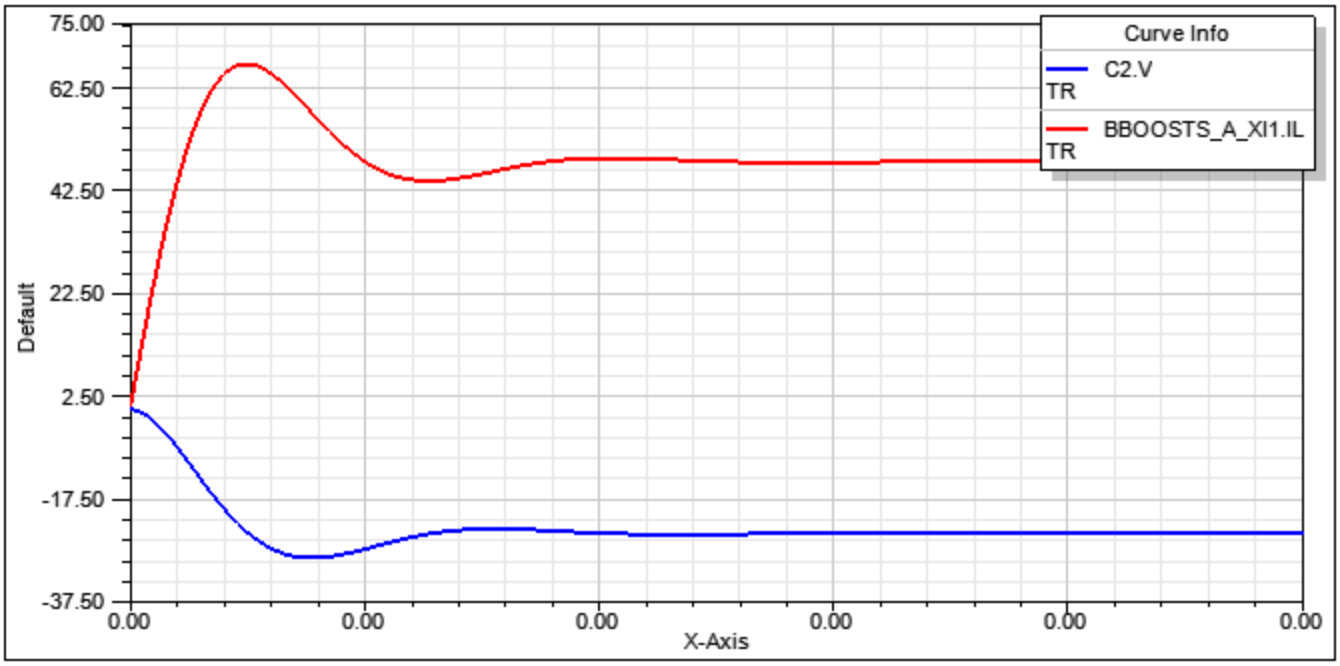

Figure 4. Simulation results-Output current (BBOOSTS_A_XI1.IL) and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Boost Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

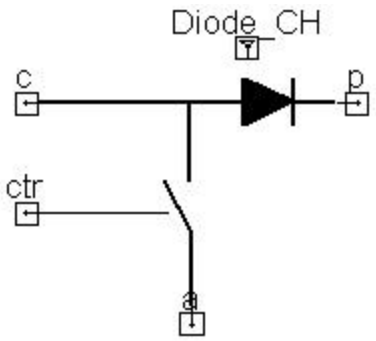

Figure 1. Component symbol

Description

This block represents the averaged model of the Boost converter. This component does not have an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

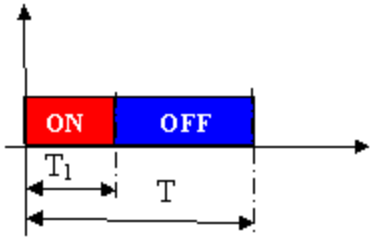

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BOOST_A_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L_EXT:= @L_EXT, Rsa:= @Rsa, Diode_CH:= @Diode_CH) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L_EXT	Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Boost Converter for transient, AC, or DC analysis.

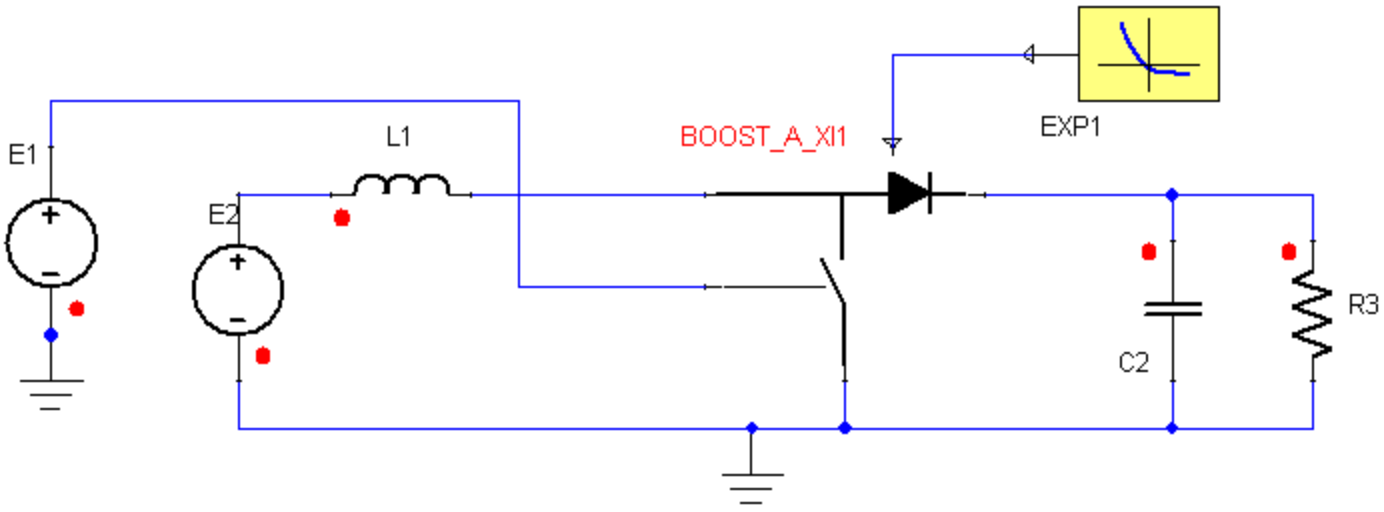

Figure 3. Application example of Non-Ideal Averaged Boost Converter.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Boost Converter BOOST_A_XI1	L_EXT	0.0001 [H]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L1	L	0.0001 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

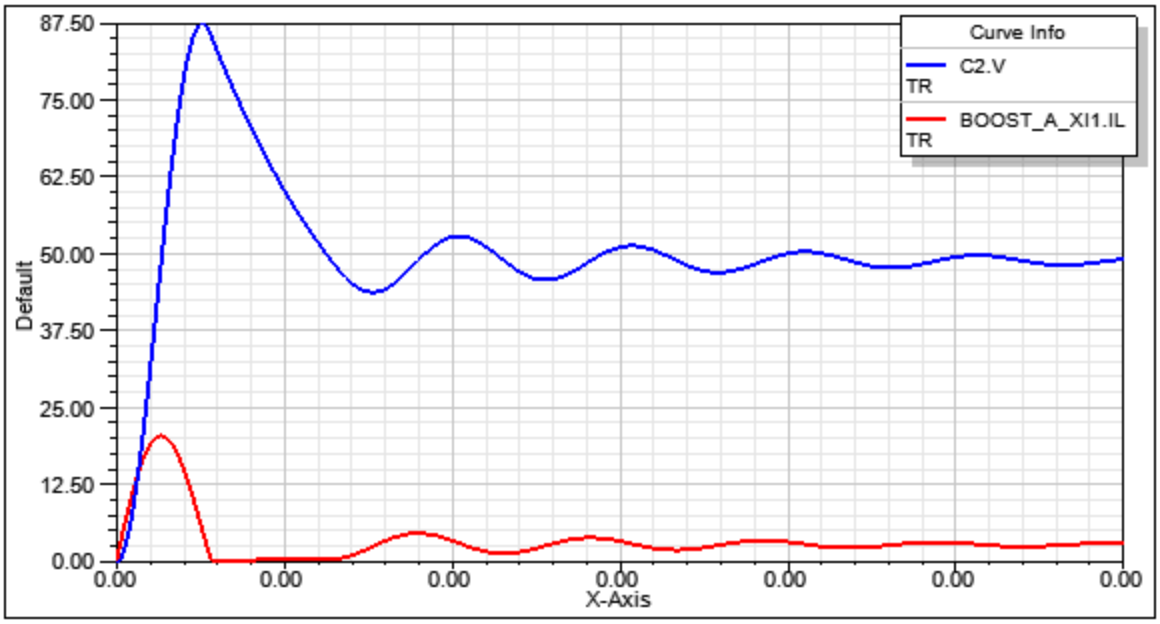

Figure 4. Simulation results-Output current (BOOST_A_XI1.IL) and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Boost Converter wir Synchronous Rectification

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

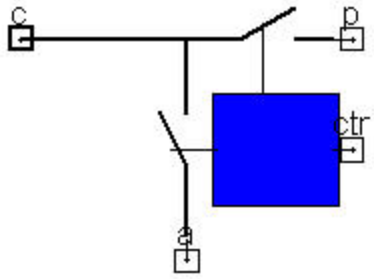

Figure 1. Component symbol

Description

This block represents the averaged model of the Boost converter with synchronous rectification. This component does not have an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

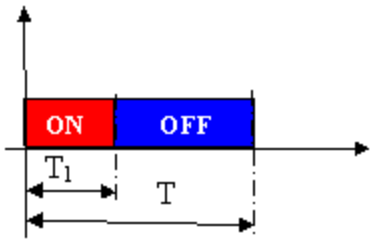

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BOOSTS_A_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Rsa:= @Rsa, Rsp:= @Rsp) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]

Rsa	ON Resistance, Low Side Switch	real	0.01 [Ohm]
Rsp	ON Resistance, High Side Switch	real	0.01 [Ohm]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Boost Converter with Synchronous Rectification for transient, AC, or DC analysis.

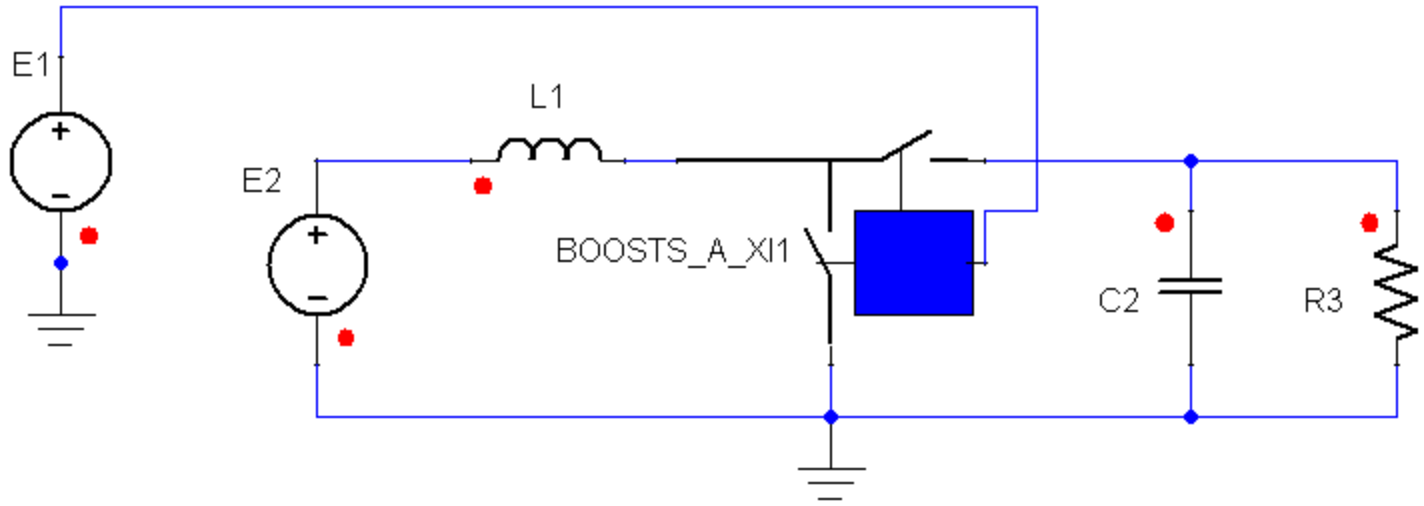

Figure 3. Application example of Non-Ideal Averaged Boost Converter with Synchronous Rectification.

Table 4. System Parameters

Component	Parameter	Value [unit]

Non-Ideal Averaged Boost Converter with Synchronous Rectification BOOSTS_A_XI1	RSA	0.01 [Ohm]
	Rsp	0.01 [Ohm]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L1	L	1e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

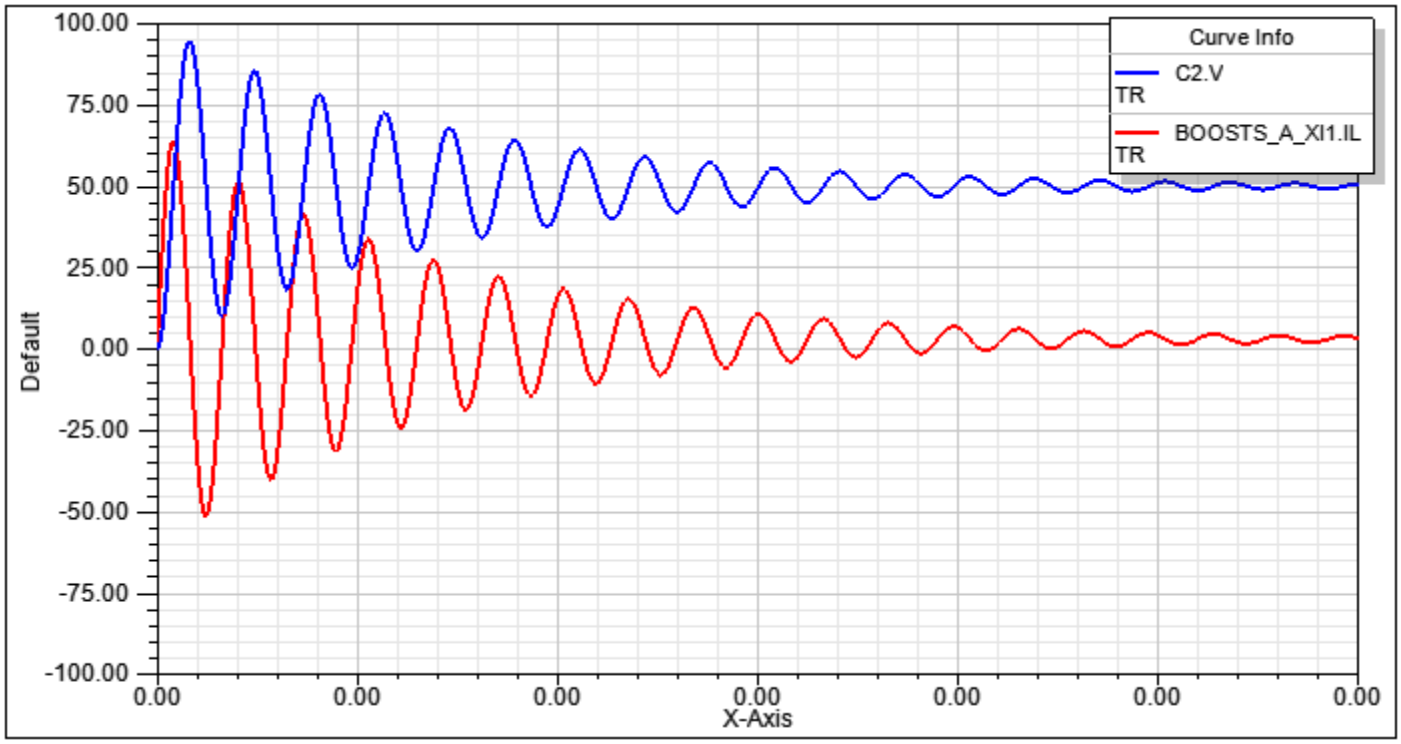

Figure 4. Simulation results-Output current (BOOSTS_A_XI1.IL) with negative current through inductor, and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Buck Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

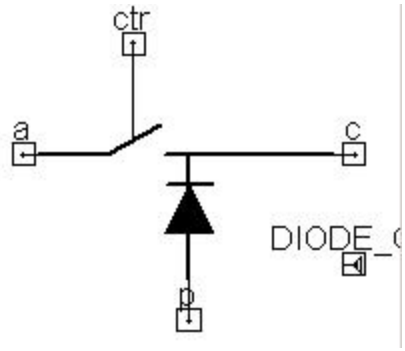

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter. It does not have an internal inductance.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

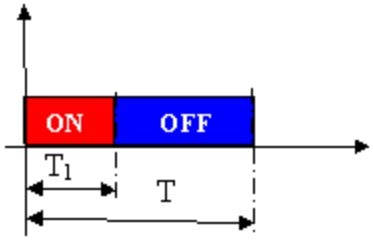

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCK_A_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L_EXT:= @L_EXT, DIODE_CH:= @DIODE_CH, Rsa:= @Rsa) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L_EXT	Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Active Switch Conduction Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristics	real	

Top

Example

This example shows an averaged model of an Non-Ideal Buck Converter for transient, AC, or DC analysis.

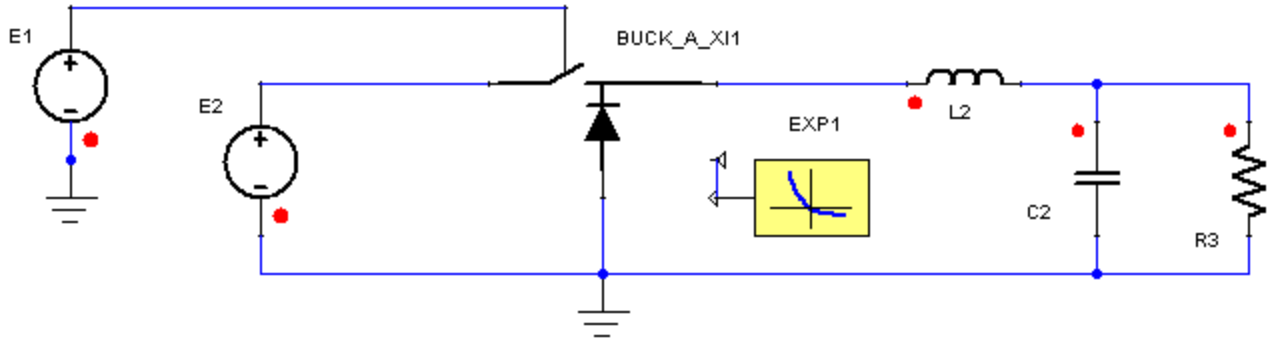

Figure 3. Application example of Non-Ideal Averaged Buck Converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Buck Converter BUCK_A_XI1	L_EXT	3e-005 [H]
	Diode_CH	EXP1.VAL

Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

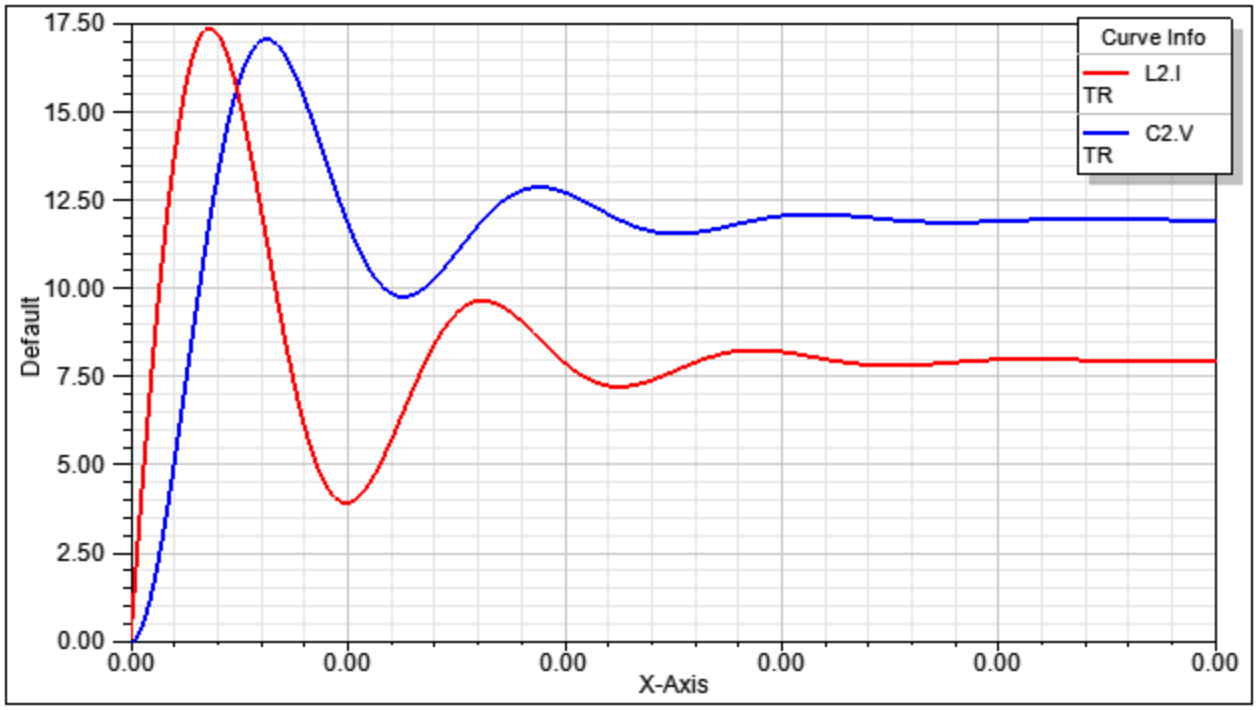

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Buck Sync Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

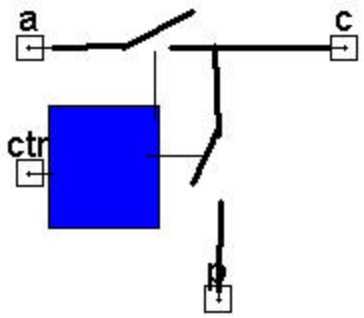

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter with synchronous rectification. It does not have an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

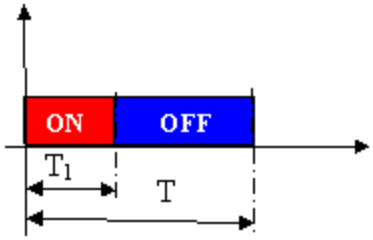

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCKS_A_XI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Rsp:= @Rsp, Rsa:= @Rsa) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Rsp	On-Resistance, Low Side Switch	real	0.01 [Ohm]
Rsa	On-Resistance, High Side Switch	real	0.01 [Ohm]

Top

Example

This example shows an averaged model of an Non-Ideal Synchronous Buck Converter for transient, AC, or DC analysis.

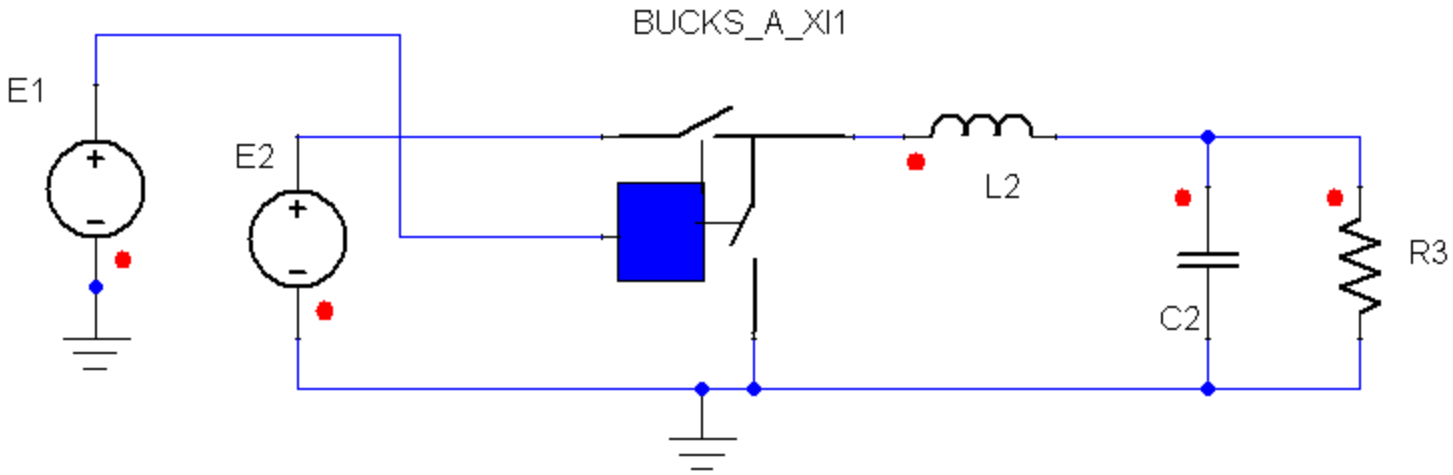

Figure 3. Application example of Non-Ideal Averaged Synchronous Buck Converter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Buck Sync Converter BUCKS_A_XI1	Rsp	0.01 [Ohm]
	Rsa	0.01

		[Ohm]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

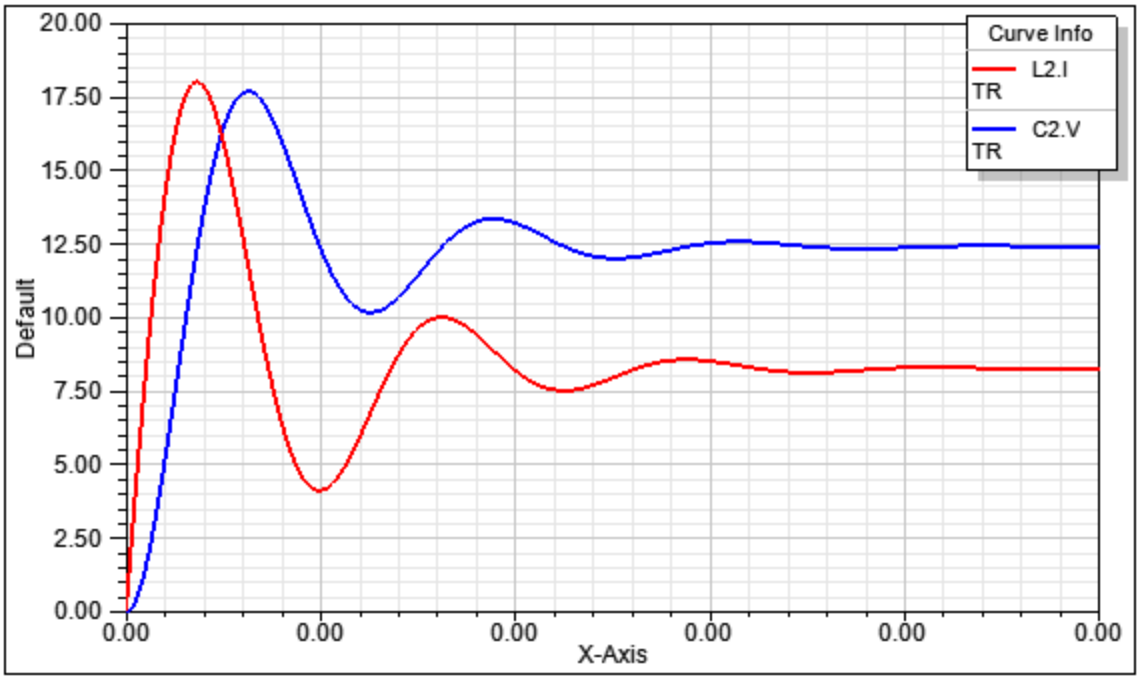

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal Inductor (BUCK_	Boost with Internal Inductor (BOOST_A_II)

	AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Non-Ideal Averaged Buck-Boost Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

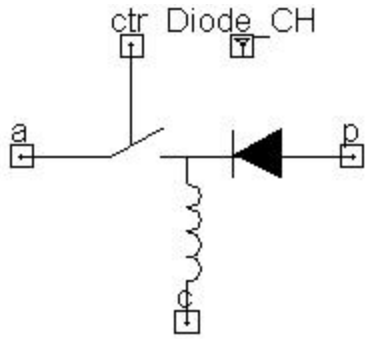

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck-Boost converter. This model includes an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

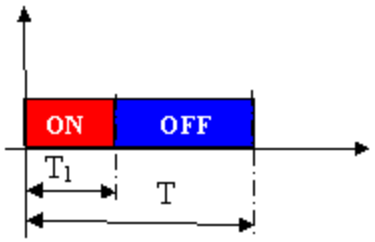

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BBOOST_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data	Default Value

		Type	[Unit]
L	Filter Inductance	real	1e-5 [H]
Fs	Switching Frequency	real	100000 [Hz]
L_IC	Inductor Initial Current	real	0.001 [A]
Rsa	Active Switch ON Resist-ance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Buck-Boost Converter with Internal Inductor for transient, AC, or DC analysis.

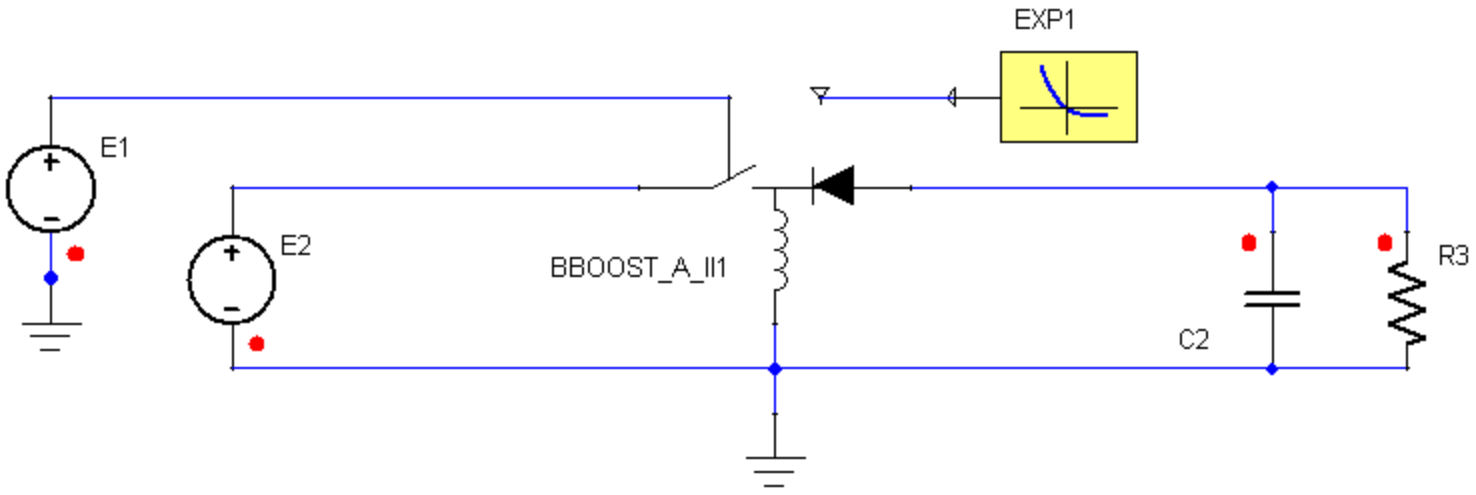

Figure 3. Application example of Non-Ideal Averaged Buck-Boost Converter with Internal Inductor.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Buck-Boost Converter with Internal Inductor BBOOST_A_II1	L	1e-005 [H]
	L_IC	0.01 [A]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

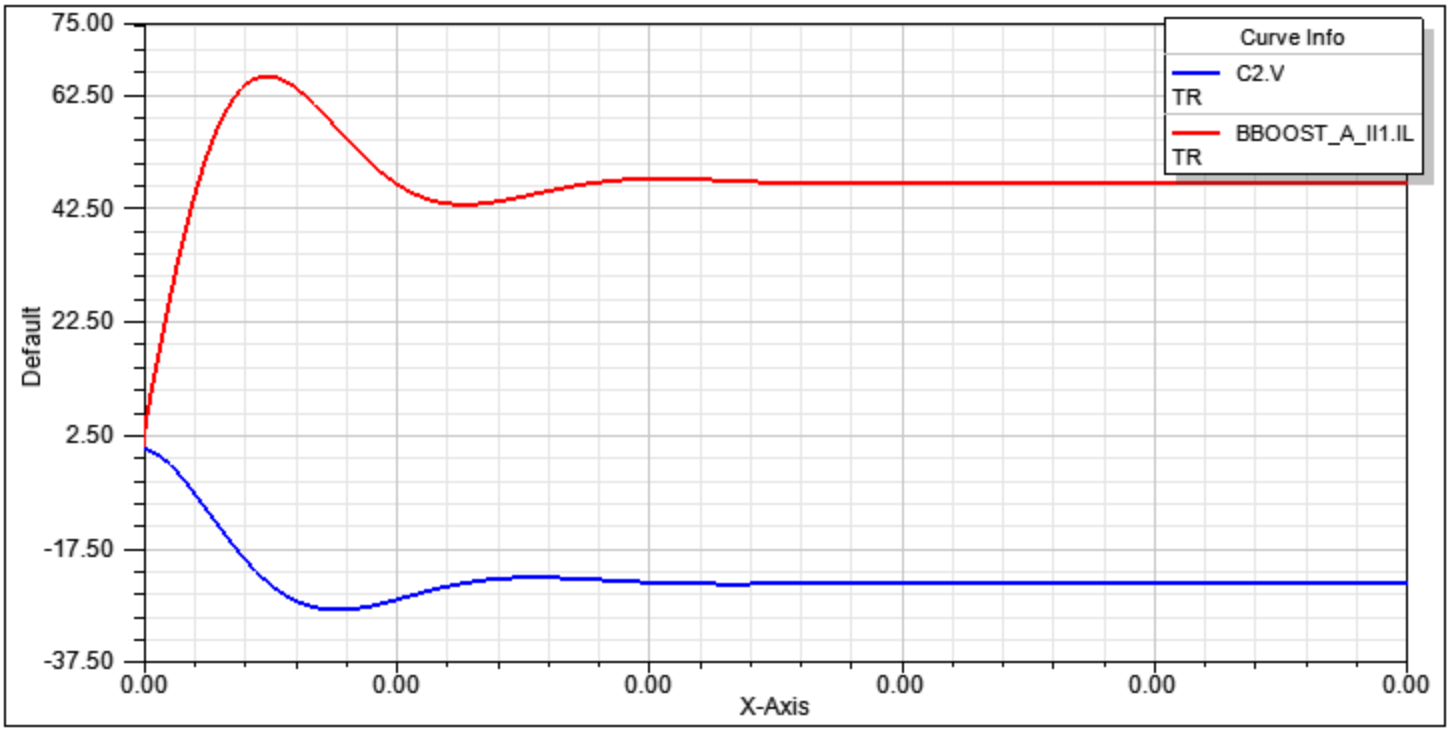

Figure 4. Simulation results-Output current (BBOOST_A_II1.IL), and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Buck-Boost Converter With Synchronous Rectification and Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

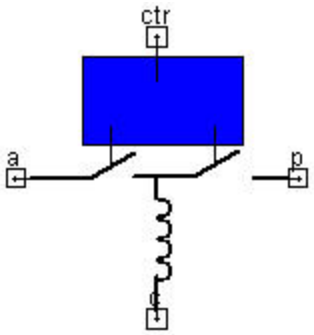

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck-Boost converter with synchronous rectification. This model includes an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

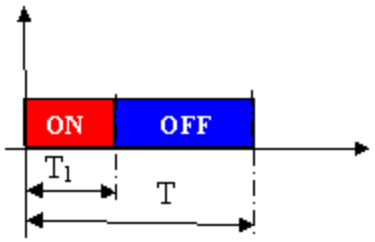

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BBOOSTS_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (L:= @L, L_IC:= @L_IC, Rsa:= @Rsa, Rsp:= @Rsp) SRC: DB(Lib:-:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data	Default Value

		Type	[Unit]
L	Filter Inductance	real	1e-5 [H]
L_IC	Inductor Initial Current	real	0.001 [A]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
Rsp	Passive Switch ON Resistance	real	0.01 [Ohm]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Buck-Boost Converter with Internal Inductor and Synchronous Rectification for transient, AC, or DC analysis.

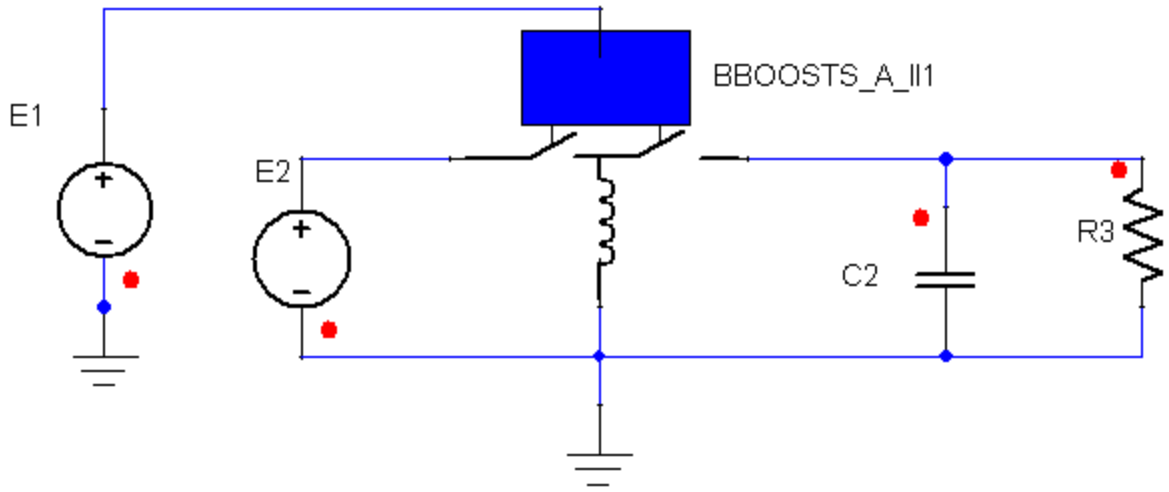

Figure 3. Application example of Non-Ideal Averaged Buck-Boost Converter with Internal Inductor and Synchronous Rectification.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Buck-Boost Converter with Internal Inductor and Sync Rectification BBOOSTS_A_II1	L	1e-005 [H]
	L_IC	0.001 [A]
	Rsa/Rsp	0.01 [Ohm]
Resistor R3	R	1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

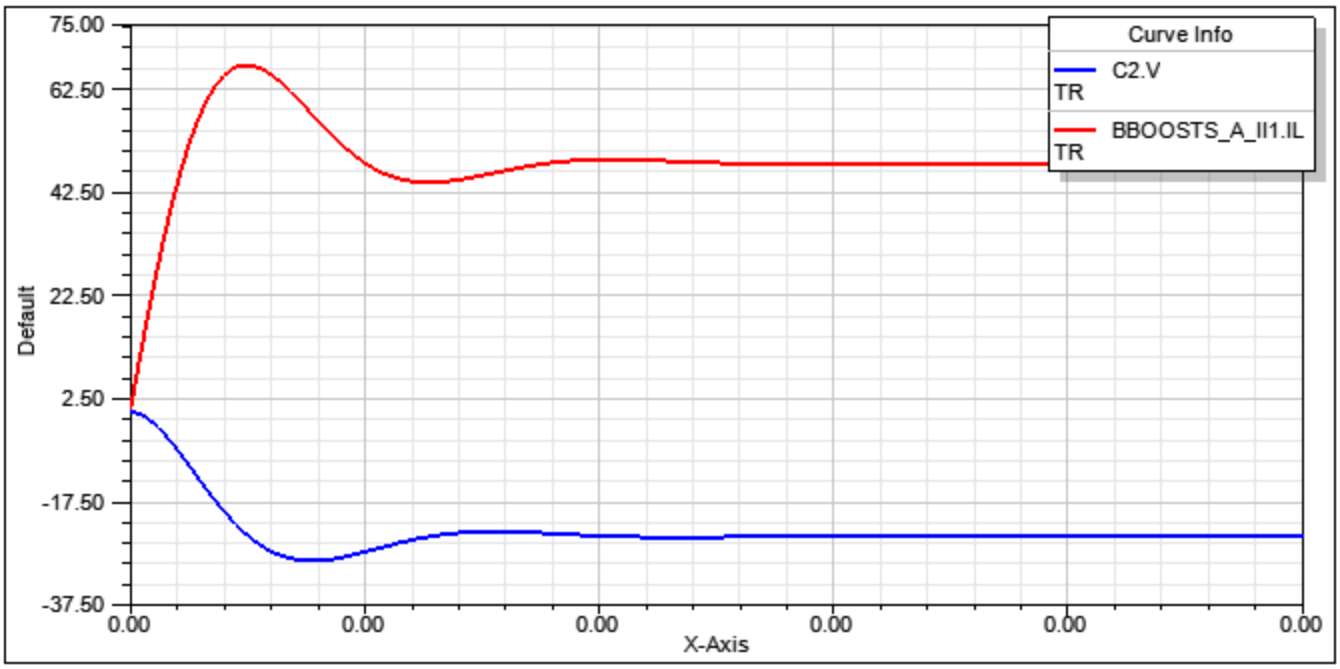

Figure 4. Simulation results-Output current (BBOOSTS_A_Il1.IL), and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Boost Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

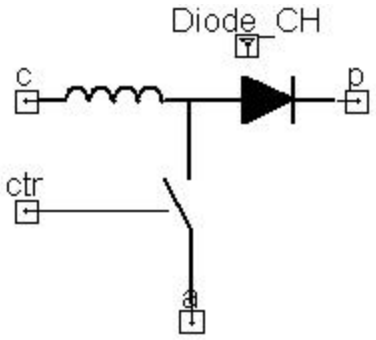

Figure 1. Component symbol

Description

This block represents the averaged model of the Boost converter. This model includes an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

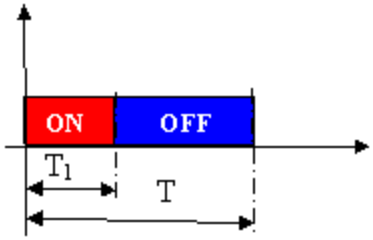

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BOOST_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Rsa:= @Rsa, Diode_CH:= @Diode_CH) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Filter Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]

L_IC	Inductor Initial Current	real	0.0001 [A]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Boost Converter with Internal Inductor for transient, AC, or DC analysis.

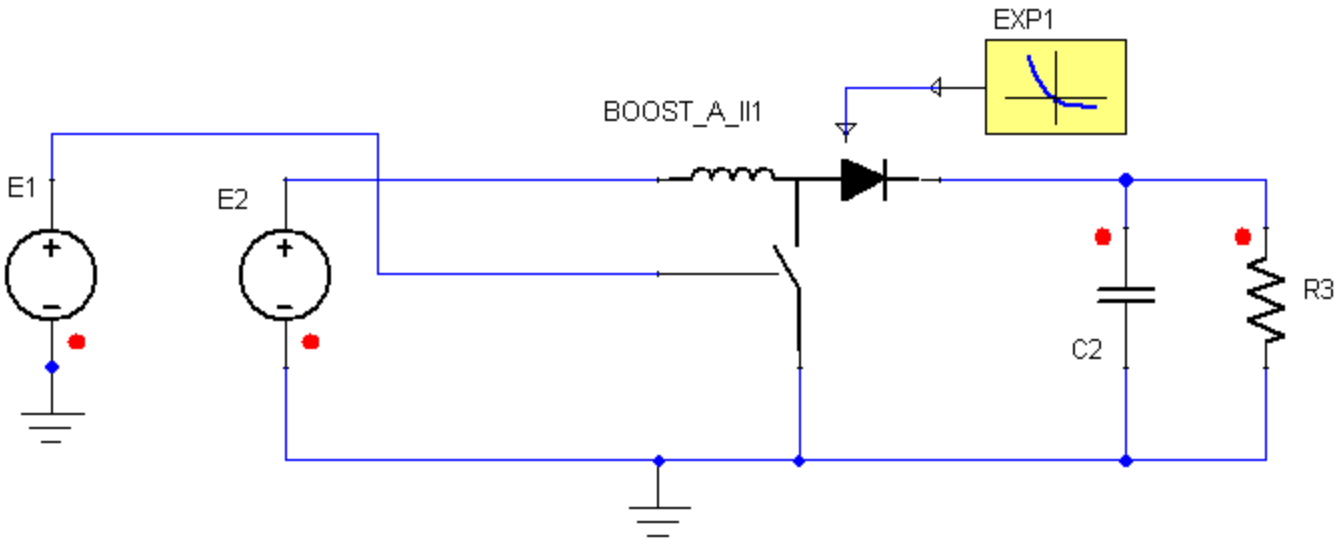

Figure 3. Application example of Non-Ideal Averaged Boost Converter with Internal Inductor.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Boost Converter with Internal Inductor BOOST_A_II1	L	0.0001 [H]
	L_IC	0.001 [A]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

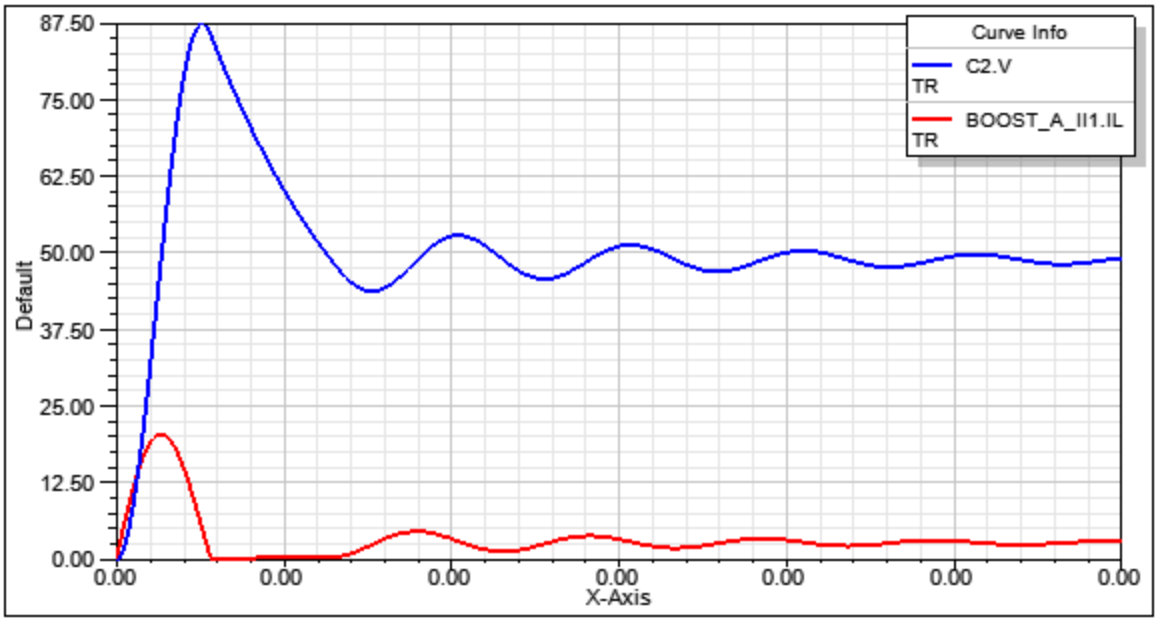

Figure 4. Simulation results-Output current (BOOST_A_Il1.IL), and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Boost Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

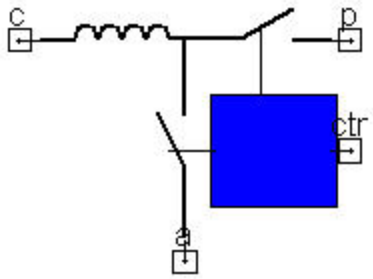

Figure 1. Component symbol

Description

This block represents the averaged model of the Boost converter with synchronous rectification. This model includes an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

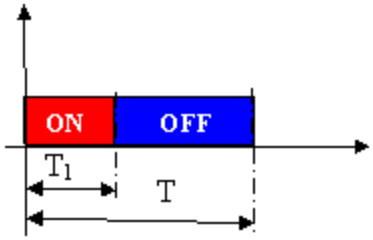

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BOOSTS_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Rsa:= @Rsa, Rsp:= @Rsp, L:= @L, L_IC:= @L_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Filter Inductance	real	1e-5 [H]
L_IC	Inductor Initial Current	real	0.001 [A]
Rsa	ON Resistance, Low Side Switch	real	0.01 [Ohm]
Rsp	ON Resistance, High Side Switch	real	0.01 [Ohm]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows an averaged model of an Non-Ideal Boost Converter with Internal Inductor and Synchronous Rectification for transient, AC, or DC analysis.

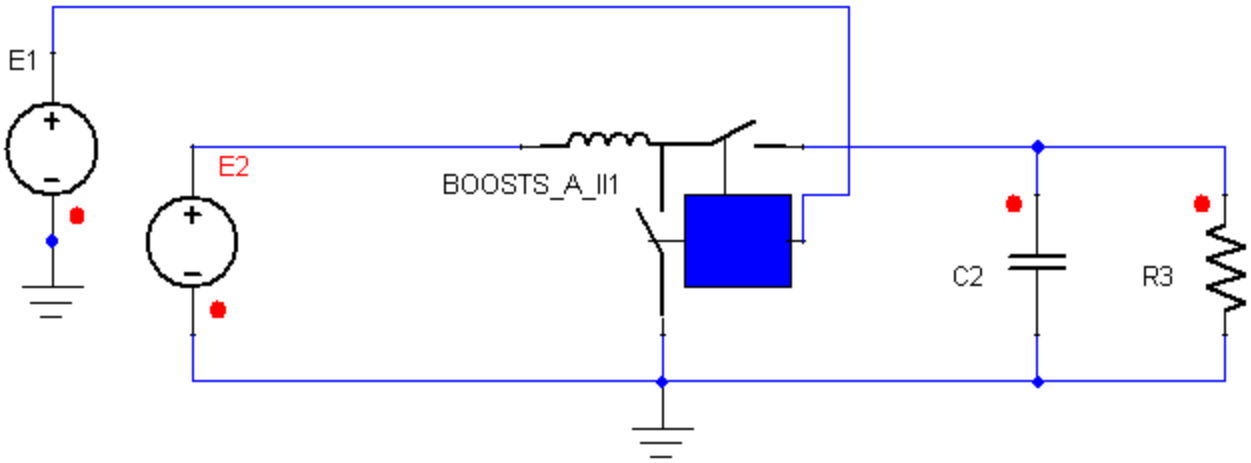

Figure 3. Application example of Non-Ideal Averaged Boost Converter with Internal Inductor and Synchronous Rectification .

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Boost Converter with Internal Inductor and Synchronous Rectification BOOSTS_A_II1	L	1e-005 [H]
	L_IC	0.001 [A]
	RSA/RSP	0.01 [Ohm]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

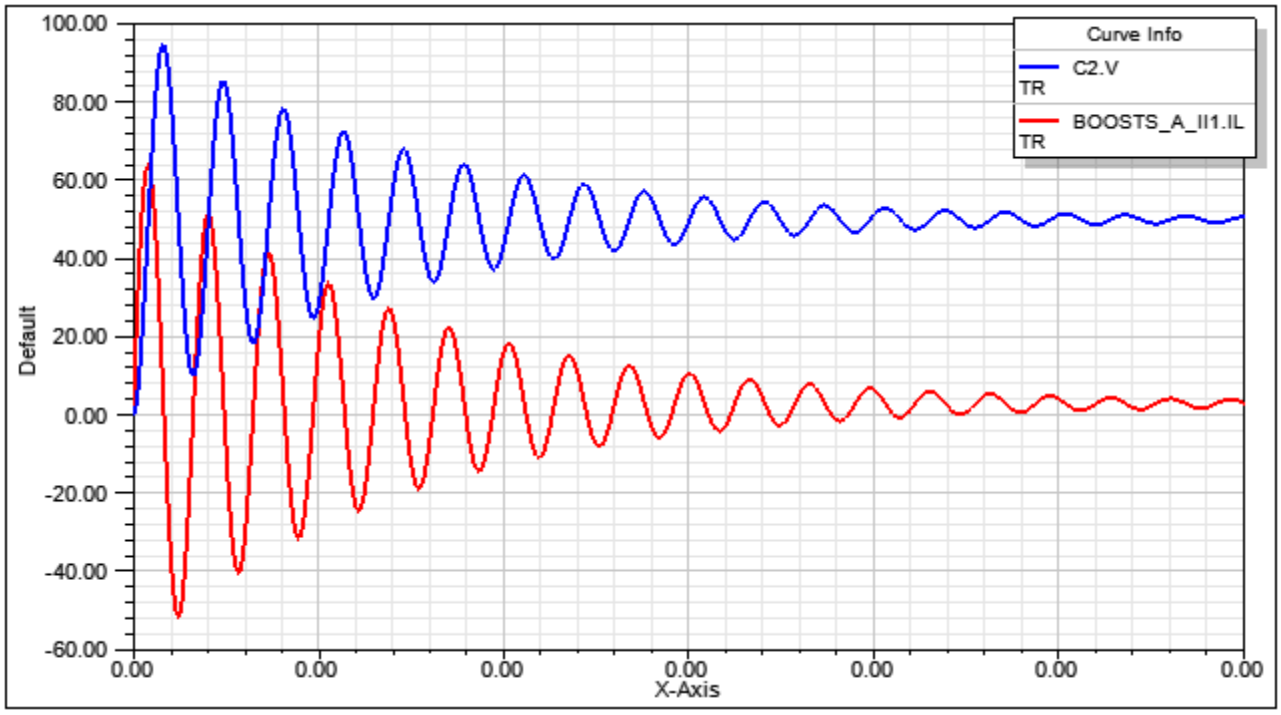

Figure 4. Simulation results-Output current (BOOSTS_A_II1.IL) which may be negative, and Output Voltage (C2.V).

Top

References

Non-Ideal Averaged Buck Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

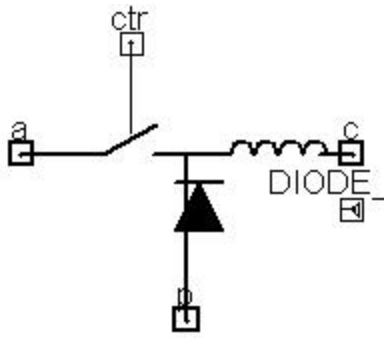

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter. This model includes an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

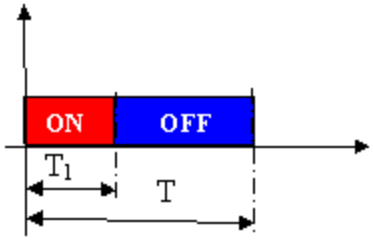

Figure 2. Duty Cycle Calculation

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Netlist Syntax

MODEL BUCK_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, DIODE_CH:= @DIODE_CH, Rsa:= @Rsa) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Filter Inductance	real	1e-4 [H]
Fs	Switching Frequency	real	100000 [Hz]

L_IC	Inductor Initial Current	real	0 [A]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

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Example

This example shows an averaged model of an Non-Ideal Buck Converter with Internal Inductor for transient, AC, or DC analysis.

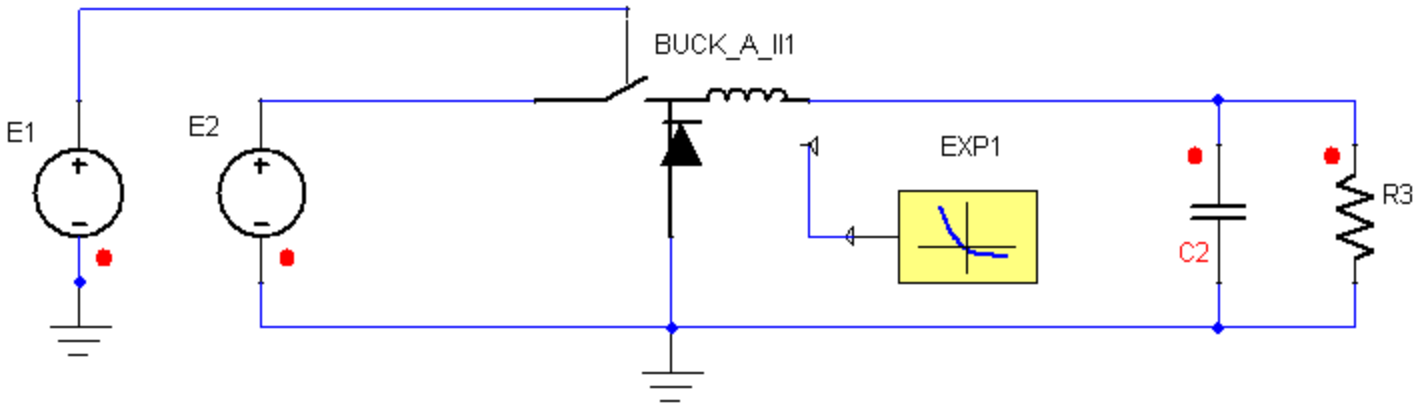

Figure 3. Application example of Non-Ideal Averaged Buck Converter with Internal Inductor.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Buck Converter	L	3e-005 [H]

with Internal Inductor BUCK_A_II1		
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

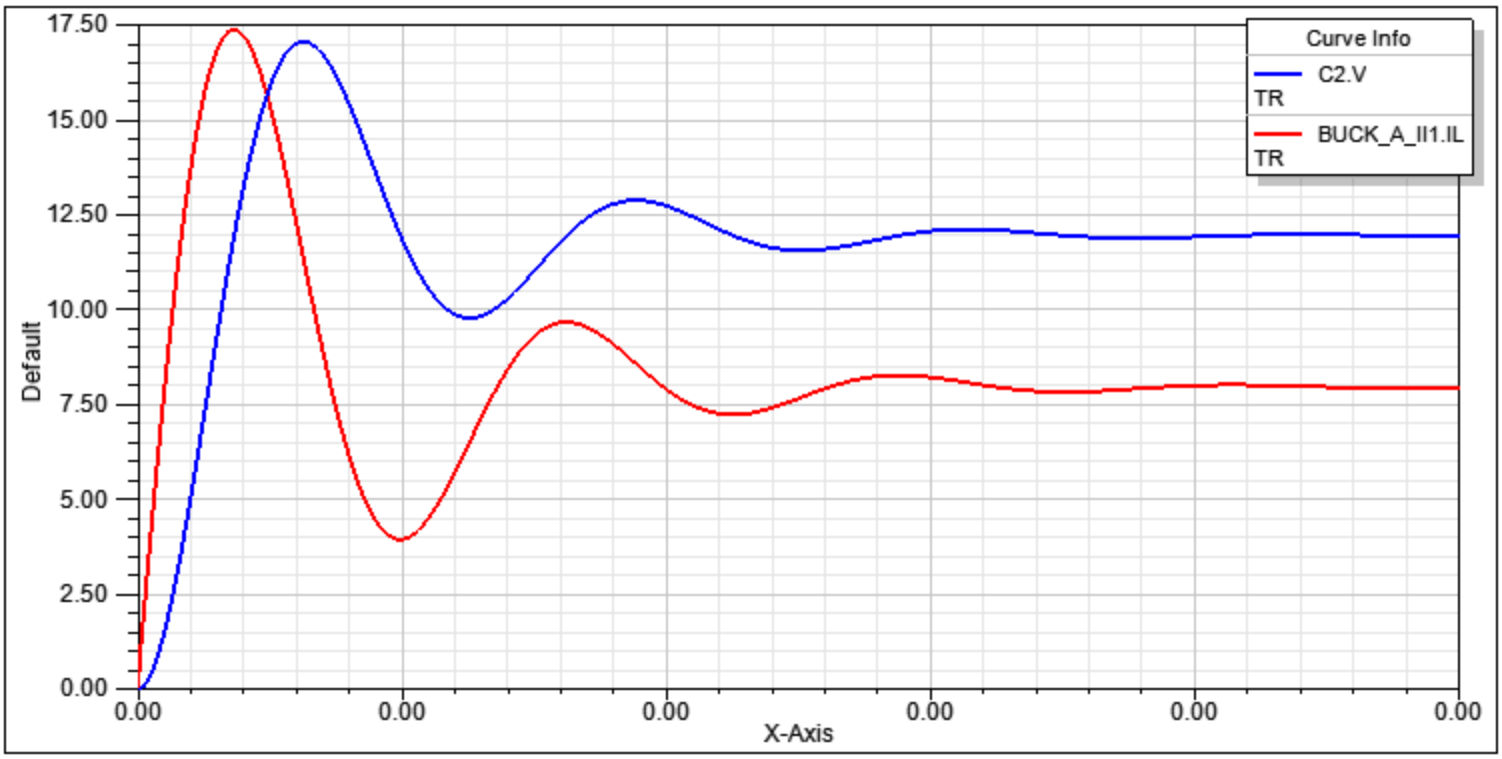

Figure 4. Simulation results-Output current (BUCK_A_II1.IL), and Output Voltage (C2.V).

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References

Non-Ideal Averaged Buck Sync Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

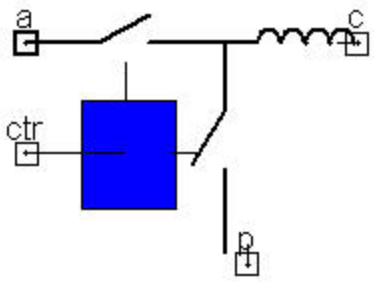

Figure 1. Component symbol

Description

This block represents the averaged model of the Buck converter with synchronous rectification. This model includes an internal inductor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

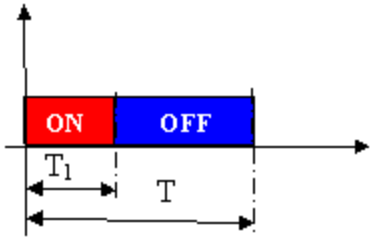

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCKS_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Rsp:= @Rsp, Rsa:= @Rsa, L:= @L, L_IC:= @L_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
L	Filter Inductance	real	1e-5 [H]
L_IC	Inductor Initial Current	real	0.01 [A]
Rsp	ON Resistance, Low Side Switch	real	0.01 [Ohm]
Rsa	ON Resistance, High Side Switch	real	0.01 [Ohm]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

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Example

This example shows an averaged model of an Non-Ideal Synchronous Buck Converter with Internal Inductor for transient, AC, or DC analysis.

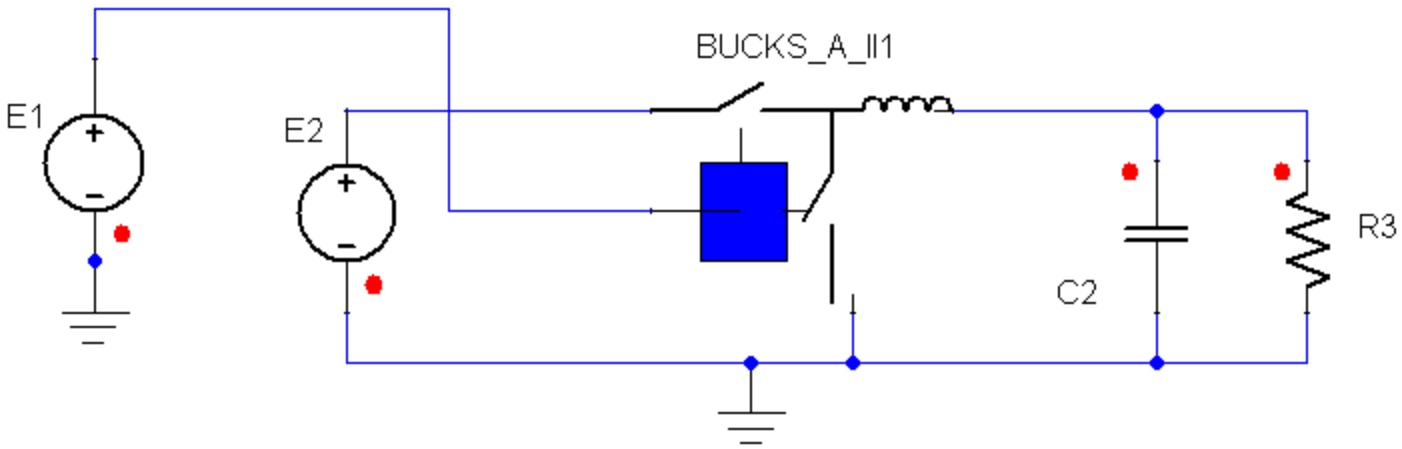

Figure 3. Application example of Non-Ideal Averaged Synchronous Buck Converter with Internal Inductor.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged Synchronous Buck Converter with Internal Inductor BUCKS_A_II1	L	3e-005 [H]
	L_IC	0.01 [A]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

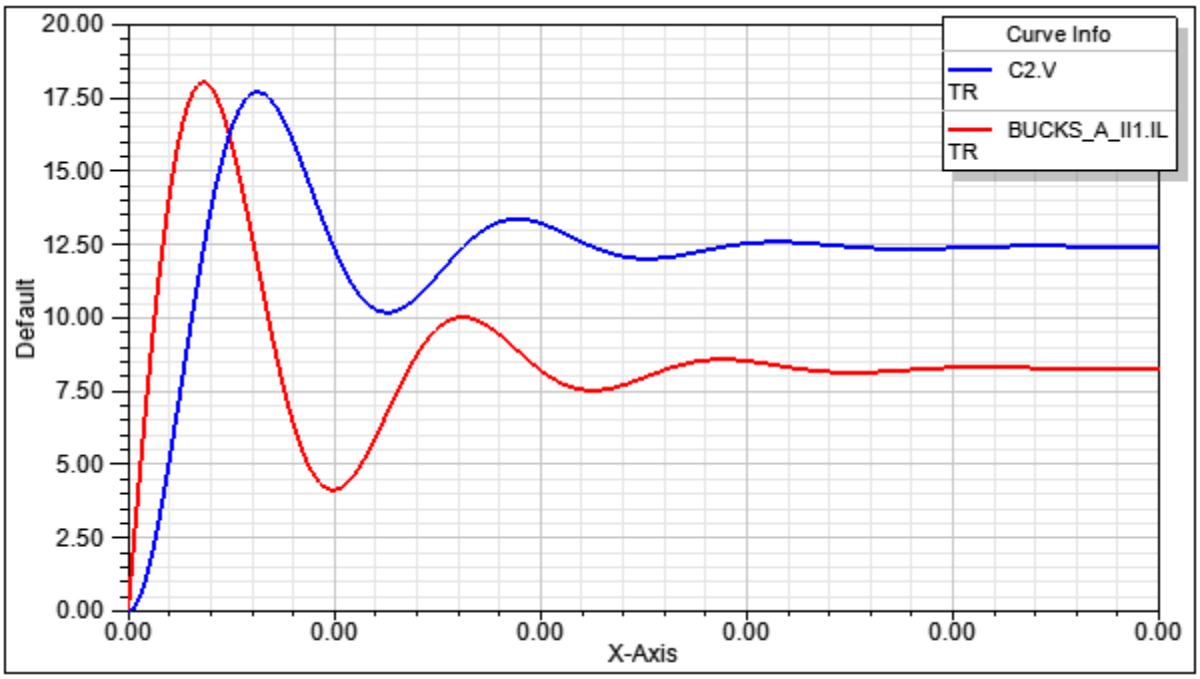

Figure 4. Simulation results-Output current (BUCKS_A_II1.IL), and Output Voltage (C2.V).

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References

Non-Ideal Averaged Cuk Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

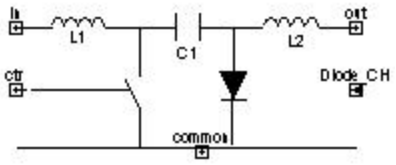

Figure 1. Component symbol

Description

This block represents the averaged model of the Cuk converter. The model also includes the inductors of the Cuk converter and the capacitor.

Top

Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

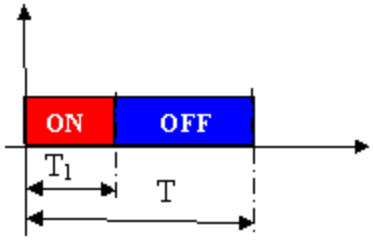

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL CUK_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) in:= %0, out:= %1, common:= %2, ctr:= %3 (Fs:= @Fs, L1:= @L1, L1_IC:= @L1_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, L2:= @L2, L2_IC:= @L2_IC, C1:= @C1, C1_IC:= @C1_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
in	input pin (corresponding to the node connected to the input voltage)	Electrical terminal
common	common pin (corresponding to the node connected to common terminal)	Electrical terminal
out	output pin (corresponding to the node connected to the output load)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]

L1	Inductance 1	real	1e-5 [H]
L2	Inductance 2	real	1e-5 [H]
L1_IC	Inductor 1 Initial Current	real	0.001 [A]
L2_IC	Inductor 2 Initial Current	real	0.001 [A]
C1	Capacitance	real	1e-4 [F]
C1_IC	Capacitor Initial Condition	real	0 [V]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL1	Inductor 1 Current [A]	Output	real
IL2	Inductor 2 Current [A]	Output	real
VC1	Capacitor Voltage [V]	Output	real

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Example

This example shows an averaged model of an Non-Ideal CUK Converter with Internal Inductor for transient, AC, or DC analysis.

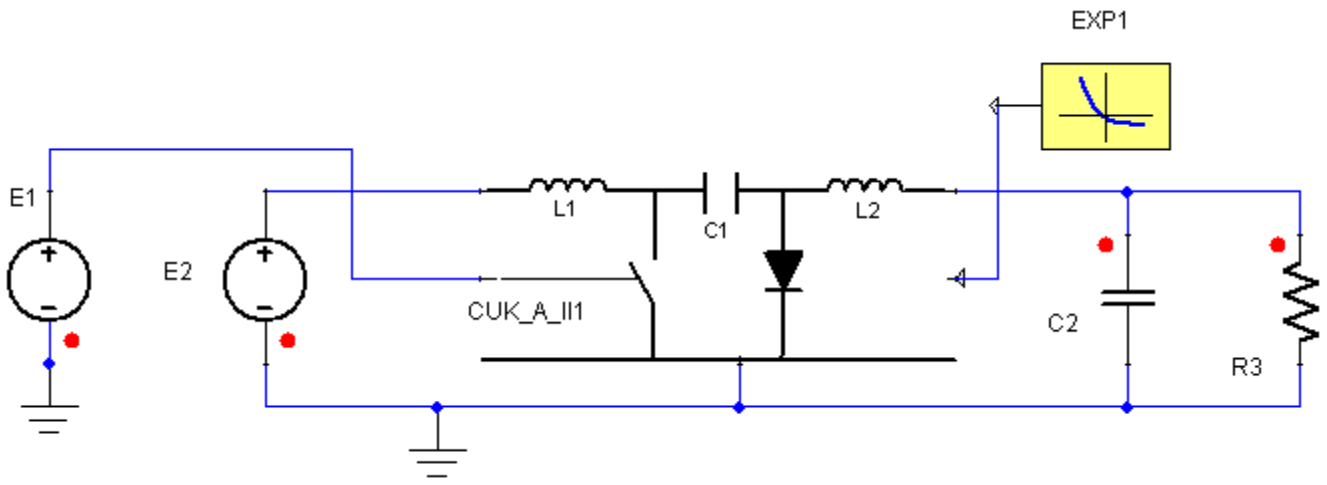

Figure 3. Application example of Non-Ideal Averaged CUK Converter with Internal Inductor.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged CUK Converter with Internal Inductor CUK_A_II1	L	1e-005 [H]
	L_IC	0.001 [A]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

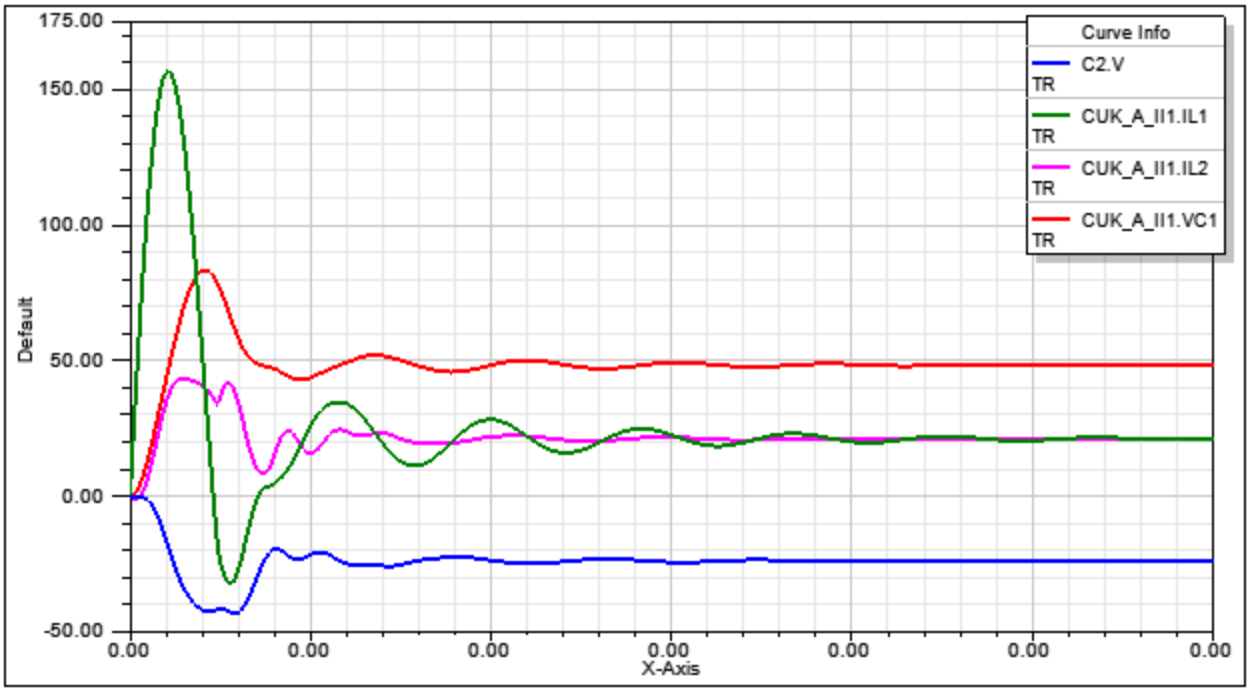

Figure 4. Simulation results-Inductor currents (CUK_A_II1.IL1, CUK_A_II1.IL2), Capacitor Voltage (CUK_A_II1.VC1) and Output Voltage (C2.V).

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References

Non-Ideal Averaged Sepic Converter With Internal Inductor

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

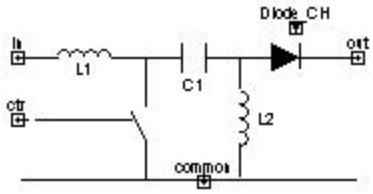

Figure 1. Component symbol

Description

This block represents the averaged model of the Sepic converter. The model also includes the inductors of the Sepic converter and the capacitor.

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Assumptions and Limitations

This model accounts for conduction losses in the switches. The model is valid for both conduction modes of operation. It automatically detects the change in the mode of operation.

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Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

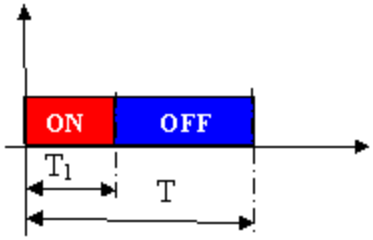

Figure 2. Duty Cycle Calculation

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Netlist Syntax

MODEL SEPIC_A_II ?InstanceName(@InstanceName):(@(Refbase)@(ID)) in:= %0, out:= %1, common:= %2, ctr:= %3 (Fs:= @Fs, L1:= @L1, L1_IC:= @L1_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, L2:= @L2, L2_IC:= @L2_IC, C1:= @C1, C1_IC:= @C1_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
in	input pin (corresponding to the node connected to the input voltage)	Electrical terminal
common	common pin (corresponding to the node connected to common terminal)	Electrical terminal
out	output pin (corresponding to the node connected to the output load)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]

L1	Inductance 1	real	1e-5 [H]
L2	Inductance 2	real	1e-5 [H]
L1_IC	Inductor 1 Initial Current	real	0.001 [A]
L2_IC	Inductor 2 Initial Current	real	0.001 [A]
C1	Capacitance	real	1e-4 [F]
C1_IC	Capacitor Initial Condition	real	0 [V]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
DIODE_CH	Diode Characteristic	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL1	Inductor 1 Current [A]	Output	real
IL2	Inductor 2 Current [A]	Output	real
VC1	Capacitor Voltage [V]	Output	real

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Example

This example shows an averaged model of an Non-Ideal SEPIC Converter with Internal Inductor for transient, AC, or DC analysis.

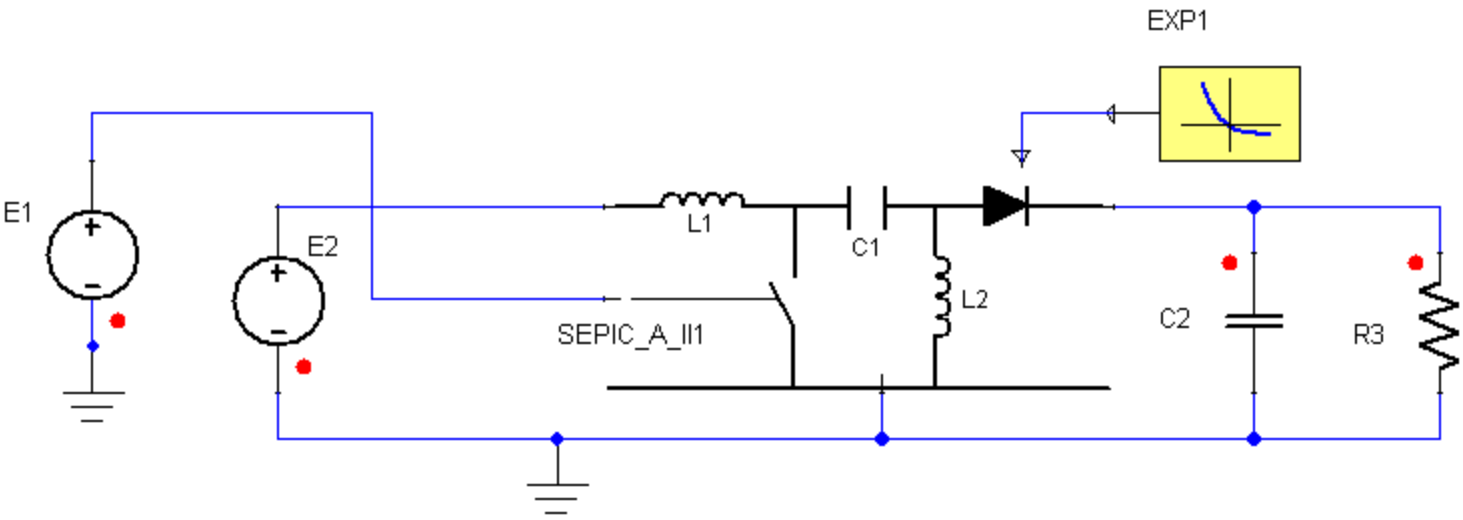

Figure 3. Application example of Non-Ideal Averaged SEPIC Converter with Internal Inductor.

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Ideal Averaged SEPIC Converter with Internal Inductor SEPIC _A_II1	L	1e-005 [H]
	L_IC	0.001 [A]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

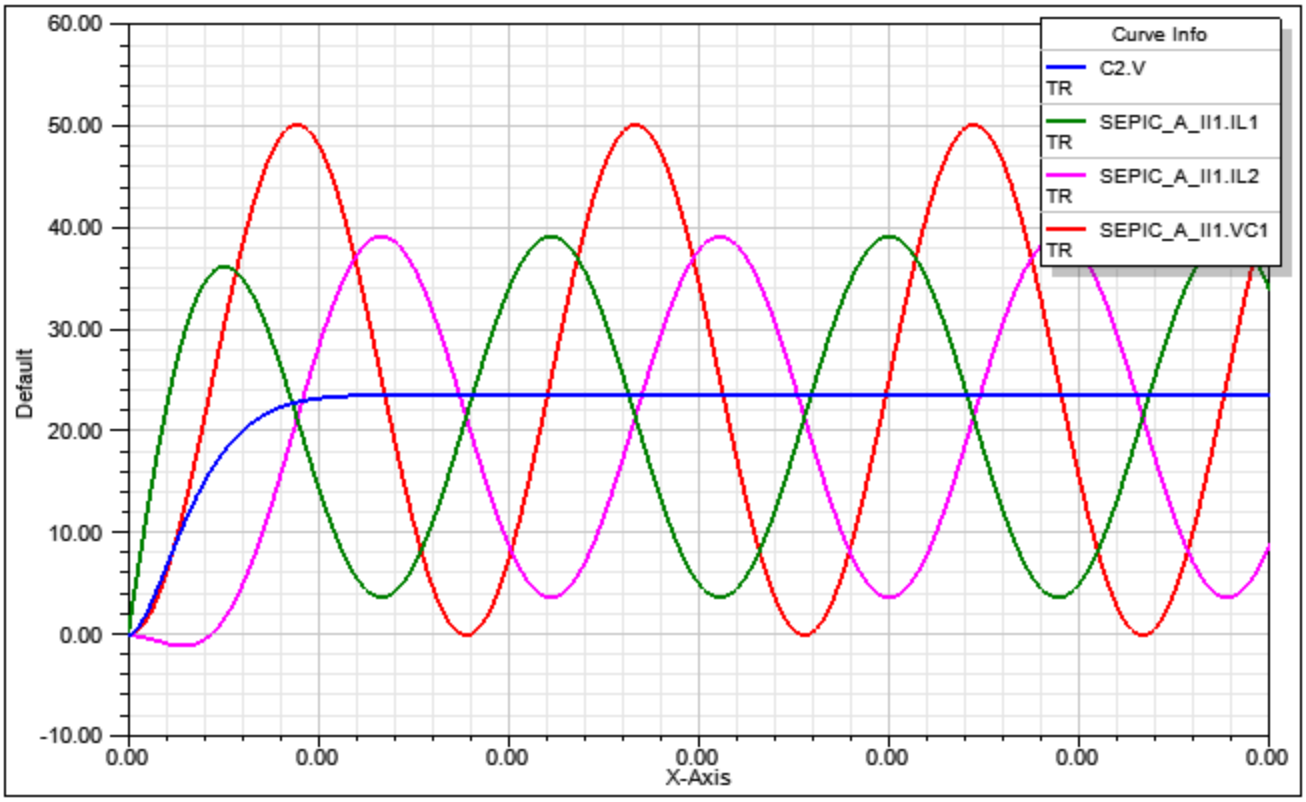

Figure 4. Simulation results-Inductor currents (SEPIC_A_II1.IL1, SEPIC_A_II1.IL2), Capacitor Voltage (SEPIC_A_II1.VC1) and Output Voltage (C2.V).

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References

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal	Boost with Internal Inductor (BOOST_A_II)

	Inductor (BUCK_AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal	Boost with Internal Inductor (BOOST_A_II)

	Inductor (BUCK_AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Switch Level Two Output FORWARD Converter with Active Clamp and Output Filter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

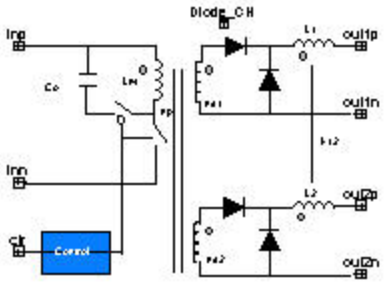

Figure 1. Component symbol

Description

This block represents the switch level model of the Forward with Active Clamp converter with two outputs.

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Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques. The model also includes the clamp capacitor, the magnetizing inductance of the transformer referred to primary and the output filter coupled inductors. This model is also valid for non coupled output filter inductors setting the coupling coefficient, k12, to zero.

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Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

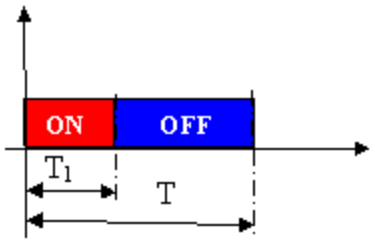

Figure 2. Duty Cycle Calculation

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Netlist Syntax

MODEL FAC_2out_Lf_SW ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, out1p:= %2, ctr:= %3, out1n:= %4, out2p:= %5, out2n:= %6 (Fs:= @Fs, np:= @np, ns1:= @ns1, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Lm:= @Lm, Lm_IC:= @Lm_IC, Co:= @Co, Co_IC:= @Co_IC, ns2:= @ns2, L1:= @L1, L2:= @L2, k12:= @k12, L1_IC:= @L1_IC, L2_IC:= @L2_IC) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	Positive input pin	Electrical terminal
inn	Negative input pin	Electrical terminal
out1_p	Positive output 1 pin	Electrical terminal
out1_n	Negative output 1 pin	Electrical terminal
out2_p	Positive output 2 pin	Electrical terminal
out2_n	Negative output 2 pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Primary Switch ON Resistance	real	0.01 [Ohm]
np	Primary Number of Turns	real	1
ns1	Secondary 1 Number of Turns	real	1
ns2	Secondary 2 Number of Turns	real	1
DIODE_CH	Diode Characteristic	real	
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]
Co	Clamping Capacitor Value	real	0.0001 [F]
Co_IC	Clamping Capacitor Initial Condition	real	0 [V]
L1	Output Filter 1 Inductor Value	real	1e-5 [H]
L2	Output Filter 2 Inductor Value	real	1e-5 [H]
L1_IC	Output Filter 1 Inductor Initial Condition	real	0.001 [A]
L2_IC	Output Filter 2 Inductor Initial Condition	real	0.001 [A]
k12	Output Filter Inductors Coupling Coefficient	real	0

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL1	Output Filter 1 Inductor Current [A]	Output	real
IL2	Output Filter 2 Inductor Current [A]	Output	real

Top

Example

This example shows a device level model of a 2 Output Forward Converter with active clamp and output filter for use in transient analysis.

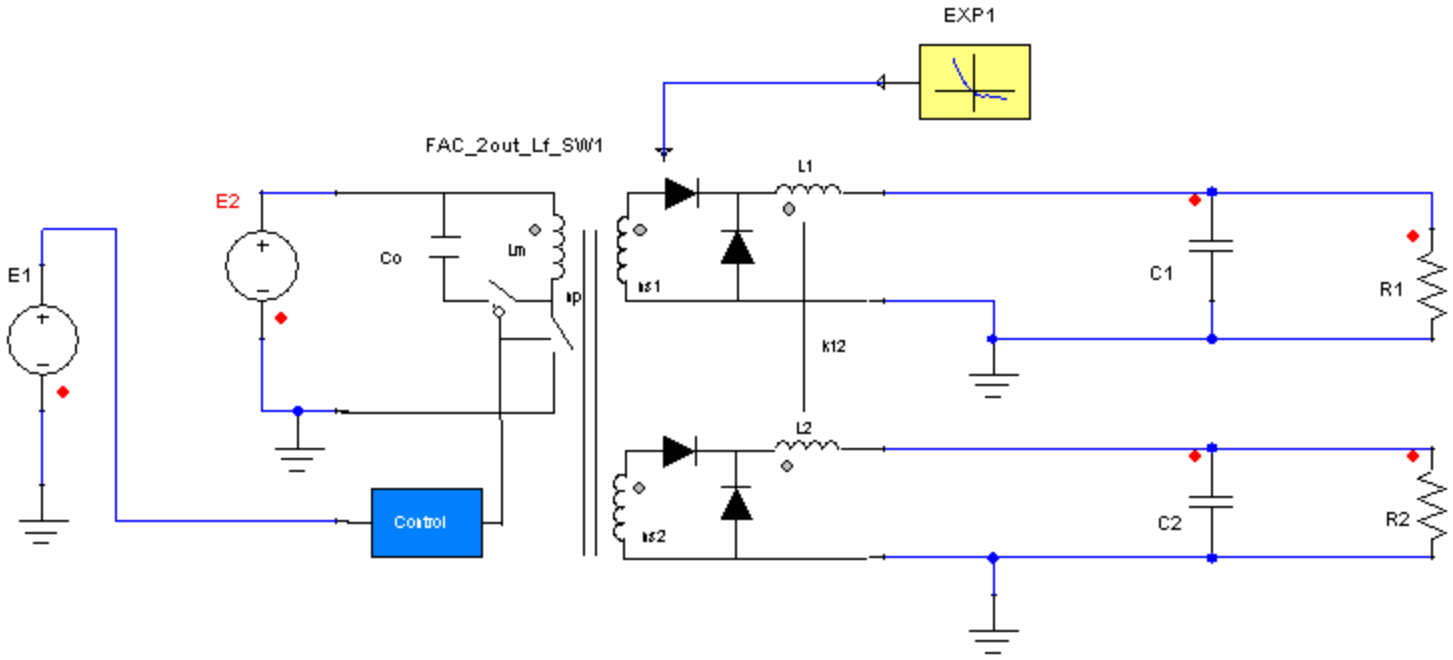

Figure 3. Application example of the Isolated 2 Output Forward Converter with Active Clamp and Output Filter.

Table 3. System Parameters

Component	Parameter	Value [unit]
Isolated 2 Output Forward Converter with Active Clampand Output Filter FAC_2out_LF_SW1	np	1
	n1	1
	n2	1
	Rsa	0.01 [Ohm]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R1	R	1 [Ohm]
Resistor R2	R	10 [Ohm]
Capacitor C1	C	5e-005 [F]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

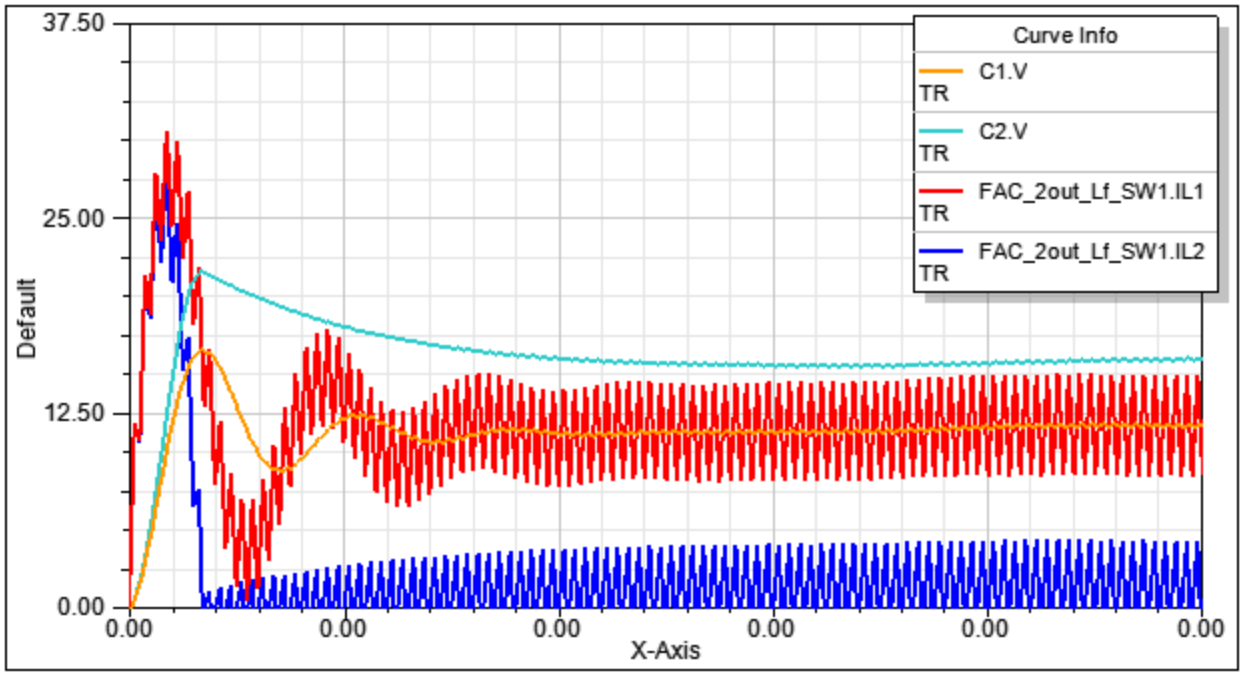

Figure 4. Simulation results-Output currents (FAC_2out_LF_SW1.IL1, FAC_2out_LF_SW1.IL2) and Output Voltages (C1.V, C2.V).

Top

References

Switch Level FORWARD Converter with Active Clamp

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

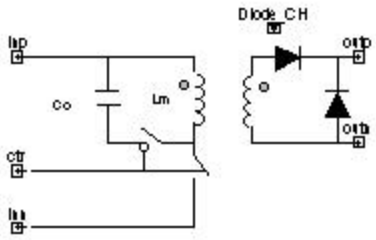

Figure 1. Component symbol

Description

This block represents the switch level model of the Forward with Active Clamp converter.

Top

Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques. The model also includes the clamp capacitor and the magnetizing inductance of the transformer referred to primary.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

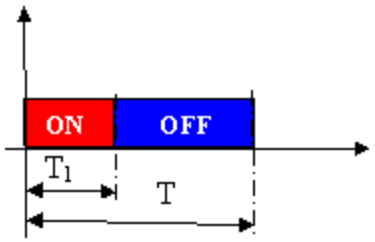

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL FAC_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, ctr:= %3, outn:= %4 (Fs:= @Fs, n1:= @n1, n2:= @n2, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Lm:= @Lm, Lm_IC:= @Lm_IC, Co:= @Co, Co_IC:= @Co_IC) SRC: DB(Lib:-:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	Positive input pin	Electrical terminal
inn	Negative input pin	Electrical terminal
outp	Positive output pin	Electrical terminal
outn	Negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Primary Switch ON Resistance	real	0.01 [Ohm]
n1	Primary Number of Turns	real	1
n2	Secondary Number of Turns	real	1
DIODE_CH	Diode Characteristic	real	
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]
Co	Clamping Capacitor Value	real	0.0001 [F]
Co_IC	Clamping Capacitor Initial Condition	real	0 [V]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
VCo	Clamping Capacitor Voltage [V]	Output	real
ILm	Magnetizing Inductance Current (Primary) [A]	Output	real

Top

Example

This example shows a switch level model of a Forward Converter with active clamp for use in transient analysis.

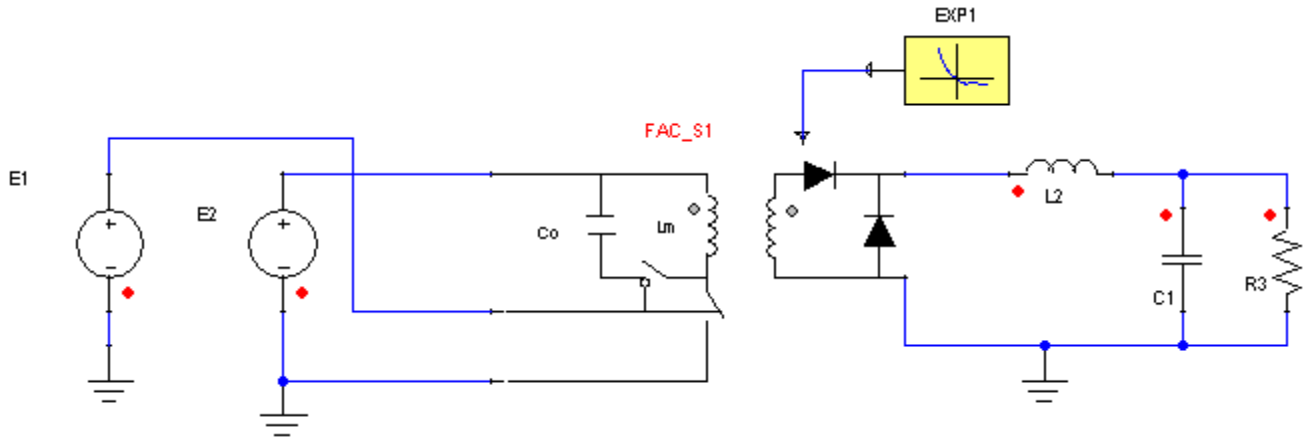

Figure 3. Application example of the Isolated Forward Converter with Active Clamp.

Table 4. System Parameters

Component	Parameter	Value [unit]
Isolated Forward Converter with Active Clamp FAC_S1	n1	1
	n2	1
	Rsa	0.01 [Ohm]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C1	C	5e-005 [F]
Inductor L2	L	3e-005 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

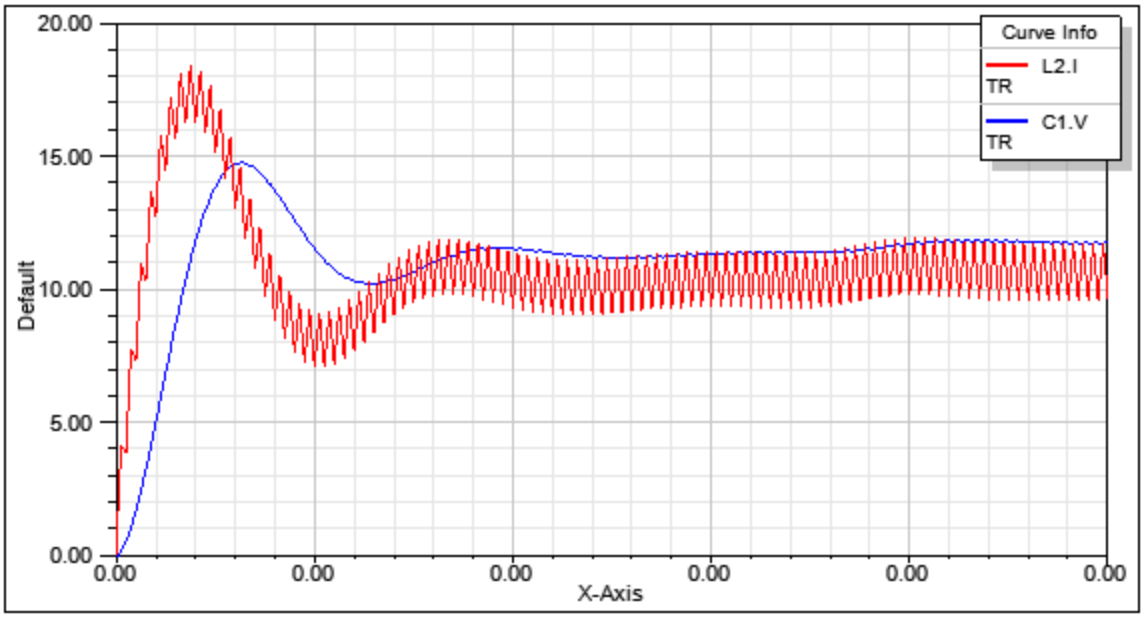

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C1.V).

Top

References

Switch Level Two Output FORWARD Converter with Active Clamp

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

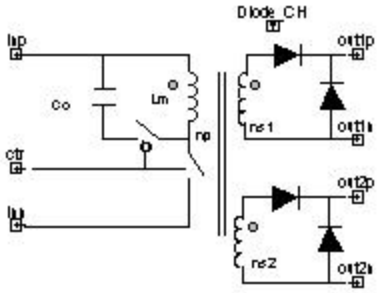

Figure 1. Component symbol

Description

This block represents the switch level model of the Forward with Active Clamp converter with two outputs.

Top

Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques. The model also includes the clamp capacitor, the magnetizing inductance of the transformer referred to primary.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

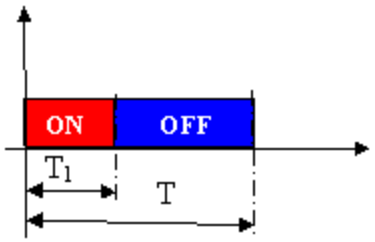

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL FAC2o_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, out1p:= %2, ctr:= %3, out1n:= %4, out2p:= %5, out2n:= %6 (Fs:= @Fs, np:= @np, ns1:= @ns1, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Lm:= @Lm, Lm_IC:= @Lm_IC, Co:= @Co, Co_IC:= @Co_IC, ns2:= @ns2) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	Positive input pin	Electrical terminal
inn	Negative input pin	Electrical terminal
out1_p	Positive output 1 pin	Electrical terminal
out1_n	Negative output 1 pin	Electrical terminal
out2_p	Positive output 2 pin	Electrical terminal
out2_n	Negative output 2 pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Primary Switch ON Resistance	real	0.01 [Ohm]
np	Primary Number of Turns	real	1
ns1	Secondary 1 Number of Turns	real	1
ns2	Secondary 2 Number of Turns	real	1
DIODE_CH	Diode Characteristic	real	
Lm	Magnetizing Inductance (Primary)	real	0.0001 [H]
Lm_IC	Magnetizing Inductance Initial Condition	real	0 [A]
Co	Clamping Capacitor Value	real	0.0001 [F]
Co_IC	Clamping Capacitor Initial Condition	real	0 [V]

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Example

This example shows a switch level model of a 2 Output Forward Converter with active clamp for use in transient analysis.

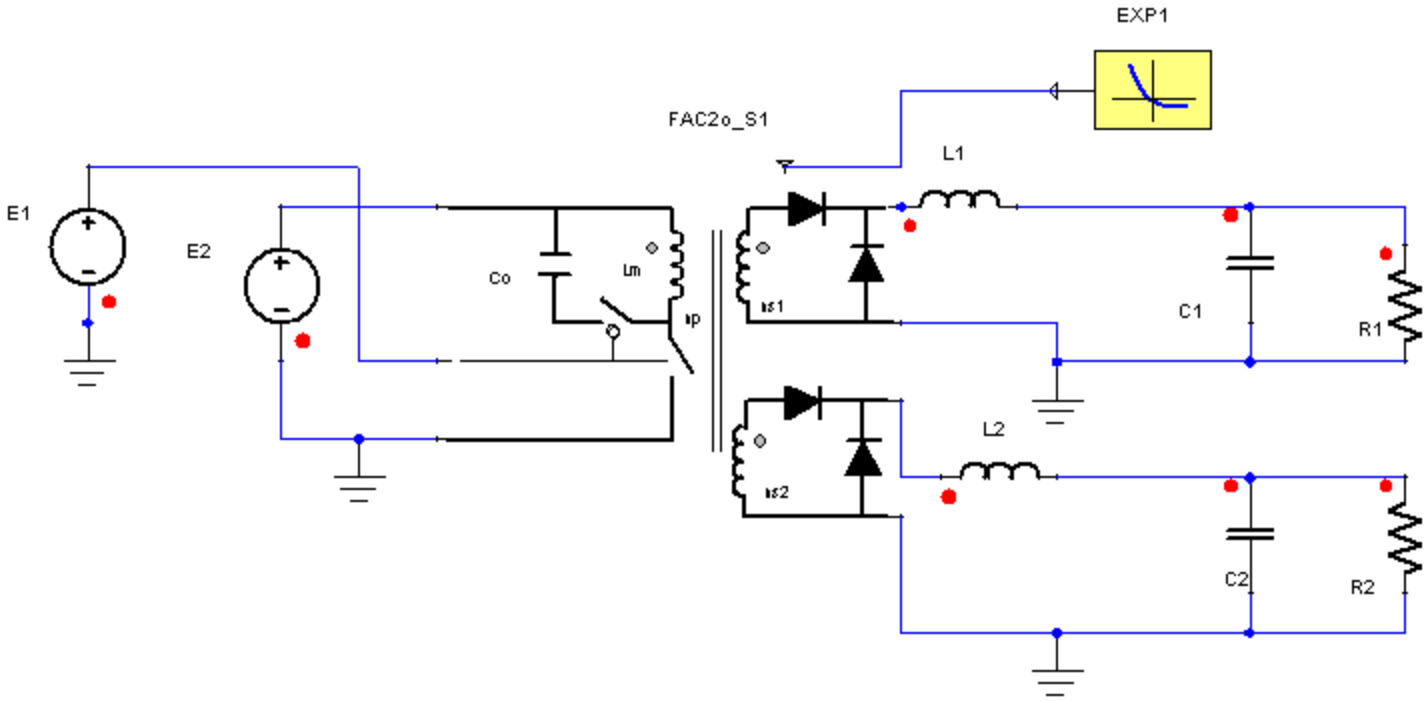

Figure 3. Application example of the Isolated 2 Output Forward Converter with Active Clamp.

Table 3. System Parameters

Component	Parameter	Value [unit]
Isolated 2 Output Forward Converter with Active Clamp FAC2o_S1	np	1
	n1	1
	n2	1
	Rsa	0.01 [Ohm]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R1	R	1 [Ohm]
Resistor R2	R	10 [Ohm]
Capacitor C1	C	5e-005 [F]
Capacitor C2	C	5e-005 [F]
Inductor L1/L2	L	0.0001 [H]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

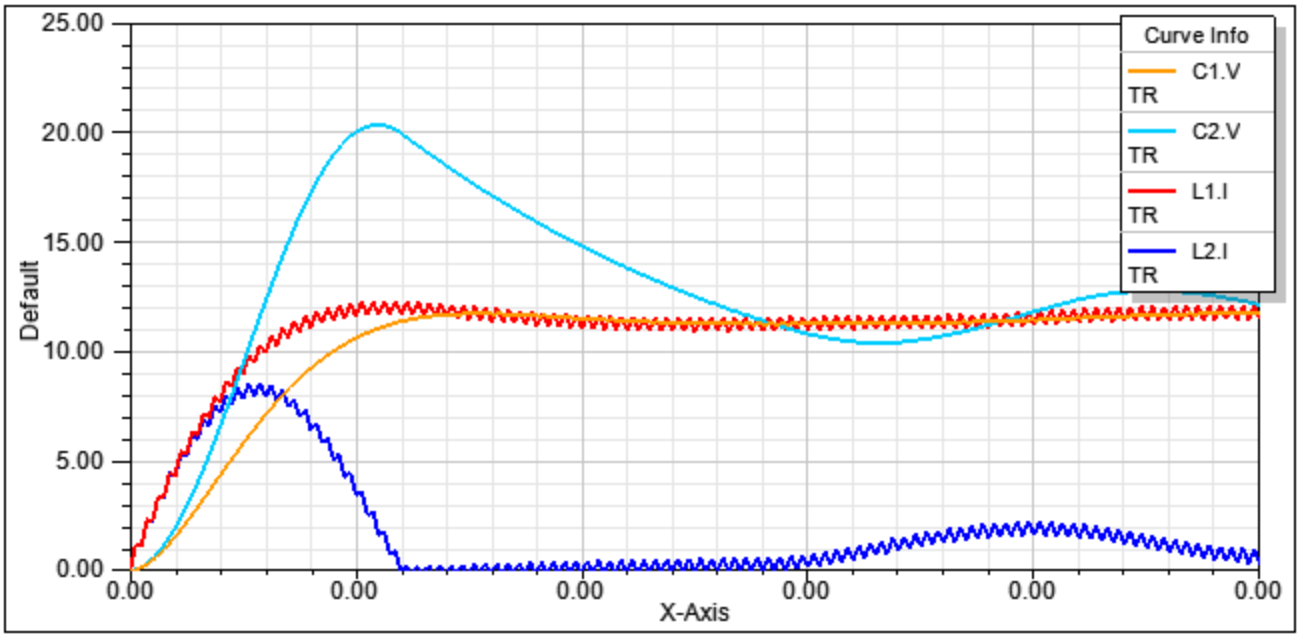

Figure 4. Simulation results-Output currents (L1.I, L2.I) and Output Voltages (C1.V, C2.V).

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References

Switch Level FLYBACK Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

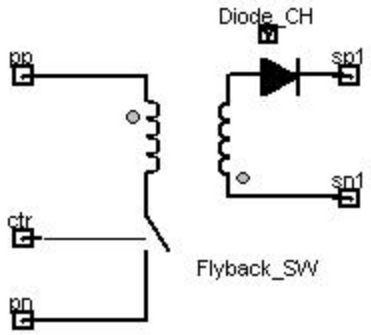

Figure 1. Component symbol

Description

This block represents the switch level model of the Flyback converter.

Top

Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques. The model also includes the magnetizing inductance of the transformer.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

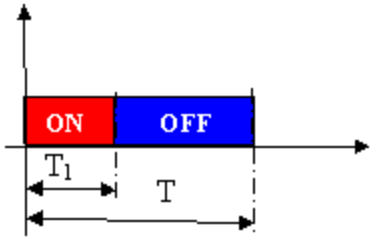

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL FLYBACK_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) pp:= %0, pn:= %1, sp1:= %2, ctr:= %3, sn1:= %4 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, np:= @np, ns1:= @ns1) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
pp	Positive input pin	Electrical terminal
pn	Negative input pin	Electrical terminal
sp1	Positive output pin	Electrical terminal
sn1	Negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
L	Magnetizing Inductance	real	1e-5 [H]
L_IC	Magnetizing Inductance Initial Current	real	0 [A]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
np	Primary Number of Turns	real	1
ns1	Secondary Number of Turns	real	1
DIODE_CH	Diode Characteristic	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
isec	Secondary Current [A]	Output	real
iprim	Primary Current [A]	Output	real

Top

Example

This example shows a averaged model of a Flyback Converter for use in transient analysis.

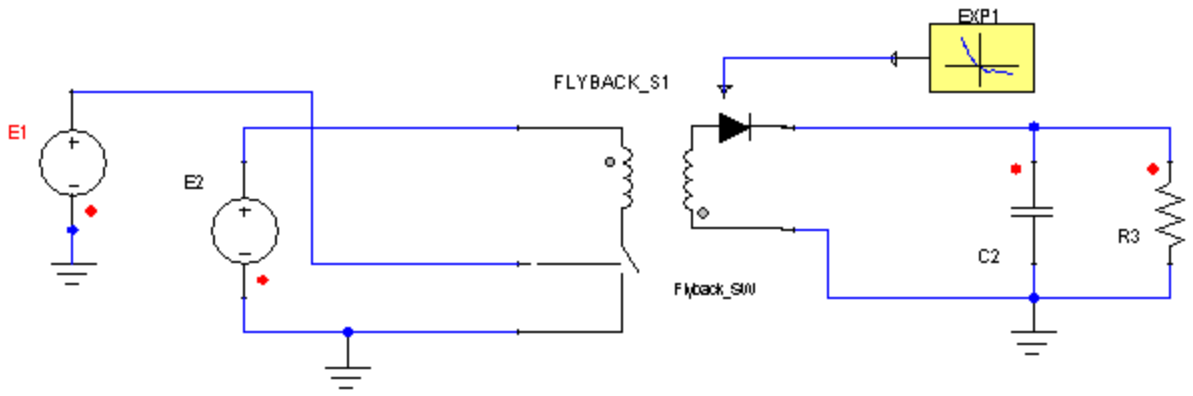

Figure 3. Application example of the Isolated FLYBACK Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Isolated Flyback Converter FLYBACK_S1	L	0.0001 [H]
	L_IC	0 [A]
	Rsa	0.01 [Ohm]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.025 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

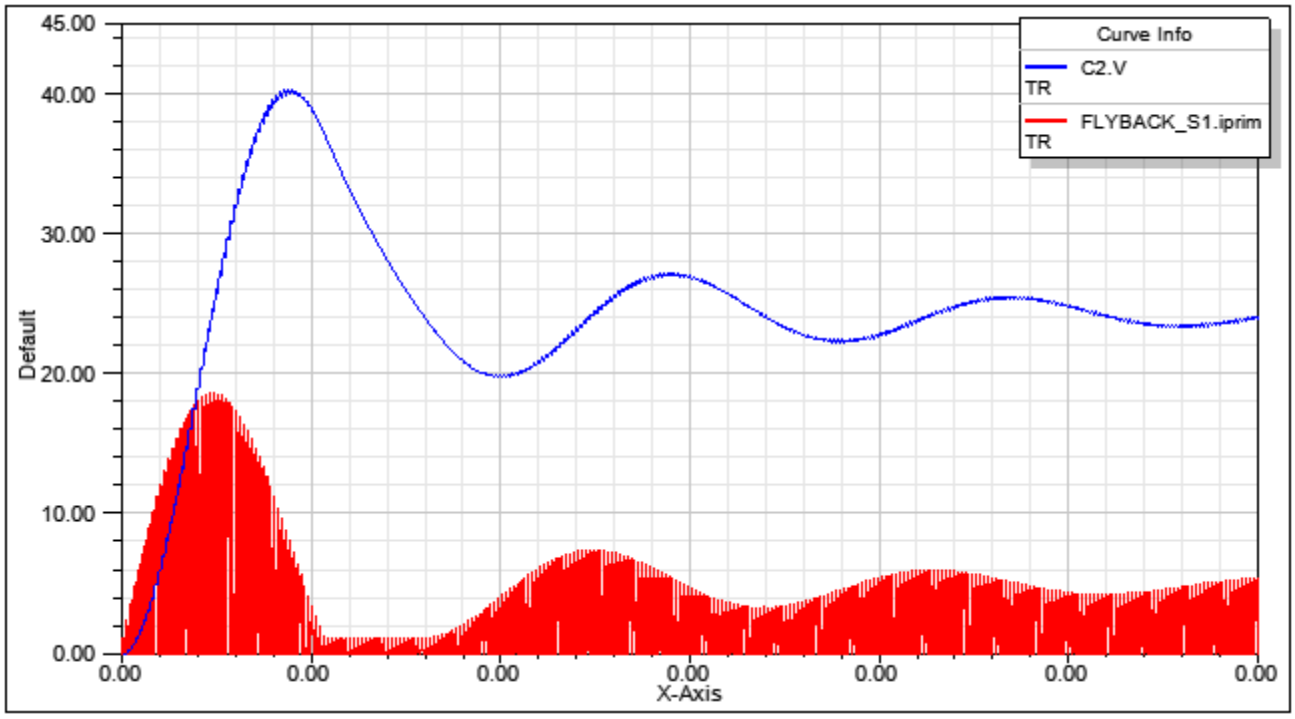

Figure 4. Simulation results-Primary current (FLYBACK_S1.iprim) and Output Voltage (C2.V).

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References

Switch Level FORWARD IDEAL Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

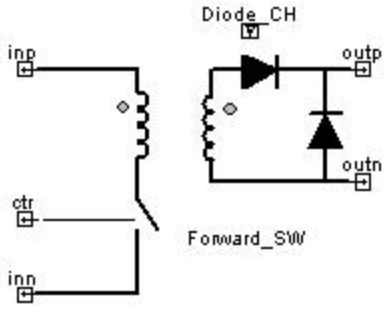

Figure 1. Component symbol

Description

This block represents the switch level model of the Forward converter.

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Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques. The model assumes demagnetization of the magnetizing inductance through some mechanism that does not affect its dynamics. It is not necessary to add any external demagnetizing circuit.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

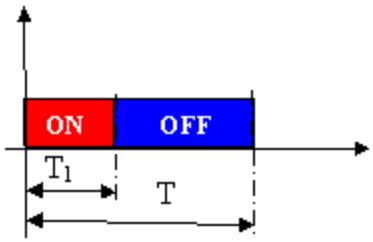

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL FORWARD_SI ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, ctr:= %3, outn:= %4 (Fs:= @Fs, n1:= @n1, n2:= @n2, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Phase_DEG:= @Phase_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	Positive input pin	Electrical terminal
inn	Negative input pin	Electrical terminal
outp	Positive output pin	Electrical terminal
outn	Negative output pin	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
Rsa	Active Switch ON Resist-ance	real	0.01 [Ohm]
n1	Primary Number of Turns	real	1
n2	Secondary Number of Turns	real	1
DIODE_ CH	Diode Characteristic	real	
Phase_ DEG	Sawtooth Phase Delay	real	0 [Deg]

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Example

This example shows a switch level model of a Forward Ideal Converter for use in transient ana-lysis.

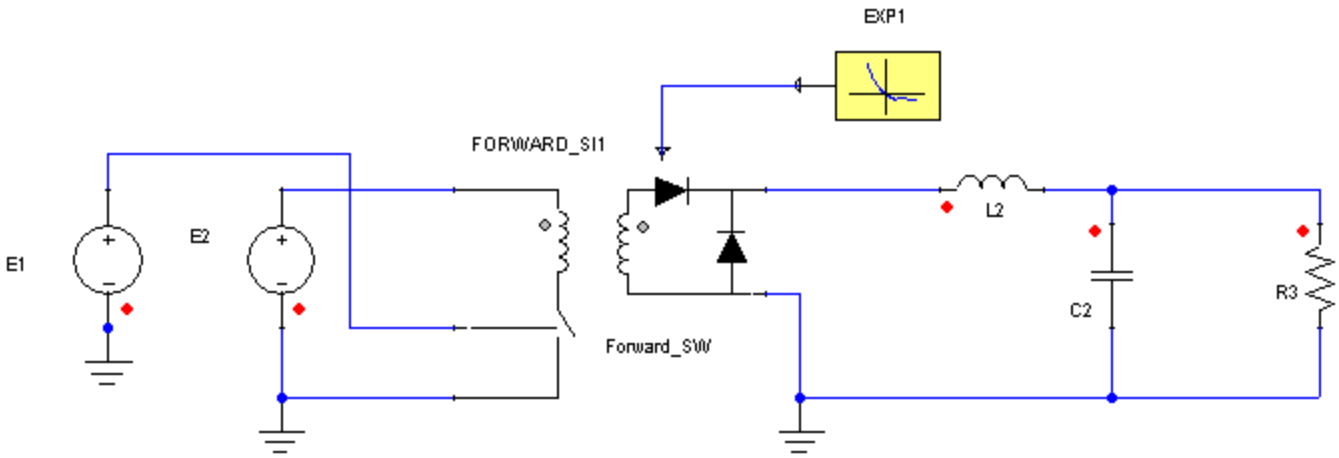

Figure 3. Application example of the Isolated Forward Ideal Power Converter

Table 3. System Parameters

Component	Parameter	Value [unit]

Isolated Forward Ideal Converter FORWARD_SI1	n1	10
	n2	1
	Rsa	0.01 [Ohm]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Inductor L2	L	0.0001 [H]
Voltage Source E1	EMF Value	0.25 [V]
Voltage Source E2	EMF Value	400 [V]

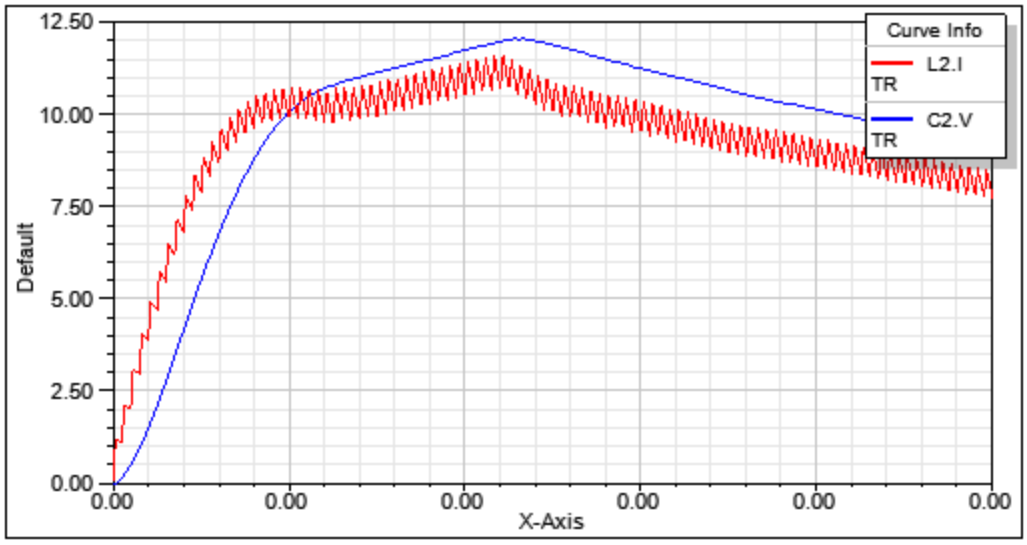

Figure 4. Simulation results-Output current (L2.I) and Output Voltage (C2.V).

Top

References

Power Converters

Averaged Power Converters

Isolated	Non-Isolated > Ideal	Non-Isolated > Non-Ideal
Forward with Active Clamp (FAC_A)	**> With External Inductor**	**> With External Inductor**
Forward with Active Clamp - Two Outputs (FAC2o_A)	Averaged Buck-Boost with External Inductor (BBOOST_AI_XI)*	Averaged Buck-Boost with External Inductor (BBOOST_A_XI)*
Flyback (FLYBACK)	Boost with External Inductor (BOOST_AI_XI)	Averaged Buck-Boost with External Inductor and Synchronous Rectification (BBOOSTS_A_XI)
Forward (FORWARD_A)	Averaged Buck with External Inductor (BUCK_AI_XI)*	Boost with External Inductor (BOOST_A_XI)
Full Bridge (Full_Bridge)	Buck Sync with External Inductor (BUCKS_AI_XI)	Boost Sync with External Inductor (BOOSTS_A_XI)
Half-Bridge with Complementary Control (HBCC_A)	PWM-Switch with External Inductor (PWMS_AI_XI)	Averaged Buck with External Inductor (BUCK_A_XI)*
Half-Bridge (Synchronous) with Complementary Control (HBCCS_A)		Buck Sync with External Inductor (BUCKS_A_XI)
Half-Bridge with Current Doubler Rectifier (HBCDR_A)	**> With Internal Inductor**	**> With Internal Inductor**
	Averaged Buck-Boost with Internal Inductor (BBOOST_AI_II)*	Averaged Buck-Boost with Internal Inductor (BBOOST_A_II)*
	Boost with Internal Inductor (BOOST_AI_II)	Averaged Buck-Boost with Internal Inductor and Synchronous Rectification (BBOOSTS_A_II)
	Averaged Buck with Internal	Boost with Internal Inductor (BOOST_A_II)

	Inductor (BUCK_AI_II)*	
	Buck Sync with Internal Inductor (BUCKS_AI_II)	Boost Sync with Internal Inductor (BOOSTS_A_II)
		Averaged Buck with Internal Inductor (BUCK_A_II)*
		Buck Sync with Internal Inductor (BUCKS_A_II)
		CUK with Internal Inductor (CUK_A_II)
		SEPIC with Internal Inductor (SEPIC_A_II)

* Valid for Continuous and Discontinuous Conduction Mode

Switch Level Power Converters

Isolated	Non-Isolated
Forward with Active Clamp - Two Outputs with Filter (FAC_2out_Lf_SW)	Buck-Boost (BBOOST_S)
Forward with Active Clamp (FAC_S)	Boost (BOOST_S)
Forward with Active Clamp - Two Outputs (FAC2o_S)	Buck (BUCK_S)
Flyback (FLYBACK_S)	Buck Synchronous (BUCK_SYNC_1PH_SW)
Forward Ideal (FORWARD_SI)	CUK (CUK_S)
	SEPIC (SEPIC_S)

Switch Level BUCK-BOOST Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

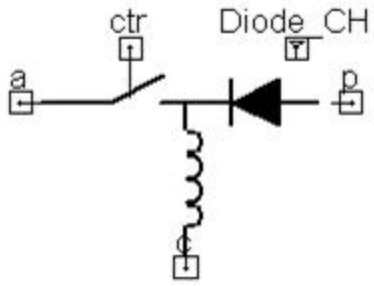

Figure 1. Component symbol

Description

This block represents the switch level model of the Buck-Boost converter.

Top

Assumptions and Limitations

The model accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques. The model also includes the inductor of the Buck-Boost converter.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

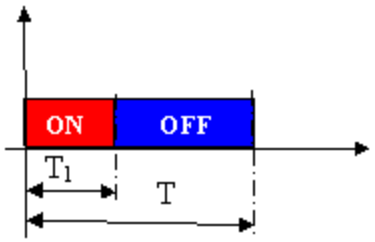

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BBOOST_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Phase_DEG:= @Phase_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data	Default Value

		Type	[Unit]
Fs	Switching Frequency	real	0 [Hz]
L	Inductance	real	0 [H]
L_IC	Inductor Initial Current	real	0 [A]
Rsa	Active Switch ON Resistance	real	0 [Ohm]
Phase_DEG	Sawtooth Phase Delay	real	0 [Deg]
DIODE_CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows a device level model of a Buck-Boost Converter for use in transient analysis.

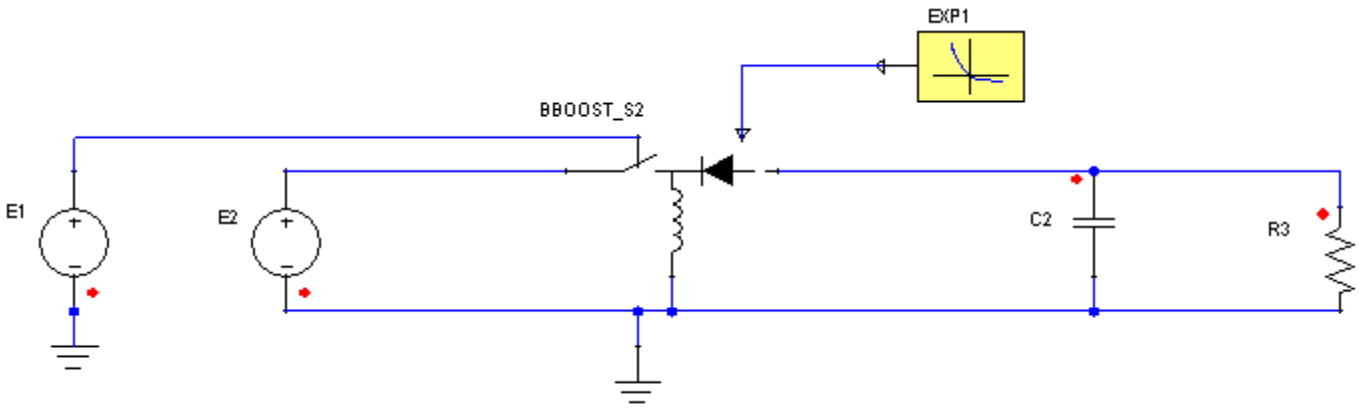

Figure 3. Application example of the Non-Isolated Buck-Boost Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Isolated Buck-Boost Converter BBOOST_S1	L	0.00001 [H]
	L_IC	0.01 [A]
	Diode_CH	EXP1.VAL
	Fs	100000 [Hz]
	Rsa	0.01 [Ohm]
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

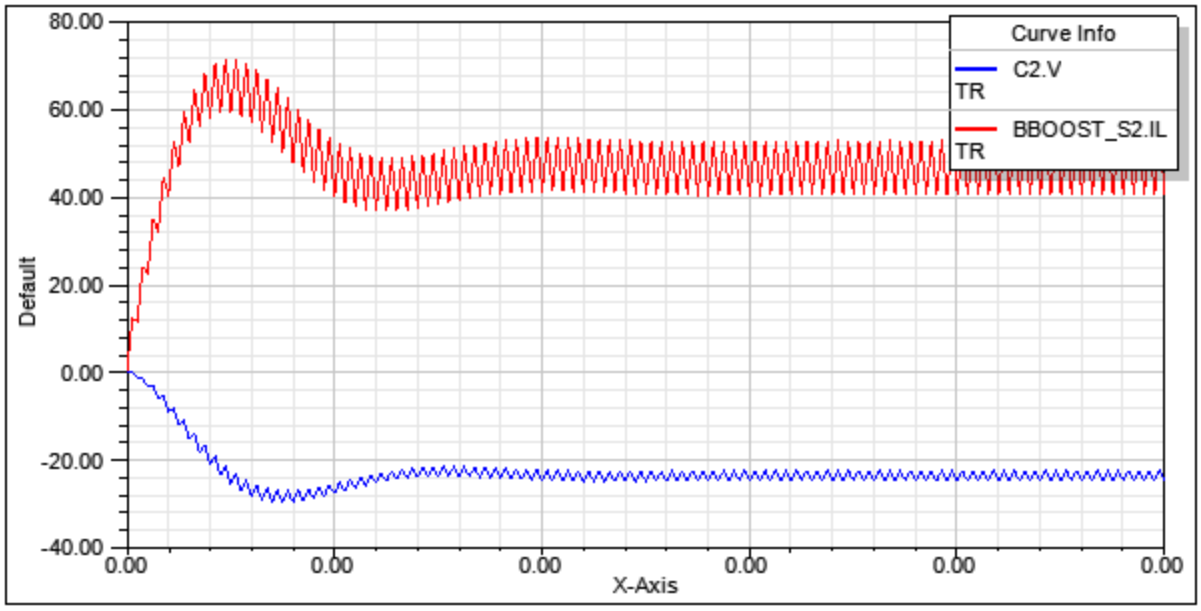

Figure 4. Simulation results-Inductor current and Output Voltage.

Top

References

Switch Level BOOST Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

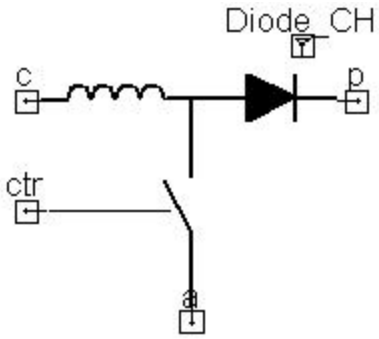

Figure 1. Component symbol

Description

This block represents the switch level model of the Boost converter.

Top

Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques. The model also includes the inductor of the Boost converter.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

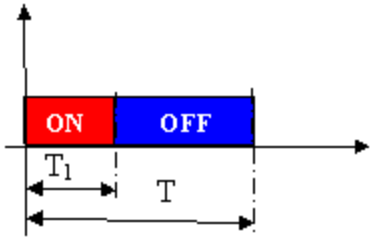

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BOOST_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Phase_DEG:= @Phase_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
L	Inductance	real	1e-5 [H]

L_IC	Inductor Initial Current	real	0 [A]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
Phase_DEG	Sawtooth Phase Delay	real	0 [Deg]
DIODE_CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows a device level model of a Boost Converter for use in transient analysis.

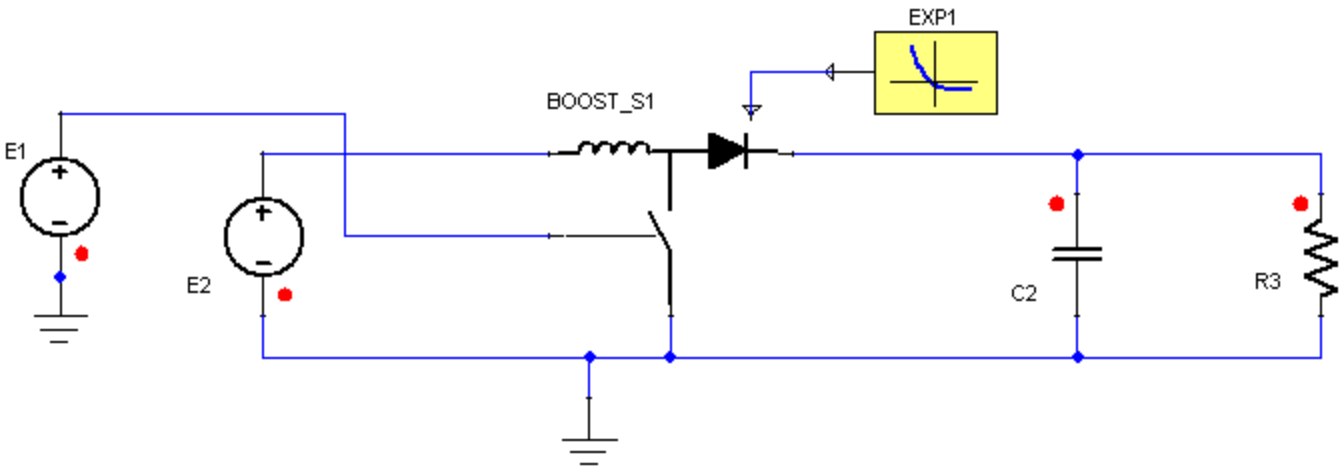

Figure 3. Application example of the Non-Isolated Boost Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Isolated Boost Converter BOOST_S1	L	0.0001 [H]
	L_IC	0.001 [A]
	Diode_CH	EXP1.VAL
	Fs	100000 [Hz]
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

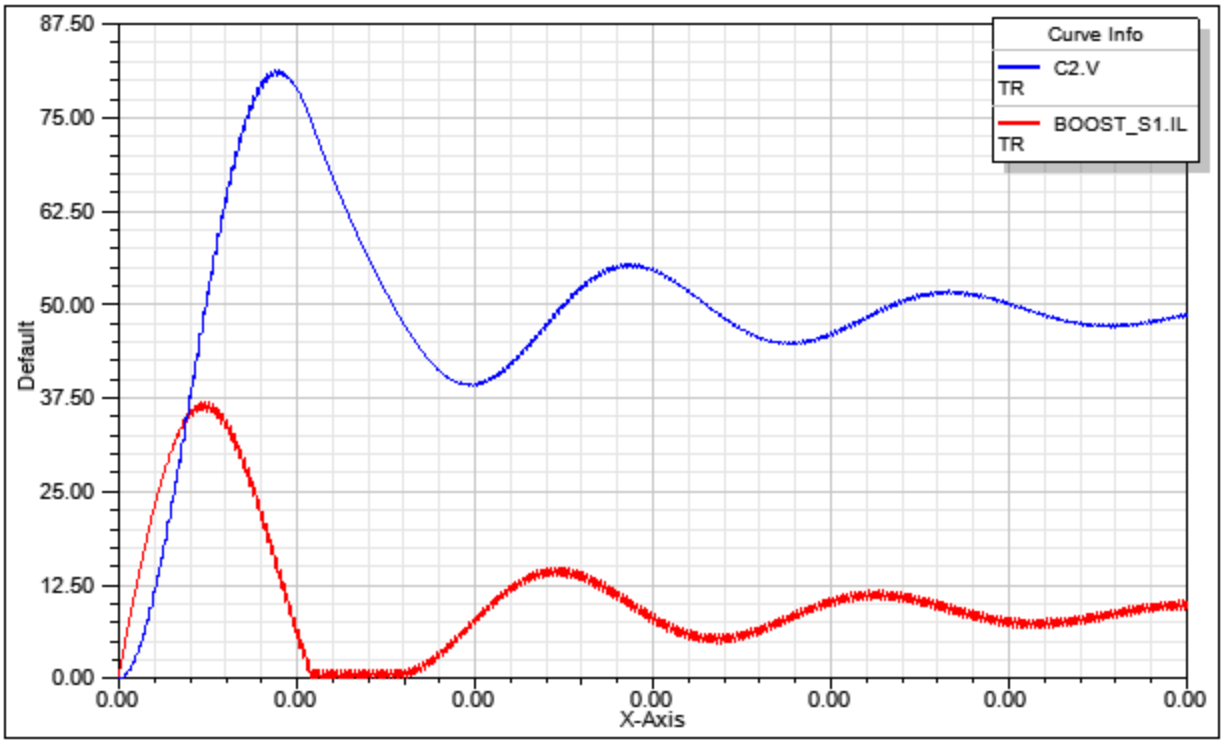

Figure 4. Simulation results-Inductor current and Output Voltage.

Top

References

Switch Level BUCK Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

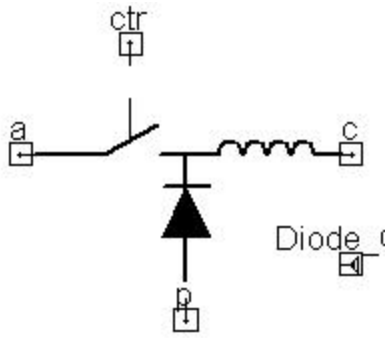

Figure 1. Component symbol

Description

This block represents the switch level model of the Buck converter.

Top

Assumptions and Limitations

The model accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

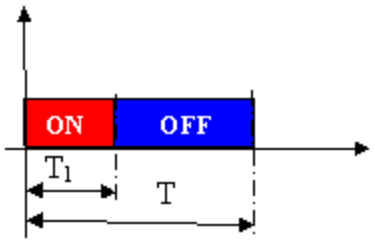

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCK_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, Phase_DEG:= @Phase_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle 0-1V	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data	Default Value

		Type	[Unit]
Fs	Switching Frequency	real	100000 [Hz]
L	Inductance	real	1e-6 [H]
L_IC	Inductor Initial Current	real	0 [A]
Rsa	Active Switch ON Resist-ance	real	0.01 [Ohm]
Phase_ DEG	Sawtooth Phase Delay	real	0 [Deg]
DIODE_ CH	Diode Characteristic	real	

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real

Top

Example

This example shows a switch level model of a Buck Converter for use in transient analysis.

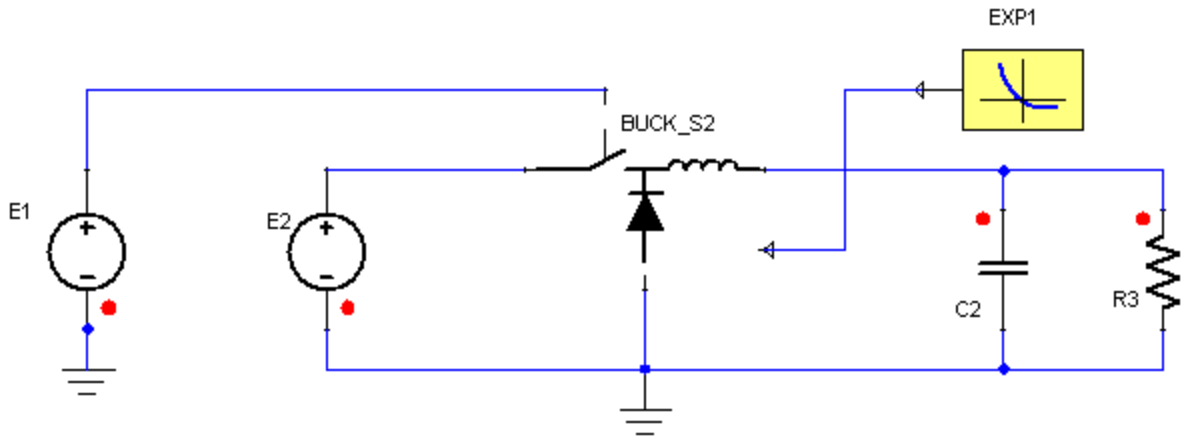

Figure 3. Application example of the Non-Isolated Buck Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Isolated Buck Converter Buck_S2	L	3e-005 [H]
	L_IC	0 [A]
	Diode_CH	EXP1.VAL
	Fs	100000 [Hz]
	Rsa	0.01 [Ohm]
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.5 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

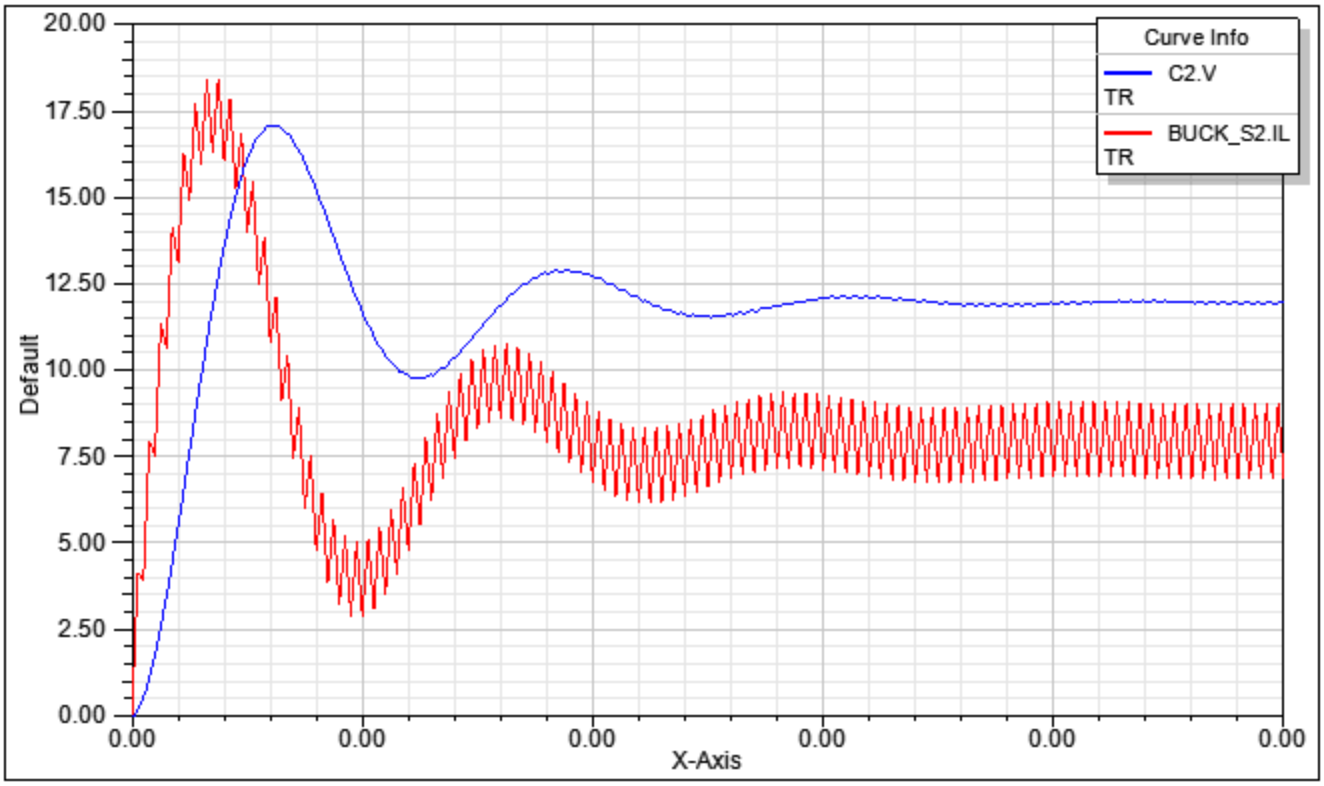

Figure 4. Simulation results-Inductor current and Output Voltage.

Top

References

Switch Level Synchronous BUCK Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

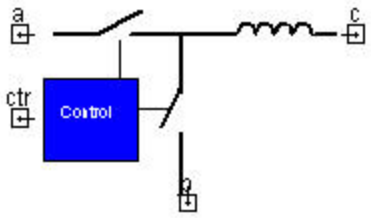

Figure 1. Component symbol

Description

This block represents the switch level model of the Buck converter with Synchronous rectification.

Top

Assumptions and Limitations

The model accounts for conduction losses in the switches. The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

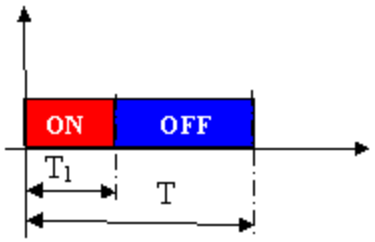

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL BUCK_SYNC_1PH_SW ?InstanceName(@InstanceName):(@(Refbase)@(ID)) a:= %0, p:= %1, c:= %2, ctr:= %3 (Fs:= @Fs, L:= @L, L_IC:= @L_IC, Rsa:= @Rsa, Phase_DEG:= @Phase_DEG, Rw:= @Rw) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
a	active pin (corresponding to the node connected to the active switch)	Electrical terminal
c	common pin (corresponding to the node connected to common terminal)	Electrical terminal
p	passive pin (corresponding to the node connected to the passive switch)	Electrical terminal
ctr	control pin: input for the duty cycle 0-1V	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data	Default Value

		Type	[Unit]
Fs	Switching Frequency	real	100000 [Hz]
L	Inductance	real	1e-5 [H]
L_IC	Inductor Initial Current	real	0 [A]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
Phase_DEG	Sawtooth Phase Delay	real	0 [Deg]
Rw	Inductor Resistance	real	0.001 [Ohm]

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL	Inductor Current [A]	Output	real
I_M1	Mosfet 1 Current [A]	Output	real
I_M2	Mosfet 2 Current [A]	Output	real
I_DM1	Antiparallel Diode 1 Current [A]	Output	real
I_DM2	Antiparallel Diode 2 Current [A]	Output	real

Top

Example

This example shows a switch level model of a Synchronous Buck Converter for use in transient analysis.

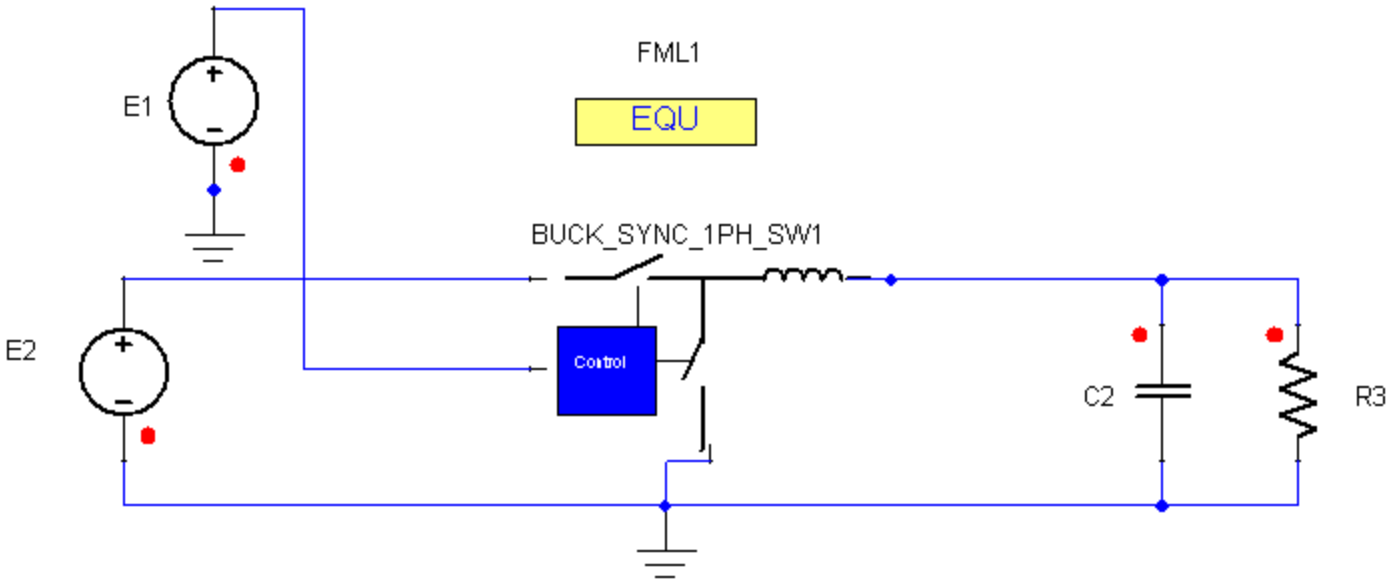

Figure 3. Application example of the Non-Isolated Buck-Sync Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Isolated Synchronous Buck Converter BUCK_SYNC_1PH_SW1	L	3e-005 [H]
	L_IC	0.1 [A]
	Fs	100000 [Hz]
	Rsa	0.01 [Ohm]
Equation Block FML1	EQU0	CTRMAX:=1
	EQU1	CTRMIN:=0
	EQU2	dmax:=0.5
	EQU3	dmin:=0
Resistor R3	R	11 [Ohm]
Capacitor C2	C	5e-005 [F]

Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

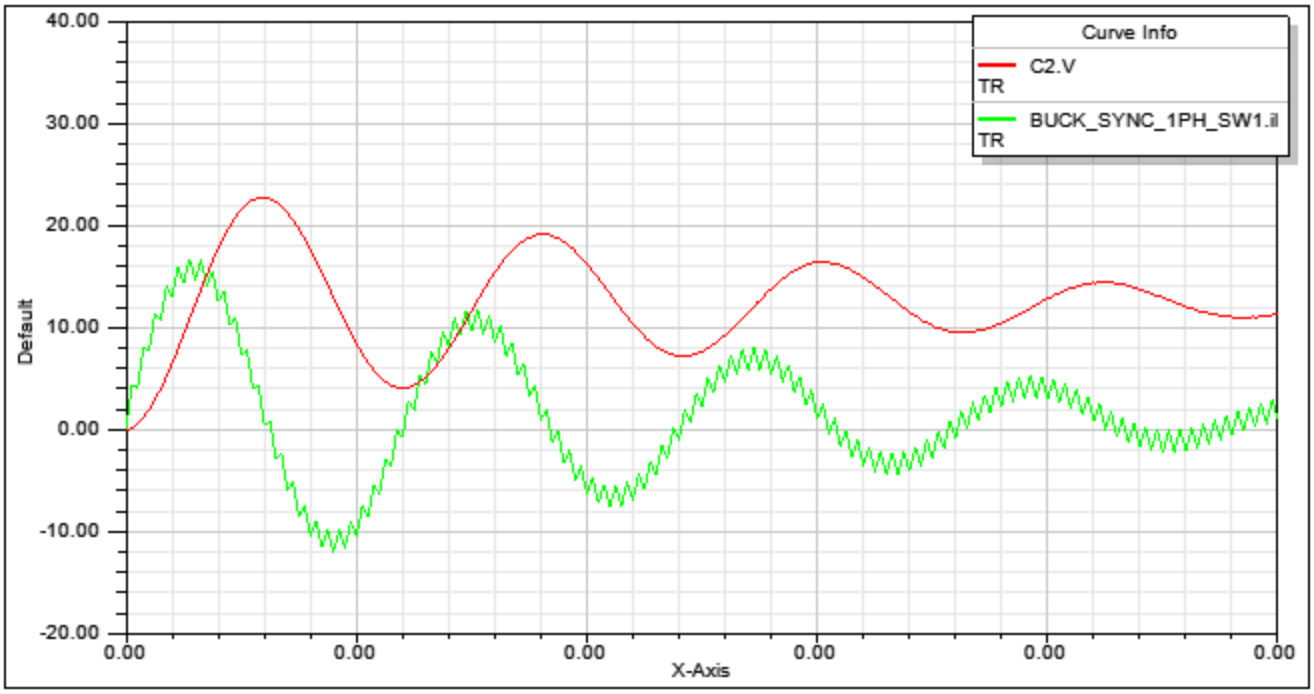

Figure 4. Simulation results-Inductor current and Output Voltage.

Top

References

Switch Level Cuk Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

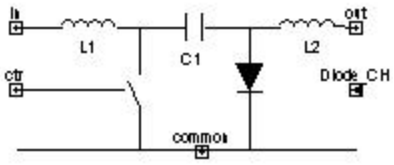

Figure 1. Component symbol

Description

This block represents a switch level model of the Cuk converter. The model also includes the inductors of the Cuk converter and the capacitor.

Top

Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

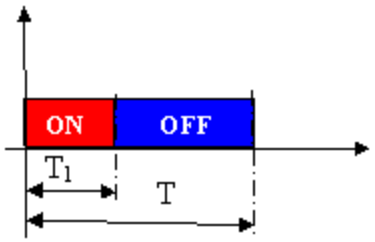

Figure 2. Duty Cycle Calculation

Top

Netlist Syntax

MODEL CUK_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) in:= %0, out:= %1, common:= %2, ctr:= %3 (Fs:= @Fs, L1:= @L1, L1_IC:= @L1_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, L2:= @L2, L2_IC:= @L2_IC, C1:= @C1, C1_IC:= @C1_IC, Phase_DEG:= @Phase_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
in	input pin (corresponding to the node connected to the input voltage)	Electrical terminal
common	common pin (corresponding to the node connected to common terminal)	Electrical terminal
out	output pin (corresponding to the node connected to the output load)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
L1	Inductance 1	real	1e-4 [H]
L2	Inductance 2	real	1e-5 [H]
L1_IC	Inductor 1 Initial Current	real	0 [A]
L2_IC	Inductor 2 Initial Current	real	0 [A]
C1	Capacitance	real	1e-4 [F]
C1_IC	Capacitor Initial Condition	real	0 [V]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
Phase_DEG	Sawtooth Phase Delay	real	0 [Deg]
DIODE_CH	Diode Characteristic	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL1	Inductor 1 Current [A]	Output	real
IL2	Inductor 2 Current [A]	Output	real
VC1	Capacitor Voltage [V]	Output	real

Top

Example

This example shows a device level model of a CUK Converter for use in transient analysis.

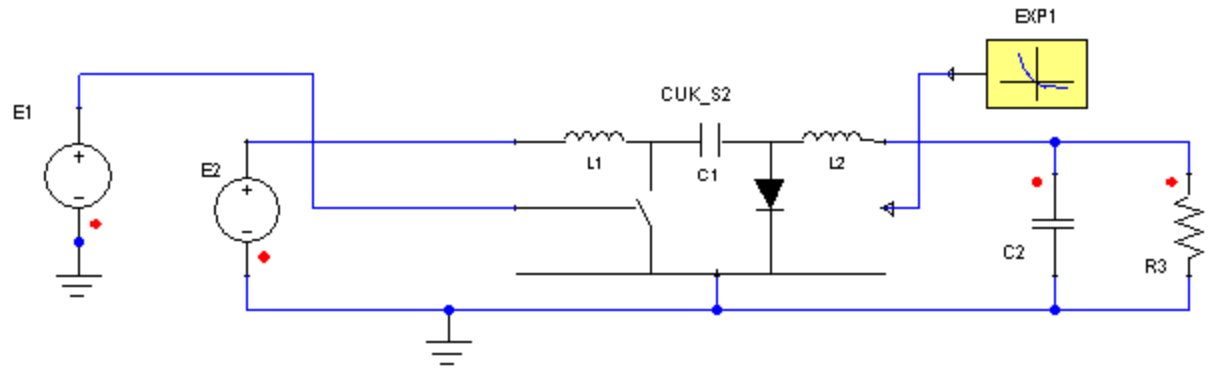

Figure 3. Application example of the Non-Isolated CUK Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Isolated CUK Converter CUK_S2	L	1e-005 [H]
	L1_IC	0.001 [A]
	L2_IC	0.001 [H]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]
Voltage Source E2	EMF Value	25 [V]

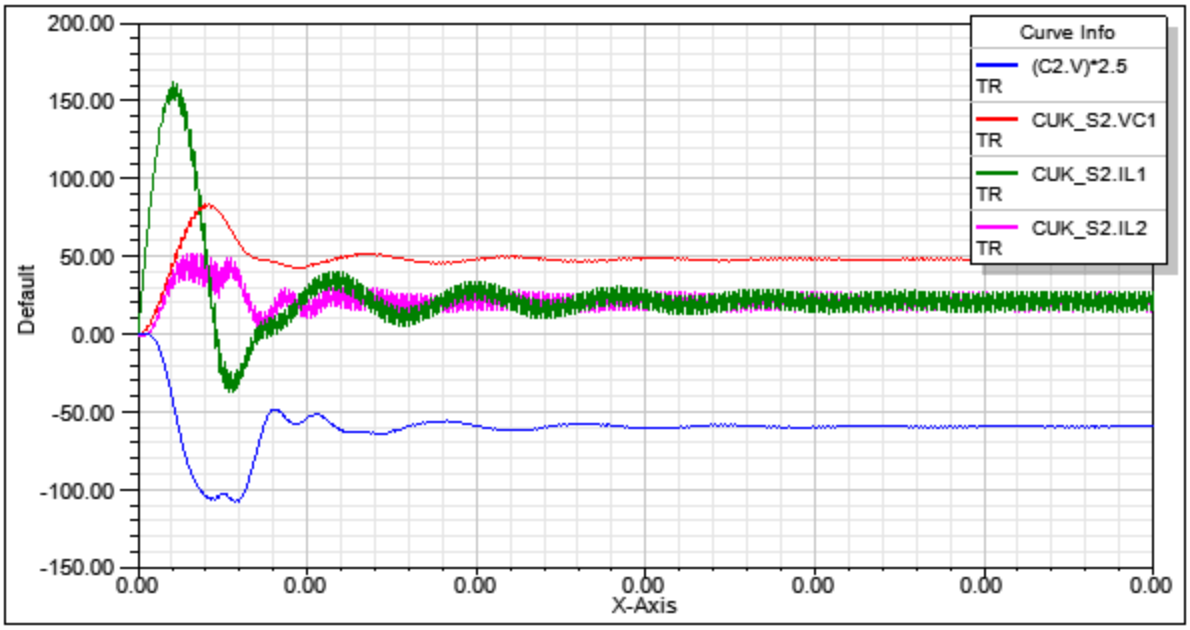

Figure 4. Simulation results-Inductor currents (CUK_S2.IL1 and CUK_S2.IL2), Output Voltage (CUK_S2.VC1) and capacitor voltage (C2.V*2.5).

Top

References

Switch Level Sepic Converter

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

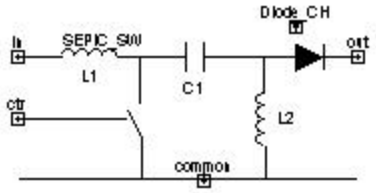

Figure 1. Component symbol

Description

This block represents a switch level model of the Sepic converter. The model also includes the inductors of the Sepic converter and the capacitor.

Top

Assumptions and Limitations

The duty cycle is controlled by the ctr pin and the switching frequency is internally generated. It is possible to add a delay to the ramp in order to facilitate the paralleling of this converter applying interleaving techniques.

Top

Mathematical Description

The duty cycle is determined by the relation between T1 (on time of active switch) and T (switching period) (see Figure 2).

$$duty = \frac{T_1}{T}$$

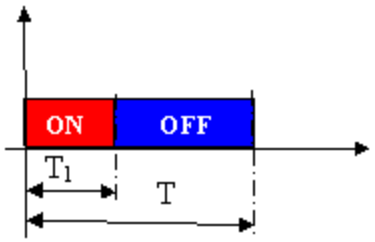

Figure 2. Duty Cycle Calculation

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Netlist Syntax

MODEL SEPIC_S ?InstanceName(@InstanceName):(@(Refbase)@(ID)) in:= %0, out:= %1, common:= %2, ctr:= %3 (Fs:= @Fs, L1:= @L1, L1_IC:= @L1_IC, Diode_CH:= @Diode_CH, Rsa:= @Rsa, L2:= @L2, L2_IC:= @L2_IC, C1:= @C1, C1_IC:= @C1_IC, Phase_DEG:= @Phase_DEG) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
in	input pin (corresponding to the node connected to the input voltage)	Electrical terminal
common	common pin (corresponding to the node connected to common terminal)	Electrical terminal
out	output pin (corresponding to the node connected to the output load)	Electrical terminal
ctr	control pin: input for the duty cycle	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Fs	Switching Frequency	real	100000 [Hz]
L1	Inductance 1	real	1e-5 [H]
L2	Inductance 2	real	1e-5 [H]
L1_IC	Inductor 1 Initial Current	real	0 [A]
L2_IC	Inductor 2 Initial Current	real	0 [A]
C1	Capacitance	real	1e-4 [F]
C1_IC	Capacitor Initial Condition	real	0 [V]
Rsa	Active Switch ON Resistance	real	0.01 [Ohm]
Phase_DEG	Sawtooth Phase Delay	real	0 [Deg]
DIODE_CH	Diode Characteristic	real	

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
IL1	Inductor 1 Current [A]	Output	real
IL2	Inductor 2 Current [A]	Output	real
VC1	Capacitor Voltage [V]	Output	real

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Example

This example shows a device level model of a SEPIC Converter for use in transient analysis.

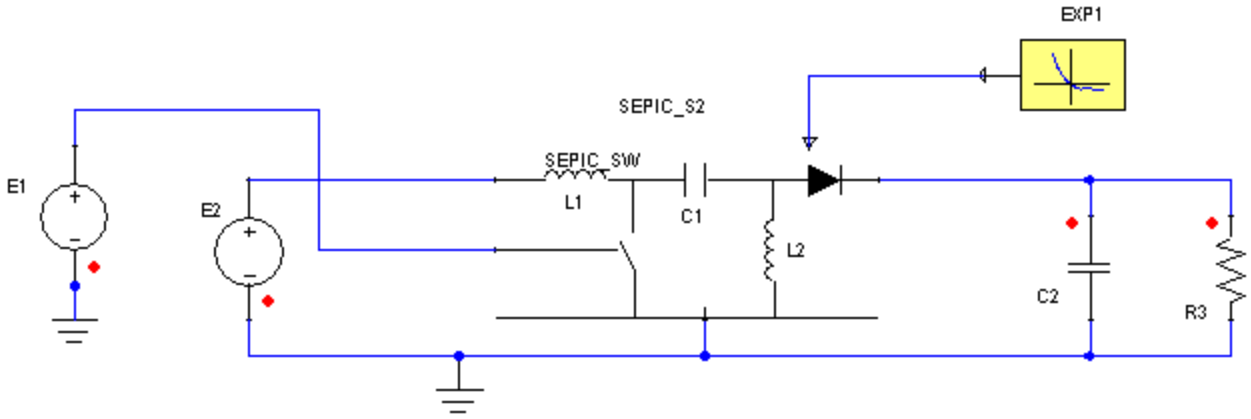

Figure 3. Application example of the Non-Isolated SEPIC Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Non-Isolated SEPIC Converter SEPIC_S2	L1	0.0001 [H]
	L1_IC	0.001 [A]
	L2	0.0001 [H]
	L2_IC	0.001 [H]
	Diode_CH	EXP1.VAL
Exponential Function EXP1	VT	0.035 [V]
	ISAT	1e-012 [A]
	RR	100000 [Ohm]
Resistor R3	R	1.1 [Ohm]
Capacitor C2	C	5e-005 [F]
Voltage Source E1	EMF Value	0.5 [V]

Voltage Source E2	EMF Value	25 [V]

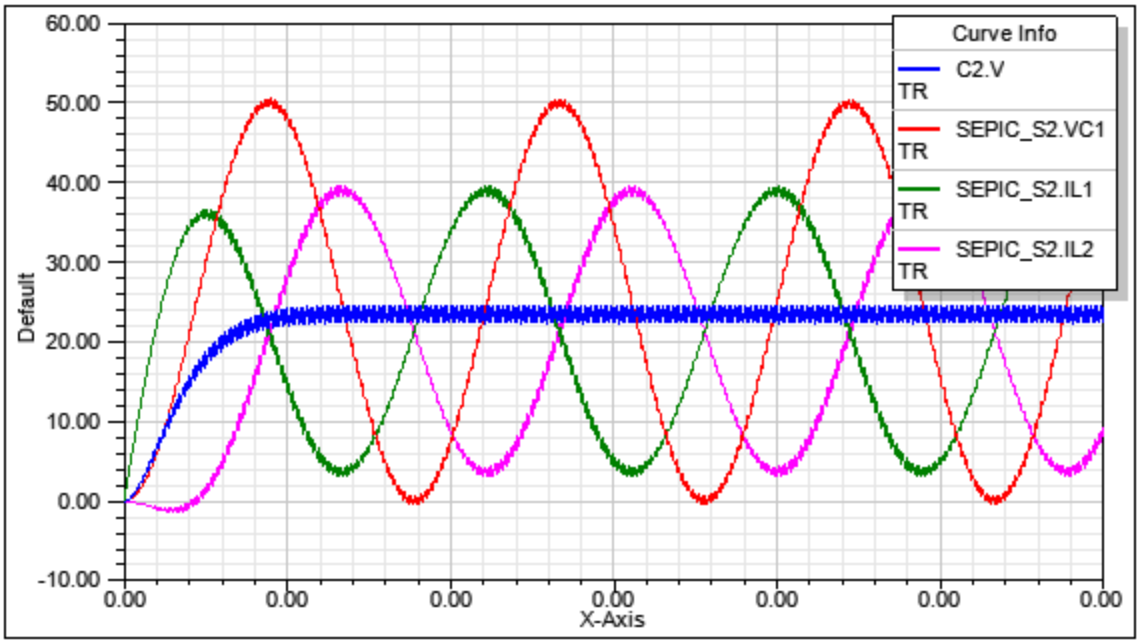

Figure 4. Simulation results-Inductor currents (SEPIC_S2.IL1 and SEPIC_S2.IL2), Output Voltage (SEPIC_S2.VC1) and capacitor voltage (C2.V).

Top

References

Power Factor Correctors

General Power Factor Corrector

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

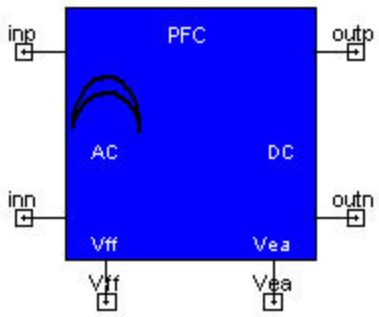

Figure 1. Component symbol

Description

This block represents a power factor corrector block without feed forward network and without output voltage control loop.

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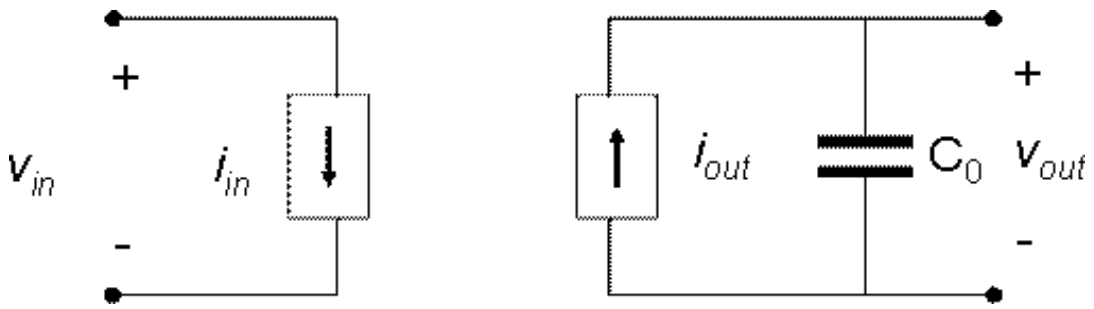
Assumptions and Limitations

This block models a Power Factor Corrector (PFC) converter. The feed forward network and the output voltage control loop are not included in order to be customized by the user.



$$i_{in}(t) = K_m \cdot \frac{V_{EA}(t)}{V_{ff}^{\ 2}(t)} \cdot v_{in}(t)$$

$$i_{out}(t) = \eta \cdot \frac{v_{in}(t) \cdot i_{in}(t)}{v_{out}(t)}$$

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Mathematical Description

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Netlist Syntax

MODEL PFC_GENERAL ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, outn:= %3, Vff:= %4, Vea:= %5 (V0_IC:= @V0_IC, C0:= @C0, Km:= @Km, EFFICIENCY:= @EFFICIENCY) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	AC Side (input) Positive Node	Electrical terminal
inn	AC Side (input) Negative Node	Electrical terminal
outp	DC Side (output) Positive Node	Electrical terminal
outn	DC Side (output) Negative Node	Electrical terminal
Vff	Feed forward of the Input Voltage	Electrical terminal
Vea	Error Amplifier Voltage	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
CO	Output Filter Capacitance	real	0.001 [F]
CO_IC	Output Voltage Initial Condition	real	100 [V]
Km	Conductance Constant	real	1 [A]
Eff	Converter Efficiency	real	100 [%]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Iin	Input Current [A]	Output	real
Vout	Output Voltage [V]	Output	real

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Example

This example illustrates a typical AC/DC converter with PFC (Power Factor Correction). The PFC SMPS Library module provides the appropriate DC output voltage with PFC of the input current. The General PFC module allows the user the connection of external voltage controller and the feed forward network of the input voltage in order to define the input and output characteristics. The schematic of the example is shown in Figure 2, system parameters are listed in the table 4, and the simulation results are shown in Figure 3.

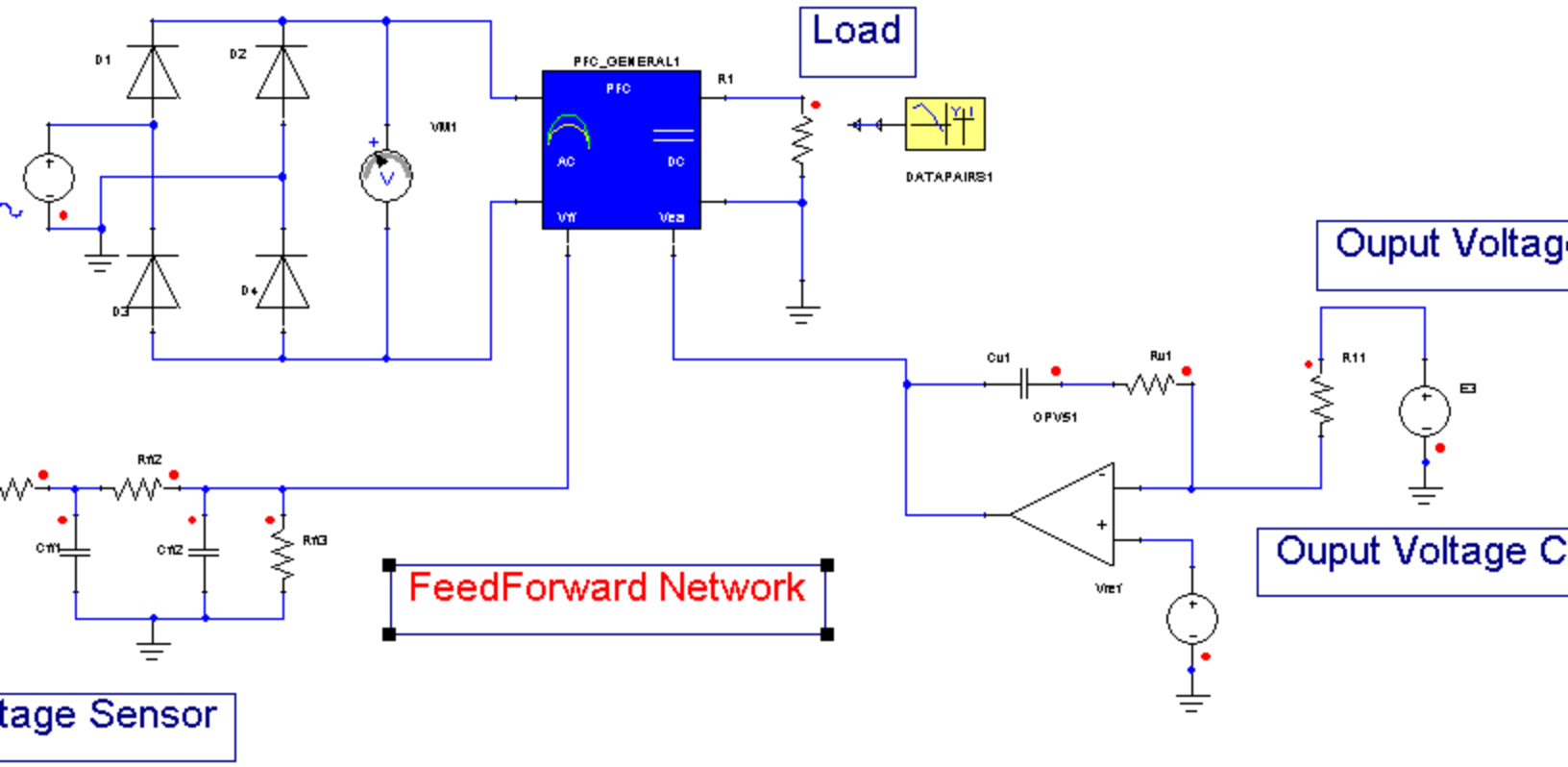
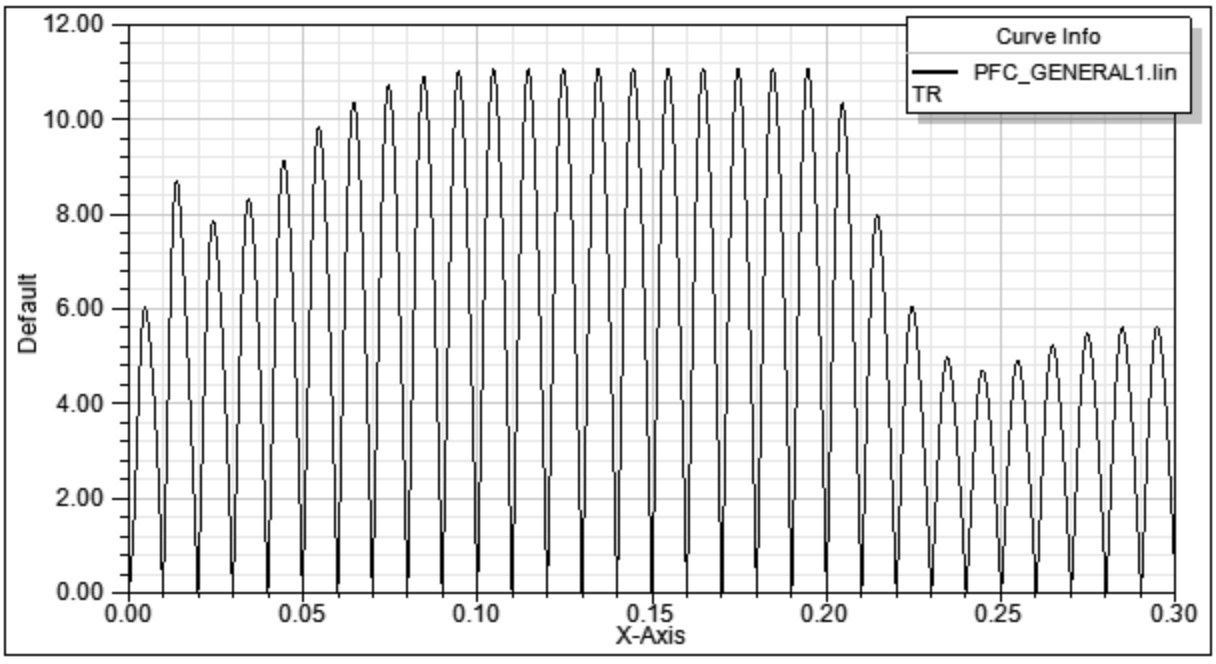


Figure 2. Application example of the General PFC Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
General Power Factor Converter PFC_ GENERAL1	C0	3e-4 [F]
	V0_IC	200 [V]
	Km	0.014
	Efficiency	95
Voltage Source (Sinus-oidal) E1	AMPL	100 [V]
	FREQ	50 [Hz]
Voltage Source (Partial Derivation) E2	EMF	VM1.V
Voltage Source (Partial Derivation) E3	EMF	R1.V*4/180
Voltage Source (Partial Derivation) Vref	EMF	4 [V]
Voltage Meter VM1	Output Value	VM1.V

Diode D1/D2/D3/D4	Type	Equiv Line
	Forward Voltage	0.8 [V]
	Bulk Resist-ance	0.001 [Ohm]
	Reverse Resistance	100000 [Ohm]
Resistor R1	Resistance	DATAPAIRS1.VAL
Resistor Rv1	Resistance	562700[Ohm]
Resistor R11	Resistance	207310[Ohm]
Resistor Rff1/Rff2	Resistance	410000[Ohm]
Resistor Rff3	Resistance	20000[Ohm]
2DLookup Table DATAPAIRS1	TPERIO	0.7 [s]
	ch_file	ExampleGeneralPFC_ ssh_Datapairs1.mdx
Capacitor Cff1	Capacitance	4.37811e-008 [F]
Capacitor Cff2	Capacitance	4.70647e-007 [F]
Capacitor Cv1	Capacitance	1e-008 [F]



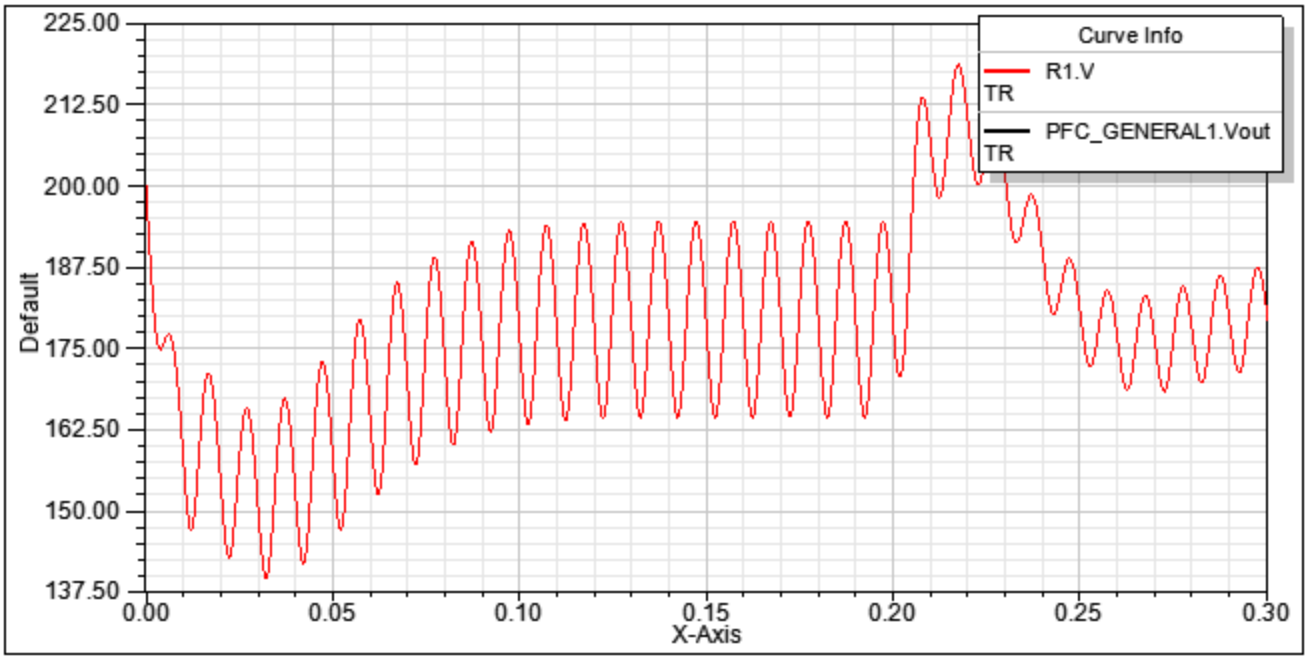


Figure 3. Simulation results – Input Current and Output Voltage of the general Power Factor Converter PFC_GENERAL1.

Top

References

Regulated Power Factor Corrector

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

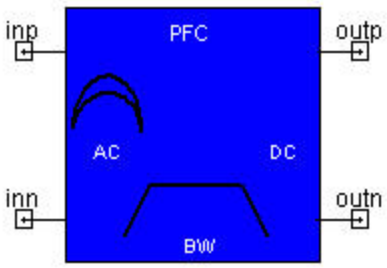


Figure 1. Component symbol

Description

This block represents a Power Factor Correction block with regulation included.

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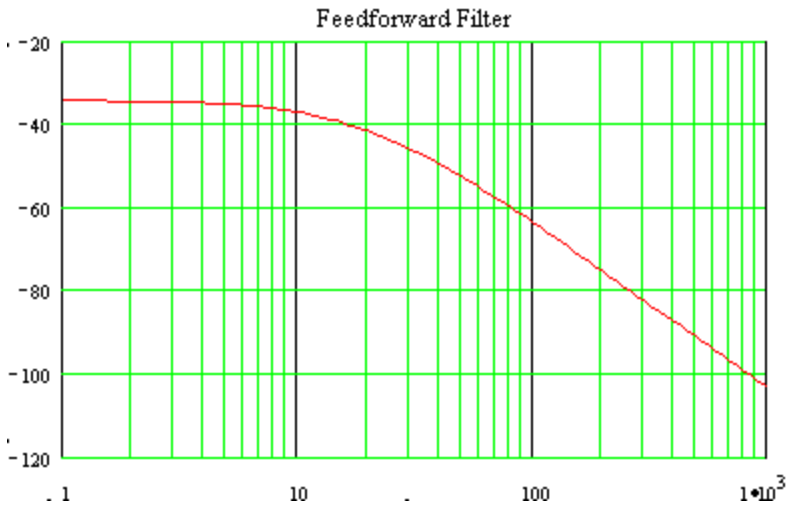
Assumptions and Limitations

In this converter, the output voltage control loop is calculated automatically in order to satisfy the bandwidth requirements of the user. In these applications the output voltage bandwidth is around 2/5 of the line frequency. The higher the bandwidth the faster the response of the voltage loop but the higher the input current distortion (THD).

Feed forward Network

The feed forward network consists on a second order filter that calculates the RMS value of the input voltage and attenuates line frequency harmonics, as shown in the following figure.



Voltage loop

The voltage loop is calculated based on the linearization of the model of the PFC converter around its operating point. The design is based on a worst case condition of constant output power load and provides 45º phase margin at the desired cutoff frequency provided by the user (Bandwidth).

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Mathematical Description

Top

Netlist Syntax

MODEL PFC_REG ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, outn:= %3 (P0:= @P0, V0:= @V0, Fline:= @Fline, C0:= @C0, Bandwidth:= @Bandwidth, C0_IC:= @C0_IC, Eff:= @Eff) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	AC Side (input) Positive Node	Electrical terminal

inn	AC Side (input) Negative Node	Electrical terminal
outp	DC Side (output) Positive Node	Electrical terminal
outn	DC Side (output) Negative Node	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
CO	Output Filter Capacitance	real	0.001 [F]
VO	Output Voltage	real	400 [V]
PO	Output Power	real	100 [W]
CO_IC	Output Voltage Initial Condition	real	400 [V]
Bandwidth	Desired Bandwidth	real	15 [Hz]
Eff	Converter Efficiency	real	100 [%]
Fline	Line Frequency	real	60 [Hz]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Iin	Input Current [A]	Output	real
Vout	Output Voltage [V]	Output	real

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Example

This example illustrates a typical AC/DC converter with PFC (Power Factor Correction). The PFC SMPS Library module provides the appropriate DC output voltage with PFC of the input current. The Regulated PFC module allows the user to define the bandwidth. The voltage controller and the feed forward network are internally included in the PFC regulated element. The schem-

atic of the example is shown in Figure 2, system parameters are listed in the table 4, and the simulation results are shown in Figure 3.

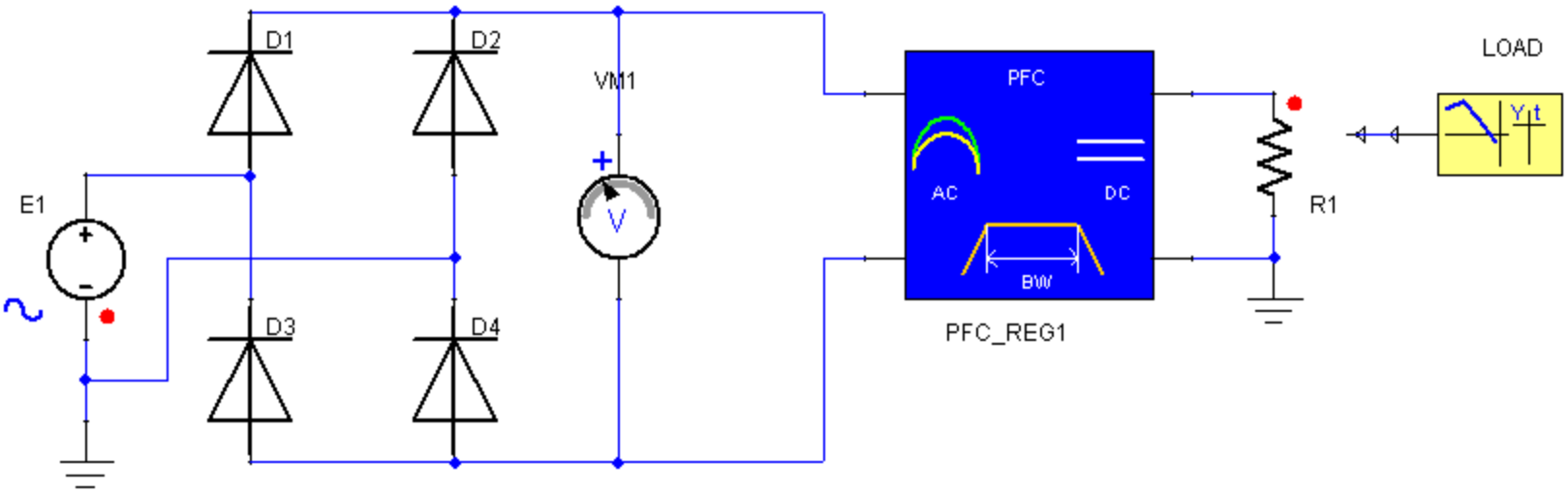
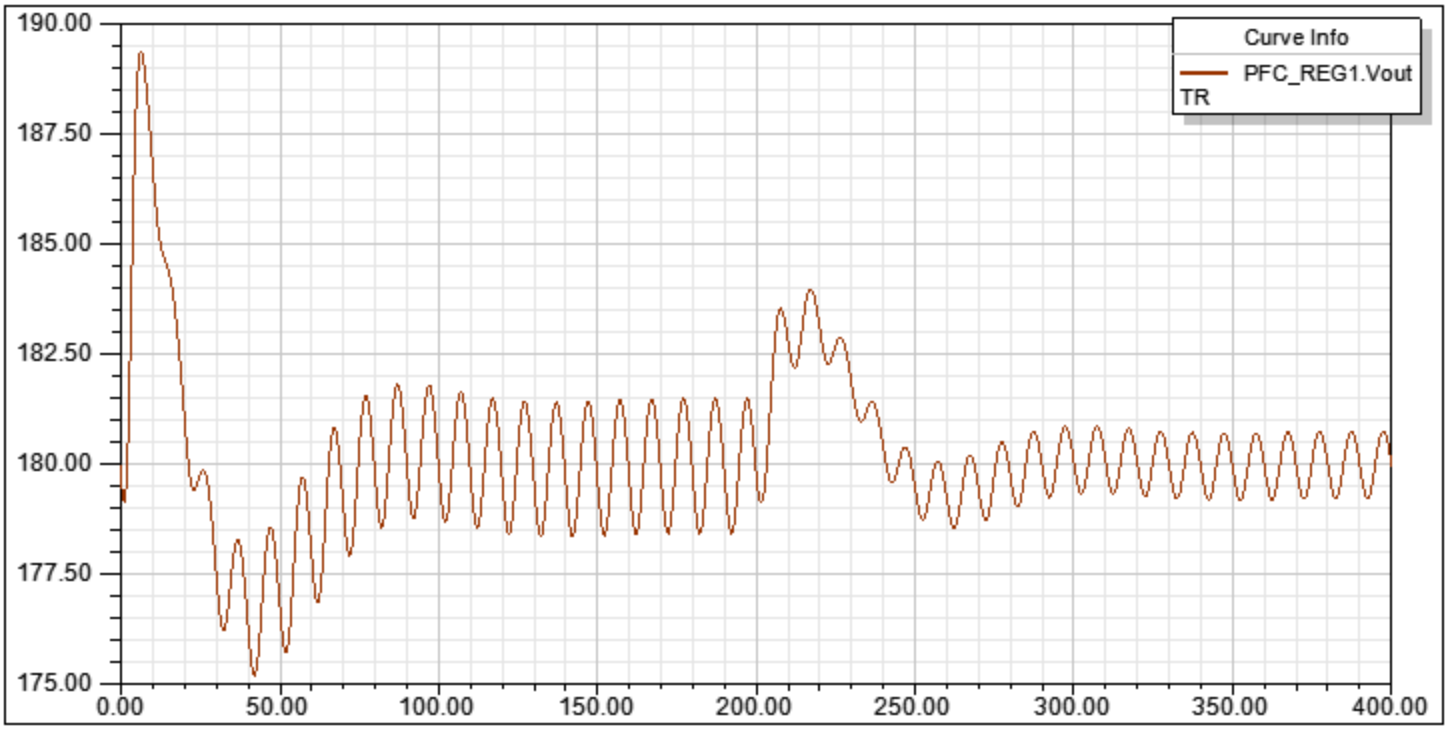


Figure 2. Application example of the Regulated PFC Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
General Power Factor Converter PFC_REG1	C0	6e-4 [F]
	V0	180 [V]
	Bandwidth	15 [Hz]
	Efficiency	100
	Fline	50 [Hz]
	C0_IC	180 [V]
Voltage Source (Sinusoidal) E1	AMPL	100 [V]
	FREQ	50 [Hz]
Diode D1/D2/D3/D4	Type	Equiv Line
	Forward Voltage	0.8 [V]
	Bulk Resistance	0.001 [Ohm]
	Reverse Resistance	100000 [Ohm]
Resistor R1	Resistance	LOAD.VAL

2DLookup Table LOAD	TPERIO	0.4 [s]
	ch_file	ExampleRegulatedPFC_ssh_LOAD.mdx



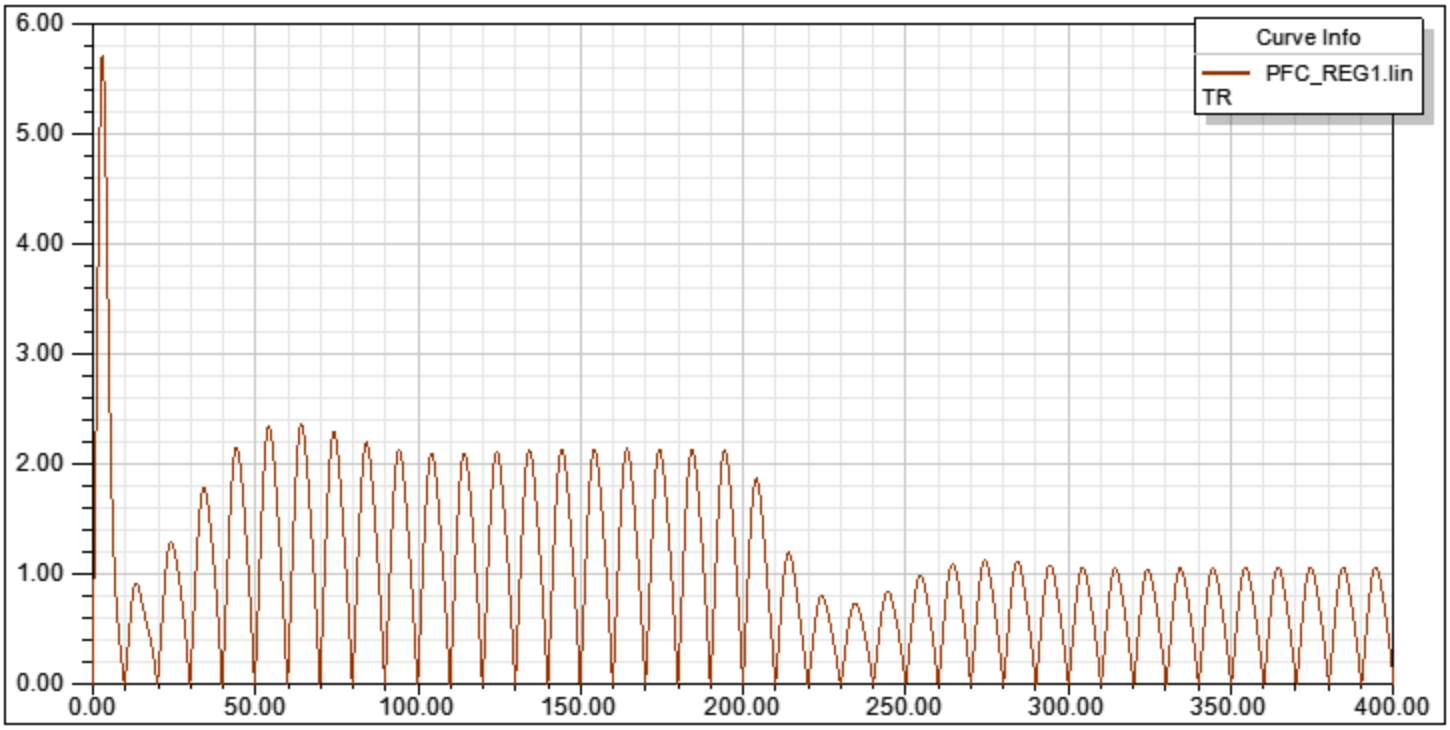


Figure 3. Simulation results – Output Voltage (PFC_REG1.Vout) and Input Current (PFC_ REG1.lin) of the regulated Power Factor Converter PFC_REG1.

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References

Regulated Power Factor Corrector THD

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

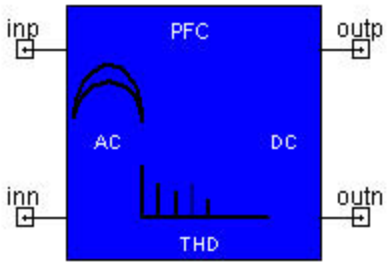

Figure 1. Component symbol

Description

This block represents a Power Factor Corrector block with Total Harmonic Distortion specifications.

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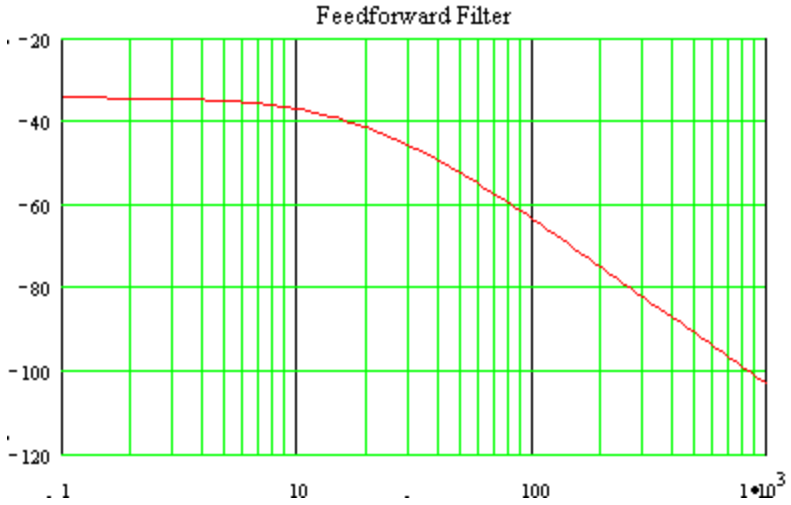
Assumptions and Limitations

In this converter the bandwidth of the output voltage control loop is calculated automatically in order to satisfy the THD requirements of the input current. The lower requirements for the THD (higher THD number) the faster the output voltage control loop.

Feed forward Network

The feed forward network consists on a second order filter that calculates the RMS value of the input voltage and attenuates line frequency harmonics, as shown in the following figure.



Voltage loop

The voltage loop is calculated based on the linearization of the model of the PFC converter around its operating point. The design is based on a worst case condition of constant output power load and provides 45º phase margin at the desired cutoff frequency that is function of the THD of the input current.

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Mathematical Description

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Netlist Syntax

MODEL PFC_THD ?InstanceName(@InstanceName):(@(Refbase)@(ID)) inp:= %0, inn:= %1, outp:= %2, outn:= %3 (P0:= @P0, V0:= @V0, Fline:= @Fline, C0:= @C0, THD:= @THD, C0_IC:= @C0_IC, Eff:= @Eff) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
inp	AC Side (input) Positive Node	Electrical terminal
inn	AC Side (input) Negative Node	Electrical terminal
outp	DC Side (output) Positive Node	Electrical terminal
outn	DC Side (output) Negative Node	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
CO	Output Filter Capacitance	real	0.001 [F]
VO	Output Voltage	real	400 [V]
PO	Output Power	real	100 [W]
CO_IC	Output Voltage Initial Condition	real	400 [V]
Eff	Converter Efficiency	real	100 [%]
Fline	Line Frequency	real	60 [Hz]
THD	Total Harmonic Distortion	real	5 [%]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Iin	Input Current [A]	Output	real
Vout	Output Voltage [V]	Output	real

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Example

This example illustrates a typical AC/DC converter with PFC (Power Factor Correction). The PFC SMPS Library module provides the appropriate DC output voltage with PFC of the input current. The Regulated THD PFC module allows the user the definition of the Total Harmonic Distortion(THD). The band width is automatically calculated. The voltage controller and the feed forward network are internally included in the PFC Regulated element. The schematic of the example is shown in Figure 2, system parameters are listed in the table 4, and the simulation results are shown in Figure 3.

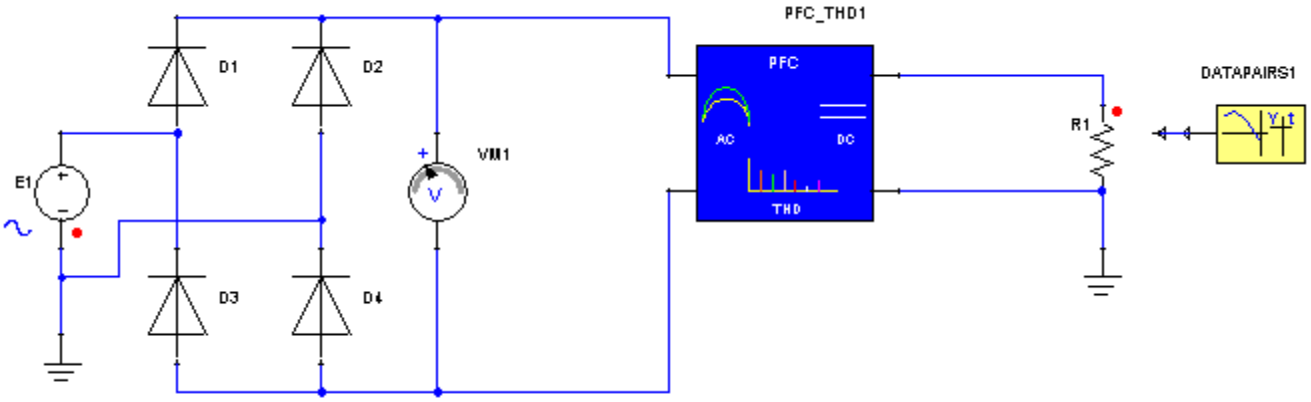

Figure 2. Application example of the Regulated PFC_THD Power Converter

Table 4. System Parameters

Component	Parameter	Value [unit]
Regulated PFC THD PFC_THD1	C0	0.0006 [F]
	V0	180 [V]
	C0_IC	180 [V]
	THD	20 [%]
	Fline	50 [Hz]
Voltage Source (Sinusoidal) E1	AMPL	100 [V]
	FREQ	50 [Hz]
Diode D1/D2/D3/D4	Type	Equiv Line
	Forward Voltage	0.8 [V]
	Bulk Resist-ance	0.001 [Ohm]
	Reverse Resistance	100000 [Ohm]
Resistor R1	Resistance	DATAPAIRS1.VAL
2DLookup Table DATAPAIRS1	TPERIO	0.4 [s]
	ch_file	ExampleRegulatedPFC THD_ssh_Datapairs1.mdx

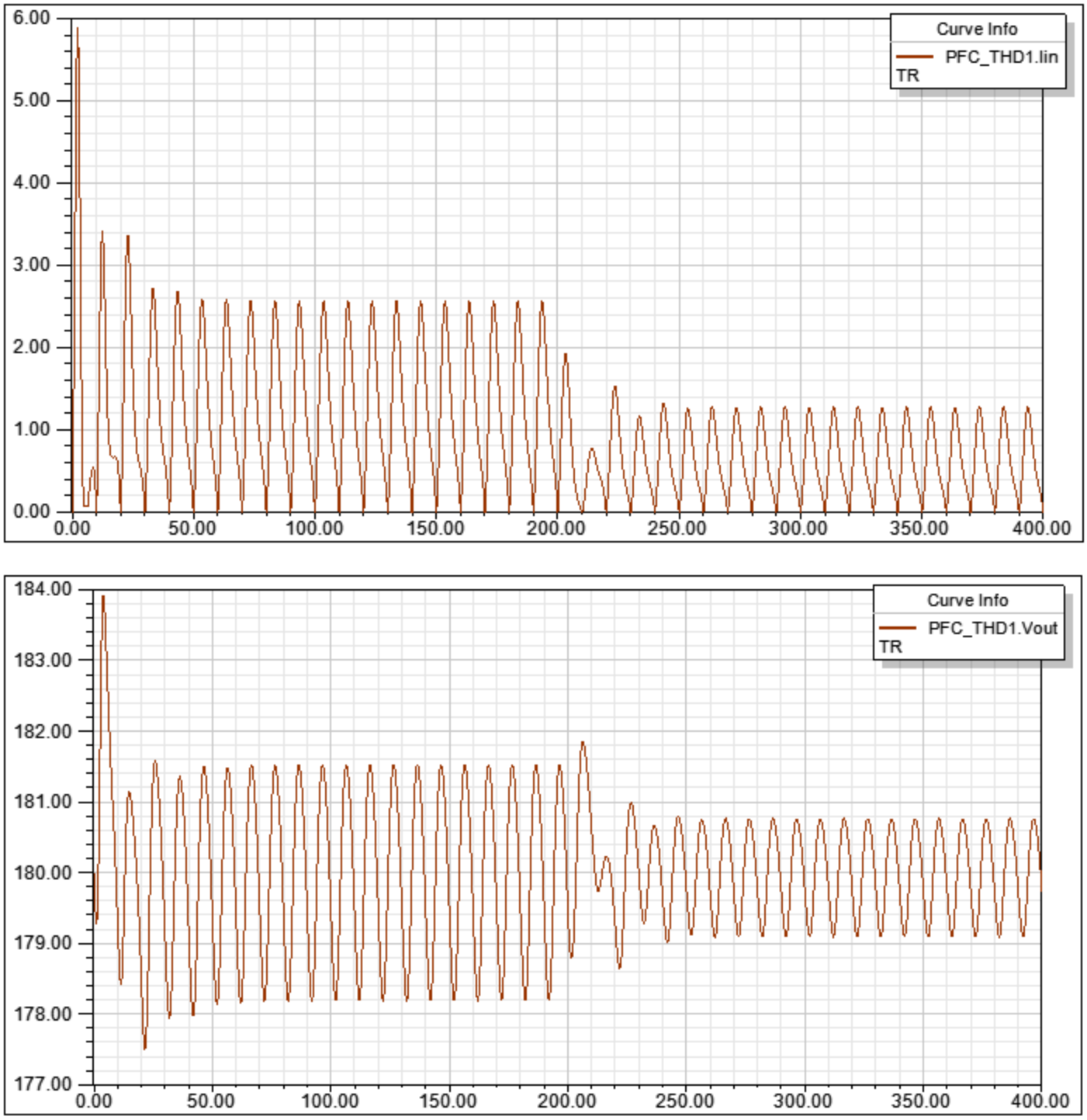

Figure 3. Simulation results – Input Current and Output Voltage of the general Power Factor Converter PFC_THD1.

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References

System Modeling

- Batteries
- Power Load
- Solar Systems

Batteries

- Alkaline N (ALKALINE_N)
- Generic Battery Cell (BATTCELL)

ALKALINE_N Alkaline N Battery

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

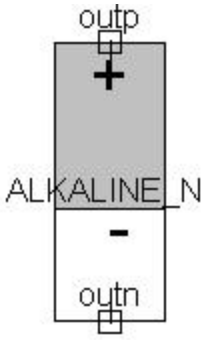

Figure 1. Component symbol

Description

This block represent an Alkaline battery. The parameter SOC indicates the state of charge with 1 being CHARGED and 0 being DISCHARGED.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

MODEL ALKALINE_N ?InstanceName(@InstanceName):(@(Refbase)@(ID)) outp:= %0, outn:= %1 (Trate:= @Trate, Capacity:= @Capacity, Rs:= @Rs, SOC_IC:= @SOC_IC) SRC: DB (Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
outp	Positive Pin	Electrical terminal
outn	Negative Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Trate	Internal Time Constant	real	10 [s]
Capacity	Nominal Capacity	real	1 [A*hours]
Rs	Series Resistance	real	1 [Ohm]
SOC_IC	Initial State of Charge	real	1

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
SOC	State of Charge	Output	real
I	Battery current	Output	real
V	Battery voltage	Output	real
SOC_EFF	Effective State of Charge	Output	real

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Example

Example of an Alkaline N Battery supplying a resistive load. The results show the battery voltage, which drops as the battery is discharged.

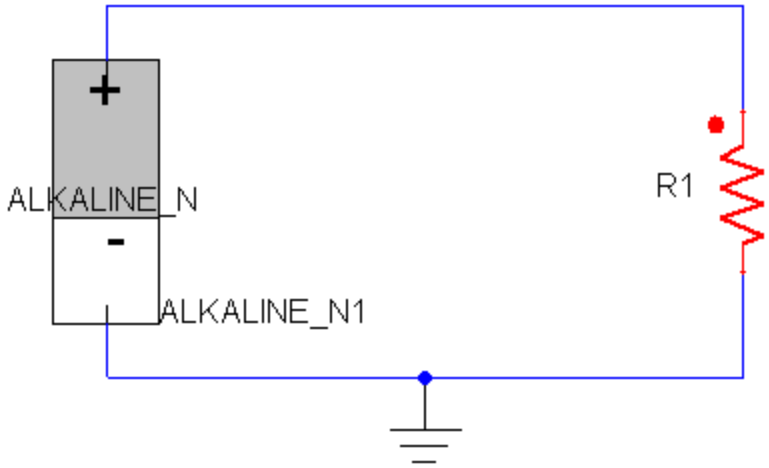

Figure 2. Application example of the Alkaline N Battery.

Table 4. System Parameters

Component	Parameter	Value [unit]
Alkaline N Battery ALKALINE_N1	Trate	10 [s]
	Capacity	1 [AHour]
	Rs	0.01 [Ohm]
	SOC	1
	SOC_IC	1
Resistor R1	R	10 [Ohm]

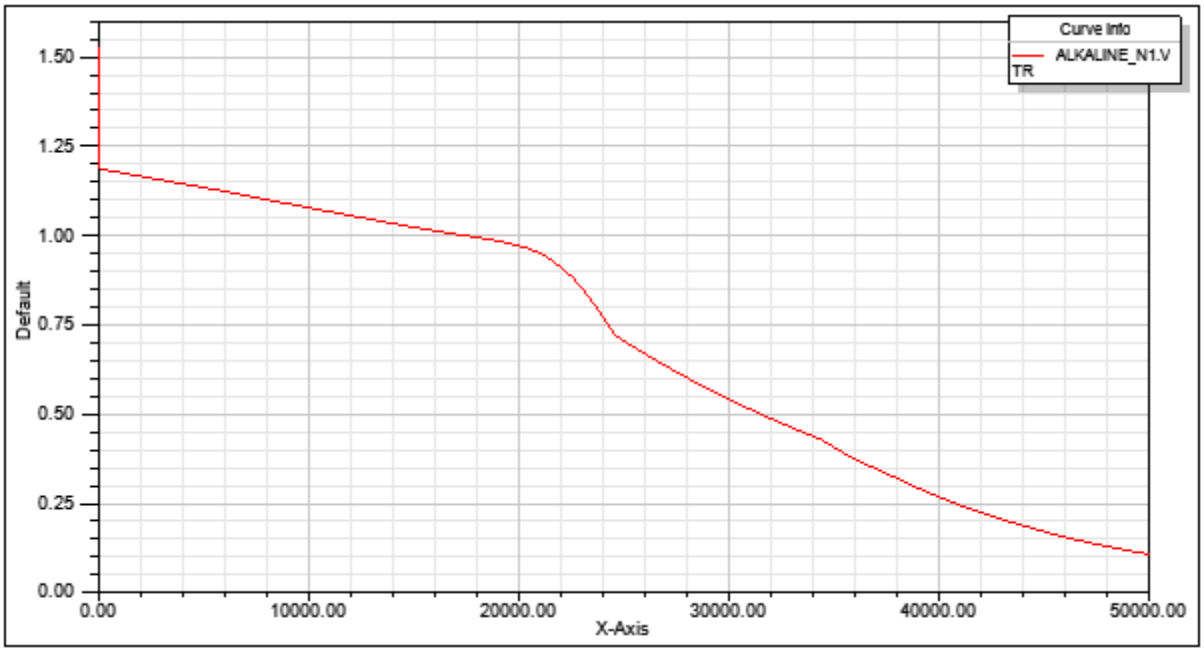

Figure 3. Simulation results-Output Voltage of Battery showing voltage drop as battery is discharged through resistor R1.

Top

References

BATTCELL Generic Battery

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

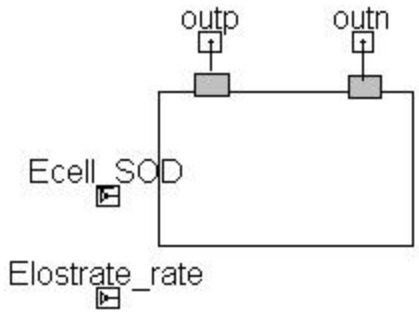

Figure 1. Component symbol

Description

This block represents a Generic battery. The parameter SOC indicates the state of charge with 1 being CHARGED and 0 being DISCHARGED.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

MODEL BATTCELL ?InstanceName(@InstanceName):(@(Refbase)@(ID)) outp:= %0, outn:= %1 (Trate:= @Trate, Capacity:= @Capacity, Rs:= @Rs, SOC_IC:= @SOC_IC, Ecell_SOD:= @Ecell_SOD, Elostrate_rate:= @Elostrate_rate) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
outp	Positive Pin	Electrical terminal
outn	Negative Pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Trate	Internal Time Constant	real	10 [s]
Capacity	Nominal Capacity	real	1 [A*hours]
Rs	Series Resistance	real	0.1 [Ohm]
SOC_IC	Initial State of Charge	real	1
Ecell_SOD	Lookup table of cell voltage vs State of Discharge	real	1
Elostrate_ rate	Lookup table of lost rate vs dis-charge rate	real	0

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
SOC	State of Charge	Output	real
I	Battery current	Output	real

V	Battery voltage	Output	real
SOC_EFF	Effective State of Charge	Output	real

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Example

Example of a Generic Battery supplying a resistive load. The results show the battery voltage. It can be seen how the voltage drops as the battery is discharged.

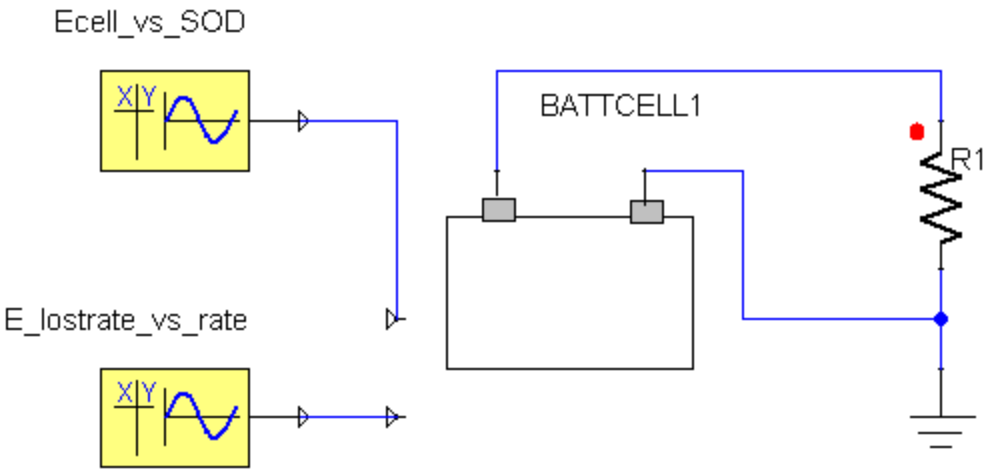

Figure 2. Application example of the Generic Battery Cell.

Table 4. System Parameters

Component	Parameter	Value [unit]
Generic Battery BATTCELL1	Trate	10 [s]
	Capacity	1 [AHour]
	Rs	0.01 [Ohm]
	Ecell_SOD	Ecell_vs_SOD.VAL
	Elostrate_rate	E_lostrate_vs_rate.VAL

Resistor R1	R	10 [Ohm]
2D LookupTable XY (Ecell_vs_SOD)	CH_FILE	ExampleGenericBatteryCell_SSH_Ecell_vs_SOD.mdx
2D LookupTable XY (E_lostrate_vs_rate)	CH_FILE	ExampleGenericBatteryCell_SSH_E_lostrate_vs_rate.mdx

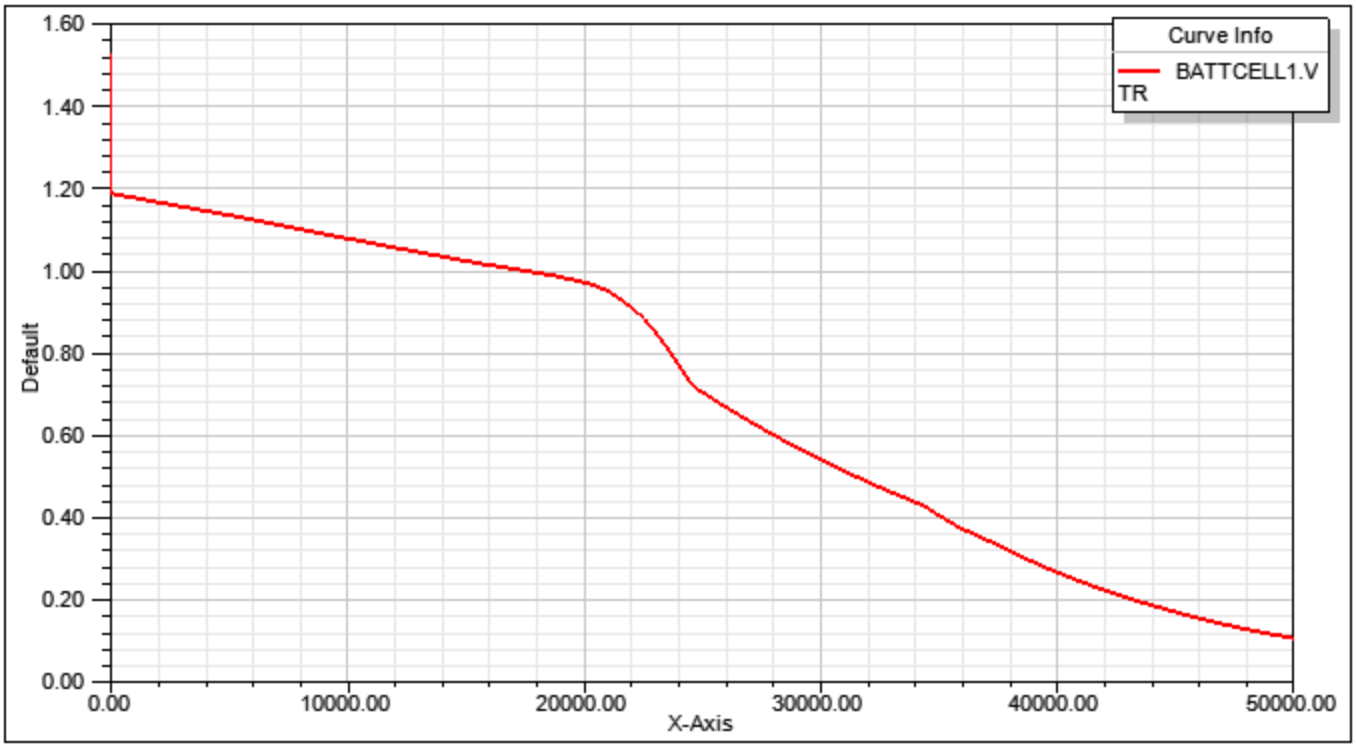

Figure 3. Simulation results-Output Voltage of Battery showing voltage drop as battery is discharged through resistor R1.

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References

Power Load

POWER_L Power Load

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

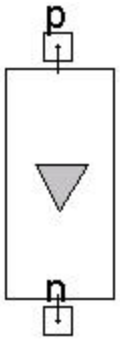

Figure 1. Component symbol

Description

It acts as a load that demands as much power as indicated by power. It has a limitation on the maximum current that it can sink.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

MODEL POWER_L ?InstanceName(@InstanceName):(@(Refbase)@(ID)) p:= %0, n:= %1 (Power:= @Power, Imax:= @Imax) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
p	Positive Pin	Electrical terminal
n	Negative Pin	Electrical terminal

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Power	Power Load (Must be > zero)	real	100 [W]
Imax	Maximum Current (Must be > zero)	real	1000 [A]

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Example

Example of a Power Load demanding a constant power. There is a current limit of 100 Amps. The results show the current and voltage.

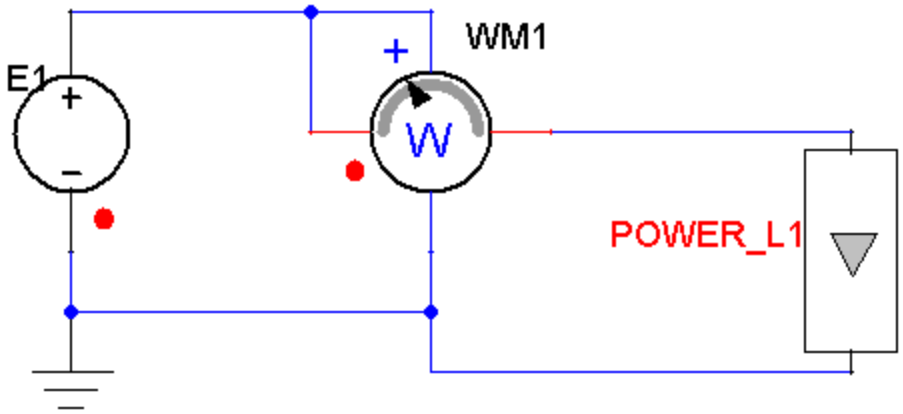

Figure 2. Application example of the Power Load model.

Table 3. System Parameters

Component	Parameter	Value [unit]
Power Load POWER_L1	Power	100 [W]
	Imax	100 [A]
Voltage Source (Sinusoidal) E1	AMPL	20 [V]
	FREQ	50 [Hz]
	Offset	30 [V]

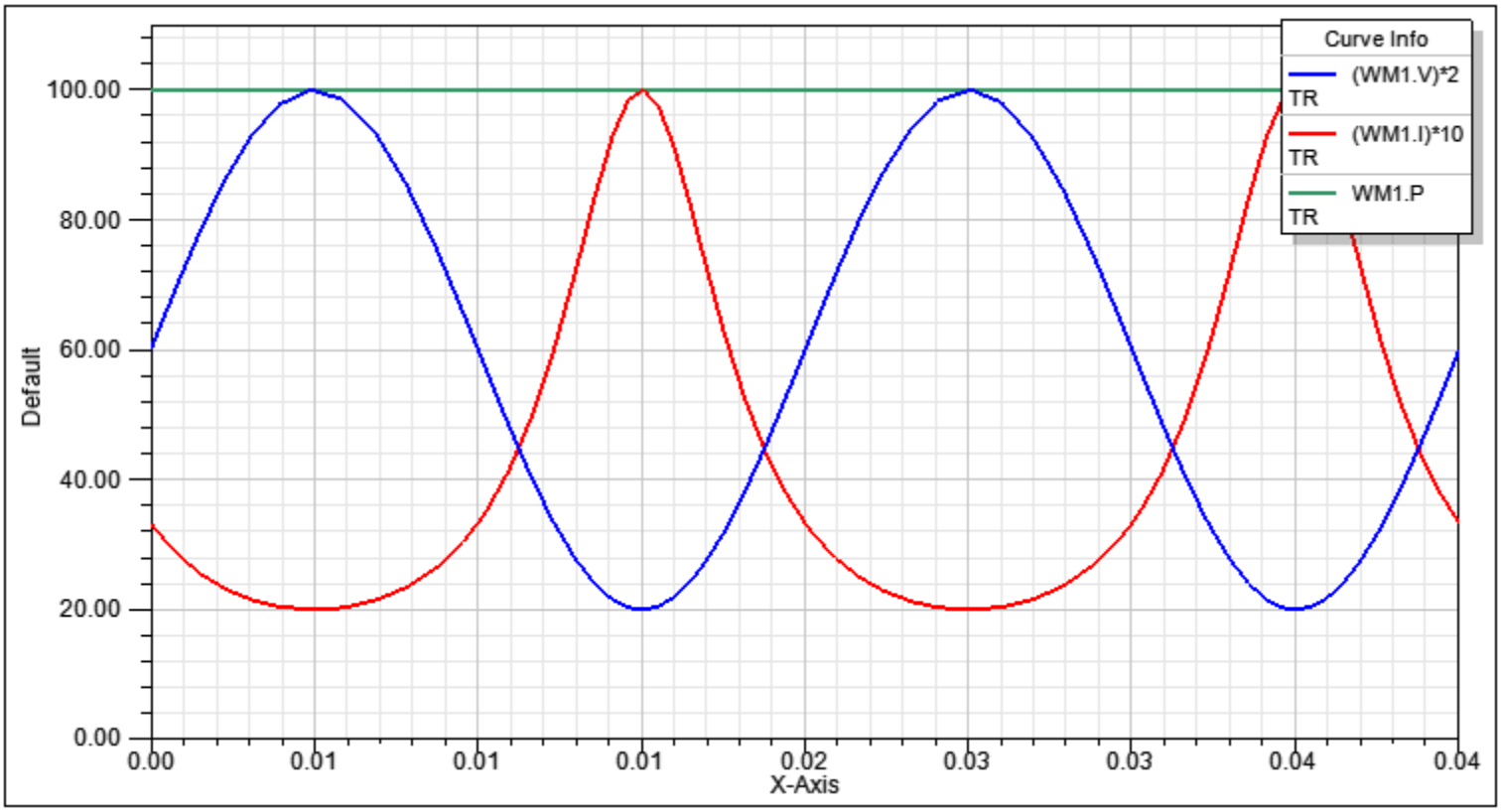

Figure 3. Simulation results-Voltage (WM1.V*2), Current (WM1.I*10) and Power (WM1.P) measured by the power meter.

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References

Solar Systems

- Irradiance (Irradiance)
- Solar Cell (SOLARCELL)

Irradiance

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

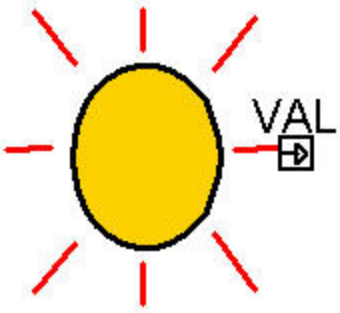

Figure 1. Component symbol

Description

This block represents aa irradiance model.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

MODEL Irradiance ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (Irradiance:= @Irradiance) SRC: DB(Lib:=@ModelLibraryName) ;

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Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
Irradiance	Irradiance input	real	1 [W/m^2]

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
Iph	VAL	Irradiance output	real

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Example

Example of a Solar Cell System excited with an Irradiance source. The results show the irradiance, the output voltage and output power.

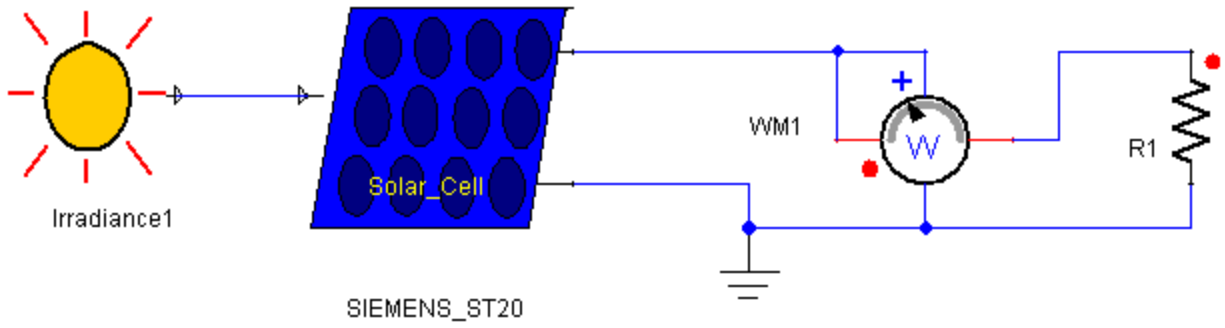

Figure 2. Application example of the Solar Cell System.

Table 3. System Parameters

Component	Parameter	Value [unit]
Solar Cell SIEMENS_ST20	Ga	Irradiance1.VAL
	TEMP_AMB	20 [cel]
	Rs	0.01 [Ohm]
	K2	0.03 [Km^2/W]
	Jo	0.001 [A/K]
Resistor R1	R	20 [Ohm]
Irradiance IRRADIANCE1	Irradiance	100+500*sin(Time)

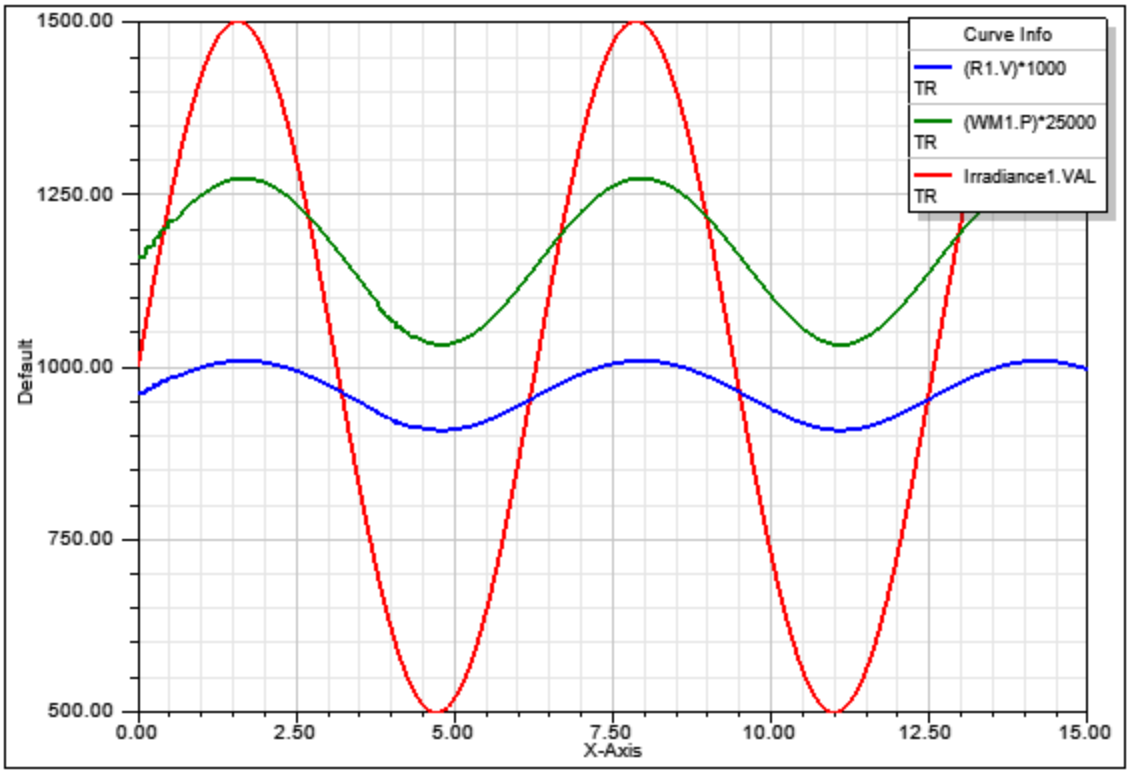

Figure 3. Simulation results-Irradiance (Irradiance1.VAL), scaled Output Power (WM1.P*25000), and scaled Output Voltage (R1.V*1000).

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References

SOLARCELL Basic Solarcell

Library: SMPS	Modeling Language: SML	Version Number: Twin Builder 2025.2

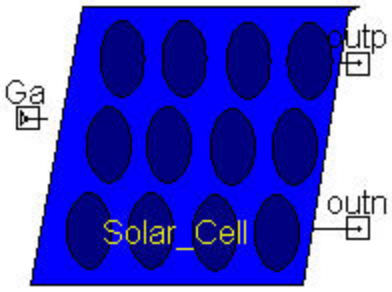

Figure 1. Component symbol

Description

This block represents a basic solar cell model.

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Assumptions and Limitations

Top

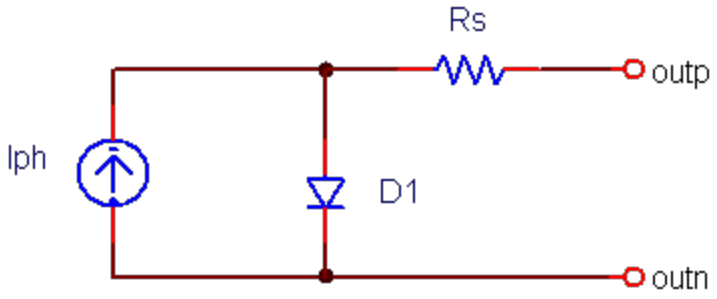
Mathematical Description

$$I_o = I_{ph} - I_{sat}\left(e^{\frac{q}{A \cdot K \cdot T_{cell}}(V_o + R_s \cdot I_o)} - 1 \right)$$

$$I_{sat}(T_{cell}) = I_{sat}(T_{ref})\left(\frac{T_{cell}}{T_{ref}}\right)^3 \left(e^{\frac{q \cdot E_{GO}}{K \cdot T_{cell}}\left(\frac{T_{cell}}{T_{ref}} - 1\right)} \right)$$

$$I_{ph} = K_1 \cdot G_a + J_o \cdot (T_{cell} - T_{ref})$$

$$T_{cell} = T_{amb} + K_2 \cdot G_a$$



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Netlist Syntax

MODEL SOLARCELL ?InstanceName(@InstanceName):(@(Refbase)@(ID)) outp:= %0, outn:= %1 (Isat_0:= @Isat_0, A:= @A, TEMP_CELL_0:= @TEMP_CELL_0, Rs:= @Rs, TEMP_AMB:= @TEMP_AMB, Rp:= @Rp, K1:= @K1, Jo:= @Jo, K2:= @K2, Ga:= @Ga) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data type
outp	Positive Pin	Electrical terminal
outn	Negative Pin	Electrical terminal

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Isat_0	Diode saturation current (@TEMP_CELL_0)	real	1e-012 [A]
A	Diode Shape factor	real	1
TEMP_CELL_0	Cell Temperature	real	25 [^{o}C]
Rs	Series Resistance	real	0.01 [Ohm]
TEMP_AMB	Ambient Temperature	real	20 [^{o}C]
Rp	Parallel Resistance	real	10000 [Ohm]
K1	Irradiation to Short-circuit current coefficient	real	1 [A/(W/m^2)]
Jo	Temperature coefficient	real	0.001 [A/K]
K2	Thermal constant	real	0.03 [K*m^2/W]
Ga	Irradiance	real	1 [W/m^2]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
Iph	Photocurrent	Output	real

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Example

Example of a Solar Cell System excited with an Irradiance source. The results show the irradiance, the output voltage and output power.

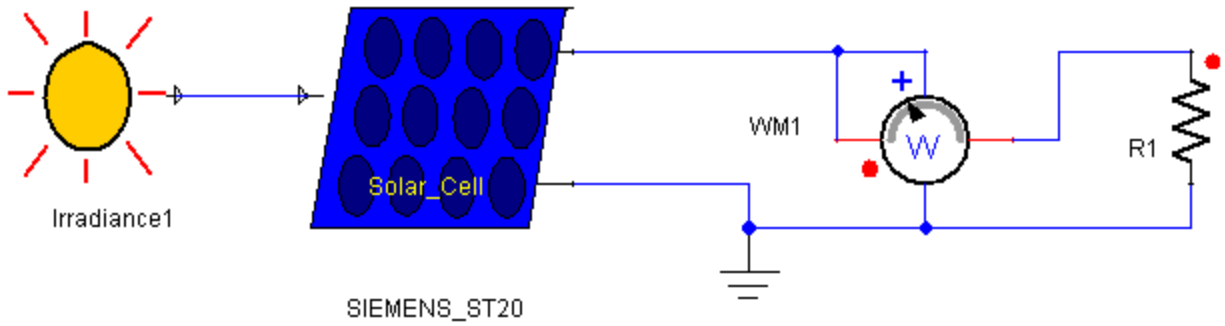

Figure 2. Application example of the Solar Cell System.

Table 4. System Parameters

Component	Parameter	Value [unit]
Solar Cell SIEMENS_ST20	Ga	Irradiance1.VAL
	TEMP_AMB	20 [cel]
	Rs	0.01 [Ohm]
	K2	0.03 [Km^2/W]
	Jo	0.001 [A/K]
Resistor R1	R	20 [Ohm]
Irradiance IRRADIANCE1	Irradiance	100+500*sin(Time)

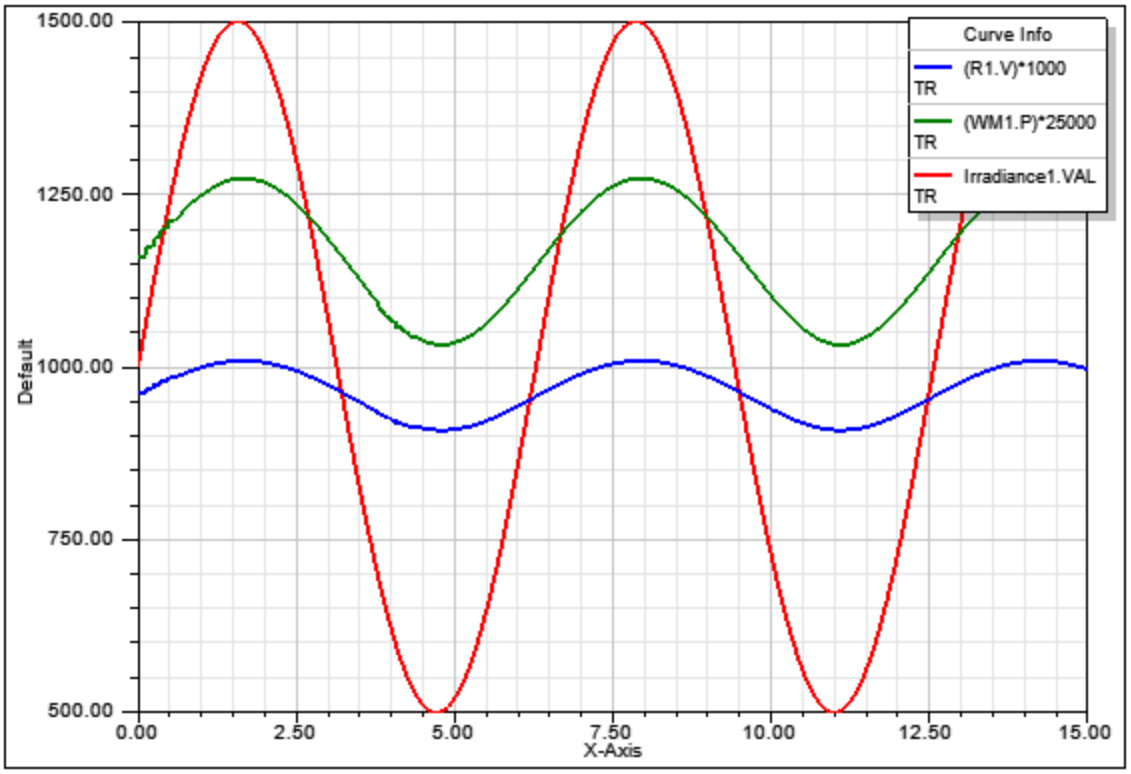

Figure 3. Simulation results-Irradiance (Irradiance1.VAL), scaled Output Power (WM1.P*25000), and scaled Output Voltage (R1.V*1000).

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