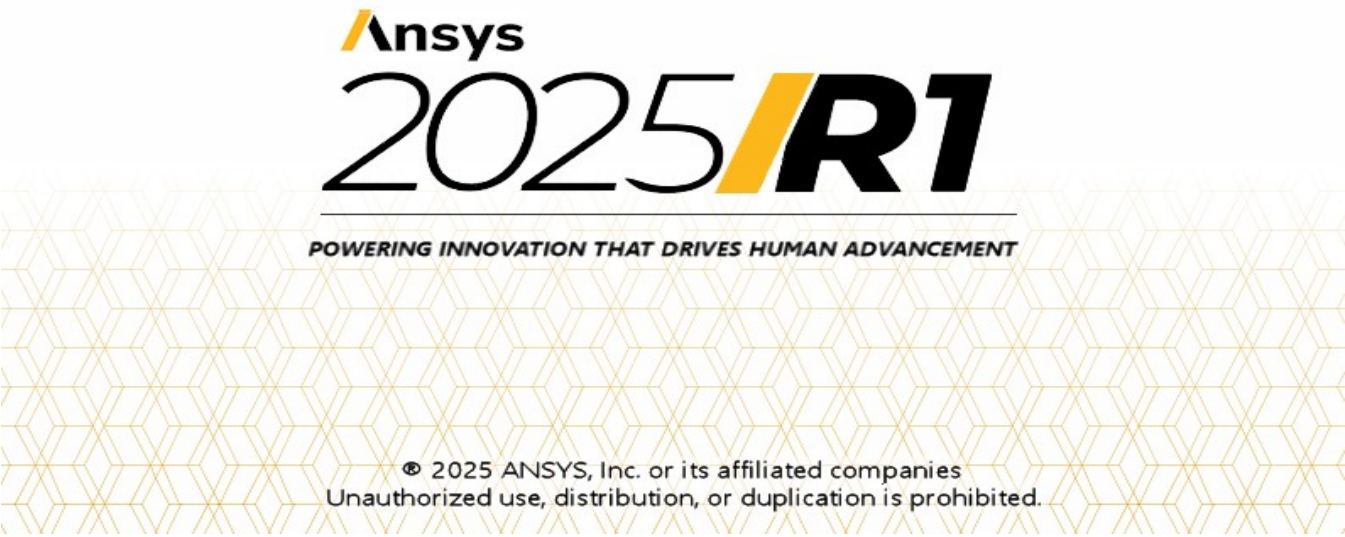

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SIwave™ Help

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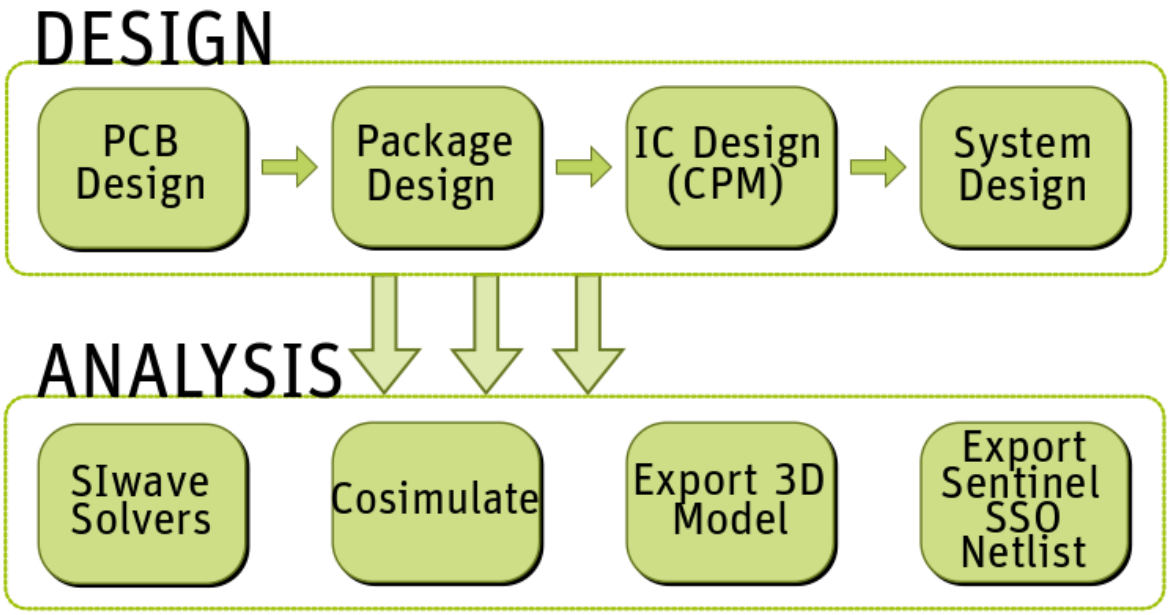
1 - Welcome to SIwave Help



Chip-Package-System (CPS) methodology in SIwave combines the Integrated Circuit (IC) model or chip, the packages that contain the chips, and the printed circuit board (PCB) into a single system for simulation. The CPS process flow includes both design and analysis activities.

Design activities include:

- **PCB Design** – Import and set up the PCB.
- **Package Design** – Import and merge packages with the PCB.
- **IC Design (CPM)** – Import and merge the IC models with the corresponding packages on the PCB.
- **System Design** – Complete the integrated PCB System by adding vias, solder balls, and decoupling components.

Analysis activities include:

- **SIwave Solvers** – Simulate with the field and circuit solvers built into SIwave.
- **Cosimulate** – Cosimulate with circuit and thermal tools.
- **Export 3D Model** – Export a 3D model to MCAD solvers.
- **Export Sentinel SSO Netlist** – Export a SPICE netlist with CPP header for Sentinel-SSO flow.

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Help Topic Conventions

The following documentation conventions are used in the help:

- Procedures are presented as numbered lists. A single bullet indicates that the procedure has only one step.
- Command font is used for:
  - Command line prompts that should be typed exactly as written.
  - Script examples.
- Bold type is used for the following:
  - Names of windows, workspaces, menu commands, and options.
    - Menu commands are often separated by angle brackets (e.g., **File** > **Open**).
  - Labeled keys on the computer keyboard (e.g., **Enter**).
- Italic type is used for the following:
  - Emphasis.
  - Publication titles.
- The plus sign (+) is used between keyboard keys to indicate that you should press the keys at the same time (e.g., “Press **Shift**+**F1**” means to press the **Shift** key and, while holding it down, press the **F1** key). You should always depress the modifier key or keys first (e.g., **Shift**, **Ctrl**, **Alt**, or **Ctrl**+**Shift**), continue to hold it/them down, and then press the last key in the instruction.

Using the Online Help Search Function

When you enter words or strings to search for in the help, the search engine, by default, lists all topics in which any of the words occur (e.g., if you enter "voltage source" without the quotation marks, the results show all topics that contain "voltage" or "source").

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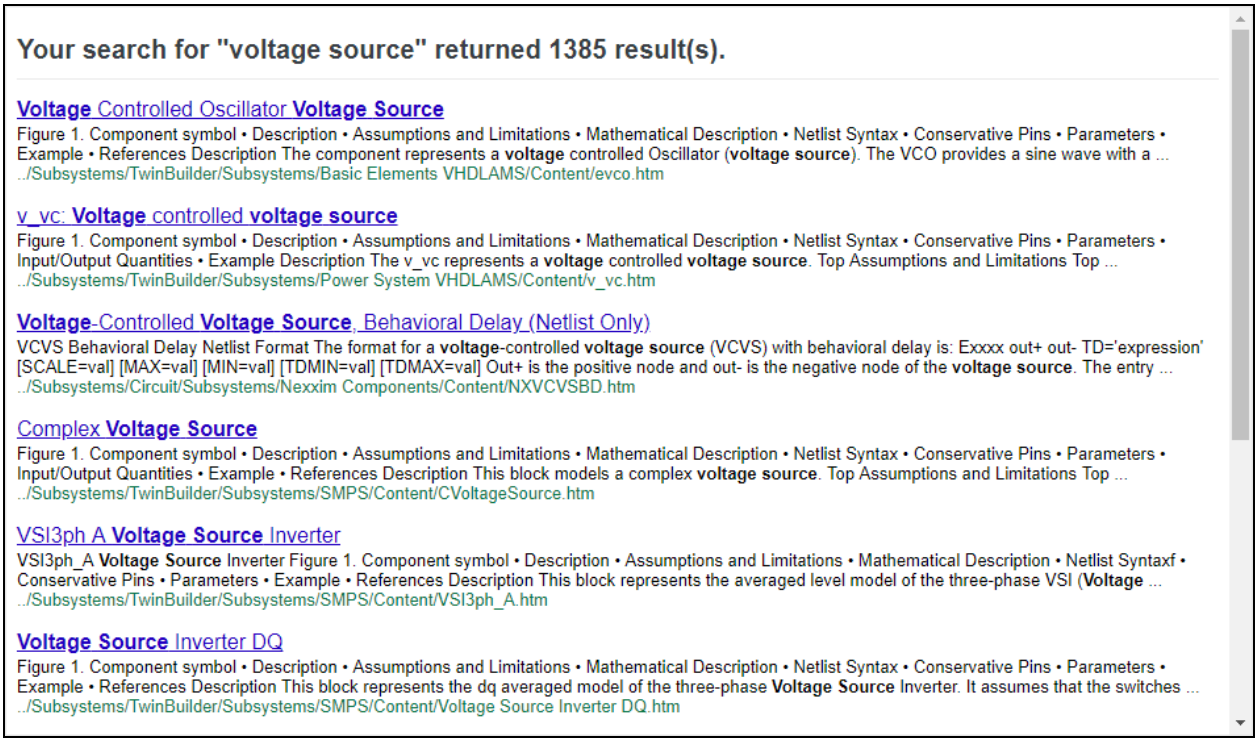

This method probably provides more hits than you want. The Search function in the help provides several methods for making searches more specific.

Performing a Basic Search

1. Type the words or string in the **Search** box.
   - The **Search** box includes a drop-down filter for specifying a product but not including its scripting guide (e.g., SIwave), specifying a product's scripting guide (e.g., SIwave Scripting), or searching across all Electronics products (for example, All Products). When

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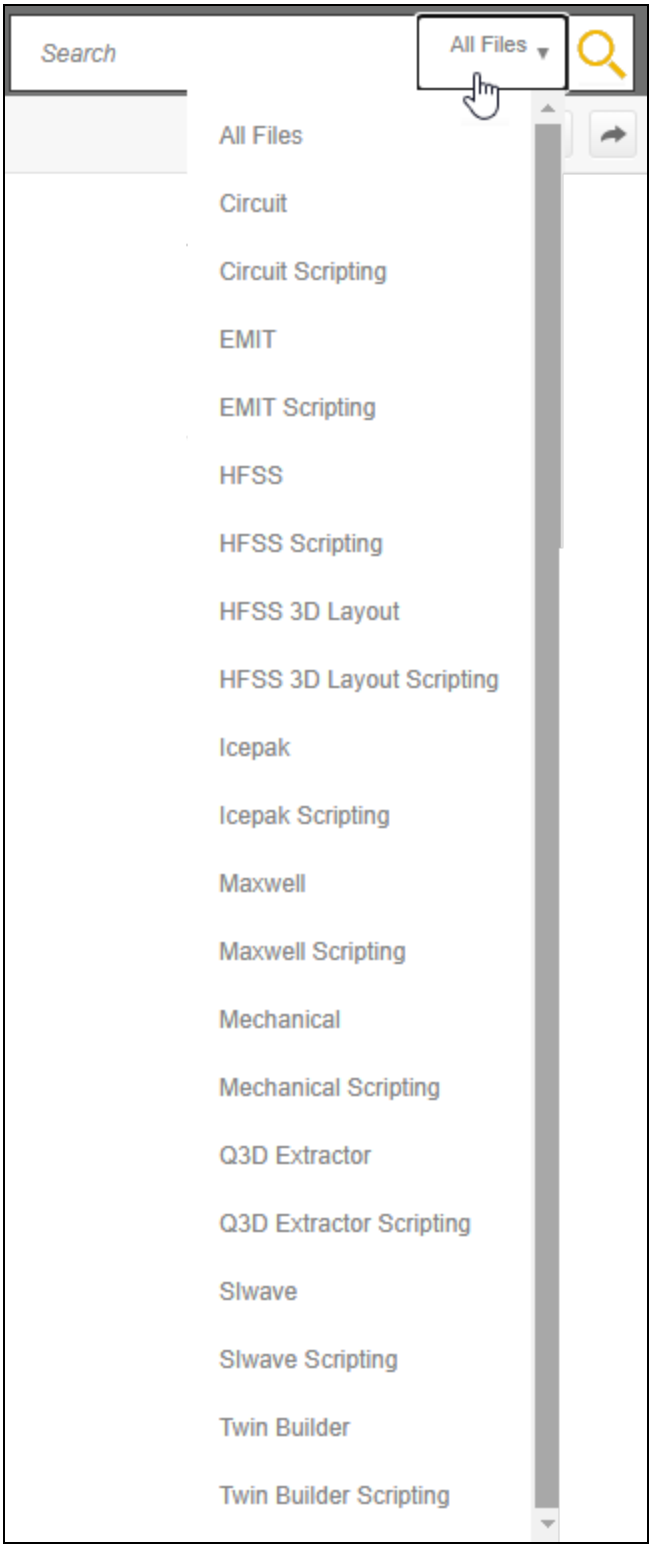
you change the filter, the results dynamically reflect the selected filter.



2. Click on the topic you want in the list results.

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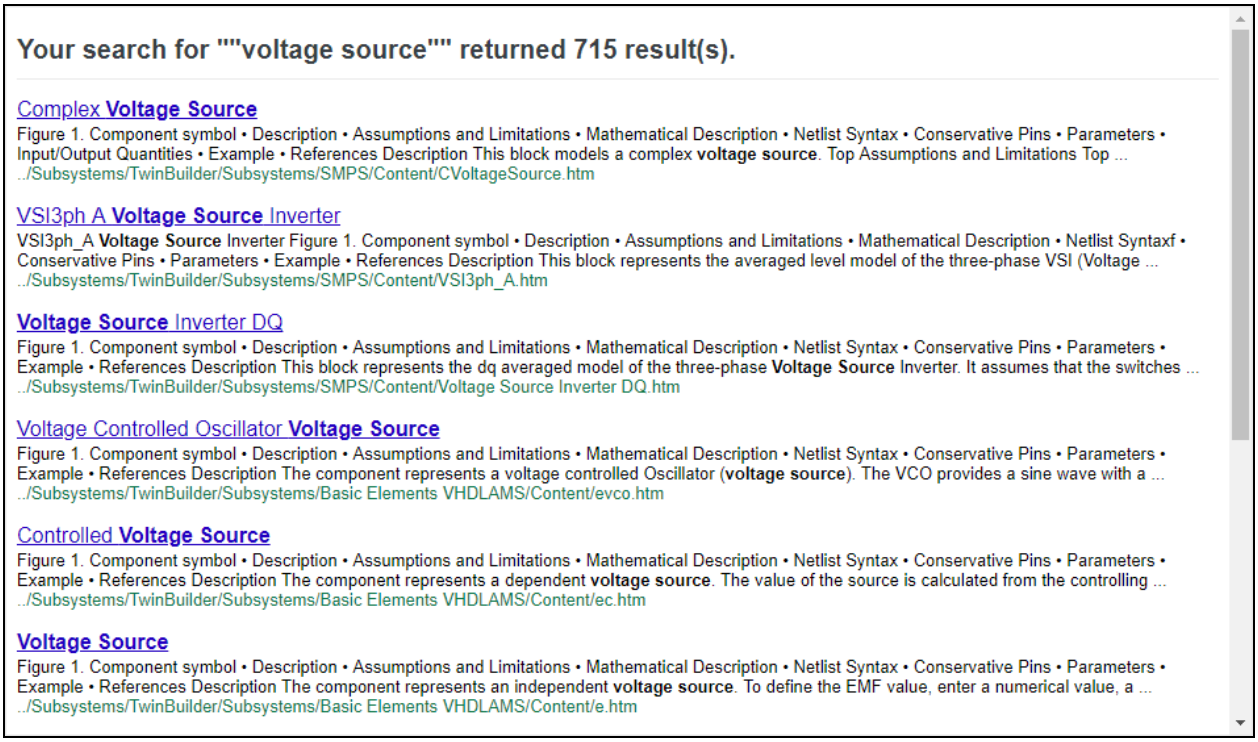
- If you want to view a different topic, press your browser's back button to return to the list results.
- To turn off highlighting on the current page, click the **Remove Highlights** icon .

Searching with Quotation Marks

If you enter "`voltage source`" (with quotation marks), the results show all topics that include the phrase.



As you can see, this returns far fewer results than the basic search.

To further limit the results, you can enter additional words, such as: "`voltage source`" `transient solver`

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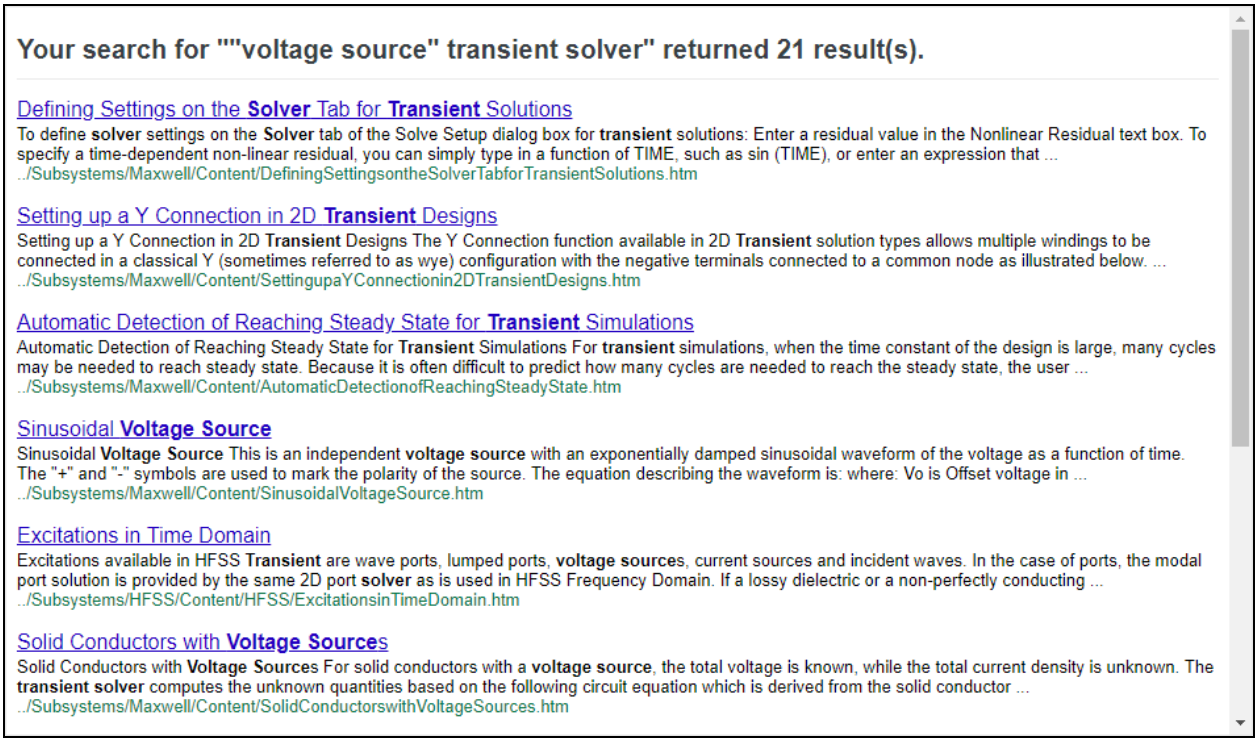

Note:

- Searches are not case sensitive, so you can type your search in uppercase or lowercase characters.
- You may search for any combination of letters (a-z) and numbers (0-9).
- Punctuation marks (period, colon, semicolon, comma, hyphen) are ignored during a search.
- When searching for a file name with an extension, group the entire string in quotation marks (e.g., "filename.ext").

Using Boolean Operators

These choices affect the number of topics listed.

Operator (s)	Usage	Example(s)
AND + &	Lists all topics that contain all of the terms.	Net AND Selection Net + Selection Net & Selection
OR	Lists all topics that	Net OR Selection

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Operator (s)	Usage	Example(s)
|	contain any of the terms.	Net | Selection
NEAR	Lists all topics that contain the terms near the other terms.	Net NEAR Selection
NOT ! ^	Lists all topics that contain the first term but not the second.	Net NOT Selection Net ! Selection Net ^ Selection

Use parentheses to group terms and operators. For example:

- solver AND (Circuit) NOT HFSS NEAR dynamic
- solver AND (HFSS OR Circuit) NOT (Q3D OR 2d) NEAR dynamic
- "dynamic link" ! (HFSS | circuit)

> **Important:**
>
> Because the characters +, &, |, !, and ^ are used as operators, you cannot search for them in the help. Doing so will result in an error.

SIwave Getting Started Guides

The **Examples/SIwave** subfolder within your Electronics Desktop installation includes sample .ANF files.

To familiarize yourself with some of the features of SIwave, you can use these files along with two Getting Started Guides:

- PCB Model

  This *Getting Started Guide* is written for SIwave beginners as well as experienced users who would like to quickly familiarize themselves with the capabilities of SIwave. This guide leads you step-by-step through creating, solving, and analyzing the results of simulating nets and planes on a PCB.

  By following the steps in this guide, you will learn how to perform the following tasks in SIwave:
  - Draw a geometric model
  - Specify solution settings for a design
  - Validate a design's setup

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- Run an SIwave simulation
- Create 2D plots of the results

- SIwave-CPA Package Model

  This *Getting Started Guide* is written for SIwave beginners as well as experienced users who would like to quickly familiarize themselves with the capabilities of SIwave-CPA. This guide leads you step-by-step through importing a package design, setting up and performing an extraction analysis, and viewing the results of the extractions.

  By following the steps in this guide, you will learn how to perform the following tasks in SIwave-CPA:

  - Import a geometric package model
  - Specify parameter settings for the extraction
  - Run an SIwave-CPA RLCG extraction
  - Review the results in tabular and graphical format

System Requirements

SIwave supports certain versions of Windows and Linux. For supported platforms and system requirements, go to the Platform Support website and select the following document:

Ansys 2025 R1 **- Platform Support by Application / Product (PDF)**

This document covers all Ansys products. Refer to the **Electronics Applications** section.

Limitations of Linux Installations:

While the majority of the Ansys Electromagnetics Suite applications and features are supported on both Windows and Linux platforms, some are not supported on Linux. See the following topic for details:

Windows vs. Linux Installations

Obtaining Information about the Software and Release

To obtain information about the software and release, click **File** > **About SIwave**.

The **About ANSYS® Electromagnetics Suite [release number]** window appears, listing information about the product.

To view a PDF of changes in the latest release, click **File** > **What's New**.

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2 - Introducing SIwave

SIwave is a software solution for power-ground plane and signal integrity analysis. It employs a powerful full-wave analysis engine to generate both frequency-domain and time-domain results. Using the highly optimized internal field solver, SIwave simulates complete board/package designs with full-wave accuracy. Simulation results can be reported graphically using advanced 2D and 3D plotting methods.

SIwave provides a seamless and integrated design flow that allows you to easily import design geometry from commercial layout packages, including:

- Mentor Graphics Board Station, Expedition, and PADS Layout

The SIwave layout editor allows you to draw your own structure, or to modify an imported geometry. SIwave can verify and analyze complex PCBs containing multiple arbitrarily shaped power and ground layers and any number of vias and signal traces. SI effects that can be modeled include:

- Resonance frequencies of complete power and ground structures
- Power and ground bounce
- Simultaneous switching noise
- Impedance discontinuities due to changes in signal layers or split supply planes
- Noise coupling between signal lines and supply planes
- Time-domain effects such as propagation delay, rise and fall times, reflections and ringing
- Frequency-domain phenomena such as resonant modes and S, Y, and Z-parameters
- Electromagnetic interference

Another key feature of SIwave is the ability to export SPICE files. SIwave enables you to export SPICE files in HSPICE, Maxwell SPICE, or Nexxim formats.

The following figure shows the main capabilities of SIwave.

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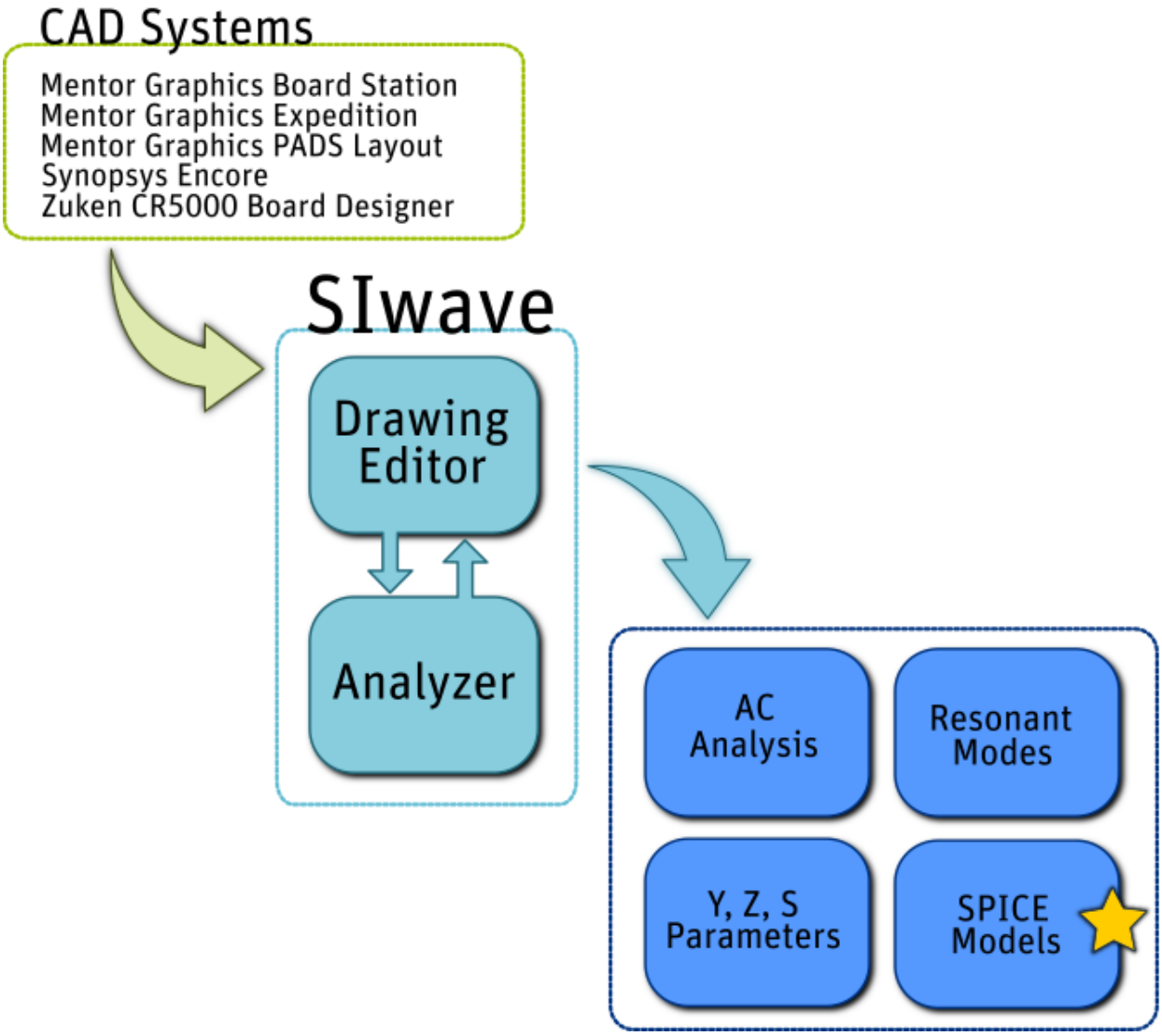

Launching SIwave

SIwave can launch from Windows or from the command line.

Launching SIwave from Windows

1. Use the Start Menu to navigate to **Ansys EM Suite [Version]** > **Ansys SIwave [Version]**. Alternately, double-click the **Ansys SIwave** icon on the desktop:

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SIwave opens, and the **Ansys Product Improvement Program** window appears.

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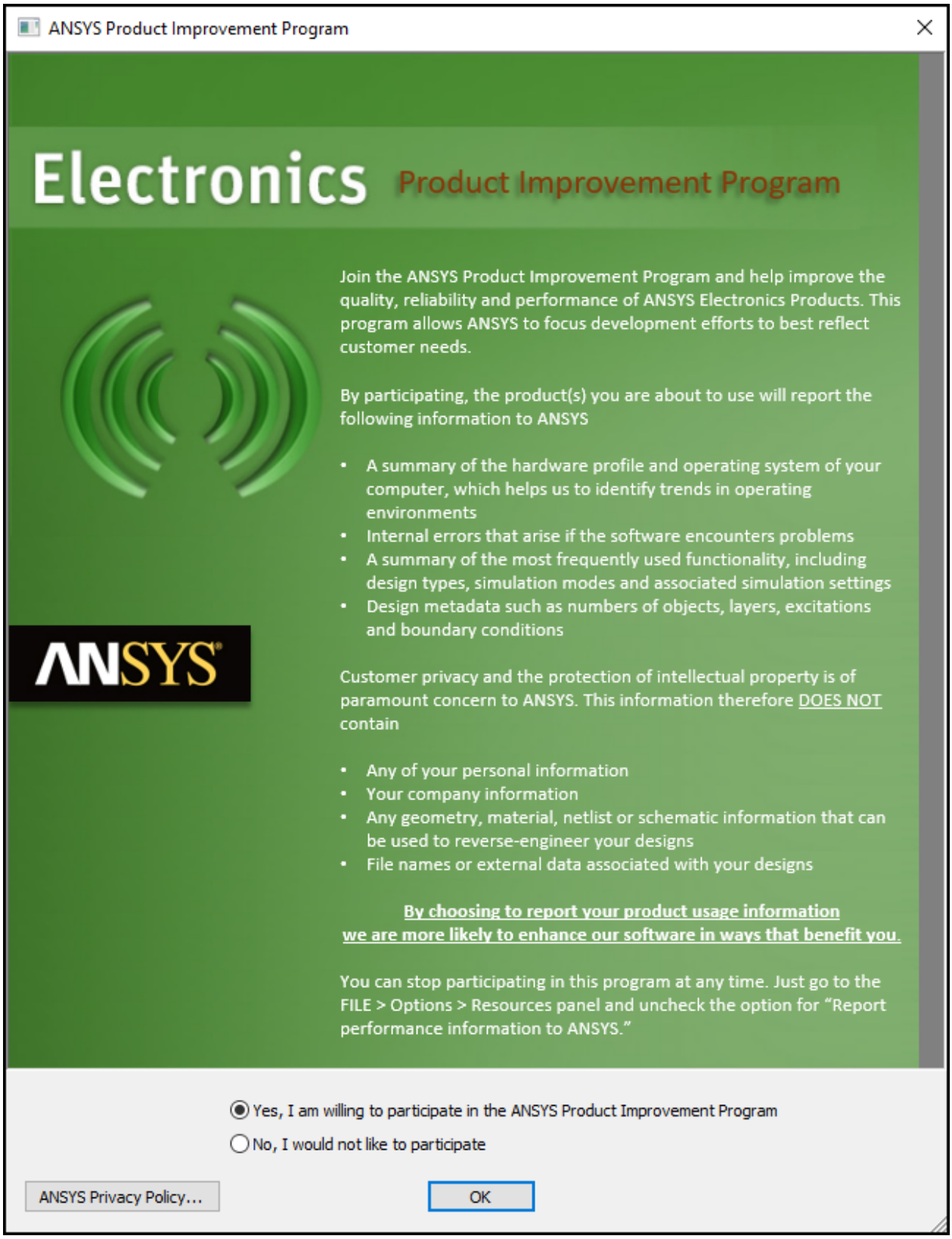

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2. If you wish to view the full privacy policy, click **Ansys Privacy Policy**.
3. Select **Yes** to participate or **No** to decline. For more information (including instructions for changing this selection), see: Ansys Product Improvement Program.
4. Click **OK**.

Ansys Product Improvement Program

SIwave is covered by the Ansys Product Improvement Program, which enables ANSYS, Inc., to collect and analyze anonymous usage data reported by our software without affecting your work or product performance. Analyzing product usage data helps us to understand customer usage trends and patterns, interests, and quality or performance issues. The data enables us to develop or enhance product features that better address your needs.

How to Participate

The program is voluntary. To participate, select **Yes** when the Product Improvement Program window appears. Only then will collection of data for this product begin.

How the Program Works

After you agree to participate, the product collects anonymous usage data during each session. When you end the session, the collected data is sent to a secure server accessible only to authorized Ansys employees. After Ansys receives the data, various statistical measures such as distributions, counts, means, medians, modes, etc., are used to understand and analyze the data.

Data We Collect

For all products that offer the Ansys Product Improvement Program, we only collect anonymous data such as session statistics, hardware information, types of loading, solution types, solution statistics, and similar data. The specific data collected varies from product to product.

For Ansys Electronics, we collect the following information:

- Application
  - Build information
  - System information
    - Country
    - Country code
    - CPU architecture
    - CPU brand
    - CPU identifier
    - Graphics card

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    - Operating system
    - Operating system version
    - Processor count
    - Time zone
    - Total RAM value
- Session
    - Workbench session
    - Total CPU time
    - Execution mode
    - Start method
    - Number of processes
    - Number of compute nodes (HPC)
    - Session begin
    - Session end
- Mesh
    - Number of nodes
    - Number of elements
    - Number of zones
    - Number of faces

Data We Do Not Collect

The Product Improvement Program does not collect any information that can identify you personally, your company, or your intellectual property. This includes (but is not limited to): names, addresses, file names, part names, geometry- or design-specific inputs, material property values, etc. We make no record of where we collect data from.

Opting Out of the Program

You may stop your participation in the program any time you wish. To do so, navigate to **FILE** > **Options**. From the **Resources** tab, uncheck the **Report performance information to ANSYS** check box. Then click **OK**. Data will no longer be collected or sent.

The ANSYS, Inc., Privacy Policy

All Ansys products are covered by the ANSYS, Inc., Privacy Policy, which you can read here.

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Frequently Asked Questions

1. *Am I required to participate in this program?*

   No, your participation is voluntary. We encourage you to participate, however, as it helps us create products that will better meet your future needs.

2. *Am I automatically enrolled in this program?*

   No. You are not enrolled unless you explicitly agree to participate.

3. *Does participating in this program put my intellectual property at risk of being collected or discovered by ANSYS?*

   No. We do not collect any project-specific, company-specific, or model-specific information.

4. *Can I stop participating even after I agree to participate?*

   Yes, you can stop participating at any time.

   To do so:

   - Click **FILE** > **Options**.
   - On the **Resources** tab, deselect the **Report performance information to ANSYS** check box.
   - Click **OK**.
   - Data will no longer be collected or sent.

5. *Will participation in the program slow the performance of the product?*

   No, the data collection does not affect the product performance in any significant way. The amount of data collected is very small.

6. *How frequently is data collected and sent to Ansys servers?*

   The data is collected during each use session of the product. The collected data is sent to a secure server once per session, when you exit the product.

7. *Is this program available in all Ansys products?*

   Not at this time, although we are adding it to more of our products at each release. The program is available in a product only if this Ansys Product Improvement Program description appears in the product documentation, as it does here for this product.

8. *If I enroll in the program for this product, am I automatically enrolled in the program for the other Ansys products I use on the same machine?*

   Yes. Your enrollment choice applies to all Ansys products you use on the same machine. Similarly, if you end your enrollment in the program for one product, you end your enrollment for all Ansys products on that machine.

9. *How is enrollment in the Product Improvement Program determined if I use Ansys products in a cluster?*

   In a cluster configuration, the Product Improvement Program enrollment is determined by the host machine setting.

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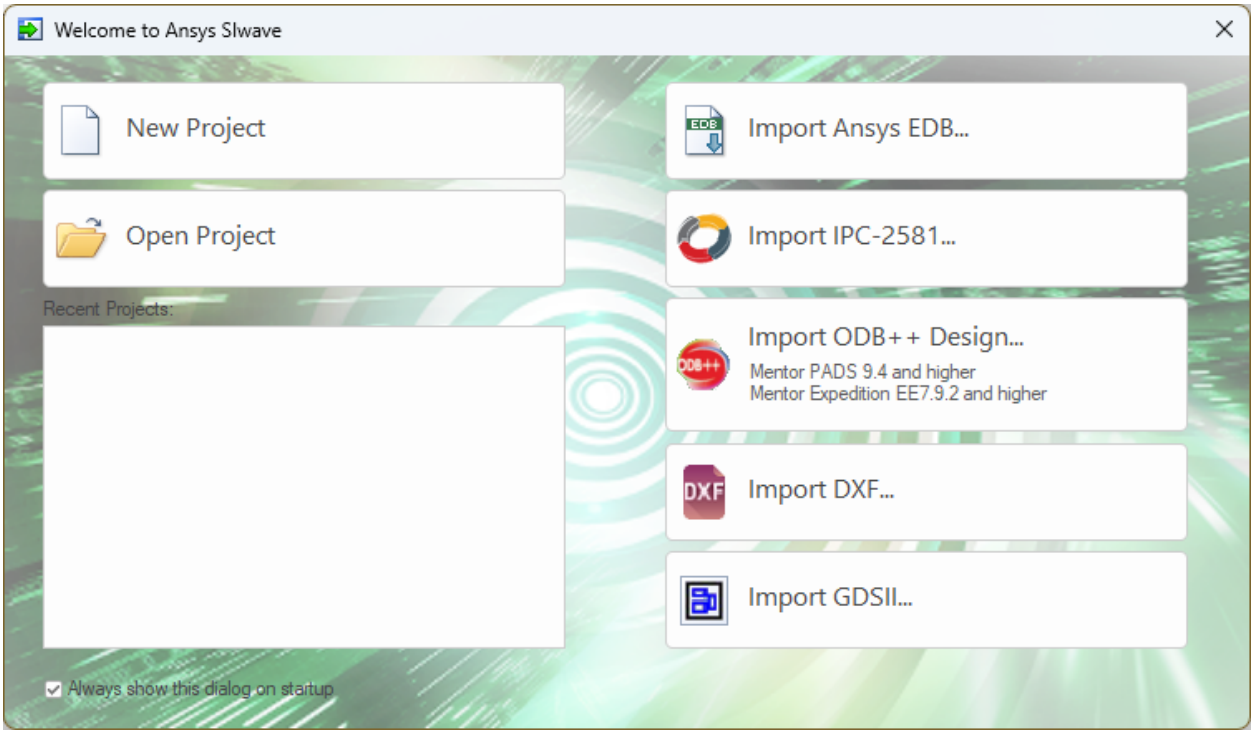
Welcome Screen

When SIwave opens for the first time, a **Welcome** window appears containing buttons for frequently used actions:

- **New Project** – Creates a new, blank project.
- **Open Project** – Opens an existing SIwave project (*.siw).
- **Recent Projects** – Displays a list of the most recently opened projects. Click a project to reopen it.
- **Import ANSYS EDB** – Imports an EDB file. See: Importing Projects.
- **Import IPC-2581** – Imports an IPC-2581 file. See: Importing IPC-2581 Designs.
- **Import ODB++ Design** – Imports an ODB++ design. See: Importing Projects.
- **Import DXF** – Imports a DXF file. See: Importing DXF Files.
- **Import GDSII** – Imports a GDSII file. See: Importing GDSII Files.



If you don't want this window to appear when you start SIwave, deselect the **Always show this dialog on start up** check box:

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To open this window at any time, click the **Welcome Dialog** icon on the left side of the Quick Access Toolbar.

SIwave Workflow Wizard

After importing a project from the Welcome Screen, **SIwave Workflow Wizard** appears to walk you through the steps to be taken getting the project ready for simulation.

Alternately, access the wizard from the Quick Access Toolbar:

1. Click the orange magic wand icon on the **Quick Access Toolbar**.

   The **SIwave Workflow Wizard** opens.

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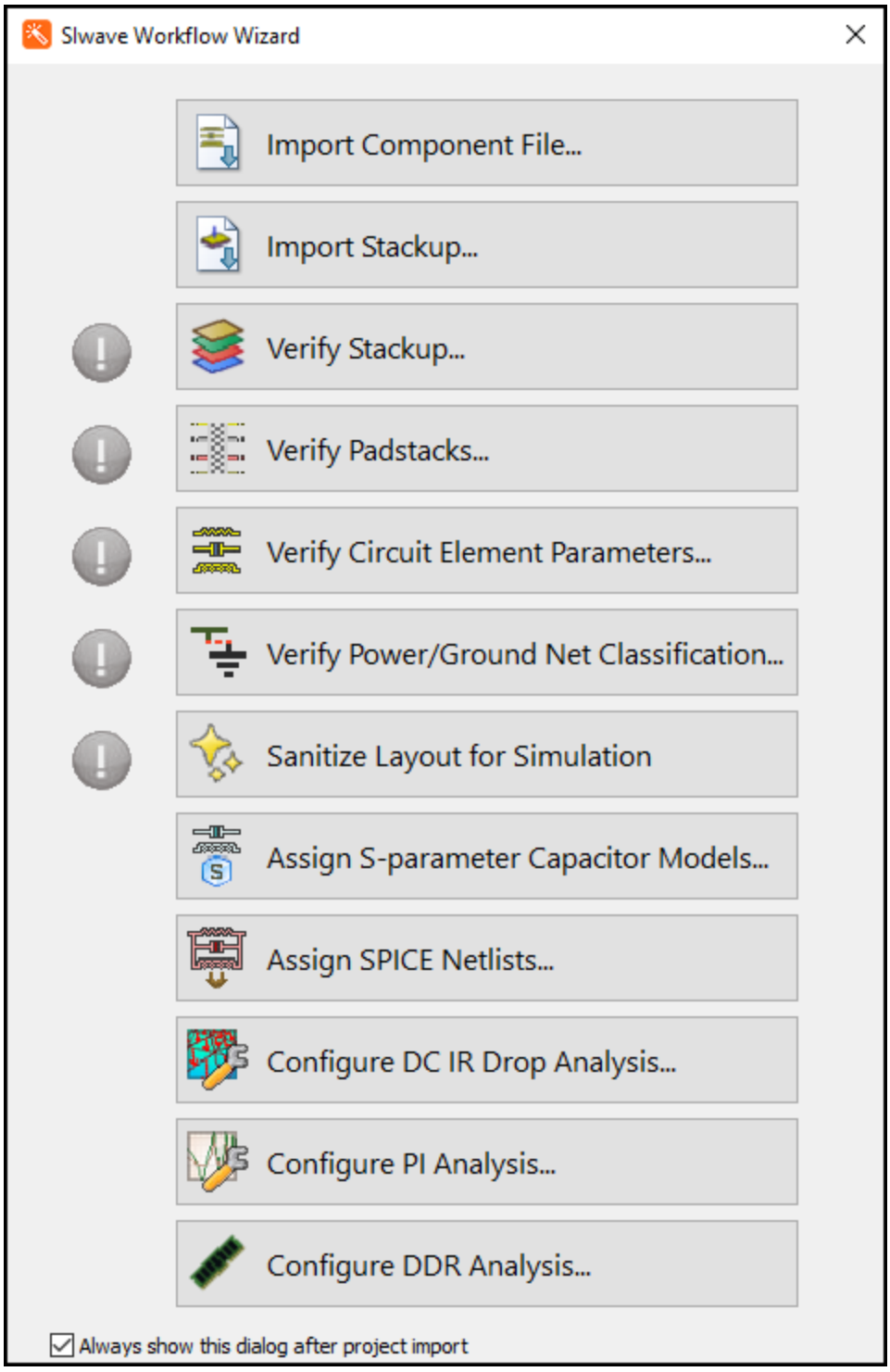

By default, the following actions are available from the wizard:

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- Import Component File
- Import Stackup
- Verify Stackup
- Verify Padstacks
- Verify Circuit Element Parameters
- Verify Power/Ground Net Classification
- Sanitize Layout for Simulation
- Assign S-Parameter Capacitor Models
- Assign SPICE Netlists
- Configure DC IR Drop Analysis
- Configure PI Analysis
- Configure DDR Analysis

2. Click buttons to go through steps, as appropriate.

Disabling the Workflow Wizard

If you no longer want the SIwave Workflow Wizard to display upon importing a project, deselect **Always show this dialog after project import**.

Customizing the Workflow Wizard

The visibility of some Workflow Wizard buttons can be customized by manually editing the file **SIwave_workflow_config.xml**.

This file is stored in the \config subfolder of your Ansys EM installation location.

The buttons you can edit are:

- Import Component File
- Import Stackup
- Assign S-Parameter Capacitor Models
- Assign SPICE Netlists
- Configure DC IR Drop Analysis
- Configure PI Analysis

The XML file lists these buttons, where 1 indicates that the corresponding button is visible and 0 indicates that the button is invisible.

For example, this is the default:

```
<?xml version="1.0" encoding="UTF-8"?>
<WorkflowWizard>
  <ImportComponentFile>1</ImportComponentFile>
```


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```
      <ImportStackup>1</ImportStackup>
      <AssignSparameterCapacitorModels>1</AssignSparameterCapacitorMod
els>
      <AssignSPICENetlists>1</AssignSPICENetlists>
      <ConfigureDCIRDropAnalysis>1</ConfigureDCIRDropAnalysis>
      <ConfigurePIAnalysis>1</ConfigurePIAnalysis>
    </WorkflowWizard>
```

SIwave Desktop

The SIwave Desktop is shown below, with the following areas highlighted:

1. Ribbon Interface
2. Nets Workspace
3. Components Workspace
4. Results Window
5. Modeling Workspace
6. Layers Workspace
7. Properties Workspace
8. Messages Workspace
9. Information/Errors/Warnings Workspace

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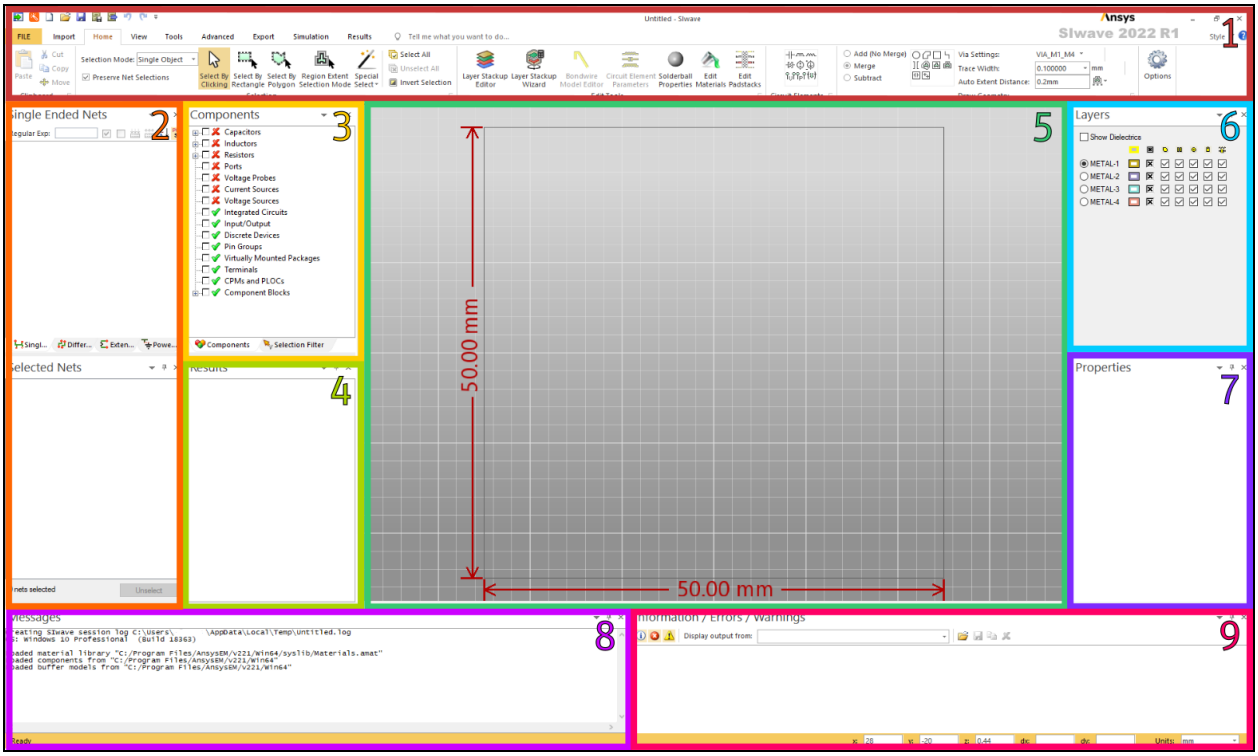

Viewing and Hiding Windows and Workspaces

From the **View** tab, use the **Workspaces** menu to show and hide workspaces.

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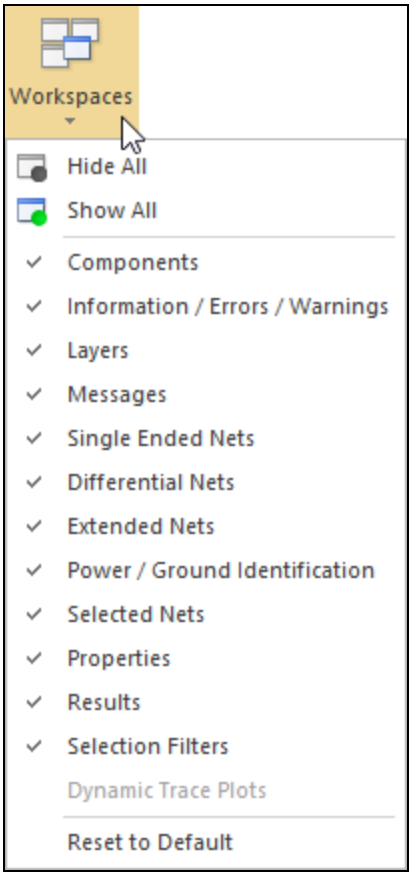
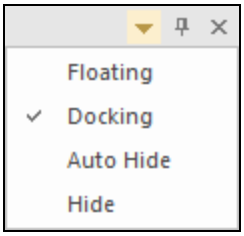


To view or hide any workspace or window in the SIwave desktop:

1. Click **View** > **Workspaces**.
2. Select and deselect items to display or remove them, or use the **Hide All** and **Show All** options.
3. Click **Reset to Default** to restore default settings.

Moving and Resizing Windows and Workspaces

You can move and resize any workspace using the icons at the upper-right area on each window.



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Click the down-arrow to open a menu for setting the window as **Floating** or **Docking**. Docked windows are fixed to their current location, while Floating windows may be moved around the screen by dragging and dropping.

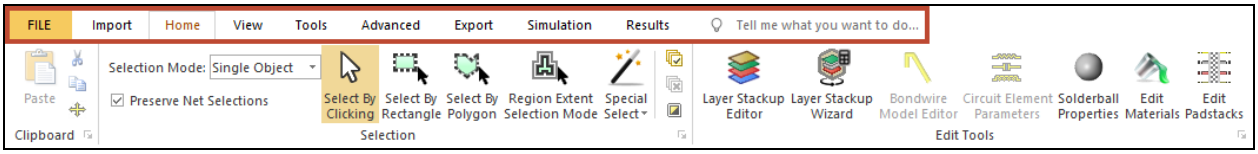
Additional options include:

- **Auto Hide** – hides the window, but leaves its name on the side of the screen for quick access. The pin icon ( ) can also be used to enable Auto Hide.
- **Hide** – removes the window from display. The **X** icon can also be used to do this.

Hidden windows can be brought back at any time using the Workspaces menu.

Ribbon Interface

The SIwave ribbon is the rectangular area across the top of the application. It contains several tabs, each one representing a subset of program functionality. The layout of the ribbon follows a user's typical flow of functionality, and the tabs contain related commands that are organized, grouped, and labeled.



The SIwave ribbon contains the following tabs:

- **FILE** – contains file operations options and SIwave release information.
- **Import** – contains actions for importing files into SIwave.
- **Home** – contains options for selecting and editing objects in the Modeling workspace.
- **View** – contains options for altering the way information is displayed in the Modeling workspace.
- **Tools** – contains tools that aid in design, transformation, and computation.
- **Advanced** – contains additional specialized editing tools.
- **Export** – contains actions for exporting files from SIwave.
- **Simulation** – contains simulation operations.
- **Results** – contains results of previously run simulations.

To the right of the tabs is a lightbulb and the text **Tell me what you want to do**. This is a search bar. Type a query to find related menu options.

To customize ribbon settings, click **FILE > Options**. The **Popular** tab allows you to customize the ribbon's color scheme and layout.

Quick Access Toolbar

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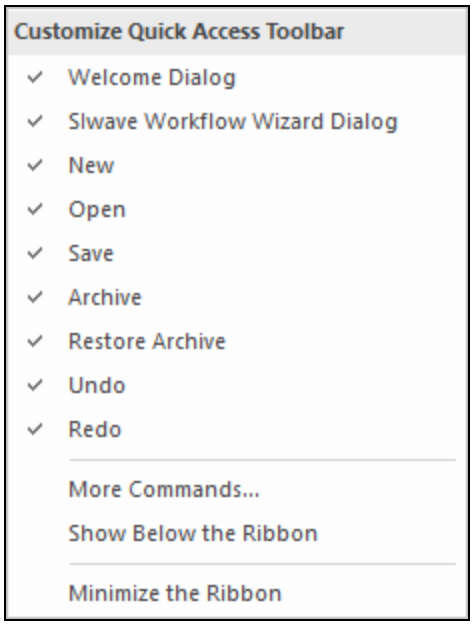
The Quick Access Toolbar (QAT) appears above the ribbon interface.

By default, this toolbar contains the above icons, in order:

- **Welcome Dialog** – reopens the window that appears when SIwave is first loaded.
- **SIwave Workflow Wizard** – opens the SIwave Workflow Wizard, where you can perform some common actions.
- **New** – creates a new SIwave file (*.siw). If a file is already open, it will ask you to save before creating a new file.
- **Open** – allows you to open any SIwave file (*.siw). If a file is already open, it will ask you to save before opening another file.
- **Save** – saves the current file.
- **Archive** – saves the file as a compressed SIwave file (*.siwz). This action automatically detects appropriate files (simulation results, referenced files, etc.) and includes them in the archive.
- **Restore Archive** – opens an archived file (*.siwz).
- **Undo** – undoes the last action taken.
- **Redo** – re-performs a previously undone action.
- **Customize Quick Access Toolbar** – opens a drop-down menu allowing you to set the visibility of icons in the QAT.



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Click an item in the drop-down menu to show or hide it. Click **More Commands...** to access the full **Options** window.

Nets Workspace

The **Nets** workspace contains two windows: one for selecting nets, and one for displaying selected nets.

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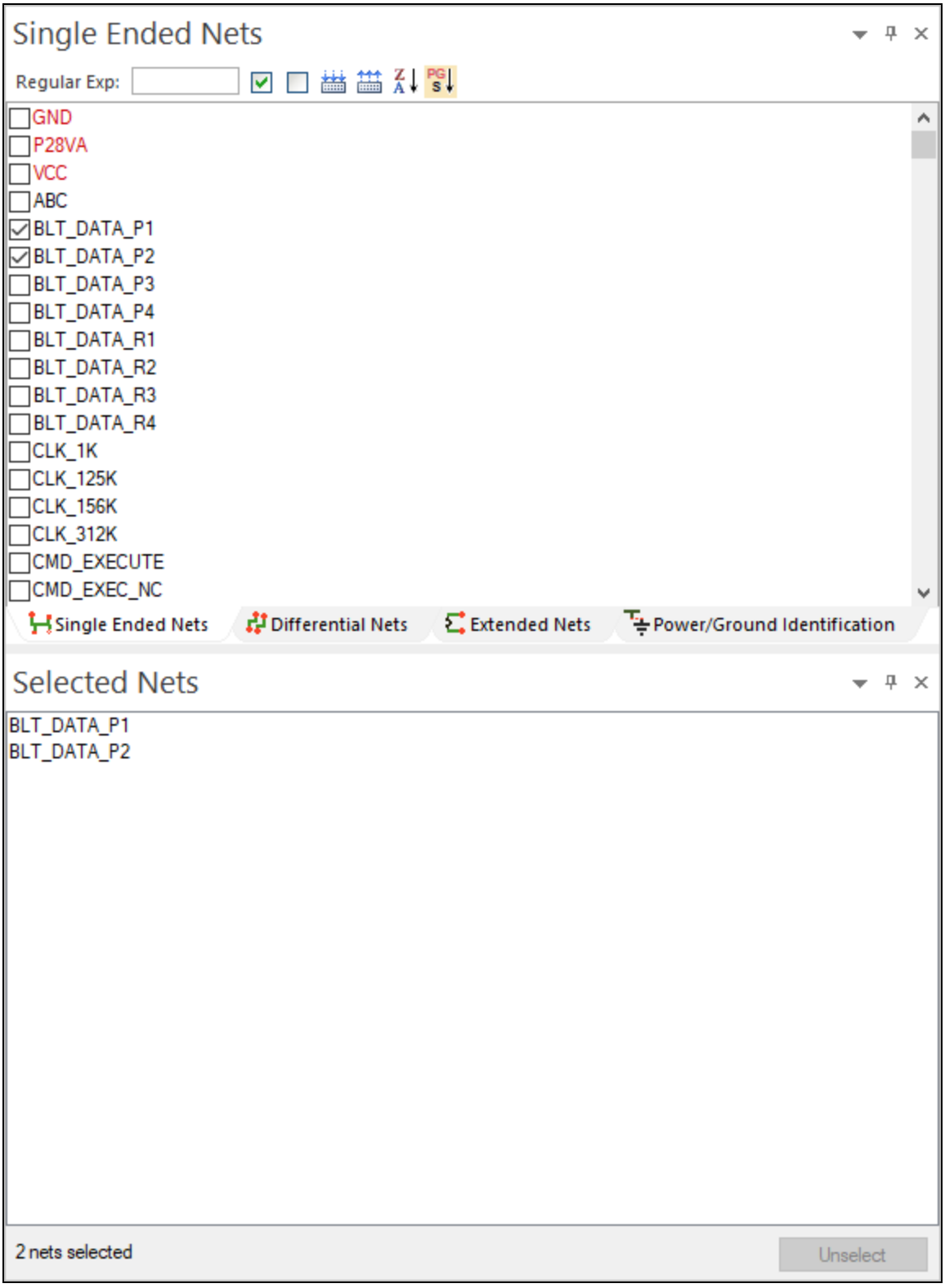

The tabs in the top window allow you to make different kinds of net selections:

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- Single Ended Nets
- Differential Nets
- Extended Nets
- Power/Ground Identification

The **Selected Nets** window shows all currently selected nets. These are also highlighted in yellow in the Modeling workspace.

Single Ended Nets

The **Single Ended Nets** tab allows you to view the properties of all single-ended nets associated with the project.

Check the box adjacent to a net to select it.

Right-click any net for the following options:

- **Edit Net Name** – rename the net.
- **Change Net Color** – choose the color in which the net displays on the map.
- **Delete Net Color** – return the net to the default color.
- **Show** – ensures the net is visible.
- **Show (Hide All Other Nets)** – hides every net except for the selected net.
- **Show All Nets** – if any nets are hidden, this option makes them visible.
- **Hide** – hides the selected net.

Differential Nets

The **Differential Nets** tab allows you to define, search, sort, and remove differential pairs.

To have SIwave automatically identify these pairs:

1. Click **Auto Identify...** to open the **Auto Identify Differential Pairs** window and automatically identify differential pairs.

Otherwise, to manually create a differential pair:

1. Select two nets in the Modeling workspace.
2. Right-click and select **Create Differential Pair**.

   The **Differential Pair** window appears.

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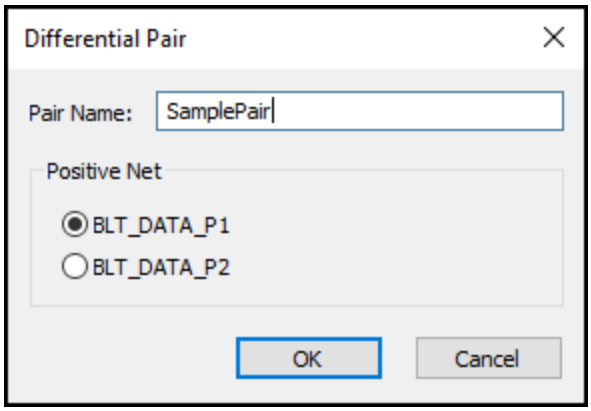

3. Specify the name of the pair, and select which net you want to be the positive one.
4. Click **OK** to close the Differential Pair window.

Extended Nets

Extended nets represent a group of nets connected by circuit elements. The **Extended Nets** tab allows you to define, search, sort, and remove extended nets.

To have SIwave automatically identify these nets:

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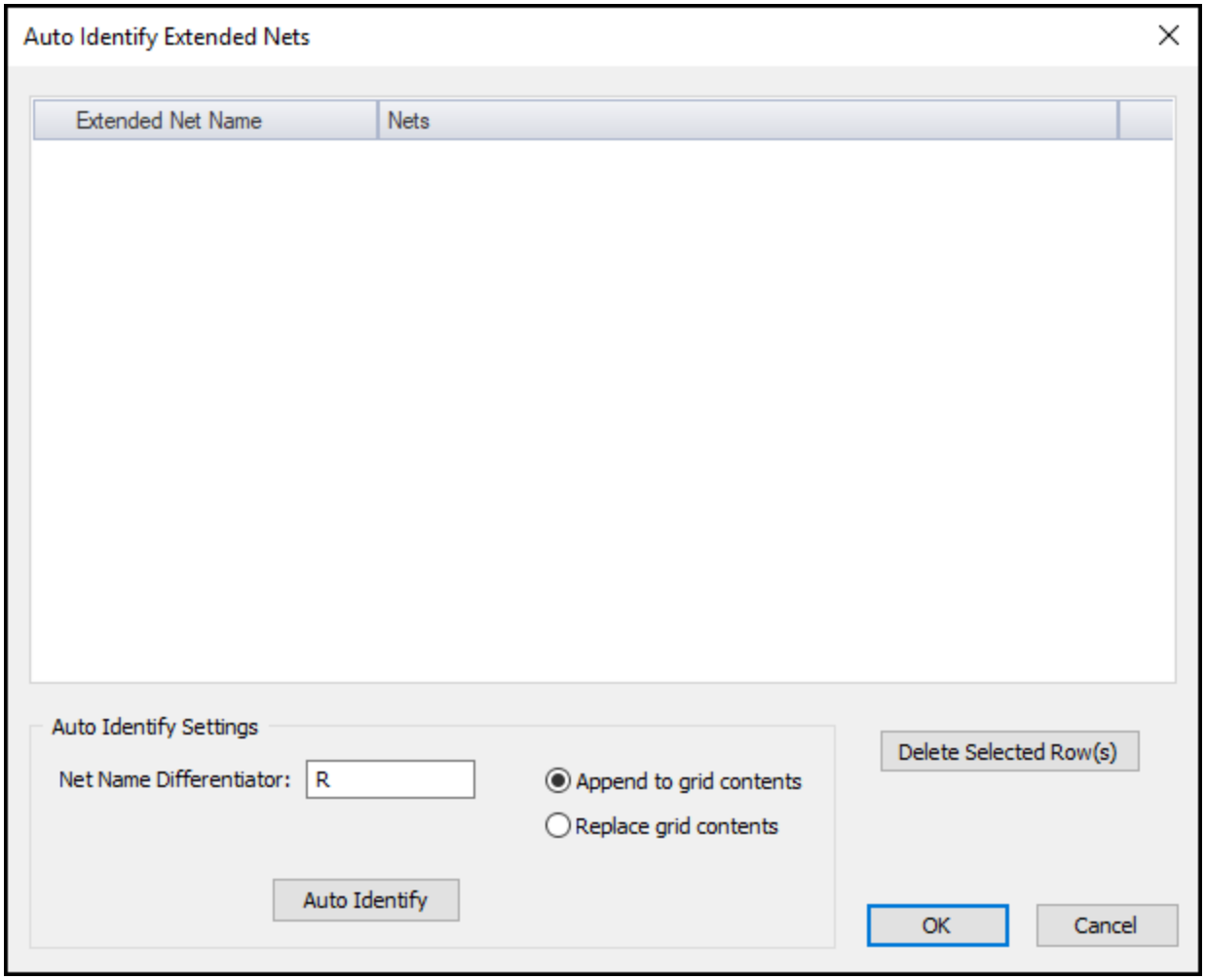
1. Click **Auto Identify...** to open the **Auto Identify Extended Nets** window.



2. Enter a **Net Name Differentiator**. This is the key character or word SIwave will use to automatically identify nets.

   Most extended nets in real usage consist of only 2 nets with names like NET1 and NET1R, connected by a resistor. In this case, the net name differentiator would be R.

   From the case of extended nets with the names NET1TEST and NET1-RTEST, the auto identify keyword would be -R.
3. Click **OK**.

SIwave also allows manual creation, which can be done two different ways:

- Select one or more nets in the Modeling workspace, right-click, and select **Create Extended Net**, or

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- Type a Net Name in the **Extended Nets** window and click the **Edit** button adjacent to it to create an extended net.

Power/Ground Identification

The **Power/Ground Identification** tab allows you to identify, select, search, sort, and remove power and ground nets.

To automatically identify power and ground nets:

- Click **Auto Identify**.

To manually identify power and ground nets:

- Move nets from the **Non Power/Ground Nets** list to the **Power/Ground Nets** list and vice versa by selecting a net and clicking the arrow buttons.

Searching Nets

From any tab, search the nets using either Perl regular expressions or wildcard search expressions.

Select the type of expression using the Net Options window (**Home** > **Options**).

The option you have selected appears as the label to the left of the search field (either **Regular Exp** or **Search Exp**).

A **Regular Expression** uses mnemonics from Perl regular expressions (e.g., D.* selects all nets starting with D).

A **Search Expression** uses a special construct with the following wild card characters:

*****	Matches any sequence of characters. For example, **net*** selects objects **net_1a**, **net_1b**, **netLength**.
?	Matches any character. For example, **net_?** selects objects **net_1**, **net_2**, **net_a**, **net_b**.

To search, formulate an expression that will find an appropriate nets and type it into the search field.

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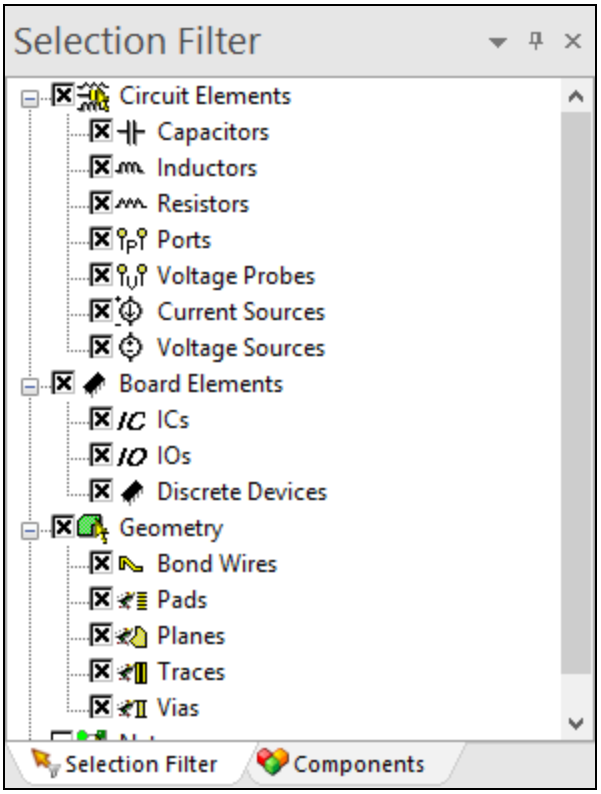
Next to the search field are check boxes for **Select Nets** and **Unselect Nets**. Enable the **Select Nets** check box to select nets that match the search. Enable the **Unselect Nets** check box to deselect any nets that match the search.

Components Workspace

The **Components** workspace contains two tabs: **Selection Filter** and **Components**.

Selection Filter Tab

The **Selection Filter** tab allows you to set the selection filter for components



To select circuit elements, board elements, geometry or nets, enable the corresponding check box.

> **Note:**
>
> Geometry and Nets cannot be selected simultaneously.

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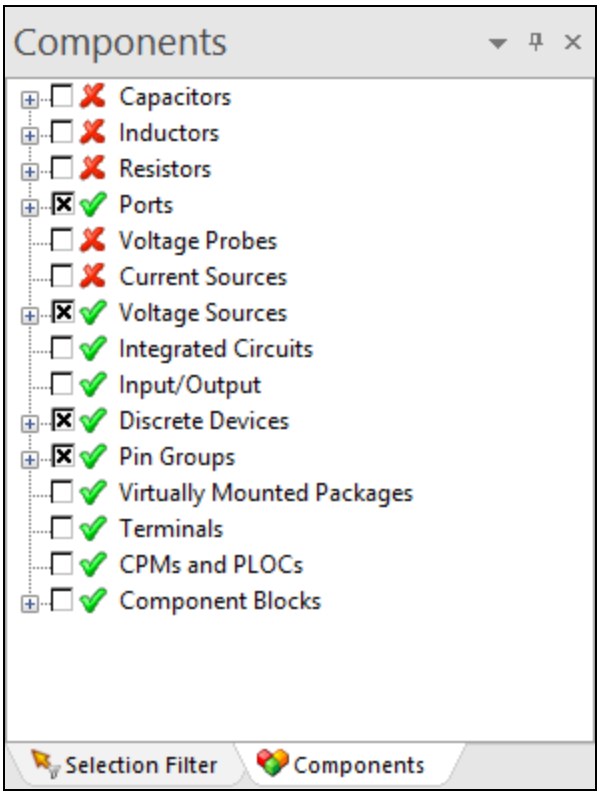
Components Tab

The **Components** tab displays all the circuit elements and manufacturer components in the model.



To see the components, part numbers and reference designators under a particular circuit element type, do one of the following to expand the tree:

- Click the **+** icon, or
- Double-click the component.

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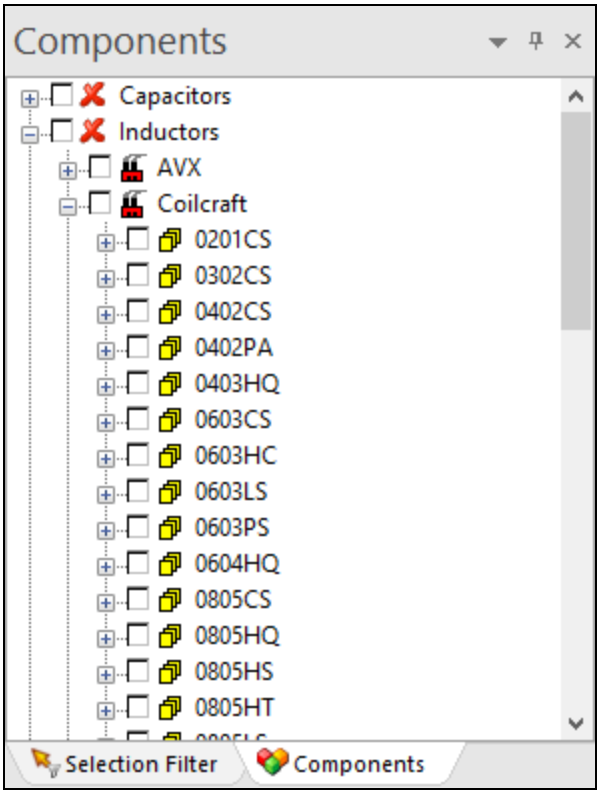
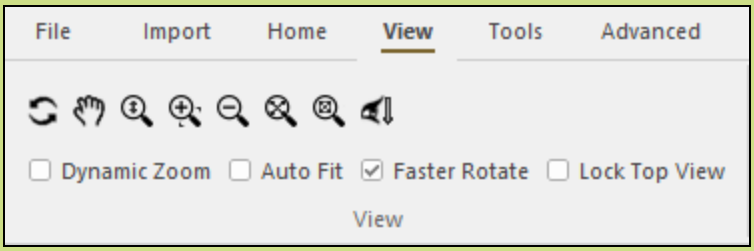


- Manufacturer-supplied components display the manufacturer name, series number, global parts, circuit elements, and pins.
- Local components display the part name, circuit elements and pins.
- Pins display the net to which they are attached.
- Click any component to select and highlight it, center it, and **Zoom In** on it in the **Modeling** workspace.

Note:

To highlight a selected component without centering or zooming in, navigate to the **View** tab and remove the check from the **Auto Fit** box.



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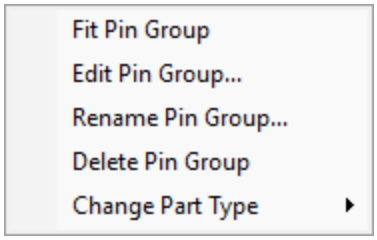
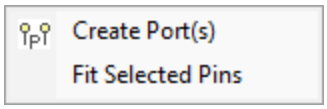
- Right-click any component to open a menu of options relevant to that component. See examples below.

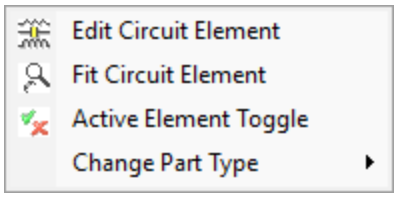
  For Pin Groups:

  For Pins:

  For Circuit Elements:

For more information about the available options, consult the help topic for the type of component you're working with:

- Circuit Elements
- Nets
- Padstacks
- Pins/Pin Groups
- Traces
- Vias

Finding and Fitting Components

SIwave can search for components based on part names or reference designators.

To find components:

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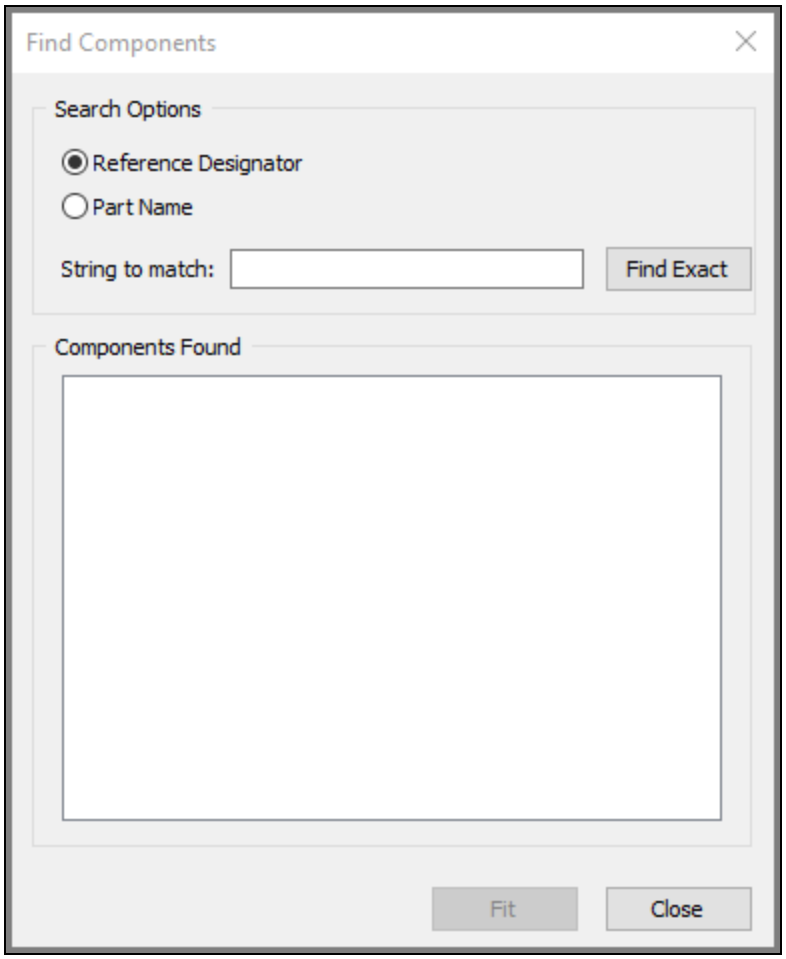
1. Click **Tools**. From the **Inspection Tools** area, click **Find Component...**

The **Find Components** window appears.



2. Click either **Reference Designator** or **Part Name**, and enter the search.

This can include wild cards:

*	Matches any sequence of characters. For example, **net*** selects objects **net_1a**, **net_1b**, **netLength**.
?	Matches any character. For example, **net_?** selects objects **net_1**, **net_2**, **net_a**, **net_b**.

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3. Click **Find Exact**.
4. To zoom in to the selected component in the Modeling workspace, click **Fit**.
5. Click **Close**.

Attaching an S-parameter Model to a Component

> **Important:**
>
> To attach S-parameter data describing two-terminal capacitors or inductors, use the instructions for:
>
> - Attaching a SPICE RLC Model, and
> - Assigning SPICE/S-parameter Vendor Models.

To attach an s-parameter model to a specific component in the layout:

1. Select the specific part in the Modeling workspace.
2. Click **Tools** > **Attach n-port s-parameter Model** to open the **S-parameter Model Setup** window. If the project has not been saved, a prompt will appear.

> **Note:**
>
> A warning may appear, informing users they can use SPICE assignments. Click **OK** to clear the warning. To avoid receiving this warning in the future, check the **Do not show again** box.

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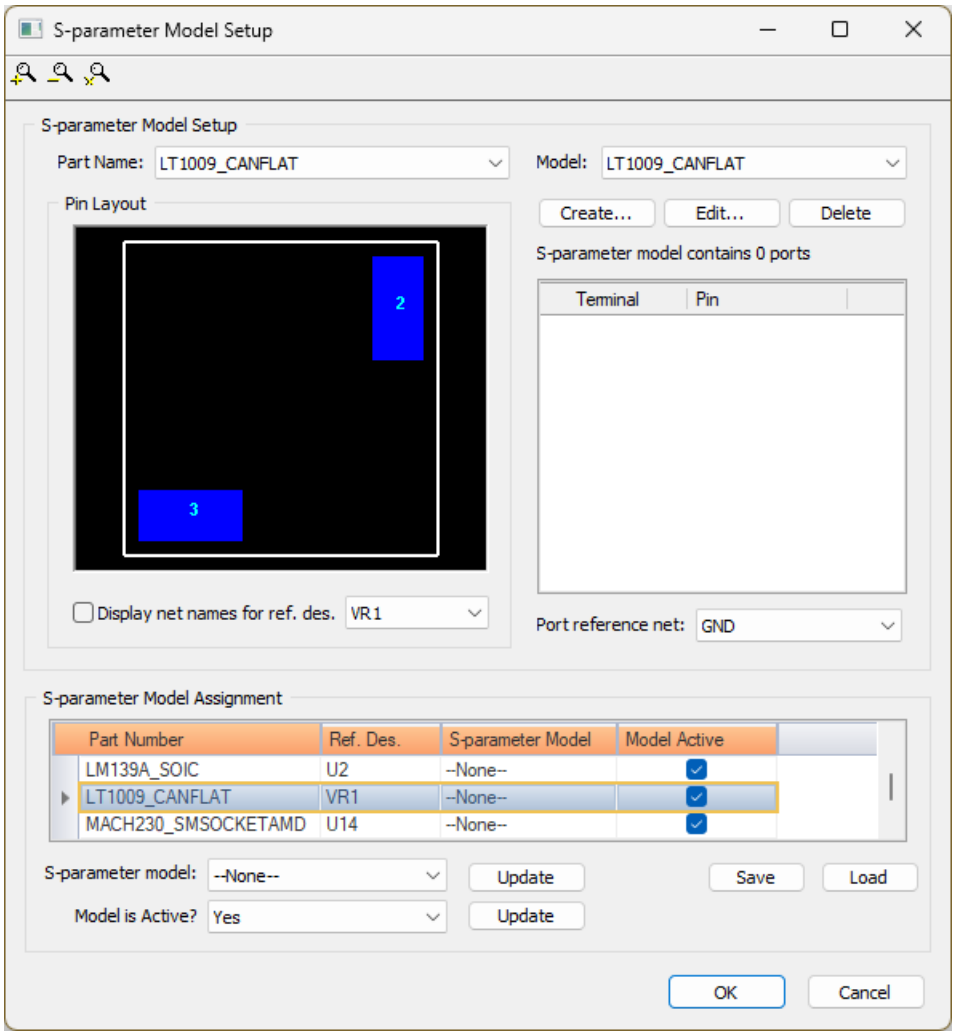

3. Select a **Part Name** from the drop-down menu to automatically populate the **Model** name drop-down menu, port list, and **Pin Layout**.
4. To see the net assignments for the component's pins, check the **Display net names for ref. des.** box and use the drop-down menu to select a reference designator.
5. To select the **Model**, do the following:
   a. Select a model from the drop-down menu, or click **Create** to create a new one. The **Create S-parameter Model** window appears, pre-populated with information from the previous window. Change this, if appropriate.

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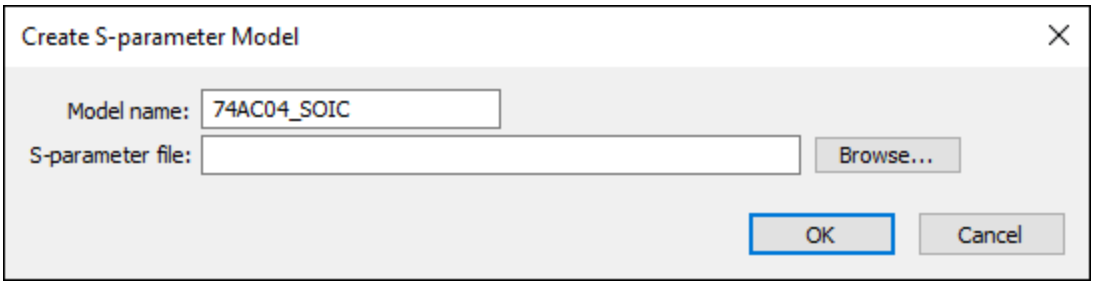

   b. Type the name and location of an **S-parameter file**, or click **Browse** to open an explorer window. Then locate a file to attach to the selected part.
   c. Click **OK** to load this file, and close the **Create S-parameter Model** window box. The selected model loads and the number of ports displays.
6. Map the ports to pins by selecting specific ports from the drop-down menu.
7. Select the **Port reference net**. By default, the **GND** or **VSS** net is selected.
8. From the **SPICE Model Assignment** table, do the following to assign an S-parameter model to a part number:

> **Note:**
>
> Select a row in the **SPICE Model Assignment** table to populate the **Part Name** and **Model** drop-down menus, **Pin Layout** area, and terminal list. If multiple rows are selected, or the sort order of the **SPICE Model Assignment** table is changed, the associated menus and areas will remain populated with the last selected row's relevant information.

   a. Select a **Part Number**.
   b. Select the **S-parameter Model** from the drop-down menu.
   c. Check the **Model Active** box to assign a model and want it to be active. If cleared, the model is assigned but is not active.
9. To assign the same s-parameter model and model active settings to multiple parts, do the following:

   a. Select parts to assign the same s-parameter model. Select multiple parts in the table by holding down **Ctrl**+**Shift**.
   b. Select the **S-parameter model** from the drop-down menu.
   c. Click **Update**.
   d. To activate the model for all the selected parts, select **Yes** from the **Model is Active?** drop-down menu, and click **Update**.
10. Click **Save** to open the **Select Spice Model Assignment Output File Name** window.

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11. Select an appropriate location to store the saved file, then enter a **File name** and select a file type from the **Save as type** list (e.g., *.smas (Spice Model Assignment File).
12. Click **Save**.
13. Click **Load** to open the **Select Spice Model Assignment File to load** window. Select a file, then click **Open** to load its values.
14. Click **OK** to confirm the SPICE model assignments and close the **RLC SPICE Model Setup** window.

> **Note:**
>
> After an s-parameter model is imported, the reference designators display with an **X** mark over them, to signify the presence of an S-parameter model.

Attaching a SPICE RLC Model to a Component

To attach a SPICE netlist to a specific component in the layout:

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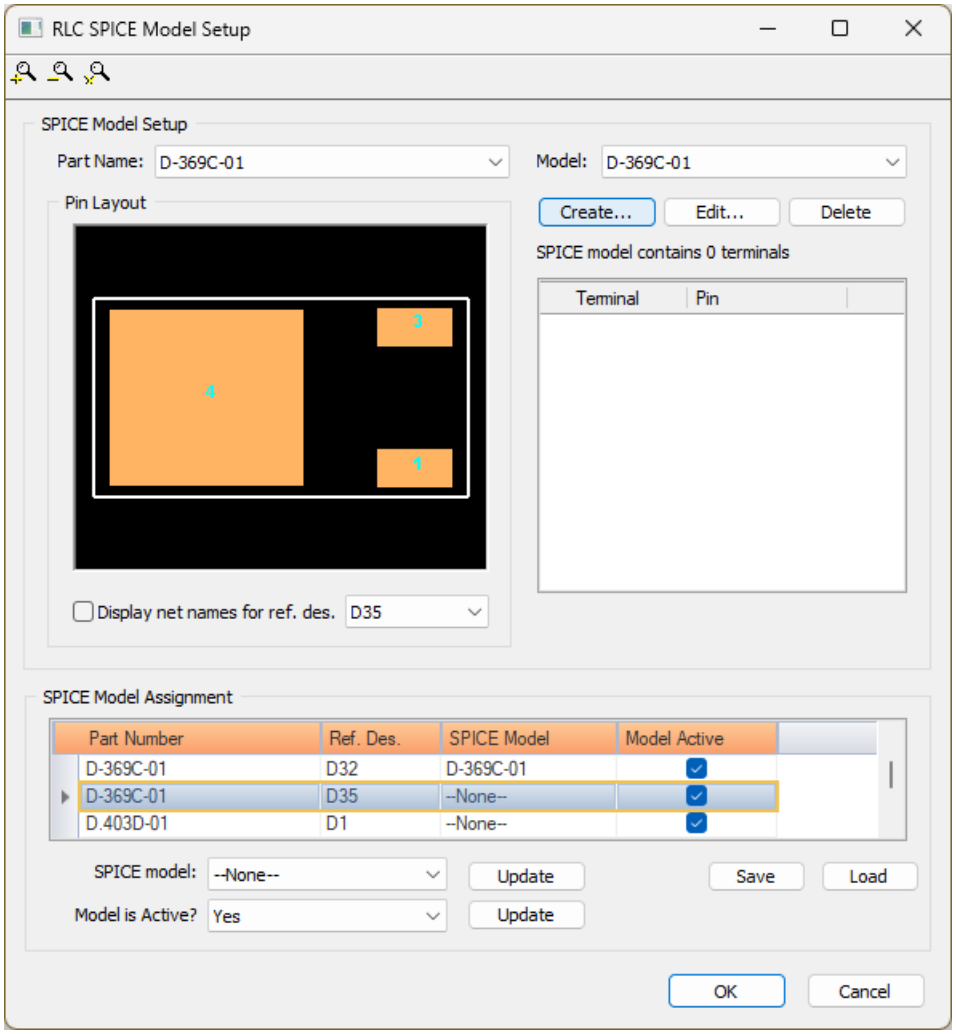
1. Select the specific part in the **Modeling** workspace.
2. Click **Tools** > **Attach SPICE RLC Model** to open the **RLC SPICE Model Setup** window.



3. Select a **Part Name** from the drop-down menu to automatically populate the **Model** name drop-down menu, terminal list, and **Pin Layout**.
4. To see the net assignments for the component's pins, check the **Display net names for ref. des.** box and use the drop-down menu to select a reference designator.
5. To select the **Model**, do the following:
   a. Select a model from the drop-down menu, or click **Create** to create a new one. The **Create RLC SPICE Model** window appears, showing the same **Model name** as the **Part Name**.

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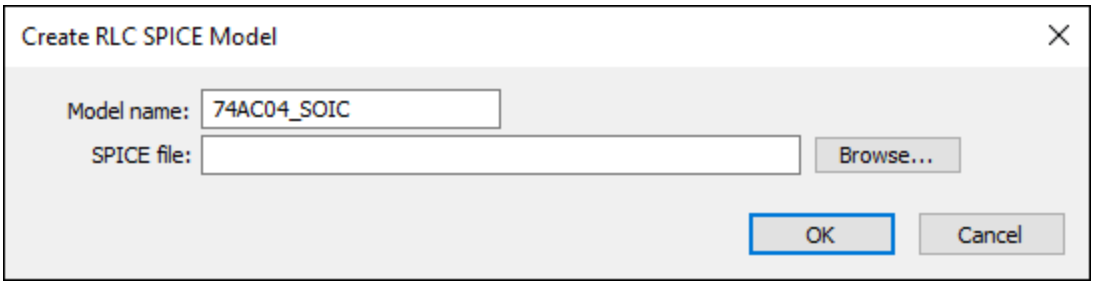

b. Type the name and location of a SPICE netlist, or click **Browse** to open an explorer window. Then locate a file to attach to the selected part. The model name is set to the SPICE subcircuit name but can be edited, if appropriate.

6. Click **OK** to close the **Create RLC SPICE Model** window. The selected model populates the **RLC SPICE Model Setup** window and the terminals in the SPICE subcircuit are displayed.

> **Note:**
>
> SIwave currently only supports netlists containing RLCK elements. No models can be created if any other type of SPICE element is detected in the netlist.

7. Map **Terminals** in the SPICE subcircuit to corresponding **Pins** belonging to the part.

> **Note:**
>
> Mapping must be performed correctly, as simulation results depend on proper connections between part pins and the SPICE subcircuit terminals.

8. From the **SPICE Model Assignment** table, do the following to assign a SPICE model:

> **Note:**
>
> Select a row in the **SPICE Model Assignment** table to populate the **Part Name** and **Model** drop-down menus, **Pin Layout** area, and terminal list. If multiple rows are selected, or the sort order of the **SPICE Model Assignment** table is changed, the associated menus and areas will remain populated with the last selected row's relevant information.

a. Select a **Part Number** and **Reference Designator**.
b. Select the **SPICE Model** from the drop-down menu.
c. Check the **Model Active** box to assign a model and want it to be active. If cleared, the model is assigned but is not active.

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9. To assign the same SPICE model and model active settings to multiple parts, do the following:
   a. Select a reference designator to assign the same SPICE model. Select multiple reference designators in the table by holding down **Ctrl**+**Shift**.
   b. Select the **SPICE model** from the drop-down menu.
   c. Click **Update**.
   d. To activate the model for all the selected parts, select **Yes** from the **Model is Active?** drop-down menu, and click **Update**.
10. Click **Save** to open the **Select Spice Model Assignment Output File Name** window.
11. Select an appropriate location to store the saved file, then enter a **File name** and select a file type from the **Save as type** list (e.g., *.smas (Spice Model Assignment File).
12. Click **Save**.
13. Click **Load** to open the **Select Spice Model Assignment File to load** window. Select a file, then click **Open** to load its values.
14. Click **OK** to confirm the SPICE model assignments and close the **RLC SPICE Model Setup** window.

> **Note:**
>
> To indicate the connection of a SPICE model, a gray rectangle containing an **X** is displayed over the reference designator(s) in the **Modeling** workspace. Activate or deactivate the SPICE model by selecting the reference designator and changing an appropriate field in the **Properties** Workspace.

Assigning SPICE/S-parameter Vendor Models

To assign SPICE/S-parameter models to components in SIwave:

1. Click **Tools**.
2. From the **Design Tools** area, click **SPICE/S-param Vendor Model Assignment**.

   The **SPICE/S-parameter Vendor Component Management** window appears.

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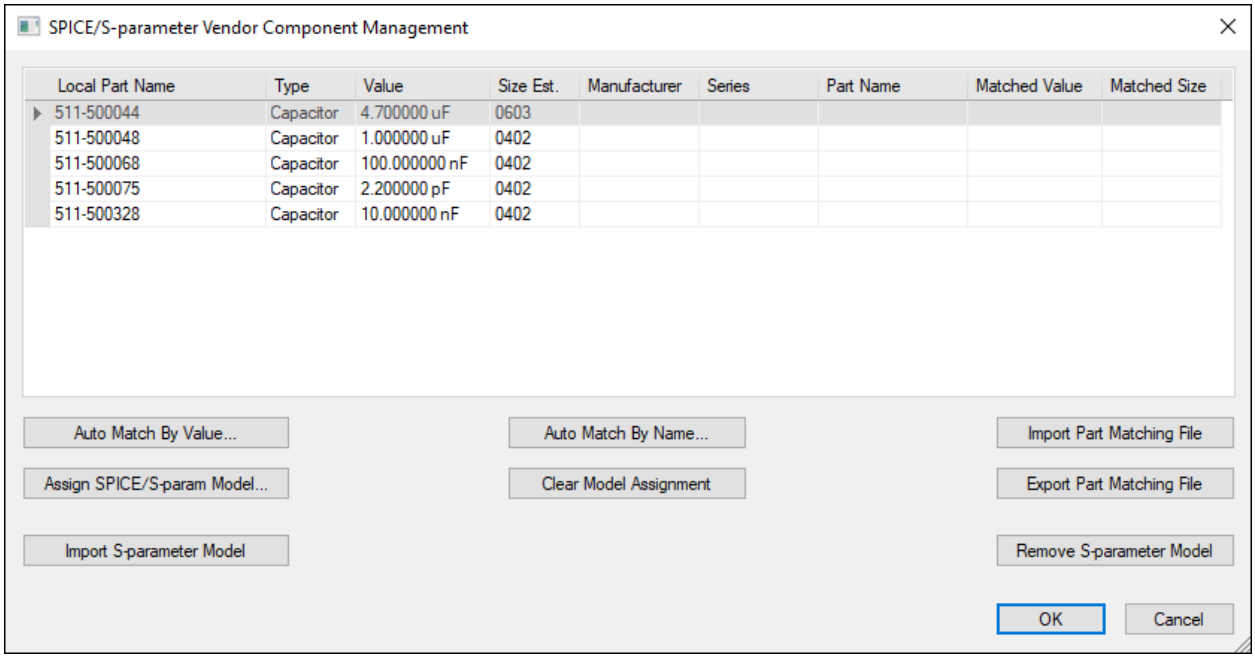

3. Select a component from the list.
4. If you have an SIwave Partname Mapping File (*.pmap), click **Import Part Matching File** to load those settings.
5. Assign specific models to parts automatically using the **Auto Match By Value** and **Auto Match By Name** buttons.
6. To assign a model to a part manually, click **Assign SPICE/S-param Model**.

   The **Select SPICE/S-parameter Vendor Model** window appears.

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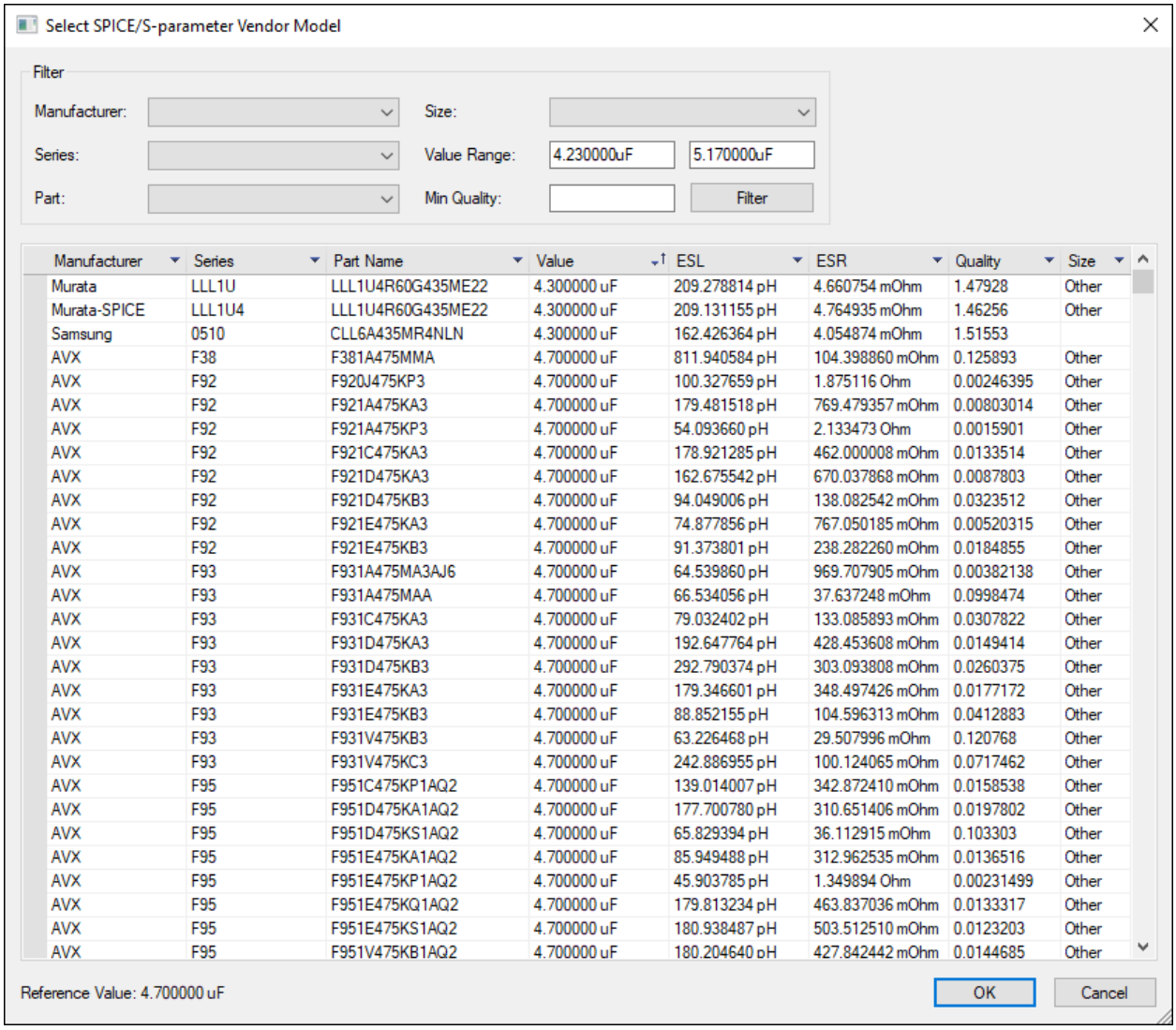

7. Use the **Filters** or scroll through the list to select a model.
8. Click **OK** to return to the **SPICE/S-parameter Vendor Component Management** window.

   The new model assignment displays in the table.

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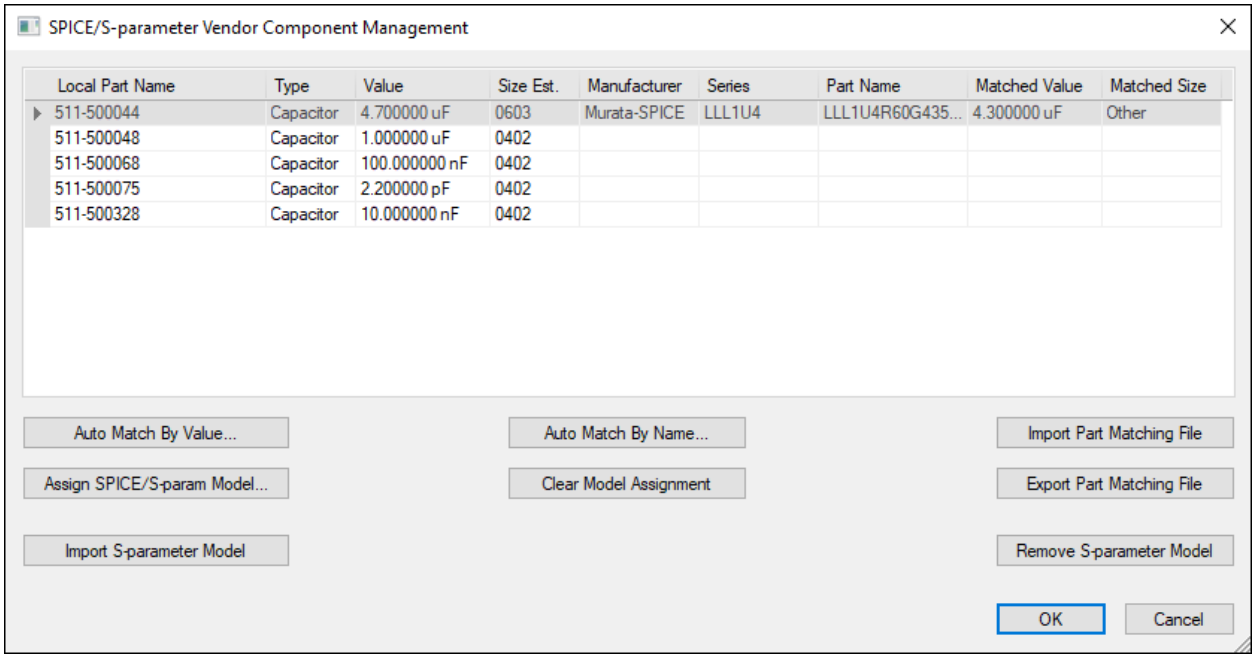

9. If appropriate, you can clear a model assignment by selecting the part and clicking **Clear Model Assignment**.
10. If appropriate, click **Export Part Matching File** to export your settings as an SIwave Partname Mapping File (*.pmap).
11. Click **OK** to save the settings.

From this window, you can also import or remove an s-parameter model. See Editing the Component Database.

Results Window

The **Results** window allows you to view the results of simulations. By default, all previously run simulations are displayed.

You can right-click a simulation to view the results.

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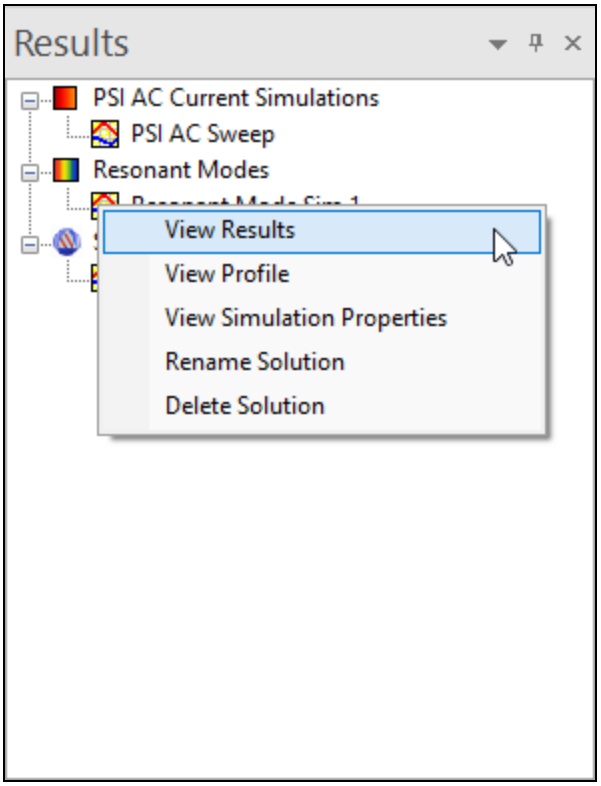

Other menu options include:

- **View Profile** – allows you to view the simulation profile and save as a .txt file.
- **View Simulation Properties** – allows you to view the settings under which the simulation was run.
- **Rename Solution** – allows you to rename the solution, as it displays in the Results window.
- **Delete Solution** – allows you to delete the solution. It will be removed from the Results window.

Depending on the type of simulation, additional options may appear.

Modeling Workspace

The **Modeling** workspace is where drawing and selection actions are performed.

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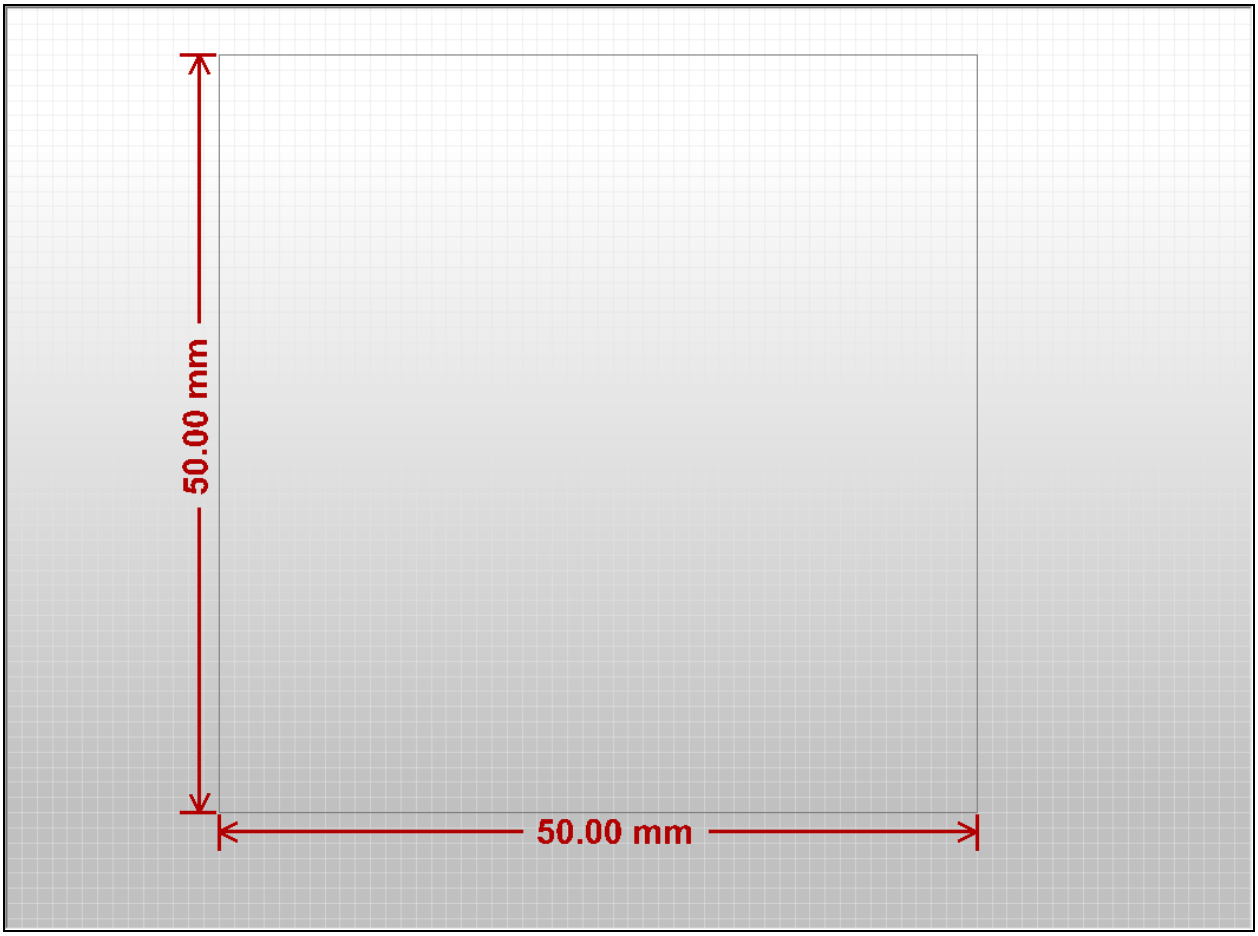

Selecting Components

To select a component, do either of the following:

- Click to highlight any component in the **Modeling** workspace and a mini toolbar containing frequently used options appears.

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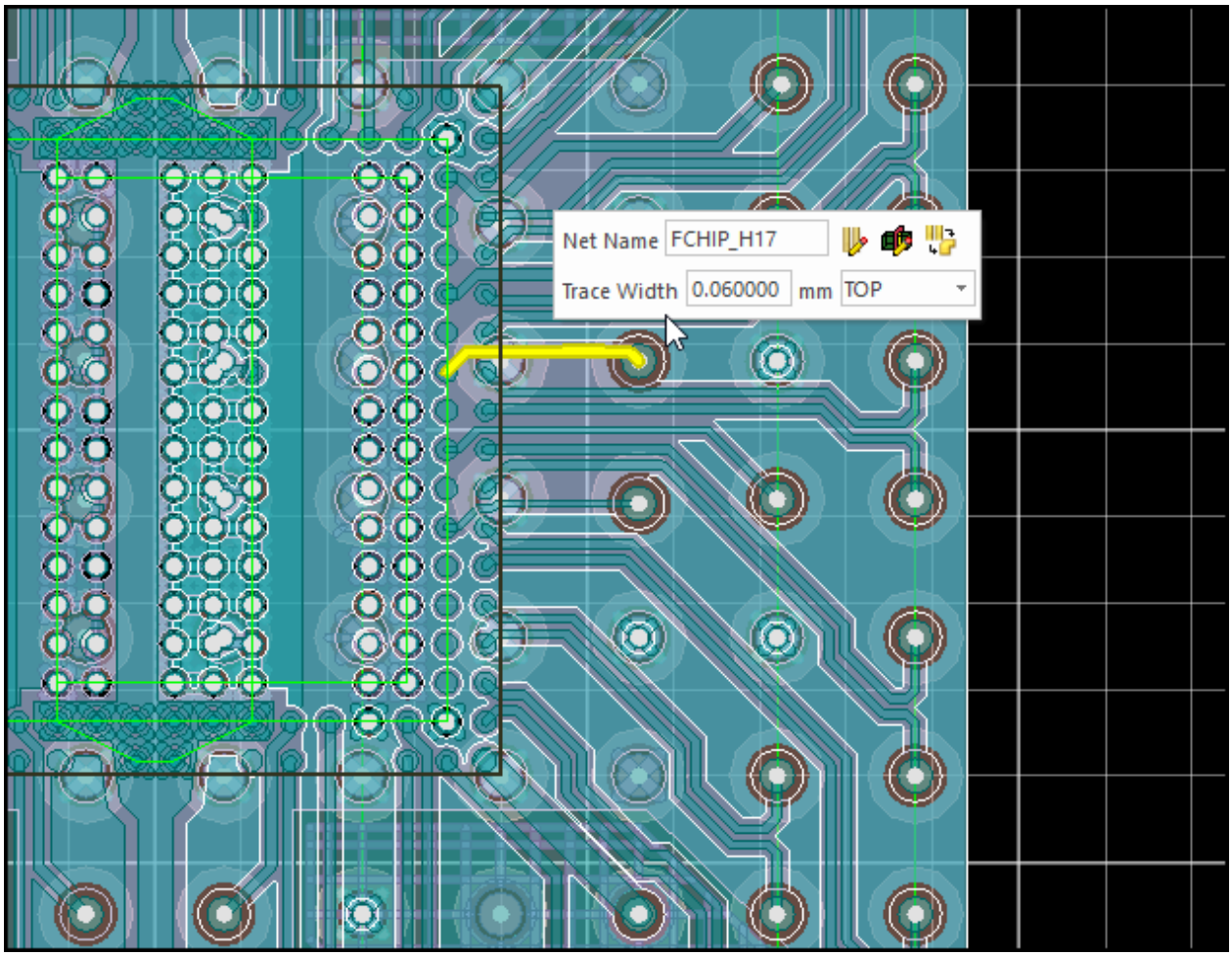

If the component layer is set to unfilled in the Layers Workspace, the selected component is highlighted with a stippled effect:

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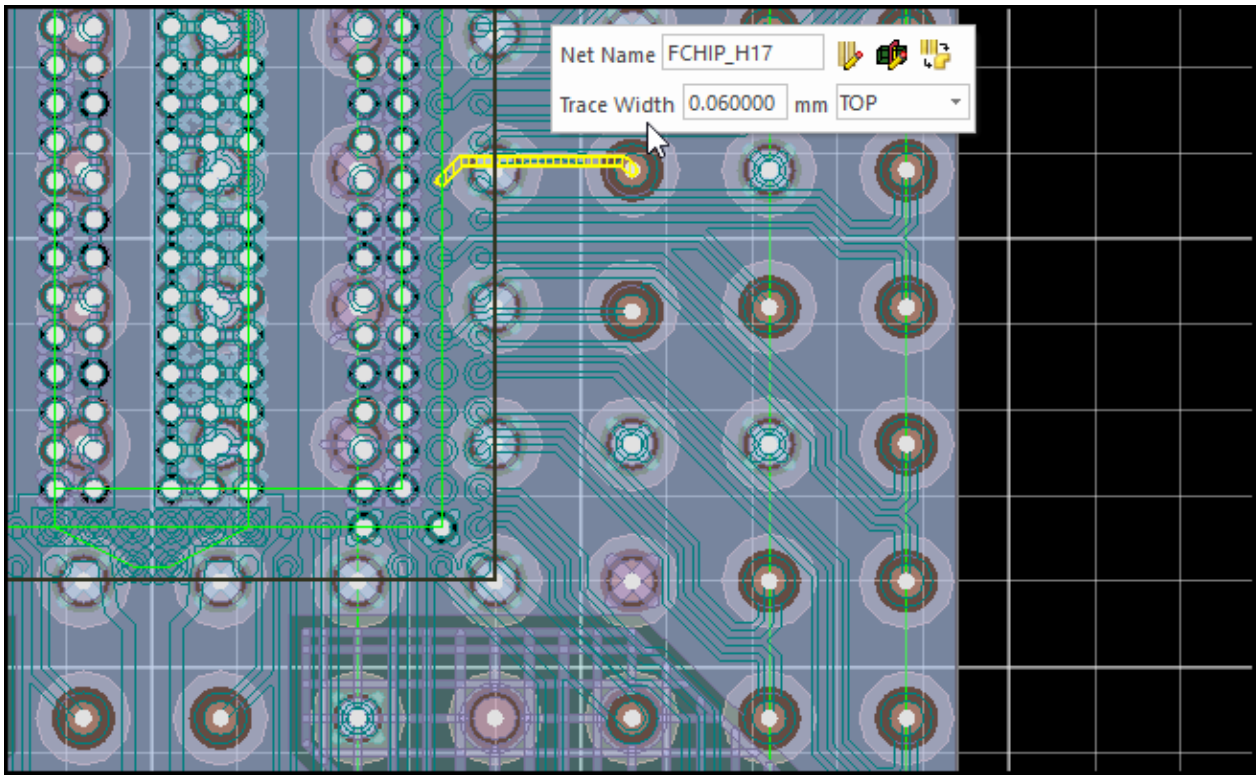

- To select the component directly behind the currently selected component, press **B**. Do **not** move the mouse. Press **F** to return to the original selection.

Refer to Geometry Selection Mode and Net Selection Mode.

Modeling Workspace Options

Right-click in the **Modeling** workspace to open the following menu.

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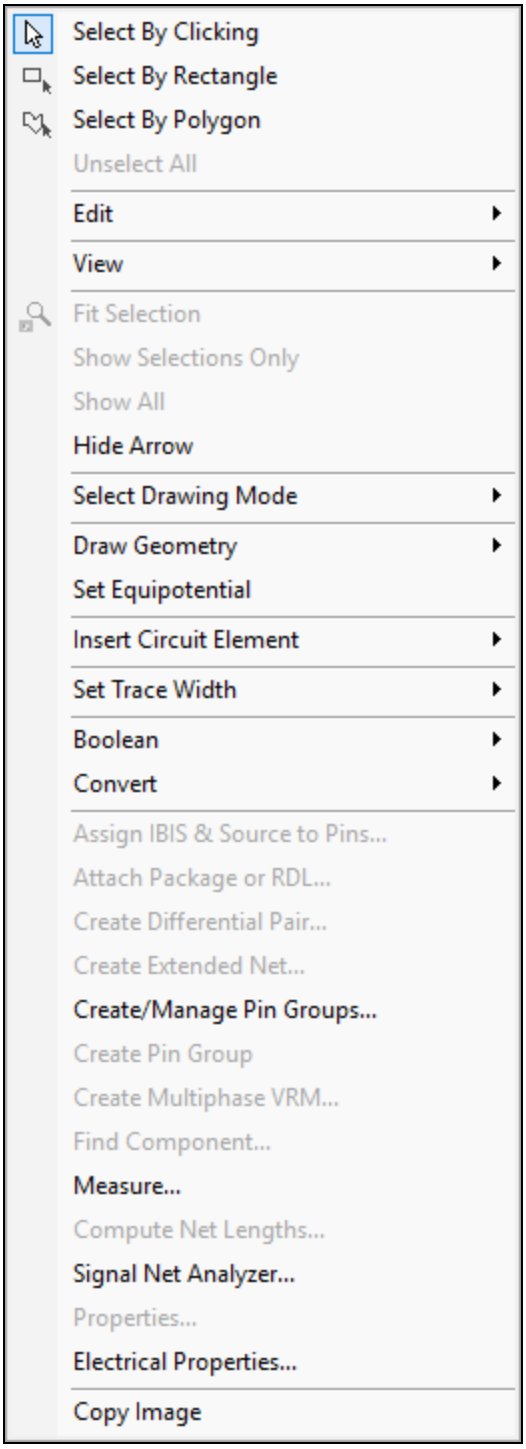

From this menu, perform the following actions:

- Choosing various drawing and selection modes
- Editing objects in the workspace

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- Modifying view settings
- Drawing geometry and circuit elements
- Component-specific menu options, such as creating differential pairs

Options in this menu allow users to change viewing options. Some of these options are also available from the **View** menu:

- Navigating the Modeling Workspace
- Changing Grid Settings
- Performing Faster Transformations
- Stretching Z
- Modifying Lighting Properties
- Viewing 2D Layers
- Editing Gradient Background
- Measuring Distances

Undo or redo any action taken in the **Modeling** workspace using the **Undo**and **Redo** buttons in the Quick Access Toolbar at the top of the ribbon.

Navigating the Modeling Workspace

The following commands allow users to control their view of the design in the **Modeling** workspace.

> **Note:**
>
> Refer to Modeling Workspace Shortcuts for a list of navigation shortcut key combinations that summarize and supplement this topic.

Zooming

Zoom options allow users to magnify or shrink the view of the design.

Zooming In

To zoom in on the design in the **Modeling** workspace, do one of the following:

- Spin the mouse wheel away from the user.
- Click the **View** tab. From the **View** area, click the **magnifying glass with a "+" in the lens**. The mouse pointer changes to a magnifying glass.
  1. Click in the **Modeling**workspace to start selecting the area to zoom in on.
  2. Drag the mouse across the zoom area.

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3. Click to stop selecting the zoom area.

Zooming Out

To zoom out from the design in the **Modeling** workspace, do one of the following:

- Spin the mouse wheel toward the user.
- Click the **View** tab. From the **View** area, click the **magnifying glass with a "-" in the lens**. The mouse pointer changes to a magnifying glass.
  1. Click in the **Modeling**workspace to start selecting the area to zoom out from.
  2. Drag the mouse across the zoom area.
  3. Click to stop selecting the zoom area.

Rotating the Model

To move the design around a center point and rotate the **Modeling** workspace, do one of the following:

- Click the **View** tab. From the **View** area, click the **circling arrows**.
- Hold down the center mouse button, then **click**+**drag** the mouse over the **Modeling** workspace.
- Hold **Alt**, then **click**+**drag** the mouse over the **Modeling** workspace.

> **Note:**
>
> Linux users, press **Ctrl**+**Alt**.

Panning Across the Design

Panning (moving the project up, down, left, or right) is the default **click**+**drag** action in SIwave. To return to panning mode after entering another mode, do one of the following:

- Click the **View** tab. From the **View** area, click the **hand**.
- Hold **Shift**, then **click**+**drag** the mouse over the **Modeling** workspace.

Fitting All Components

By default, SIwave fits the entire design in the **Modeling** workspace. To return to this view after zooming in/out, use the **Fit All** option one of two ways:

- Click the **View** tab. From the **View** area, click the **magnifying glass with four out-facing arrows in the lens**.
- Use the keyboard shortcut **Ctrl+D**.

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Note:

To improve response time when SIwave is streaming over a remote desktop:

- Informational tool tips will not appear.
- Dynamic zoom is deactivated.
- Faster transformation is activated.

Returning to the Default View

By default, SIwave displays a top-down view of the design. To return to the top-down view, do one of the following:

- Click the **View** tab. From the **View** area, click the eye adjacent to a down-facing arrow.
- Hold **Alt**, then double-click the **Top** of the **Modeling** workspace. Refer to Changing the Model View with Alt+Double-Click Areas.

To lock the top-down view:

- Click the **View** tab. From the **View** area, check the **Lock Top View** box.

Note:

When the top-down view is locked, the design can only be rotated by its z-axis.

Modeling Workspace Shortcuts

The following shortcut key combinations are available when the **Modeling** workspace is active.

Note:

LMB is an abbreviation for *Left Mouse Button*, and **MMB** means *Middle Mouse Button*.

Wheel refers to rotation of the mouse wheel that is integrated with the middle button.

View Navigation:	
Ctrl + **D**	**Fit** view
Ctrl + **'+'**	**Zoom in** (screen center)
Ctrl + **'-'**	**Zoom out** (screen center)
Alt + **double-click**	Change the view orientation to one of nine predefined views depending on where users double-click in the **Modeling** workspace. See Changing the Model View with Alt+Double-Click Areas.

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MMB + **drag** (no modifier)	Freely **rotate** the view orientation (except when clicking and dragging near the window border). When clicking near the window border, rotation is constrained about the screen-normal axis. **Note:** In 2D plots, **MMB**+**drag** functions the same as **Ctrl** + **MMB** + drag, panning the view.
Shift + **Arrow Key**	**Rotate** the view orientation; limited by the design's orientation before rotation begins as the starting position.
Wheel	Rotate the mouse wheel to **zoom** in and out. Rotate the wheel away from the user to zoom **in** closer, and rotate the wheel toward the user to zoom **out**.
Shift + **MMB + drag**	**Zoom** in or out. Moving the cursor upward zooms in closer. Moving it downward zooms out.
Ctrl + **MMB** + **drag** or **Ctrl** + **Arrow Key**	**Pan** the view

Changing the Design View with Alt+Double-Click Areas

From the following figure, the colored boxes show the nine view orientations you can obtain by using **Alt** + **double-click** in the corresponding areas of the **Modeling** workspace. Each face is a unique color and is named according to standard view orientation names.

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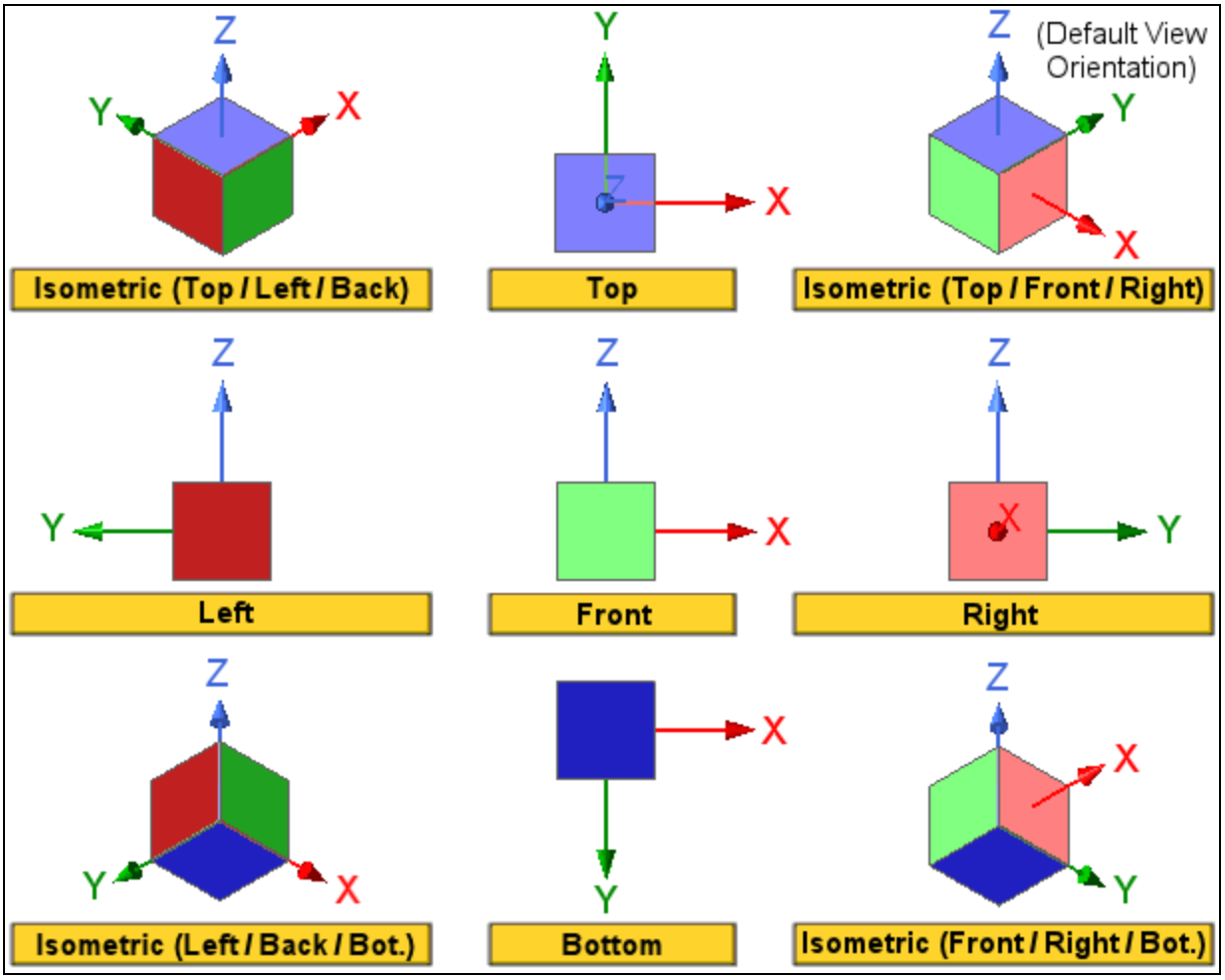

Mini Toolbar

In SIwave options, **Show Mini Toolbar on selection** is enabled by default.

The mini toolbar provides basic operations and relevant actions for a selected object. Click on an object in the Modeling workspace to select it and show its mini toolbar.

Below are two mini toolbars, for a via and a trace.

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You can also select multiple similar objects and modify their properties using the mini toolbar.

The following types of objects show a mini toolbar:

- Trace
- Via
- Plane
- Bondwire
- Net
- Pin Group
- S-parameter Model / Spice RLC Model
- Circuit Element
- Board Element (ICs / IOs / PinPlates)

Changing Grid Settings

By default, the Modeling workspace displays a grid and drawing elements snap to the grid.

To toggle the grid, click **View**. From the **Show/Hide** section, click the icon.

To toggle grid snapping, click **View**. From the Show/Hide section, click the icon.

To change grid spacing, click **View**. From the View Options section, check the **User Grid Spacing** box and type the spacing you would like, in millimeters.

Performing Faster Transformations

SIwave allows you to view a simplified model during rotate, zoom or pan operations.

To perform faster transformations, click **View**. From the View section, check the **Faster Rotate** check box.

In order to speed up performance while you are rotating, zooming or panning in, planes are represented in 2D, and vias and circuit elements are not displayed. The complete design is displayed only after you finish the operation.

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Note:

To improve the response time when SIwave is run over a remote desktop:

- Informational tool tips will not appear.
- Dynamic zoom is deactivated.
- Faster transformation is activated.

Stretching Z

To artificially scale Z values, so that very thin planar objects have a 3D appearance:

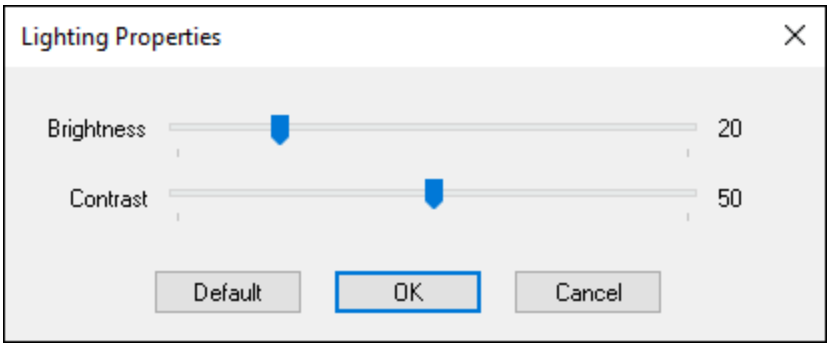
1. Click **View**.
2. From the View Options section, use the **Z Stretch** slider to set the scaling factor to any discrete value between 1 and 25.

Modifying Lighting Properties

To change the lighting in SIwave:

1. Click **View** > **Lighting**.

The **Lighting Properties** window appears.



2. Use the **Brightness** and **Contrast** sliders to change the settings to any discrete value between 1 and 100.
3. Click **OK** to save the settings.
4. If you need to return to the default values, open the **Lighting Properties** window and click **Default**.

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Viewing in 2D

To draw metallic objects quickly, you can consider them two-dimensional (2D) sheets with zero thickness. This ignores the side and top geometries and reduces memory usage when viewing large designs.

To view the project in 2D, click **View**. Then check the **2D View** check box.

> **Note:**
>
> All planar entities can be drawn as 2D sheets, but vias are always represented in 3D. Only the visual representation of the planar entities is affected, and not the manner in which they are electrically represented.

Editing Gradient Background

By default, the Modeling workspace displays a gray gradient as its background.

To change the background:

1. Click **View**. From the View Options section, click **Background**.
   The **Gradient Background Editor** window appears.

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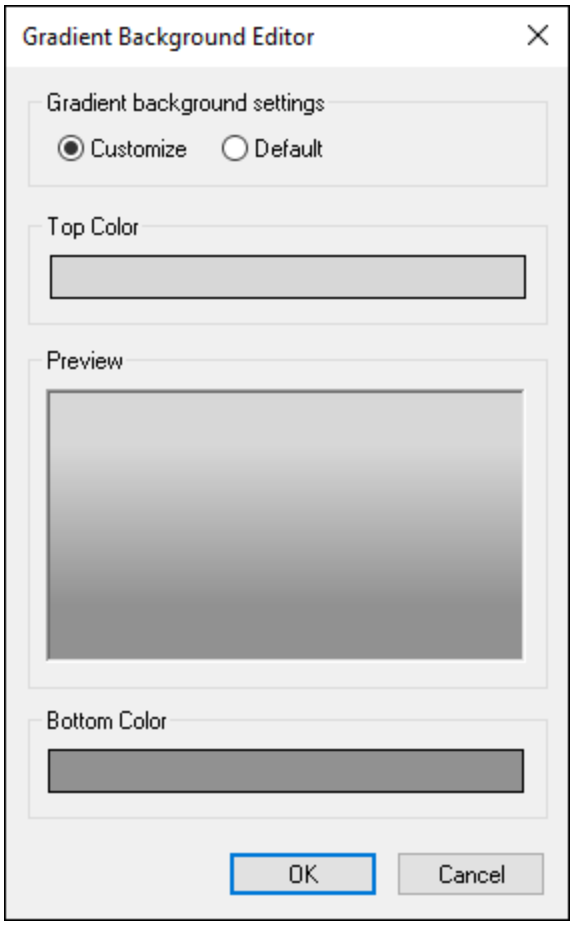

2. Ensure the **Customize** radio button is selected.
3. Click the color swatches in the **Top Color** and **Bottom Color** sections to change the colors. The **Color** window appears.

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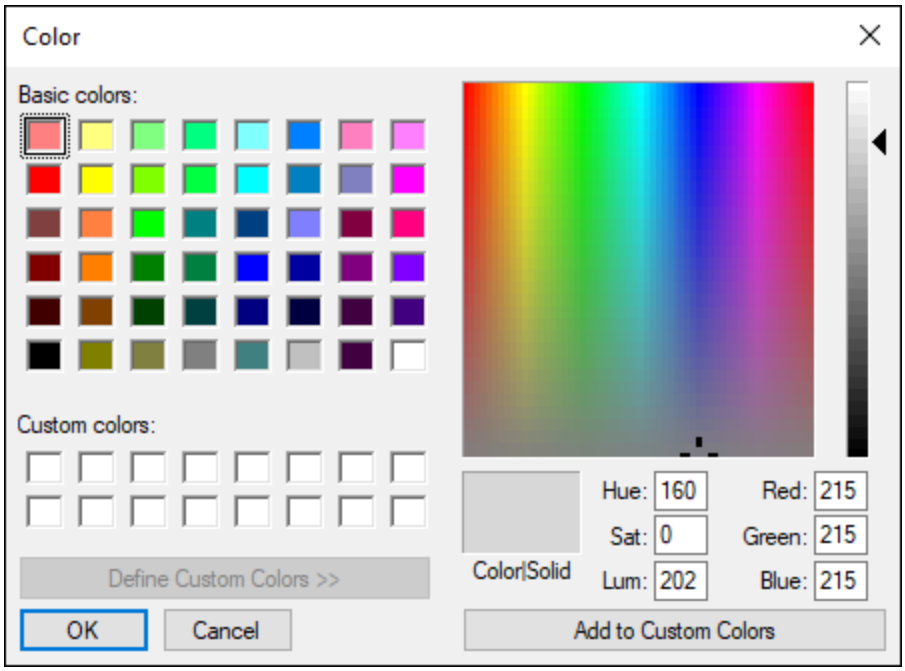

4. Select your colors and click **OK**.

   Your selections preview in the **Gradient Background Editor** window.

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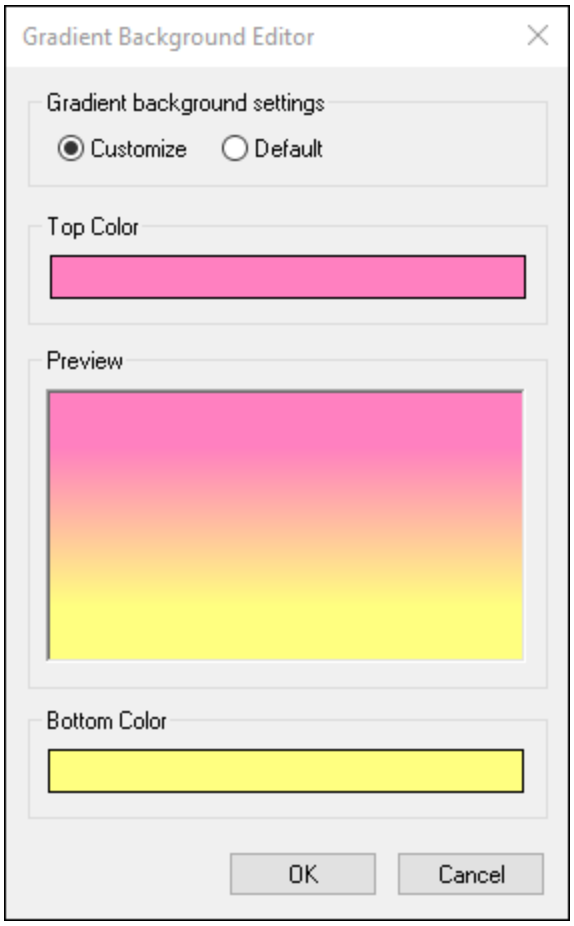

5. Click **OK**.

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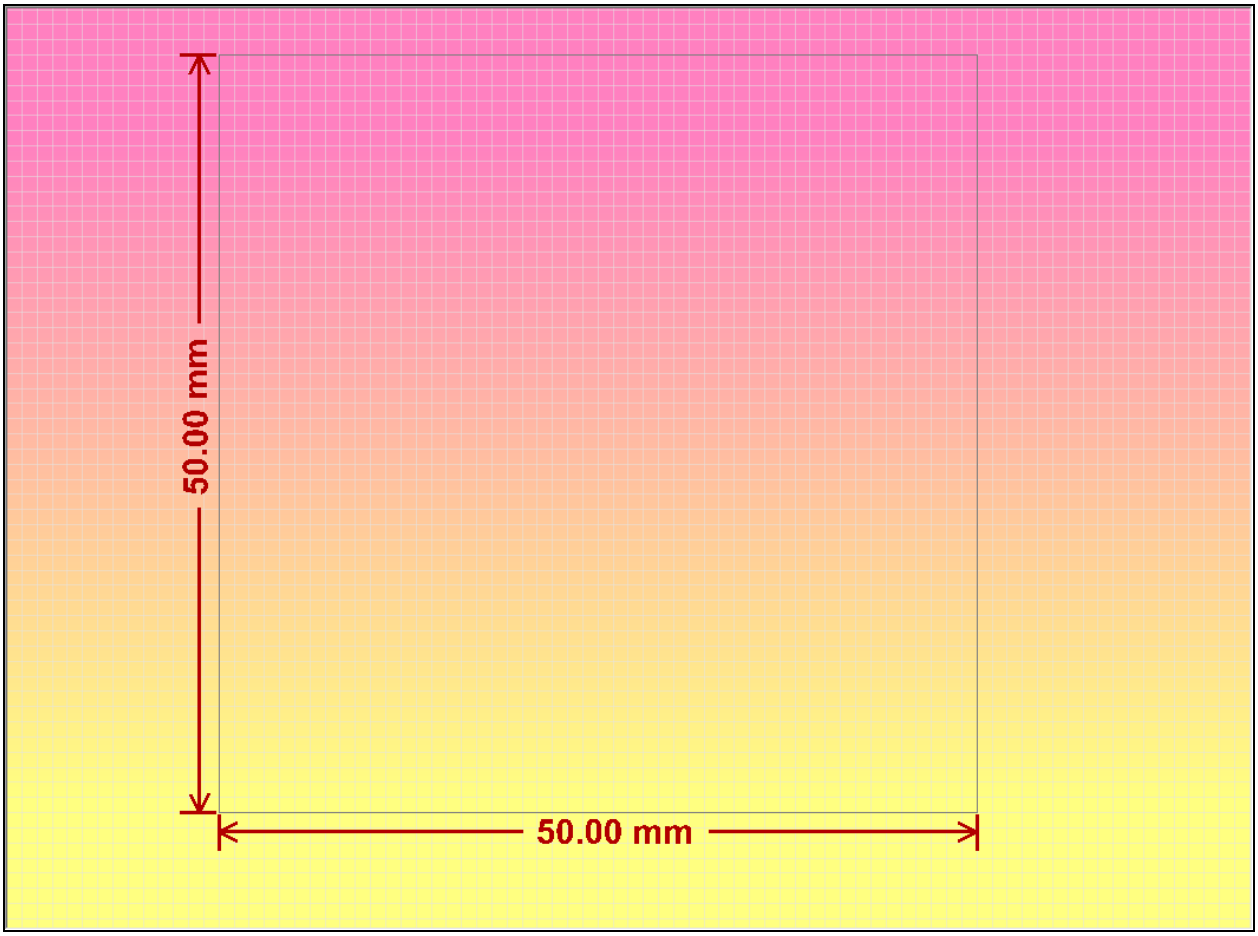

If at any time you wish to return to default settings, open the **Gradient Background Editor** and select **Default**. Then click **OK**.

Measuring Distances

SIwave allows you to measure the distance between points and spacing between edges.

To measure data, click **Tools**. From the **Inspection Tools** area, click **Measure**.

The **Measure Data** window appears. You can dock or hide it by right-clicking anywhere in the window.

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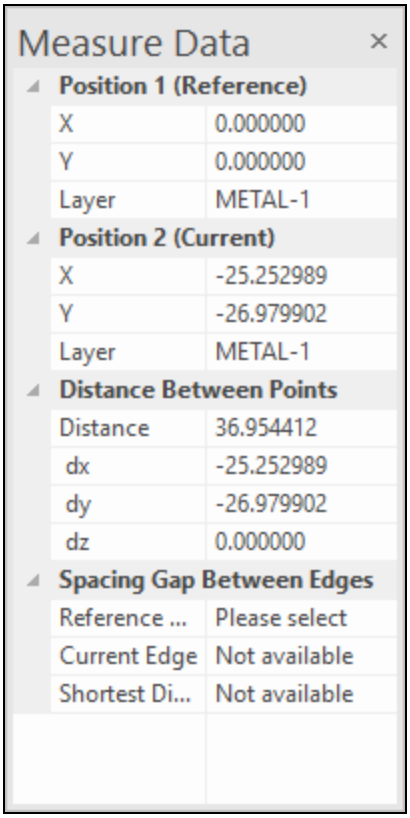

Before measuring data, ensure you are in **Select by Clicking** mode on the **Home** tab.

To measure the distance between two points:

- Click any point for a reference coordinate. This is displayed as **Position 1**.
- Move the cursor in the Modeling workspace to see the values for **Position 2** and **Distance between Points**.
- The data updates as the cursor is moved. The shape of the cursor changes when it is snapped to a corner or mid-point.

To measure the shortest distance between two edges:

- Select an edge in the Modeling workspace. This is displayed as the **Reference Edge**.
- Move the cursor over another edge to see the values for **Current Edge** and **Shortest Distance**.

Layers Workspace

This area allows you to view the properties of all the layers associated with the project.

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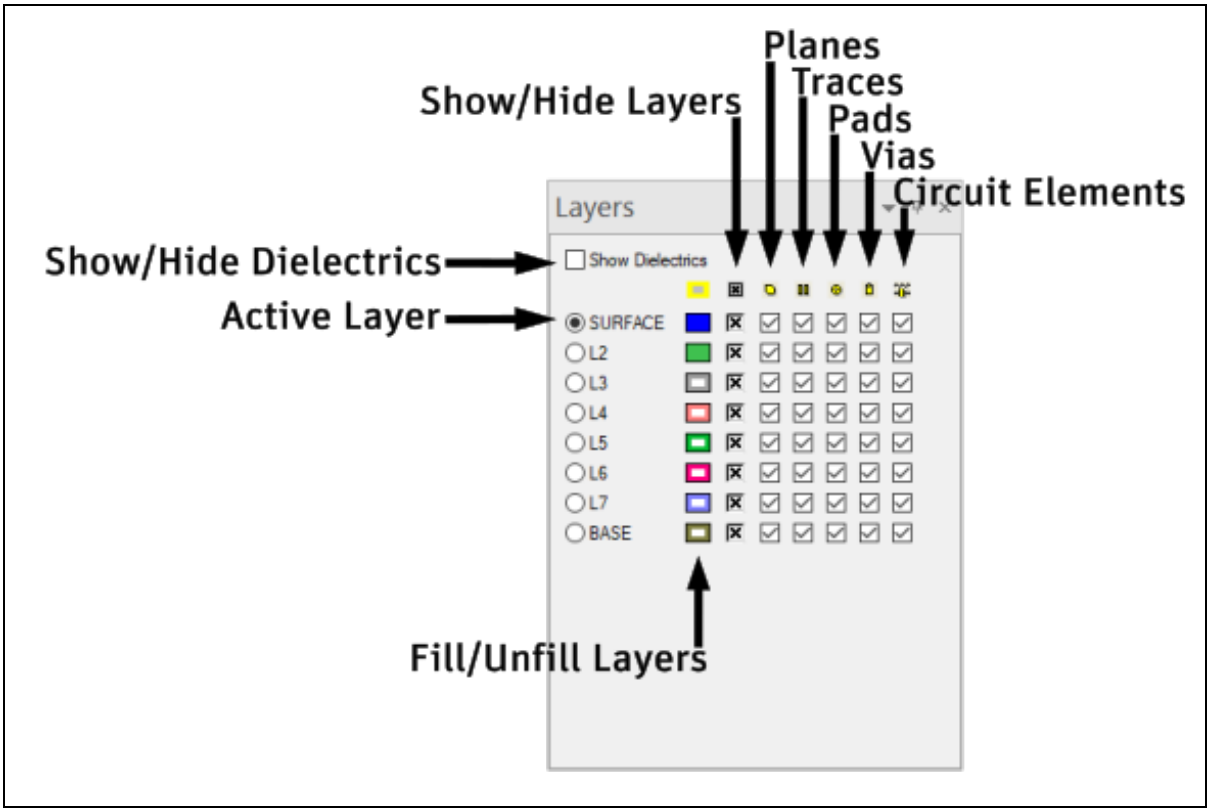

To select a layer, click the radio button next its name. When a layer is selected, its properties open and can be edited in the Properties workspace.

> **Note:**
>
> You can also use the up and down arrow keys to switch active layers. Doing so will override visibility settings so that only the selected layer is visible.

To fill or unfill a layer, click inside the layer's color box.

To show or hide a layer, use the Show/Hide check box.

To show or hide dielectric layers, use the **Show Dielectrics** check box.

To show or hide planes, traces, pads, or circuit elements on a particular layer, use the corresponding check boxes.

Right-click any layer to edit its properties.

Right-click any area other than a layer name to open a pop-up menu with the following options:

- **Hide All Layers** – makes all layers in the Modeling workspace invisible.
- **Show All Layers** – makes all layers in the Modeling workspace visible.

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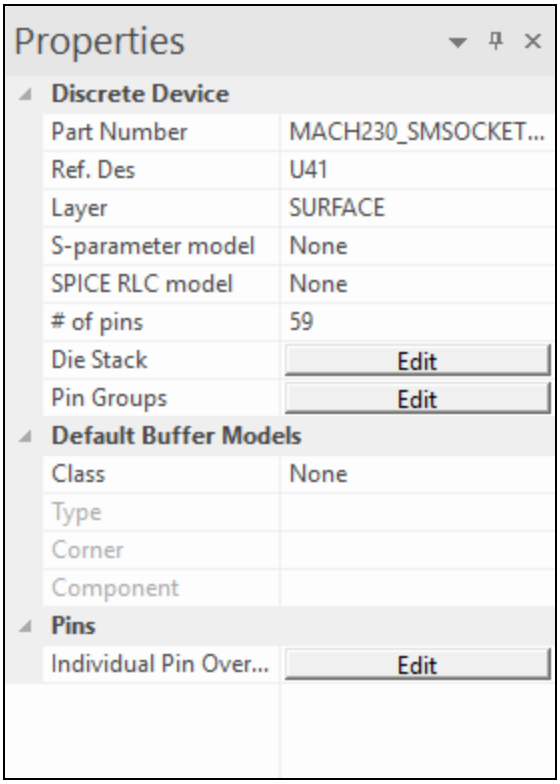
- **Unfill All Layers** – removes fill color from all layers in the Modeling workspace.
- **Fill All Layers** – fills the color of all layers in the Modeling workspace.

Properties Workspace

The **Properties** workspace allows users to view and modify the properties of the selected components.



The **Properties Workspace** presents different properties, depending on the type of component selected.

Viewing Electrical Properties

To view the electrical properties of a trace, bondwire, or via:

1. Select a trace, bondwire, or via to populate the **Properties** workspace. View the properties of multiple traces, bondwires, or vias at once by selecting more than one.

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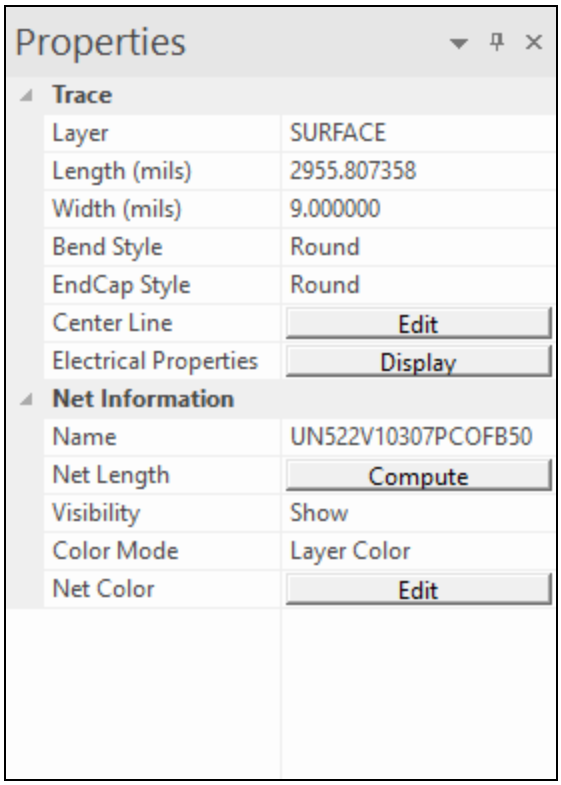

2. Click the **Display** button next to **Electrical Properties** to open the **Electrical Properties** window.

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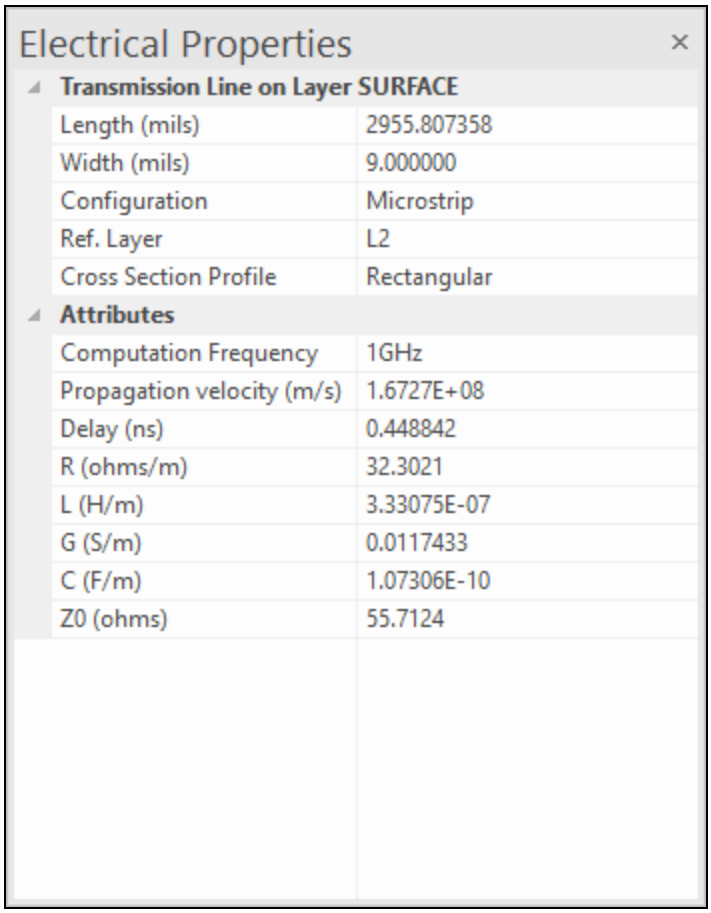

Viewing the Differential Electrical Parameters for a Trace/Bondwire or a Via

1. Select two coupled traces that belong to a differential pair to populate the **Properties** workspace.
2. Click the **Display** button next to **Electrical Properties** to open the **Electrical Properties** window.

Estimating |Z11| at a Port

1. Click in the center of a port to populate the **Properties Workspace**.
2. Next to **|Z11| Estimate**, **click** Display to open the **Estimated |Z11| at port** window.
3. The **Estimated |Z11| at port** window is functionally similar to the PI Advisor Wizard. Refer to Running the PI Advisor.

Messages Workspace

The **Messages** workspace displays messages pertaining to each part of the project. These include notification of incomplete projects. By default, it is always displayed.

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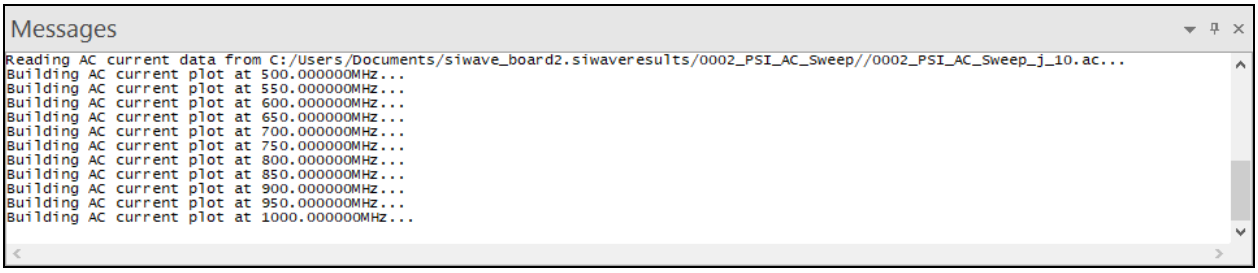
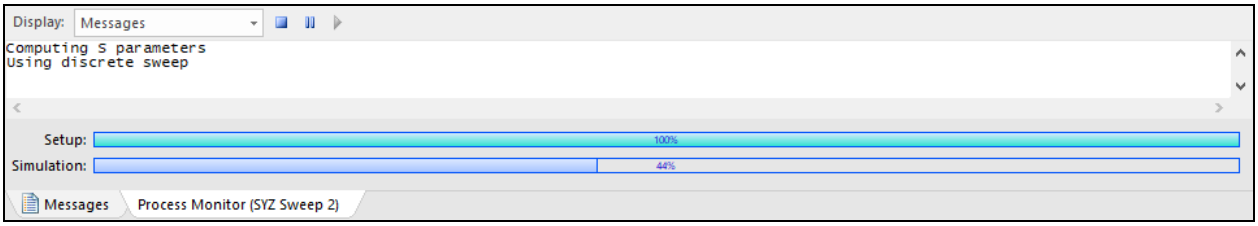


Right-click within the **Messages** workspace to open a menu. Using this shortcut menu, you can perform the following actions:

- **Copy** – copy text from the Messages window for pasting into the Messages window or into any text editor. You can also use **Ctrl+C**.
- **Select All** – select all of the text in the window. You can also use **Ctrl+A**.

When a simulation starts, the **Process Monitor** tab appears within the **Messages** workspace.



You can stop, pause, or resume the simulation using the icons at the top of this tab.

You can also use the Display drop-down menu to select **Profile** and view more information about what the simulation is doing.

Information/Errors/Warnings Workspace

The **Information/Errors/Warnings** workspace displays certain messages pertaining to the project.

- **Information** – general status and properties messages. These are denoted by a white circle containing the letter *i*.
- **Warnings** – notifications of issues that may affect simulation capabilities. These are denoted by a yellow triangle with an exclamation point.
- **Errors** – notifications of failures. These are denoted by a red circle containing the letter *x*.

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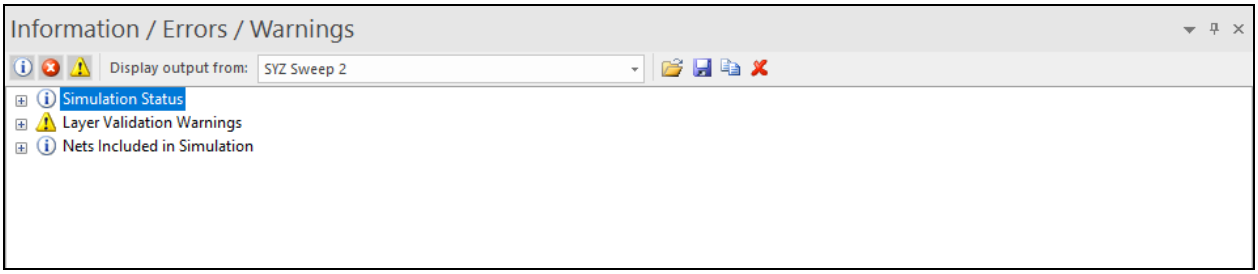

You can choose which types of messages (information, warnings, errors) to display using the icons at the top-left of the window.

The **Display output from** drop-down menu allows you to select the simulation for which to view results.

Using the **Save** and **Open** icons, you can save the contents of the **Information/Errors/Warnings** file as a Workplace transcript file (*.iew), and open previously saved .iew files.

You can copy the Information/Errors/Warnings window contents using the **Copy** button, and paste the information into any text editor.

You can also **clear** the contents of the window using the red X on the right-hand side of the toolbar.

Exit Codes

When SIwave runs a simulation, the **Information/Errors/Warnings** workspace displays an exit code.

The table below lists some common codes and their meanings:

Code	Description
0	Successful simulation.
1	Unknown failure.
2	SIwave couldn't open file.
3	SIwave couldn't read file.
4	SIwave couldn't write to file.
5	Invalid solver inputs.
6	No source file defined.
7	Illegal geometry or connections found.
8	Invalid trace cross section.
12	Could not solve resonant modes.

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Code	Description
13	Singular matrix.
14	Failed to mesh, or invalid mesh.
100	Insufficient memory to solve.

SIwave Options

To set program-wide options in SIwave, click **FILE** > **Options**.

The **Options** window contains five tabs:

- **Popular** – contains SIwave display options.
- **Library Directories** – allows you to specify directories for the component library and IBIS buffer library.
- **Quick Access Toolbar** – allows you to add and remove items from the Quick Access Toolbar.
- **Resources** – contains links to various internet resources.

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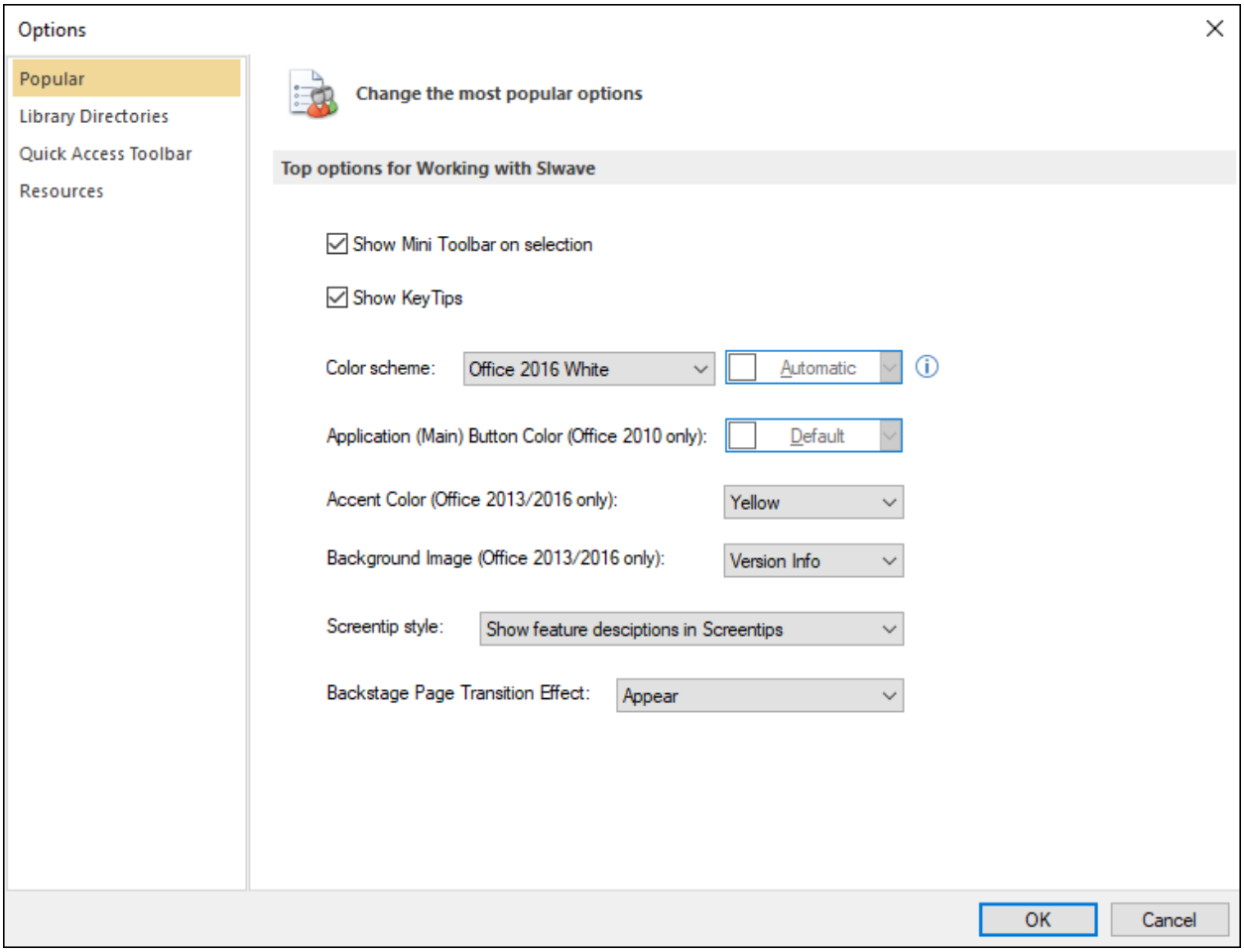
Popular Tab



Use the **Popular** options to show or hide the mini toolbar and key tips, and to change SIwave's color scheme and background effects.

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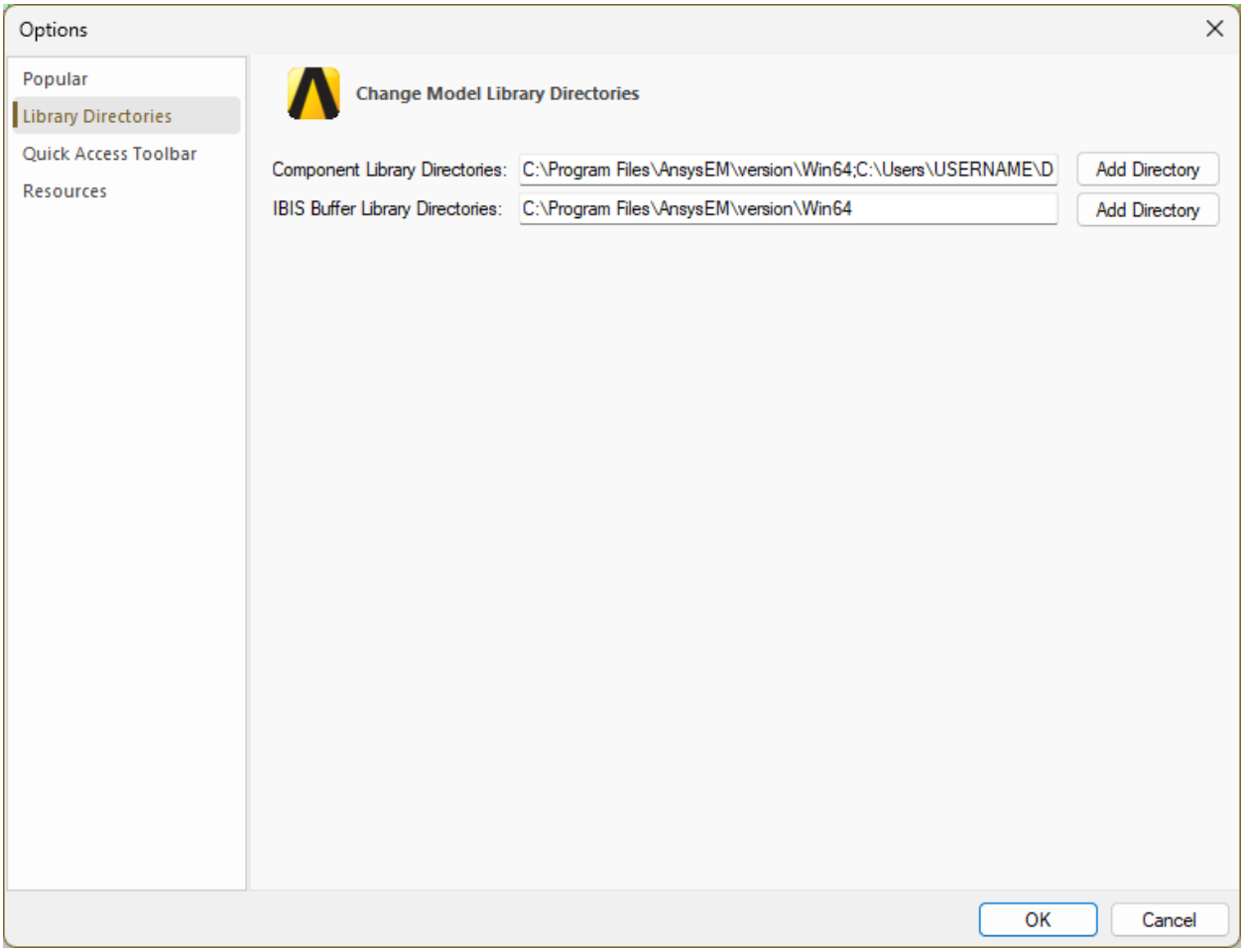
Library Directories Tab



The Component Library directories store third-party capacitor and inductor S-parameter models. By default, the directories are (separated by a semicolon): *C:\Program Files\AnsysEM\<version>\Win64* and *C:\Users\<USERNAME>\Documents\Ansoft\PersonalLib*.

> **Note:**
>
> From the **C:\Program Files\AnsysEM\<*version*>\Win64** directory, components are stored in a folder called "**complib**".

The IBIS Buffer Library stores IBIS driver/receiver models and defaults to *C:\Program Files\AnsysEM\<version>\Win64*.

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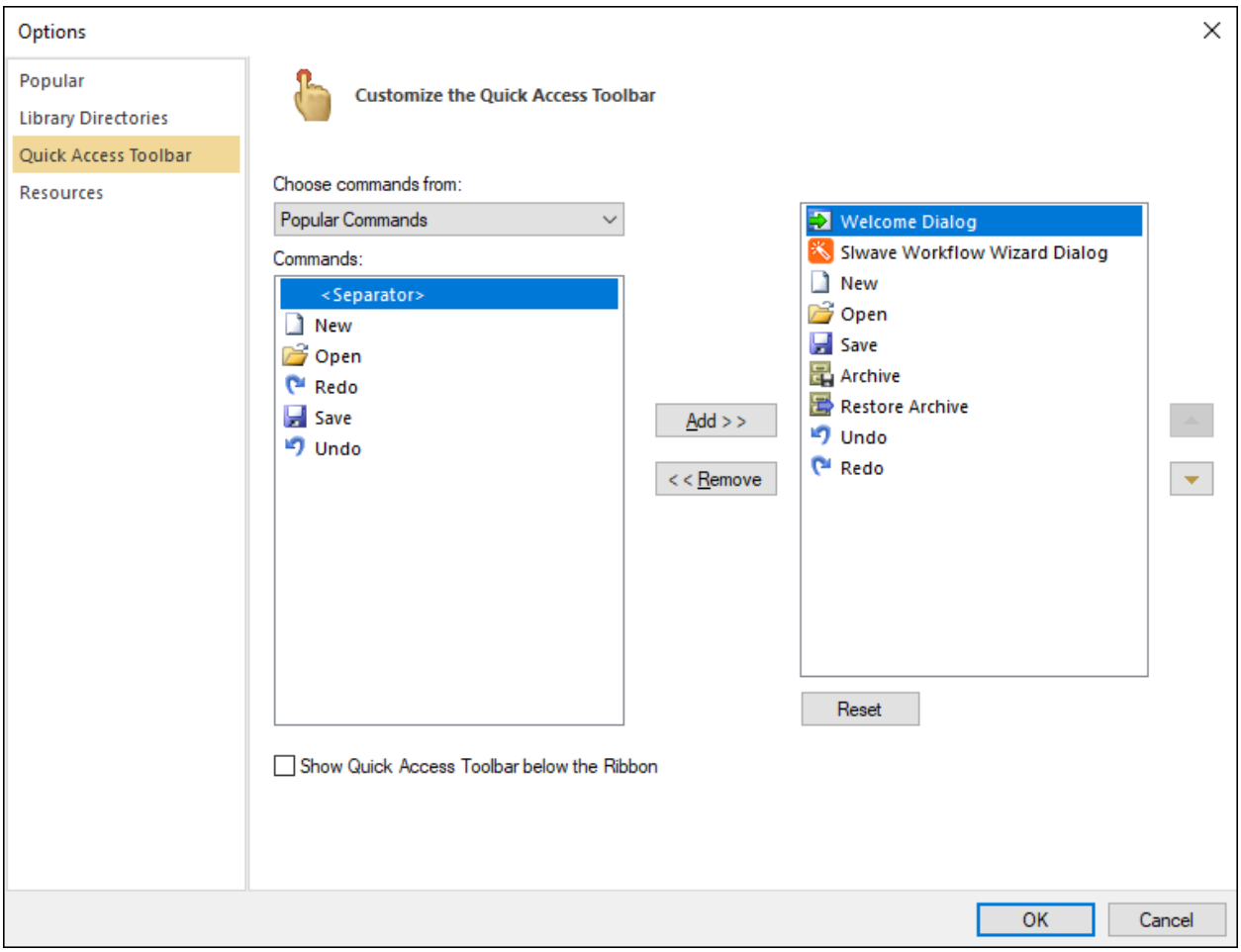
> **Note:**
>
> From the C:\Program Files\AnsysEM\<*version*>\Win64\ directory, components are stored in a folder called "**buflib**".

Use the **Add Directory** buttons to specify directories. SIwave supports the selection of multiple directories. If you specify more than one directory (e.g., to have a primary and a backup directory), the directories display in their field separated by a semicolon.

Quick Access Toolbar Tab



Move items to and from the Quick Access Toolbar using the **Add>>** and **<<Remove** buttons. You can also **Reset** the toolbar to its default settings, or select **Show Quick Access Toolbar below the Ribbon** to change its placement.

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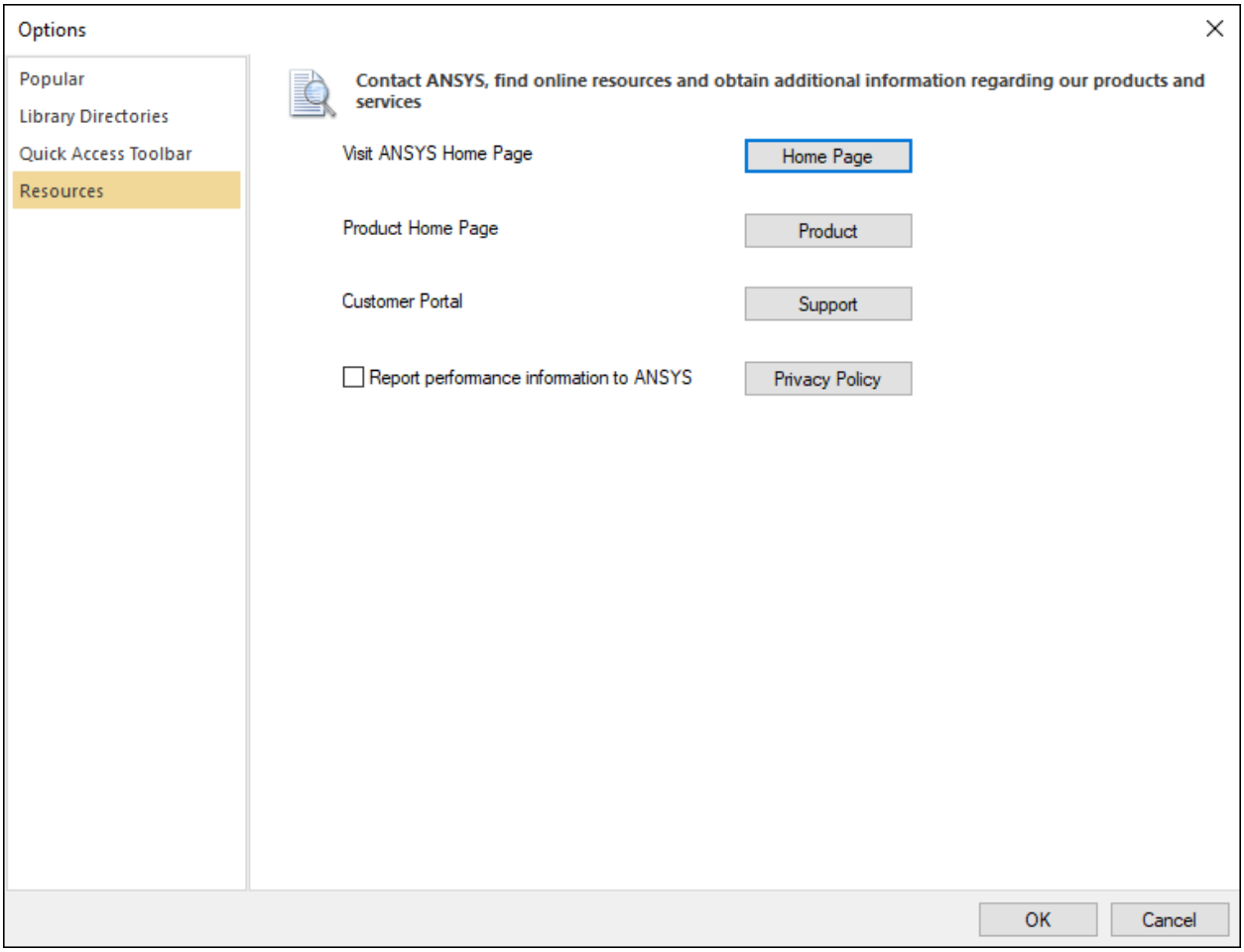
Resources Tab



Click the links to visit the Ansys home page, SIwave home page, or Customer Portal. You can also choose whether you want to take part in the Ansys Product Improvement Program.

Importing and Exporting SIwave Settings Files

Some project settings can be exported to an SIwave Settings File (*.sef) and later imported into new projects.

To export an *.sef file:

1. Click **Export** > **Settings File**.

   The **Settings File Export Options** appear.

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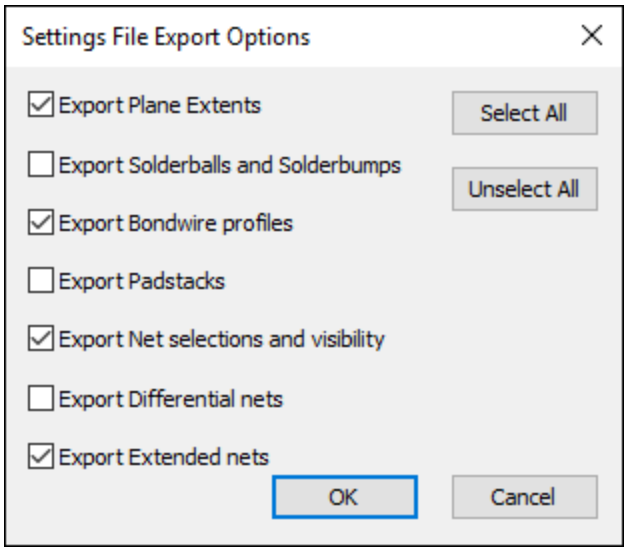

2. Select an appropriate options.
3. Click **OK**.

   A file browser window appears.
4. Enter a **File Name** and select a save location.
5. Click **Save**.

To import an existing *.sef file:

1. Click **Import** > **Settings File**.

   A file browser window appears.
2. Browse to the *.sef file and click **Open**.

   The settings are applied.

Opening and Closing a Project

Creating a New Project

To create a new SIwave project file, click **FILE** > **New**, or click the **New** icon in the Quick Access Toolbar. Alternately, you may press **Ctrl+N** on your keyboard. If another file is already open, you will be asked to save it before creating a new file.

A new project named Untitled displays.

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Opening an Existing Project

To open a previously saved project file, click **FILE** > **Open**, or click the **Open** icon in the Quick Access Toolbar. Alternately, you may press **Ctrl+O** on your keyboard. Select the file you want to open. If another file is already open, you will be asked to save it before opening.

You can use the **Open** option to open SIwave projects (*.siw) and SIwave template files (*.sit).

If you wish to open an SIwave archive file (*.siwz), you must use **FILE** > **Restore Archive**, or the **Restore Archive** icon in the Quick Access Toolbar.

Saving a Project File

To save a project, click **FILE** > **Save**, or click the **Save** icon in the Quick Access Toolbar. Alternately, you may press **Ctrl+S** on your keyboard.

To save a project as something other than its existing file name, click **FILE** > **Save As**.

Archiving and Restoring Projects

You can place a project and any other files related to the project that you want to include in an SIwave archive file (*.siwz). An .siwz file is a compressed file type that can be opened in any program that can read .zip files. The **Archive** command automatically detects an appropriate files for linked projects and includes them in the archive. The project file, simulation results, and all externally referenced files, including component library parts, are included in the archive.

Archiving a Project

Complete the following steps to archive a project.

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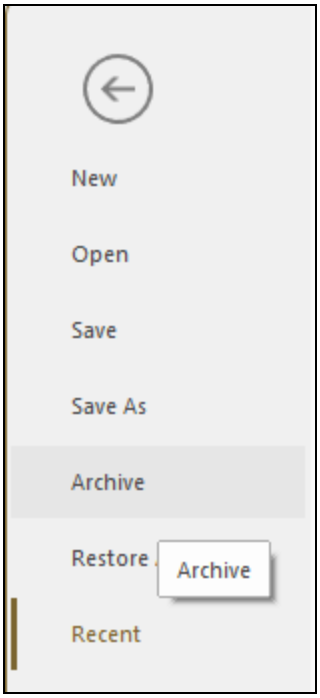
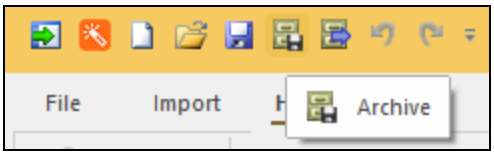
1. Do either of the following to open an explorer window.
   - Navigate to **File** > **Archive**.



   - From the **Quick Access Toolbar**, select **Archive**.



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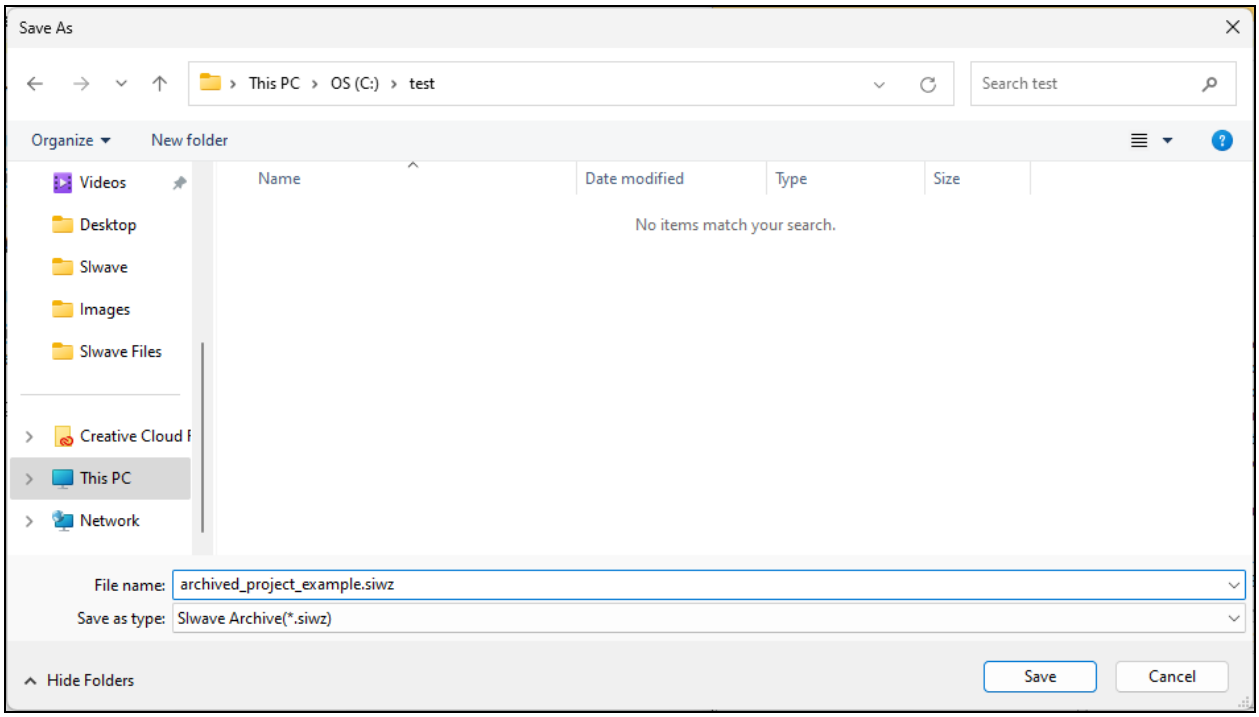
2. Navigate to an appropriate directory and enter a **File name** for the archive (e.g., archived_project_example.siwz). Then click **Save**.



The procedure is complete.

Restoring an Archived Project

Complete the following steps to restore an archived project.

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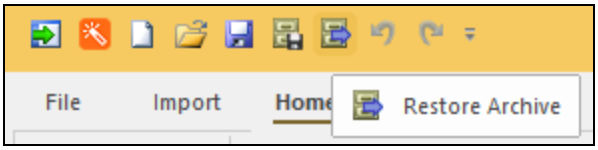
1. Do either of the following to open an explorer window:
   - Navigate to **File** > **Restore Archive**.

   - From the **Quick Access Toolbar**, select **Retore Archive**.



2. Navigate to an appropriate file and select it (e.g., **archived_project_example.siwz**). Then click **Open**. Users will be immediately prompted to save the unarchived .siw project file (i.e.,

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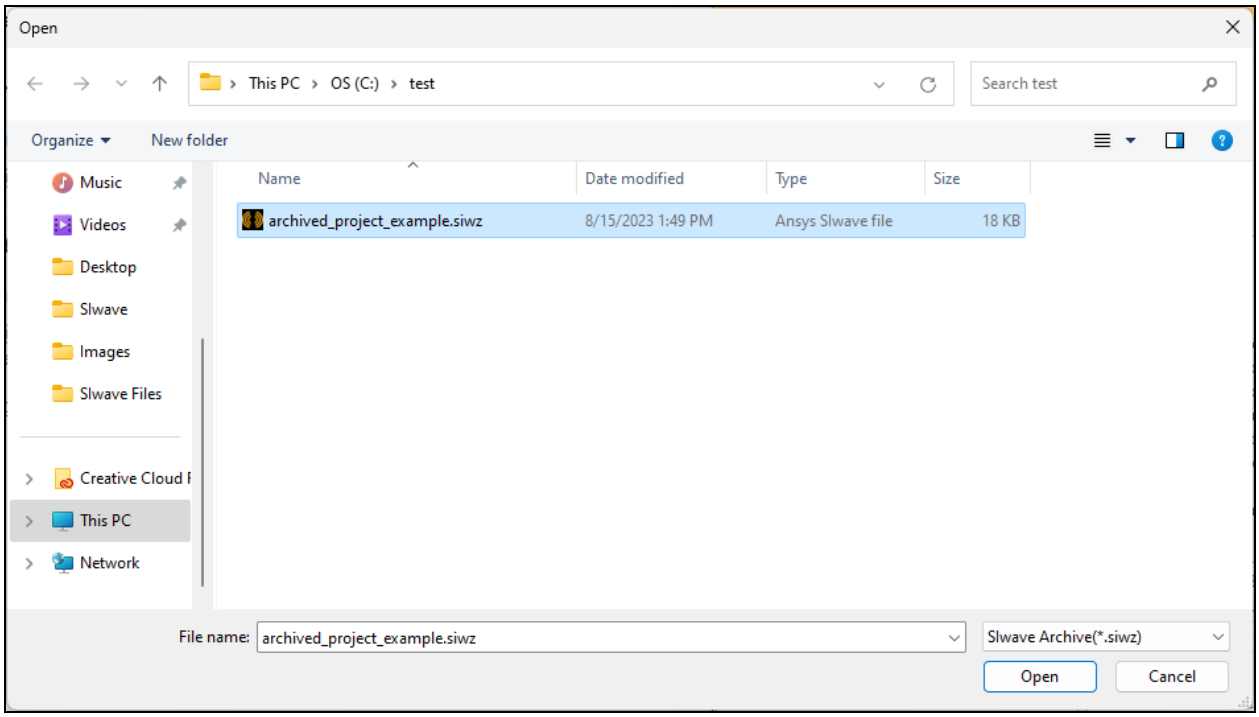
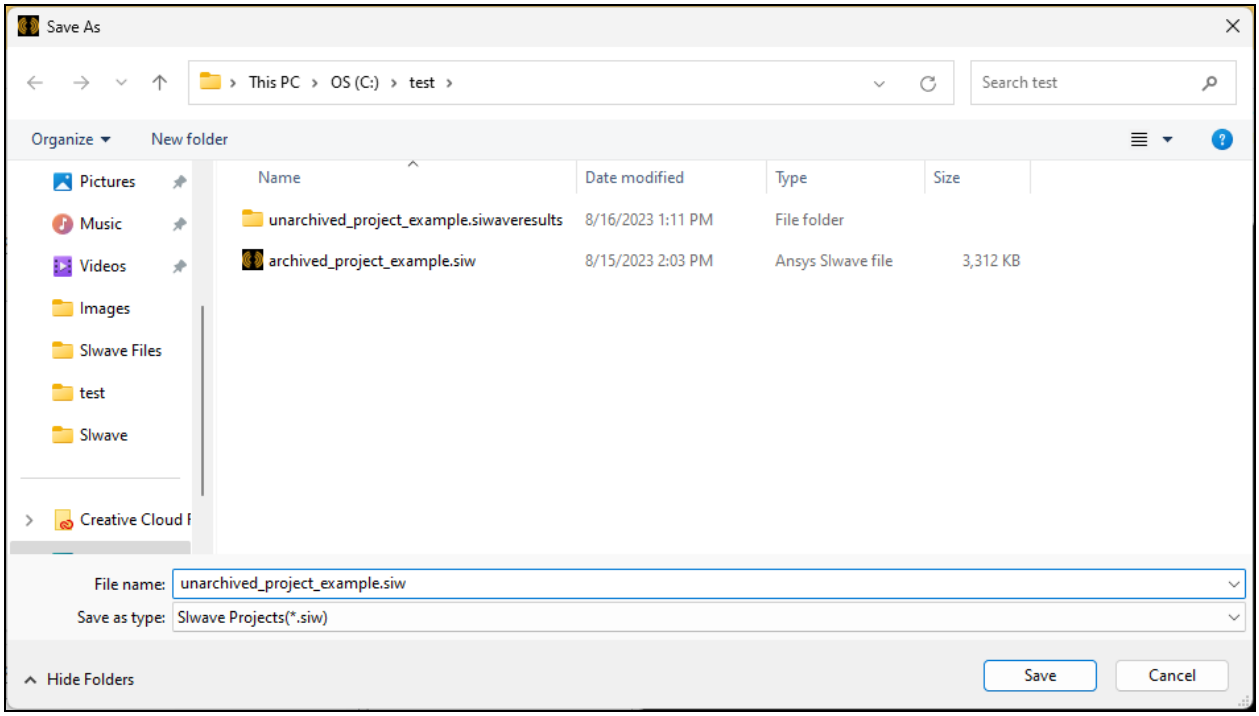
SIwave file).



3. Navigate to an appropriate directory and enter a **File name** for the archive (e.g., **unarchived_project_example.siw**). Then click **Save** to continue extraction.



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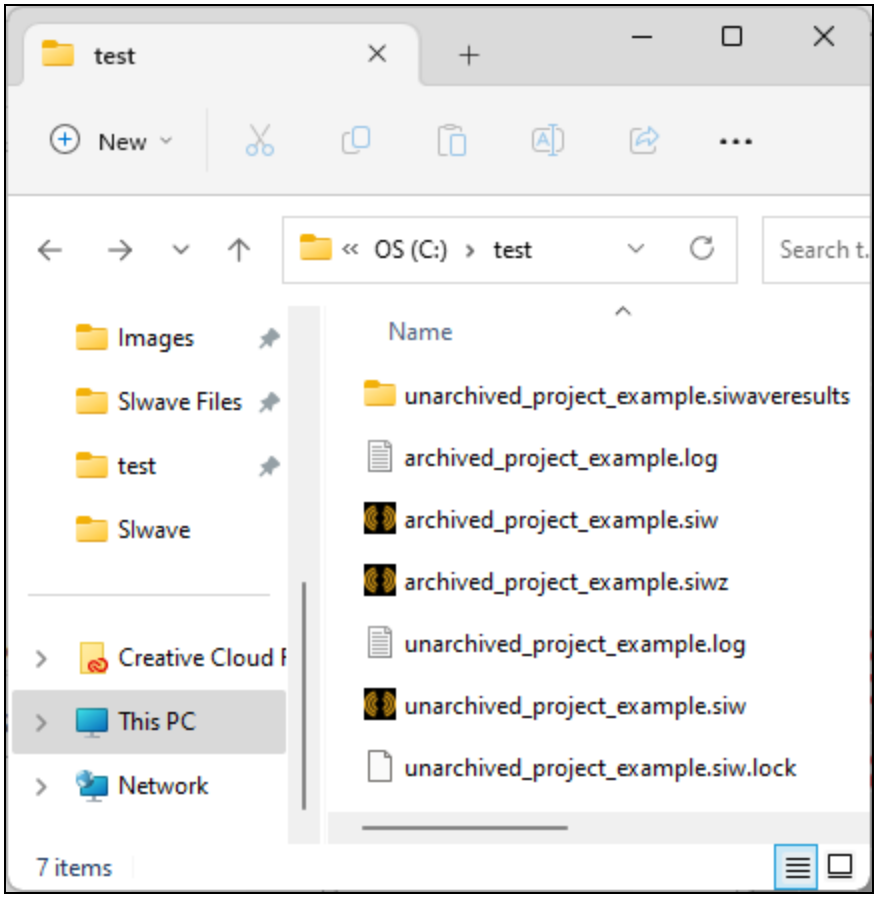
4. The contents of the .siwz file are extracted to the location selected in step **3**.



5. Components that are not part of the standard component library found in the installation directory are extracted to subfolders in the first writable component library location (i.e., by default, the users' **PersonalLib** folder located at C:\Users\<*USERNAME*>\Documents\Ansoft\PersonalLib).

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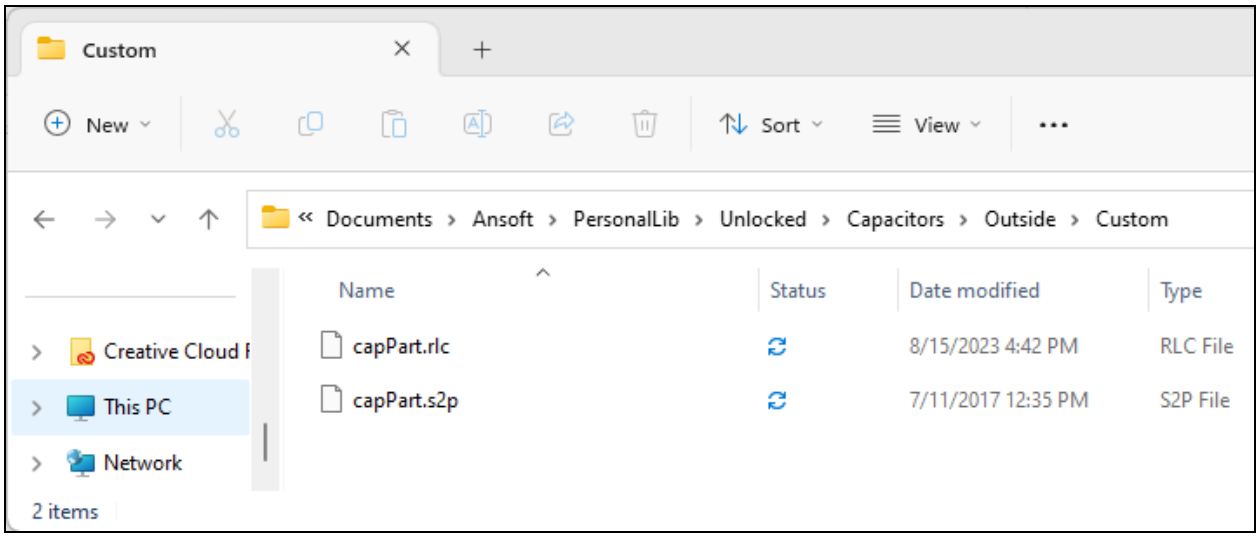

The procedure is complete.

Running SIwave from the Command Line

You can open SIwave and perform various functions directly from the command line.

To run SIwave from the command line, use the following syntax:

```
<path to siwave.exe> <path to *.siw file> <optionalArgs>
```

Optional Command Line Arguments

SIwave can accept the following command line arguments:

Argument	Description
-batch	Runs SIwave in batch mode.
-edb <path>	Specifies an EDB folder name for import. **Example:** "C:\[InstallDirectory]\siwave.exe" -edb "C:\Examples\Signal Integrity\SSN.aedb"
-edb_design <cellName>	Specifies a cell name within EDB to import (in case EDB contains multiple cells).
-exec_ac	Executes a Frequency Sweep.
-exec_cpa	Executes a CPA simulation.
-exec_crosstalk_scan	Executes a Frequency Domain Crosstalk Scan.

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Argument	Description
-exec_dc	Executes a DC simulation.
-exec_eigen	Executes a Resonant Modes simulation.
-exec_ff	Executes a Far Fields simulation.
-exec_iv	Executes an Induced Voltage simulation.
-exec_nf	Executes a Near Fields simulation.
-exec_psi_ac	Executes a PSI AC scan.
-exec_psi_syz	Executes a PSI SYZ scan.
-exec_syz	Executes an SYZ simulation.
-exec_td_crosstalk_scan	Executes a Time Domain Crosstalk Scan.
-exec_vc	Executes a Validation Check.
-exec_z0_scan	Executes an Impedance Scan.
-f <path>	Specifies an ANF file for import.
-ng	Invokes SIwave in iconified mode.
-ownEdb	Takes ownership of an EDB file.
-resetWorkspaces	Resets UI workspaces (in case of registry corruption).
-runscript <path>	Specifies a VBS or IPY script to execute.
-runscriptandexit <path>	Specifies a VBS or IPY script to execute, and shuts down SIwave afterward.
-useElectronicsPPE <bool>	Selects Pro, Premium, Enterprise product licensing. 1 = activate. 0 = deactivate.
-waitforlicense	Waits until required licenses are available.

Running SIwave in Non-Graphical Batch Mode

In batch mode, the SIwave GUI never opens.

To run SIwave in non-graphical batchmode, use the following syntax:

```
siwave_ng <path to .siw> <path to .exec file> -formatOutput -
useSubdir
```

This command, in addition to executing a requested simulation type, creates an appropriate directory hierarchy so that results can be post-processed in the UI. The arguments do the following:

- **formatOutput** – instructs SIwave to generate information/error/warning messages in a verbose format that is intended for consumption by the SIwave user interface.

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- **`useSubdir`** – instructs siwave_ng *not* to create a separate .siwaveresults working directory for simulation setup and execution. Processing is performed in the directory containing the SIwave project (or AEDB) passed as the first argument.

> **Note:**
>
> An `.aedb` directory file (e.g., Ansys Electronics Database) or `.siwz` archive file may be substituted for an `.siw` file.

Running Batch Mode Simulations Remotely

To run a simulation on a remote server, use the following syntax:

```
-rs <server_name> <TCP/IP port number on server> <remote_project_
name>
```

Example:

```
siwave_ng pcb.siw syz.exec -rs remotesrv01 31000 pcb
```

> **Note:**
>
> The remote server must be preconfigured as described in Running a Remote Solve for Windows or Linux.

Exec File Strings

The .exec file should contain one at least one of the following strings (which specify the type of analysis to execute):

String	Result

`AddSwp` `<fstart> <fstop> <numpts> <Decade|Linear> [linear frequency step size]`	Adds additional sweep points, allowing for changes in the number of points used and sweep type.
	Used in conjunction with `SetSwp`.
	Example:
	`SetSwp 0 1000 10 Decade`
	`AddSwp 1000 5e9 500 Linear 5`

`AutoIdPgNets`	Auto identification of signal & power/ground nets.
`ClearDiffNetClassification`	Clears differential net classification on the attached project.
`Compute DcL` `<boolean>`	Determines whether to perform DCL calculation during DC IR simulation.

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String	Result
ComputeExactDcPt <boolean>	Run an SYZ simulation with the exact DC point computation enabled.
CpaSimulationFidelity	Arguments are optimal or exhaustive. When optimal is used as an argument, you can see partial inductance in RLGC matrix. If exhaustive is used as an argument, you will see loop inductance.
CpaUseQ3D <boolean>	Determines whether to use Q3D solver during CPA RLGC solve.
CpaChannelSetup <boolean>	For a CPA simulation, 1 selects CPA channel setup. 0 selects individual source/sink setup.
CpaEsdrModel <boolean>	For a CPA simulation, 1 selects ESD R Model. 0 selects RLCG model.
CrosstalkScanConfigFile <path>	Specifies the path to a Crosstalk Scan configuration file. See Crosstalk Scan Automation. **Example:** `CrosstalkScanConfigFile "C:/Folder/xtalk_config.xml"`
CrosstalkThreshold	Corresponds to the coupling threshold set in SI/PI Advanced Options.

DiffNetDifferentiators	Used to classify nets as differential based on the specified net name suffix pair; two strings separated by a semicolon should be provided on each `DiffNetDifferentiators` line in the EXEC file
	Example:
	`DiffNetDifferentiators _P;_N`
	`DiffNetDifferentiators +;-`

DistributeCpa HpcHostName <machine_name|IP address> <CPUs_to_use> <%Memory>	Configures CPA-Q3D simulations for distribution.
	Example:
	`DistributeCpa`
	`HpcHostName \\cdcebudevw10 8 80`
	`HpcHostName \\cdcebudevw14 8 90`

DistributePsiSyz HpcHostName <machine_name|IP address> <CPUs_to_use> <%Memory>	Configures PSI SYZ simulations for distribution. **Example:**

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String	Result

	`DistributePsiSyz`
	`HpcHostName \\cdcebudevw10 8 80`
	`HpcHostName \\cdcebudevw14 8 90`

`DistributeSIwaveSyz` `HpcHostName <machine_name|IP address> <CPUs_to_use> <%Memory>`	Configures SIwave SYZ simulations for distribution.
	Example:
	`DistributeSIwaveSyz`
	`HpcHostName \\pitansoft10 6 80`
	`HpcHostName \\pitansoft11 6 80`
	`HpcHostName \\pitansoft12 6 80`

`EmiScanRulesFile` `<path>`	Sets the EMI Scanner rules file. A rules file can be generated using the Export Rules File button in EMI Scanner. **Example:** `EmiScanRulesFile "E:/Ansys/Scripting/EMI_scanner_rules.xml"`
`EmiScanTagsFile` `<path>`	Sets the EMI Scanner tags file. A tags file can be generated using the Export Tags File button in EMI Scanner. **Example:** `EmiScanTagsFile "E:/Ansys/Scripting/EMI_scanner_tags.tgs"`
`EnableQ3dDomains` `<boolean>`	Enables 3D DDM during SIwave SYZ sweep.
`ExecAcSim`	Computes a Frequency Sweep.
`ExecCrosstalkSim`	Computes a frequency domain Crosstalk Scan.
`ExecDcSim`	Computes a DC IR Drop simulation.
`ExecEmiScanSim`	Computes an EMI Scan.
`ExecFfSim`	Computes a Far Fields simulation.
`ExecFwsSim`	Computes full wave SPICE subcircuits.
`ExecHfssPiSyzSim`	Pulls HFSS solve license and computes SYZ parameters using HFSS-PI.
`ExecIcepakSim`	Computes an Icepak simulation.

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String	Result
ExecInducedVoltageSim	Computes an Induced Voltage simulation.
ExecMTTFSim	Computes an EM MTTF simulation.
ExecNfSim	Computes a Near Fields simulation.
ExecPdnSim	Computes a PDN Channel Builder simulation.
ExecPiOptSim	Computes a PI Advisor simulation.
ExecPsiPdnSim	Computes a PDN Channel Builder simulation using PSI.
ExecResModeSim	Computes a Resonant Modes simulation.
ExecSentinelCpaSim	Computes a CPA simulation.
ExecSentinelPsiAcSim	Computes AC currents using the PSI solver.
ExecSentinelPsiSyzSim	Computes SYZ parameters using the PSI solver.
ExecSyzSim	Computes SYZ parameters using SIwave.
ExecTimeDomainCrosstalkSim	Computes a time domain Crosstalk scan.
ExecZ0Sim	Computes an Impedance scan.
ExportIBIS <path>	Specifies the path to an IBIS file to export after S-parameter simulation (either SIwave or PSI) completes. **Example:** `ExportIBIS "C:/Simulation Results/SIwave/IBIS/package_design_rev1.ibs"`
ExportDcThermalData <boolean>	Determines whether to export DC thermal data during DC IR simulation.
ExportNearField	Exports Near Field data to the project directory.
ExportTouchstone <path>	Exports Touchstone data to the specified directory. **Example:** `ExportTouchstone "C:/Test"`
HpcHostName	Specifies the name of a machine to use for distributed solves; the machine name can be provided as an IP address or in UNC format. Two additional parameters after the machine name specify the number of cores to use on the machine and the fraction (as a percentage) of total memory available for simulation on that machine. **Example:**

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String	Result
	`HpcHostName \\cdcebudevw10 8 80` `HpcHostName 10.3.27111 8 80`
IBISExportFrequency	Specifies the frequency at which the IBIS export (specified by the ExportIBIS directive) is to be performed. **Example:** `IBISExportFrequency "500MHz"`
IcepakThermalDataDir	Specifies the location of the dcthermal power files for use in an Icepak simulation. This takes priority over the dcthermal location for the DC simulation on which the Icepak simulation is based.
IncludeInfGnd	Specifies the elevation of an infinite ground plane below the bottom-most metal layer. Such infinite ground planes only impact SIwave AC (resonant mode, frequency sweep, SYZ and impedance/crosstalk scans) simulations. **Example:** `IncludeInfGnd 100mil`
InterpSwpCvg `<Relative error for S>`	Specifies the relative error for S during an interpolating sweep.
MinCutoutArea	Specifies an area threshold for small cutout/void defeaturing in planes. All voids under this threshold are considered as filled in metal during SIwave AC (resonant mode, frequency sweep, SYZ, impedance/crosstalk) simulations. **Example:** `MinCutoutArea 3mm2`
MpiVendor `<Intel|Microsoft>`	Specifies the MPI vendor (either Intel or Microsoft) to use during distributed simulations. **Example:** `MpiVendor Intel`
MpiVersion `<2018|2021>`	Specifies the MPI version to use during distributed simulations. **Example:** `MpiVersion 2021`

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String	Result
MTTFSimConfigFile <path>	Specifies the path to an EM MTTF configuration file. See EM MTTF Simulation Automation. **Example:** `MTTFSimConfigFile "C:/Folder/mttf_config.xml"`

NetsToSimulate .*	The token following "NetsToSimulate" is interpreted as a Perl regular expression, so you can filter out/include nets.
	Example:
	`ExecSyzSim`
	`NetsToSimulate VCC.*`
	`NetsToSimulate GND.*`
	`NetsToSimulate ^A-MII.*`
	`NetsToSimulate ^RAM.*`
	`ExecZ0Sim NetsToSimulate ".*" SetNumCpus 30`
	`ExecCrosstalkSim NetsToSimulate ".*" SetNumCpus 30`

NumInterpPts <int>	Specifies the number of points for the interpolating sweep.

NumProcsPerPsiEngine <int>	Used in PSI SYZ distribution.
	Example:
	`ExecSentinelPsiSyzSim`
	`DistributePsiSyz`
	`NumProcsPerPsiEngine 6`
	`HpcHostName \\cdcebudevw10 8 80`
	`HpcHostName \\cdcebudevw14 8 90`

PerformErc <true|false>	Determines whether to perform ERC during simulation setup.
ProjectDir <path>	Specifies the project directory.
PsiSyzEnforceDcPtAndCausality	Checks for the presence of DC points in the Results folder *.sNp file.

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String	Result
PsiSyzSetAdaptiveSampling	Checks for the presence of DC points in the Results folder *.sNp file. Adds frequency points near changes in response. A larger number of frequency points will be outputted in the *.SBin and Touchstone files.
PsiSyzSetFastSwp	Checks for the presence of "Fastsweep has been selected" in the _PSI.log file. The number of frequencies required to simulate should be smaller at the expense of more memory.
PsiSyzSetInterpSwp	Use Interpolating sweep.
PsiWorkingDir	Specifies a temporary working directory for the PSI solver to use during simulation. This directory must be writable. **Example:** `PsiWorkingDir "C:/Temp"`
PsiSharedDir	Specifies a shared directory that all machines specified in the distributed solve setup for PSI SYZ simulations must be able to access and write into. **Example:** `PsiSharedDir "\\cdcebudevw10\users\john\psi_shared_dir"`
RemoveCutoutsByArea <yes|no>	Specifies whether voids whose areas fall under the threshold indicated by the `MinCutoutArea` directive are to be removed during SIwave AC simulations. **Example:** `RemoveCutoutsByArea yes`
SaveArchive <*.siwz path>	Saves the SIwave archive.
SaveEdb <*.aedb path>	Saves the Ansys Electronics Database file.
SaveSiw <*.siw path>	Saves the SIwave project.
SaveSiwWithModels <*.siw path>	Saves SIwave project and all associated vendor capacitor and inductor S-parameter models into a single *.siw file that can be simulated on a different system without loss of model assignments.
SetDCSimName - <name>	Sets the name of a DC IR simulation.

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String	Result
SetDiscreteSwp	Tells the simulation to use a discrete sweep.
SetEmiScanSimName - <name>	Sets the name of an EMI scan.
SetFdXtalkScanSimName - <name>	Sets the name of a Frequency Domain Crosstalk scan.
SetMTTFSimName - <name>	Sets the name of an EM MTTF simulation.
SetIcepakSimName - <name>	Sets the name of an Icepak simulation.
SetInterpSwp	Tells the simulation to use an interpolating sweep.
SetNumCpus <int>	Sets the number of CPUs.
SetSIwaveSyzSimName - <name>	Sets the name of an SIwave SYZ simulation.
SetSwp <freq_start> <freq_end> <num_pts> <linear|decade> [linear frequency step size]	Used to specify Frequency Sweep parameters. **Examples:** SetSwp 0 1000 10 Decade SetSwp 0 5e9 100 Linear SetSwp 5e9 10e9 100 Linear 10e6 (Sweep from 5GHz to 10GHz with a frequency step size of 10MHz)
SetTdXtalkScanSimName - <name>	Sets the name of a Time Domain Crosstalk scan.
SetZ0ScanSimName - <name>	Sets the name of an Impedance scan.
SIwaveSyzEnforceCausality <boolean>	Enforces causality for a discrete or interpolating SYZ sweep.
SIwaveSyzEnforcePassivity <boolean>	Enforces passivity for a discrete or interpolating SYZ sweep.
SolverMemLimit <%Memory>	Sets the maximum percentage of memory to be used by the solver on a machine when using a HPC License. Used in conjunction with UseHpcLicenses. **Example:** UseHpcLicenses pack SolverMemLimit 80
TraceReturnCurrentDist <1|0>	Specifies whether to activate trace return current calculation during SIwave AC simulations. 1 = activate. 0 = deactivate. **Example:**

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String	Result
	`TraceReturnCurrentDist 1`
`UniformTemperature` `<int>`	Sets the uniform design temperature, in Celcius. **Example:** `UniformTemperature 100`
`UseElectronicsPPE` `<bool>`	Forces the use of Pro, Premium, Enterprise product licensing if it isn't selected in the SIwave UI. 1 = activate. 0 = deactivate.
`UseHpcLicenses` `<pack|pool>`	Specifies HPC license type.
`UseHpcLicenseVendor` `<ansys|electronics>`	Specifies the HPC license vendor.
`WaitForLicense` `<boolean>`	Specifies whether to wait for a solve license if one is unavailable.

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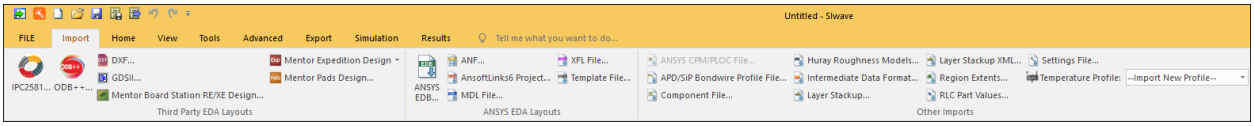
3 - Importing Projects

SIwave enables you to import a project from a variety of sources.

Types of files SIwave can import include:

- DXF
- GDSII
- Mentor Board Station RE/XE Design
- Mentor Expedition Design
- Mentor PADS Design
- IPC2581
- ODB++
- Lead Frame Design
- ANF
- Ansys EDB
- Legacy ALinks (AnsoftLinks6) Project
- MDL
- XFL
- Template

To import a project, click the **Import** tab.



Select the option for the type of file/folder you would like to import. Then browse to the file and click **Open**.

The import of some file types requires additional steps. Those are:

- DXF
- GDSII
- IPC2581
- Altium Designer R10 ODB++
- Component
- RLC Part Values

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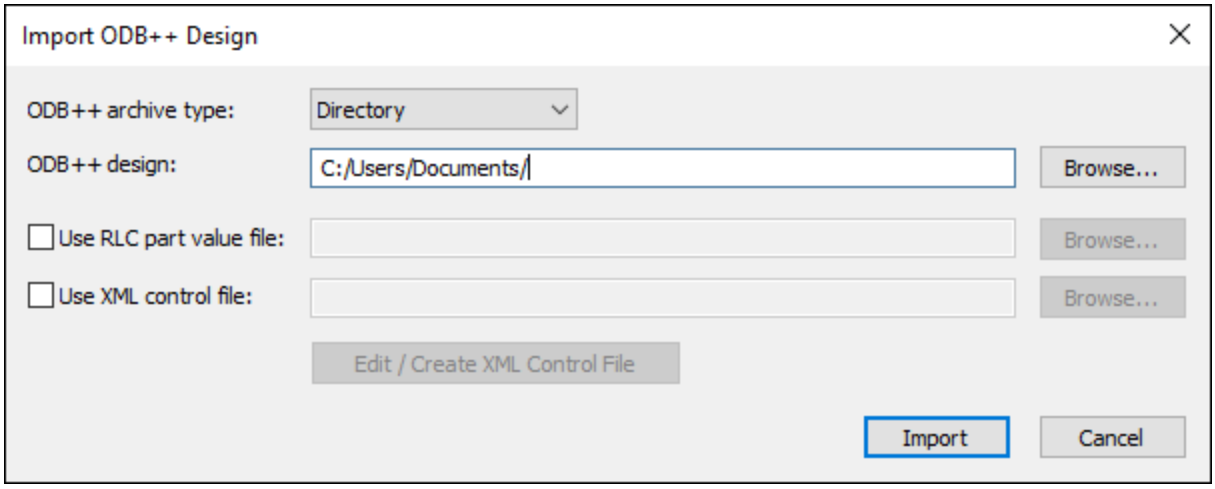
Importing Altium Designer R10 ODB++ Design

To import an existing ODB++ design from Altium Designer R10 into SIwave:

1. Click **Import** > **ODB++ Design**.

   The **Import ODB++ Design** window appears. You can import a file or directory.



2. To import a file:
   a. Select **File** from the **ODB++ archive type** drop-down menu.
   b. Select the **ODB++ design** you want to open. Click **Browse** to select a design file. By default, files with .**tgz** extensions are displayed.
3. To import a directory:
   a. Select **Directory** from the **ODB++ archive type** drop-down menu.
   b. Select the **ODB++ design** you want to open. Click **Browse** to select a design directory.
4. Click the **Use RLC part value file** check box if you want to use a part value file. Click **Browse** to select an existing part value file. By default, files with **.rlc** extensions are displayed.
5. Click the **Use XML control file** check box if you want to use a control file. Click **Browse** to select an existing control file. By default, files with .**xml** extensions are displayed.

   To edit the selected control file or create a new XML control file, click the **Edit/Create XML Control File** button. The XML Control File Editor opens. Make an appropriate additions or modifications, assign a name for a new control file, and click **Save**.

6. Choose **Import** to complete the selection.

Importing DXF Files

To import an existing DXF file design into SIwave:

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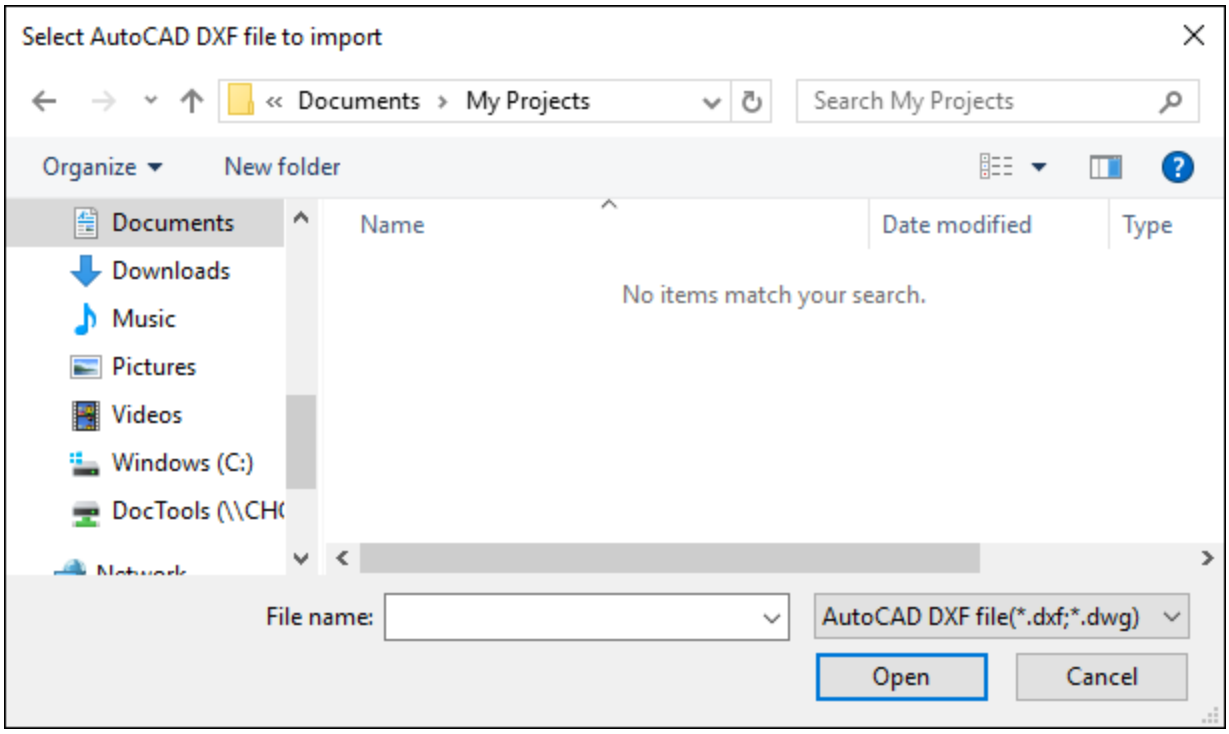
1. Click **Import** > **DXF**.

   The **Open** window appears.



2. Select the file you want to open. By default, files with .**dxf** and **.dwg** extensions are displayed.

   The **AutoCAD Import** window appears.

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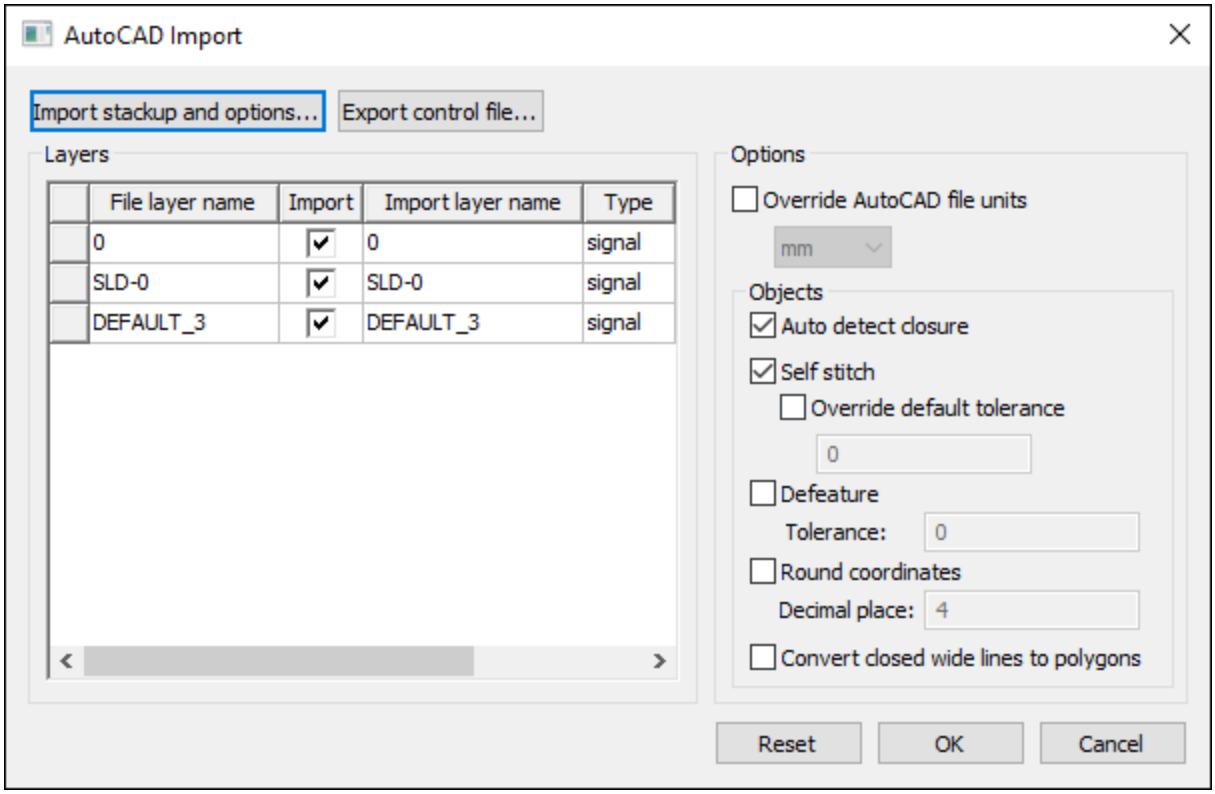

3. Click **Import stackup and options** to import the information from an xml control file or a layer mapping file. The layer choices and information in the window are replaced with the layer information from the imported file.
4. Click **Export control file** to write to an xml control file based on the information in the window to the location specified.
5. From the **Layers** panel:
   a. Select the **Import** check box to specify which layers to import.
   b. Modify the **Import layer name** if needed.
   c. Modify the **Type** if needed. This identifies the layer type that will be used to place each layer in the file. Use **via** type to identify a layer as a "via layer" that can be used to create vias in the design. When a GDSII layer is marked to be a via, the objects on the layer will be used to create vias that connect from the previous layer to the following layer (as found in the grid control of the import window). The top and bottom layer cannot be marked as via layers because there are not two layers to connect, and there also may not be more than one consecutive via layer.
6. From the **Options** panel:

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a. Select the **Override AUTOCAD file units** check box to modify the units.
b. Select **Auto detect closure** to check polylines to see whether or not they are closed. If a polyline is closed, a polygon is created in the design.
c. Select **Self stitch** to cause multiple straight line segments to be joined to form polylines. Tolerance is used to decide if two coordinates are the "same" and should be considered for joining. If the resulting polyline is closed, a polygon is created. You have the choice of two different tolerances for self stitching: Default Tolerance and explicit Tolerance. Default tolerance is a geometric tolerance based on the extents of the project being imported. You can **Override default tolerance** and enter a value for explicit tolerance to expand the tolerance based on your knowledge of the dxf project being imported.
d. Select **Defeature** to remove certain small features in the imported geometry to reduce complexity. The features that are removed include multiple points placed within the specified distance, thin or narrow regions ("thins" and "spikes"), and extraneous points along straight line segments. Specify the distance in the **Tolerance** box.
e. Select **Round coordinates** to round all imported data to the specified number of decimal places.
f. Select **Convert closed wide lines to polygons** to import wide polylines as polygons. You have more flexibility to change the shape of such an object when it is imported as a polygon.

The following DXF entities can be imported as 2 dimensional objects from AutoCAD:

- Arc
- Solid
- Circle
- Block
- Ellipse
- Array of blocks (MInsert)
- 2D Polyline, Polyline, and Line

Click **OK** to import the file.

Importing GDSII Files

To import an existing GDSII file design into SIwave:

1. Click **Import** > **GDSII**.

   The **Open** window appears.

2. Select the file you want to open. By default, files with **.gds** and **.strm** extensions are displayed.

   The **GDSII Import** window appears.

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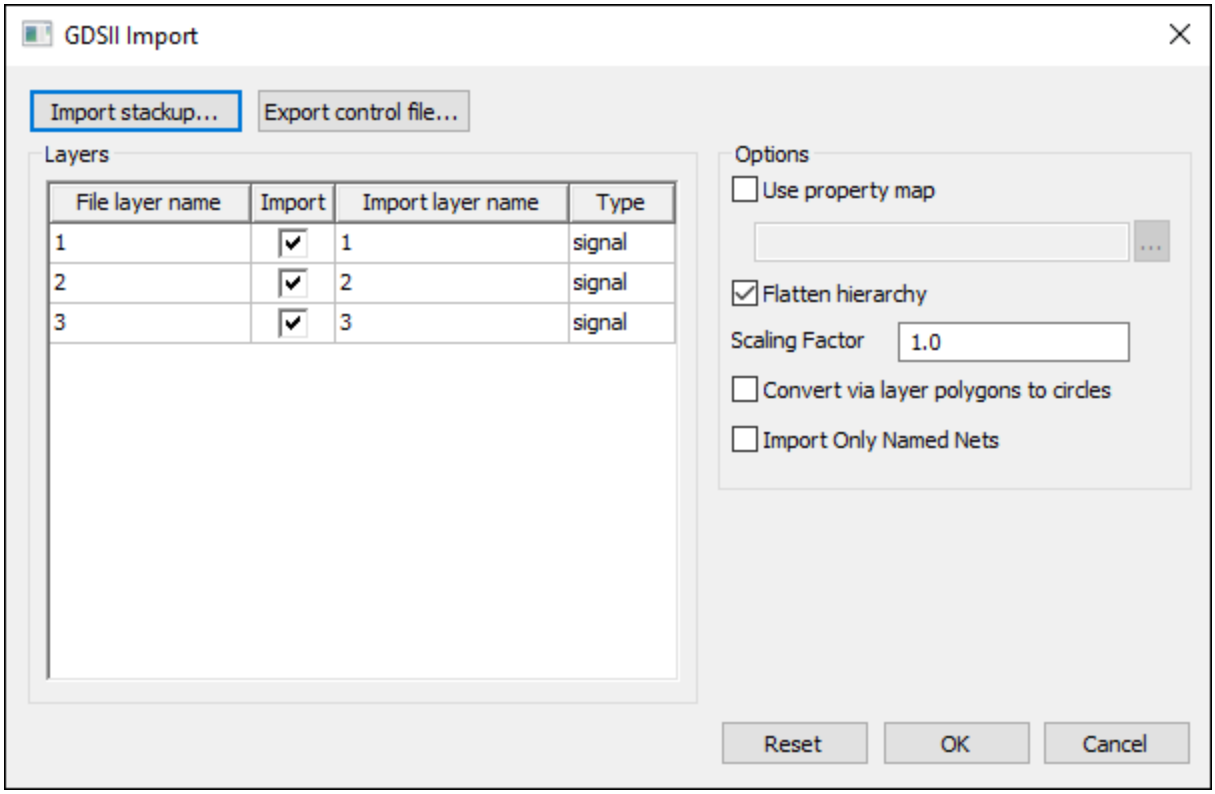

3. Click **Import stackup and options** to import the information from an xml control file or a layer mapping file into the window. The layer choices and information in the window are replaced with the layer information from the imported file.
4. Click **Export control file** to write to an xml control file based on the information in the window to the location specified.
5. From the **Layers** panel:
   a. Select the **Import** check box to specify which layers to import.
   b. Modify the **Import layer name** if needed.
   c. Modify the **Type** if needed. This identifies the layer type that will be used to place each layer in the file. Use **via** type to identify a layer as a "via layer" that can be used to create vias in the design. When a GDSII layer is marked to be a via, the objects on the layer will be used to create vias that connect from the previous layer to the following layer (as found in the grid control of the import window). The top and bottom layer cannot be marked as via layers because there are not two layers to connect, and there also may not be more than one consecutive via layer.
6. From the **Options** panel:

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a. Click **Use property map** and the browse button to specify a Property Mapping File.
b. Click **Flatten hierarchy** to flatten the hierarchy in the original GDSII design or preserve it.
c. Click **Convert via layer polygons to circles** to simplify via creation by converting polygons to circles on layers marked as via layers. SIwave finds the center of the polygon and treats it as the center of the circle. The radius is the distance to one vertex from the center. A polygon is converted to a circle only when the difference in area between the polygon and the circle is less than 10 percent of the area of the circle.

7. Click **OK** to import the file.

   The **Choose EDB Design** window appears.

8. Select a design to be imported, and click **OK**.

Property Mapping File

The format for the .txt property mapping file is:

```
<stream id> <object type> <destination property name>
```

If you specify a property mapping file, the GDSII import creates properties with id and object type combinations found in the map file using the property name specified. The import creates properties on id and object type combinations not found in the mapping file with the name `STREAM PROPERTY #<strmid>`.

Valid objects types are: Dot, Line, Path, Polygon, Rect, Text, ArrayInst, and ScalarInst.

If you do not specify a mapping file, the import interprets properties values as a list of properties separated by the property separator character with the form:

```
<property name> = <property value>
```

For example, height=10, width=20 yields two properties, the first named height with a value of 10, and the second named width with a value of 20.

Lines in the file that are blank and lines beginning with the comment character # are ignored.

Sample Property Mapping File

#Stream	ID	Object Name
1	Rect	instP11
2	Polygon	poly1
3	Path	sigName
4	Text	pad32
5	Pin	io_term

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Importing IPC2581 Design

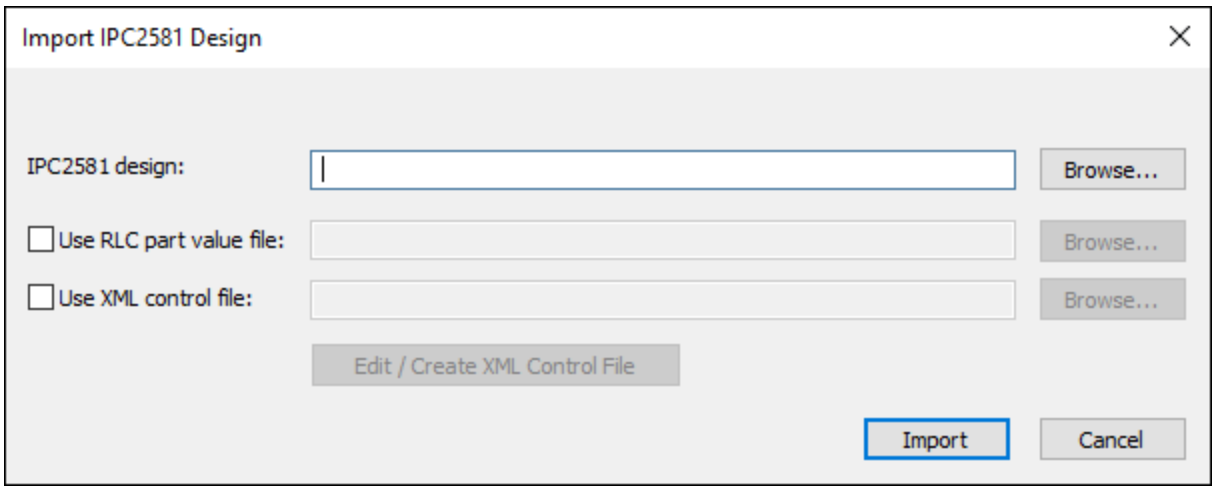
IPC-2581 is an open-source standard developed by the Institute for Printed Circuits IPC-2581 Consortium in 2004.

For more information, visit the IPC-2581 website.

To import an existing IPC-2581 file into SIwave:

1. Click **Import** > **IPC2581**.

   The **Import IPC2581 Design** window appears.



2. Select the IPC2581 design file for import. You can select a *.**cvg** or *.**xml** file.
3. If you want to specify an RLC part value file, check the **Use RLC part value file** check box and click **Browse** to select it.
4. If you want to specify an XML control file, check the **Use XML control file** check box and click **Browse** to select it.
5. Optionally, click **Edit/Create XML Control File** to open the **XML Control File Editor**.
6. Click **Import**.

   The **Select nets to import** window appears.

   a. Optionally, select the **Net Configuration File** to be loaded.
   b. Optionally, select the net(s) to be included from the **Net Name** list. By default all nets are imported.
   c. Optionally, enter the search characters for a **Wild card** search. Then click **Select Matching Rows**.

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d. Select the **Operations** you want to do: You can choose to **Import** selected nets. You can also setup ports between selected nets: Click **Setup Ports**, and choose the corresponding reference net from the **Ports Reference Net** list.
e. Optionally, click **Save Net Configuration File** to save the file as *.**ncf.**
f. Click **Import Configuration**.

This reads the selected file into the current window.

ALinks

SIwave has incorporated all functionality formerly available in the standalone AnsoftLinks product. Using ALinks, SIwave can integrate with third party layout design tools.This allows models to be edited using an external 3D modeler, then be used immediately as the foundations for electromagnetic and thermal analysis.

Upon installation of **Ansys Layout Integration for ECAD**, an ALinks module is incorporated into third-party PCB/package layout tools, and you can export salient design information—such as 2D geometry, layer stackup, and net names—into the SIwave user interface.

Importing Legacy AnsoftLinks6 Files

To import an AnsoftLinks6 (*.APX) file:

1. From the **Import** tab, click **AnsoftLinks6 Project**.
2. Browse to the project directory and select it.
3. Click **OK**.

Accessing SIwave with ALinks from Layout Tools

You can access the interface directly or from a third-party layout package, or create an Ansys Neutral File (ANF) in third-party tools.

The third-party layout tools you can use to create ANFs and access SIwave are listed below. Click a product for more information:

- Zuken CR-8000
- Mentor Board Station
- Mentor PADS

Q3D and HFSS 3D Layout

SIwave with ALinks can also generate Q3D and HFSS 3D Layout projects. Consult the Q3D or HFSS 3D Layout help for more information about running simulations using those products.

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Note:

The **terminalnames.init** file contains default naming conventions for HFSS ports and Q3D sources and sinks, and is located in the installation directory. You can either use the default conventions or you can modify the values in this file.

SIwave ALinks in Mentor Layout Tools

SIwave ALinks connect to Mentor Xpedition and Mentor Boardstation to provide the following capabilities:

- Export Mentor Xpedition design as ODB++
- Write Ansys Neutral File (*.anf) from Mentor Boardstation
- Launch ALinks from Mentor Boardstation
- Launch SIwave from Mentor Boardstation

The Ansys How To Videos YouTube channel contains detailed walkthroughs of these workflows. For example:

- Video: "Mentor Xpedition to Ansys via ODB++"

Launching SIwave with ALinks from Mentor Boardstation

To open SIwave with ALinks from *Mentor Boardstation*:

1. Set the **ALINKS_UNCONNECTED_PINS** environment variable to **No** if you do not want the unconnected pins written to the ANF.

   By default, unconnected pins (not connected to any trace or plane) are written to the ANF.
2. Click **Ansys** > **Launch ALinks**.

   The **ALinks** window appears, with the ANF displayed.

SIwave ALinks in Mentor PADS

In Mentor PADS, SIwave ALinks provide the following capabilities:

- Export Mentor PADS design as ODB++

The Ansys How To Videos YouTube channel contains detailed walkthroughs of these workflows. For example:

- Video: "Mentor PADS to Ansys - ECAD XV"

Exporting a Mentor PADS Design to ODB++

To export an ODB++ file from Mentor PADS:

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1. From the **File** menu, click **Export**.
2. Browse to a save location and enter a **File Name**.
3. From the **Save as Type** drop-down menu, select **ODB++ (*.tgz)**.
4. Click **Save**.

   The **ODB++ Export** window appears.
5. Select options as appropriate:
   - **Neutralize Nets** – enable to neutralize nets. Disabled by default.
   - **Prefer Closed Shapes** – enable to prefer closed changes. Enabled by default.
   - **Format** – select the ODB++ version number.
   - **Unhatched Copper Pours** – ensure this option is set to **Fill**.
   - **Non Shape Pins** – for pins with or without pad shape definition, select Prefer Drill.
   - **Component Outline Layer** – select the component outline layer.
   - **Export Action** – select **Export Only**, or elect to view the generated ODB++ file or run a CAM Compare.
6. Click **OK**.

   The ODB++ (*.tgz) file is created. If there were any warnings or errors, a dialog box will alert you to review these messages.

SIwave ALinks in Zuken CR-8000

In Zuken CR-8000, SIwave ALinks provide the following capabilities:

- Export Zuken design as ANF or EDB
- Export intermediate data file (*.bdf)
- Import Ansys EDB
- Import PI Advisor

The Ansys How To Videos YouTube channel contains detailed walkthroughs of these workflows. For Example:

- Video: "Zuken CR-8000 Design Force to Ansys SIwave - ECAD XVI"

Exporting a Zuken Design to ANF

To export a Zuken design to ANF:

1. In Zuken CR-8000, select the **File** tab.
2. Click **Ansys** and use the drop-down menu to select **Export (ANF)**.

   An export dialog box appears.

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3. Specify the following options:
   - **ANF File** – Click the ellipses button (**...**) to browse to the location where you want to save the file. Enter a name for it and click **Save**.
   - **Parameter File** – Optional. Click the ellipses button (**...**) to select a parameter file (*.ldf) that alters export settings.
   - **Power is handled same as ground** – Toggle on or off. When activated, selected nets are set as Power/Ground nets on export. When deactivated, selected nets are exported as signal nets.
   - **Specify output signal** – Toggle on or off. When activated, you can specify which nets to export.
   - **Add ground net to output signal** – Toggle on or off. When activated, a ground net is automatically added.
   - **Output layer** – When **Add ground net to output signal** is activated, use this field to specify the layer on which to add the ground net.
4. Click **Execute**.

   Zuken exports an ANF and CMP file to the specified location.

   A dialog box appears, listing all layers that were successfully exported.

> **Note:**
>
> Solder resist layers in Zuken CR-8000 will not be exported unless a parameter file is specified with the following line:
>
> `ResistOutput : On`
>
> Consult Zuken help for additional parameters that can be specified.

Exporting a Zuken Design to Ansys EDB

Zuken can export either a full boardor a specified region to an EDB file.

To export a Zuken board to EDB:

1. In Zuken CR-8000, select the **File** tab.
2. Click **Ansys** and use the drop-down menu to select **Export (EDB)**.

   An export dialog box appears.
3. Specify the following options:
   - **EDB Folder** – Click the ellipses button (**...**) to browse to the location where you want to save the file. Enter a name for it and click **Save**.
   - **Output resister layer** – Toggle on or off. Adds a solder resist layer to top and bottom.
   - **Output air layer** – Toggle on or off. Adds a layer of air to top and bottom.

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- **Output mesh plane by true shape** – Toggle on or off. Exports a mesh plane as an area filled with mesh.
- **Merge figures** – Merges area fills and lines and outputs the result as an area fill.
- **Output diode as passive component** – Toggle on or off. Exports diodes between signal and ground as capacitors, and diodes between signals as 0 Ohm resistors.
- **Reference header of branch component** – Any component with the specified reference header will export as a 0 Ohm resistor.
- **Attr. name for simulation library** – Substitutes component part names with the specified attribute.
- **Power is handled the same as ground** – Toggle on or off. When activated, selected nets are set as Power/Ground nets on export. When deactivated, selected nets are exported as signal nets.
- **Specify output signal** – Toggle on or off. When activated, you can specify nets for export.
- **Add ground net to output signal** – Toggle on or off. When activated, a ground net is automatically added.
- **Port to output** – Opens a window that allows you to assign ports to terminals.
- **Output layer** – When **Add ground net to output signal** is activated, use this field to specify the layer on which to add the ground net.
- **Simulator options** – Allows you to specify some simulation options.

> **Important:**
>
> For best performance, do no specify options here. Specify them directly in SIwave or Electronics Desktop.

4. Click **Execute**.

   Zuken exports an EDB file to the specified location.

   A dialog box appears, noting that translation is complete.

Importing Component and RLC Part Values Files

This section deals with the component files that accompany a design imported from a 3rd party layout tool.

Equivalent Model for RLC Circuit Elements

Import Component File

Import RLC Part Values File

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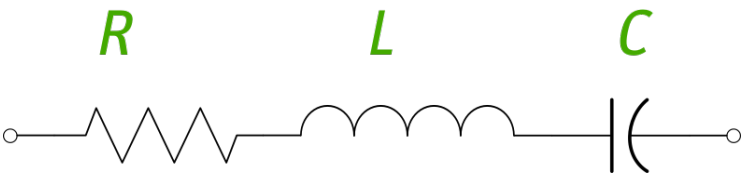
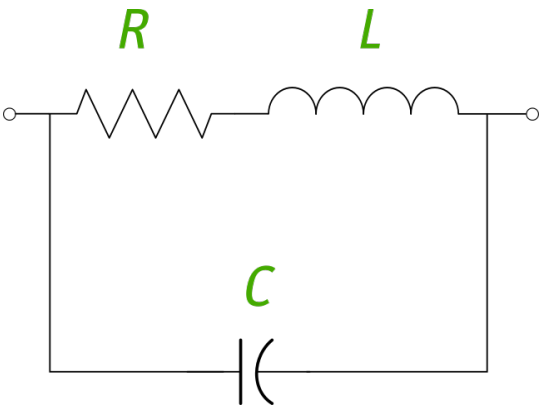
Equivalent Model for RLC Circuit Elements

For a non-ideal capacitor, the circuit model is series (R, L, C), as in the following figure.



For a non-ideal inductor or resistor, the circuit model is parallel (C, series (R, L)), as in the following figure.



Importing Component Files

SIwave allows you to import component files generated by third-party layout tools. You do not have to re-draw components while transferring the design.

To import an existing component file into SIwave:

1. Click **Import** > **Component File**.

   The **Open** window appears.

2. Select the file that you want to import.

   You can select a particular Component File (.**cmp**). This file contains detailed pin information for discrete devices, input/output devices and integrated circuits and is generated during design data transfer from 3rd-party layout tools into SIwave.

3. Click **Open**.

   This reads the selected file into the current window.

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Importing RLC Part Values Files

An RLC Part Values File allows you to correctly classify and assign values (both nominal and parasitic) to capacitors, inductors and resistors during design import from third-party layout tools (e.g., Mentor Expedition).

To import an existing RLC Part Values file into SIwave:

1. Click **Import** > **RLC Part Values**.

   The **Open** window appears.

2. Select the file that you want to import.
3. Click **Open**.

   This reads the selected file into the current window.

Below is a sample part mapping file:

```
* part mapping file

* Syntax for specifying part RLC values:

* <part name> Cap <capacitance>

* <part name> Ind <inductance>

* <part name> Res <resistance>

* <part name> NonIdealCap <capacitance> <ESL> <ESR>

* <part name> NonIdealInd <parasitic C> <inductance> <parasitic
resistance>

* <part name> NonIdealRes <parasitic C> <parasitic L> <resistance>


DNI_CAP_1003 Cap 0.33u (1,0)

DNI_CAP_1005 NonIdealCap 0.1u 0.1n 0.2 (1,0)

DNI_IND_1005 NonIdealInd 20p 10n 0.1 (1,0)

ELCH0001054 NonIdealInd 20p 10n 0.1 (1,0)

ELCH0001056 NonIdealInd 20p 10n 0.1 (1,0)

ELCH0001057 NonIdealInd 20p 10n 0.1 (1,0)

ELCH0001406 NonIdealInd 20p 10n 0.1 (1,0)

ELCH0001408 NonIdealInd 20p 10n 0.1 (1,0)
```


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```
ELCH0001421 NonIdealInd 20p 10n 0.1 (1,0)
```

Comment lines start with an asterisk (*). The first field on each line specifies the part number to which the values are to be applied. The second field is one of the following:

```
Cap

Ind

Res

NonIdealCap

NonIdealInd

NonIdealRes
```

If parasitic values are not required, nominal values for capacitors, inductors and resistors can be specified using the "Cap," "Ind," and "Res" strings followed by the actual value. If parasitic value assignment is needed, three numbers need to follow the "NonIdeal*" keyword (however the order of these numbers is: capacitance is always first, inductance always second, and resistance always third).

The final fields on each line specify the pin order. For two terminal devices, the pin order will simply be (1,0). For more complex multi-terminal devices though, the pin order should indicate how the device can be decomposed into equivalent two-terminal elements (e.g., a three-terminal capacitor can have a pin order resembling "(1,0) (2,0)". This tells SIwave to create two equivalent capacitors-one connecting pin 1 and pin 0, the other connecting pin 2 and pin 0. The nominal value of each of these two capacitors will be half of the original capacitors value (and the parasitic ESL/ESR will be double).).

Exporting Component and RLC Part Values Files

This section deals with exporting the component files that accompany a design imported from a 3rd party layout tool.

Saving Component File

Saving RLC Part Values File

Saving Component Files

You can save (export) component files generated by third-party layout tools.

To export an existing component file from SIwave:

1. Click **Export** > **Component File**.

   The **Save As** window appears.

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2. Enter the name and location where you want to save the file. The Component File (.**cmp**) extension is automatically added to the file.
3. Click **Save**.

Saving RLC Part Values Files

You can save (export) RLC Part Values Files generated by third-party layout tools.

To export an existing RLC Part Values File from SIwave:

1. Click **Export** > **RLC Part Values**.

   The **Save As** window appears.

2. Enter the name and location where you want to save the file. The RLC Part Values (.**dat**) extension is automatically added to the file.
3. Click **Save**.

Importing Huray Roughness Models

To import an existing Huray roughness model into SIwave:

1. Click **Import**.
2. From the **Other Imports** area, click **Huray Roughness Models**.

   The **Select Huray Roughness Model to import** window appears.

3. Select the Huray Roughness Model file (*.hrm) you want to import.
4. Click **Open**.

   This reads the selected file into the current window.

Net Selection on Import

After selecting a project file for import, SIwave typically opens the **Select nets** window.

Use the **Select nets** window to select individual nets to import, or leave the default (all nets will be imported).

You can choose to create ports on selected nets.

You can select a port reference, if different from the default (GND). Click **OK** to continue with the import.

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4 - Layers and Materials

This section explains how to work with the layers and materials that represent the physical properties of the PCB model.

Layers

Materials

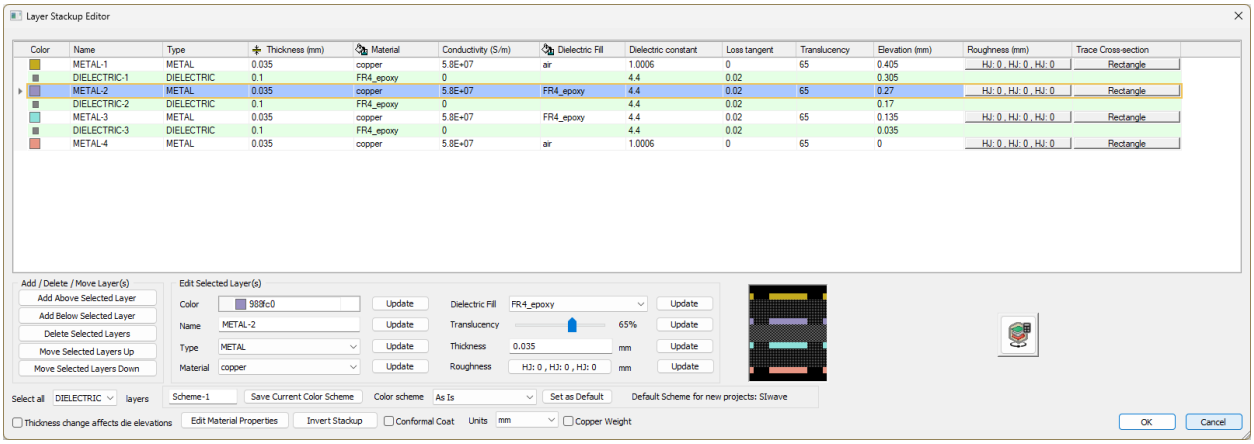
Layers

Before drawing or modifying geometry in the Modeling workspace, you must verify the layers and materials to be used for this design. You can do this within SIwave using the Layer Stackup Editor, which presents both a table view and 2D preview of the layers, or using the Layer Stackup Wizard, which presents the layers as a 3D model and can perform trace and impedance calculations.

Using the Layer Stackup Editor

The **Layer Stackup Editor** window allows you to define the characteristics of each layer. Complete these steps to modify layer properties.

1. Click **Home** > **Layer Stackup Editor** to open the **Layer Stackup Editor** window.



2. From this window, perform the following actions:

   - Add a or delete layers
   - Edit layer properties
   - Click **3D View** or the Layer Stackup Wizard button ( ) to launch the Layer Stackup Wizard.

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- Click any button in the Trace Cross-section column to open the **Trace Cross Section Shape Editor** window. The option is available for any **METAL** layer. Refer to Modifying the Cross Section Traces.

Using the Layer Stackup Wizard

The **Layer Stackup Wizard** is a powerful utility that allows users to build and modify laminate layer stacks to meet precise impedance requirements for single-ended and differential microstrips and striplines. SIwave's fast and accurate Method of Moments transmission line solver is used in all calculations and fully accounts for frequency-dependent dielectrics, non-uniform (e.g., trapezoidal) trace cross-sections, and surface roughness parameters. In Analysis mode, users can assess the impact of changing material parameters, layer thicknesses, etc., on the impedance of single-ended and differential lines whose width and separation are fixed. In Synthesis mode, users can compute trace width required to achieve a specified impedance value on a given layer. For differential nets, users can compute either trace width or trace separation to achieve a given impedance and trace separation (or width) values. Computed trace widths can then be applied to SIwave's layout editor. Traces that are subsequently routed on layers with updated width values will have the exact impedance value specified in the Stackup Wizard.

A key component of this utility is the interactive, 3D visualization of the layer stack. This view, which can be panned, zoomed, and rotated using the mouse, provides an intuitive understanding of the dimensions and composition of the layer stack.

Complete these steps to use the Layer Stackup Wizard.

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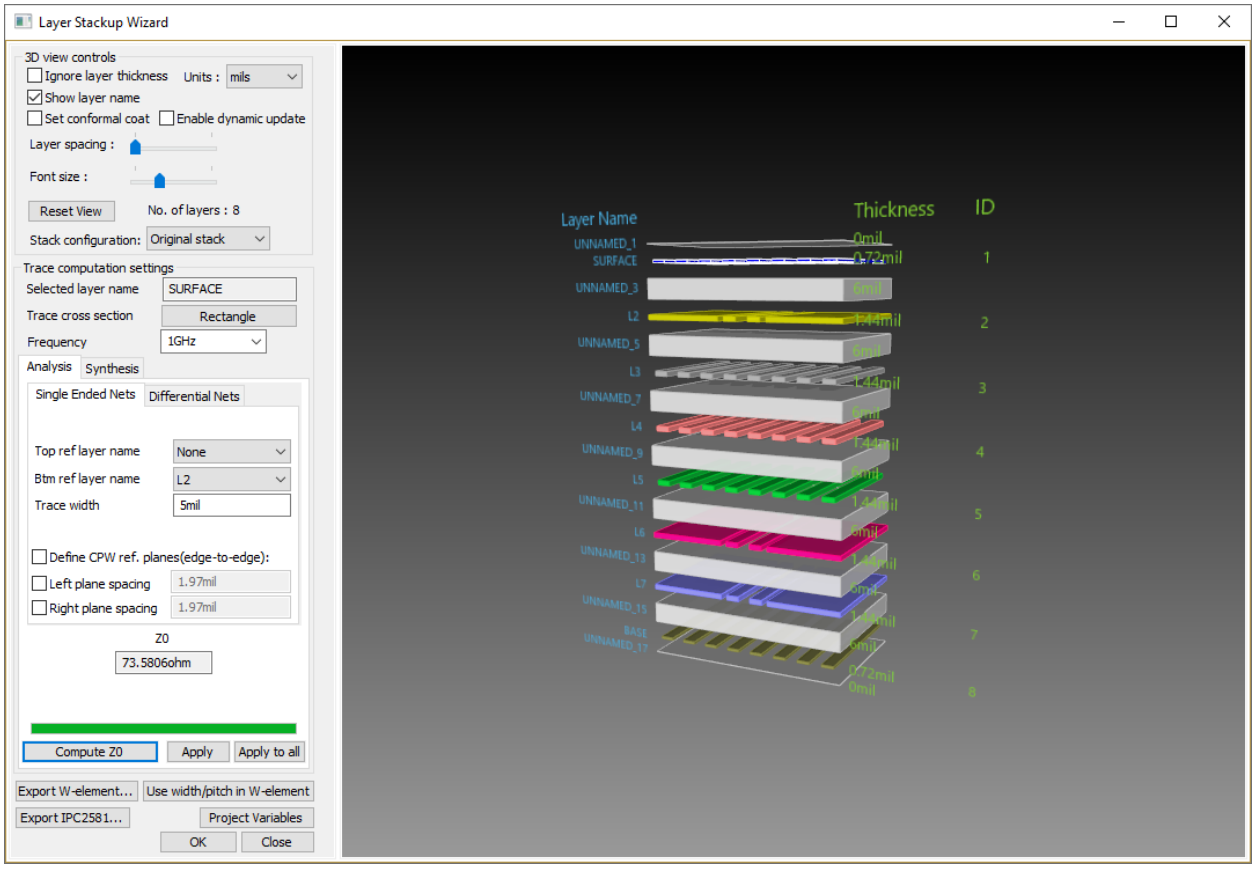
1. Click **Home** > **Layer Stackup Wizard**. to open the **Layer Stackup Wizard** window.



The window contains two panes:

- **Control Pane** – located on the left, this pane allows you to configure the layer stack, and to calculate impedance, differential impedance, and trace width/pitch.
- **View Pane** – located on the right, this pane displays the current layer stack. The pane automatically updates as you change settings in the Control Pane, and you can add, remove, or edit certain layer properties directly from this pane. Use the mouse or hot keys to rotate and zoom the model. Use Ctrl+D to auto-zoom.

To configure the layer stackup from the Control Pane:

1. From the **3D View Controls** area, select your appropriate options:
   - **Ignore layer thickness** – checking this renders all layers at the same thickness. If this option is unchecked, layers display at their actual thicknesses.
   - **Show layer name** – checking this displays layer names. If this option is unchecked, layer material names display instead.
   - **Set conformal coat** – select this check box to add conformal coat layers. These layers are a set of dielectric layers on the top and bottom of all packages and PCBs in the

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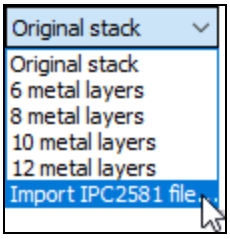
design. They have a default material of "SolderMask" and a default thickness of 15 microns. They are shown with a Layer Type of "CONFORMAL_COAT".

> **Note:**
>
> If dielectric layers are already present above the top layer and below the bottom layer, their material is changed to SolderMask and the layer type is changed to Conformal Coat.

- **Units** – use this drop-down menu to update the units displayed in the View Pane, as well as in the impedance calculator.
- **Enable Dynamic Update** – when enabled, dynamic update performs the following actions when any change is made in the Layer Stackup window:
  - The design updates.
  - Impedance and differential impedance are recalculated.
  - W-element plots are recalculated and replotted.
- **Layer spacing** – use the slider to increase or decrease the space between layers.
- **Font size** – use the slider to increase or decrease the size of the font in the View Pane.
- **Stack Configuration** – use the drop-down menu to select Original Stack, or select a specific number of metal layers for display. You can also import an IPC2581 file.



- **Selected Layer Name** – displays the name of the currently selected layer. Select layers from the View Pane.
- **Trace Cross Section** – displays the shape of the current trace cross section, if any. Clicking this opens the **Trace Cross Section Shape Editor**. See: Modifying the Cross Section of Traces.
- **Frequency** – drop-down menu that allows you to select a frequency.
- **Reset View** – click to reset the View Pane to its default view.
- **Export IPC2581 File** – prompts you to select an *.xml or *.cvg file for export.
- **Export W-Element** – allows you to export the w-element.
- **Use width/pitch in W-element** – uses the calculated trace width or pitch in the w-element analysis.

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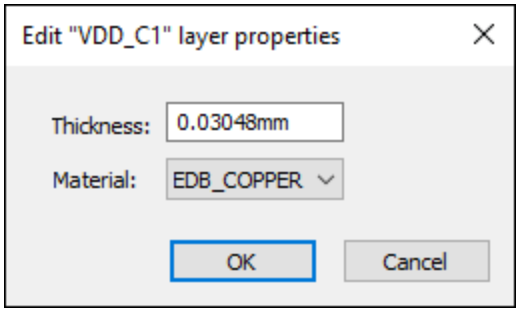
- **Project Variables** – opens a window that allows you to define project variables for w-element export.

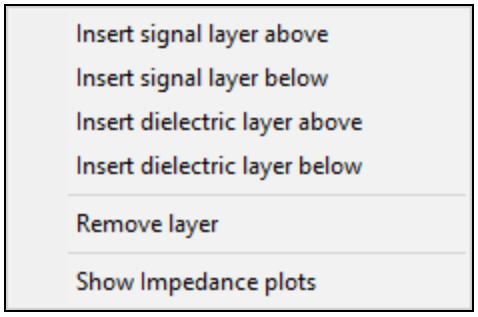
To configure the layer stackup from the View Pane:

- Double-click any layer to open its **Layer Properties** window.



From here, you can change the layer's **Thickness** and **Material**.

- Right-click a layer in the View Pane to view additional options:



You can insert signal or dielectric layers, or remove the selected layer.

You can also right-click any layer and click **Show Impedance Plots** to open the plots in a new window:

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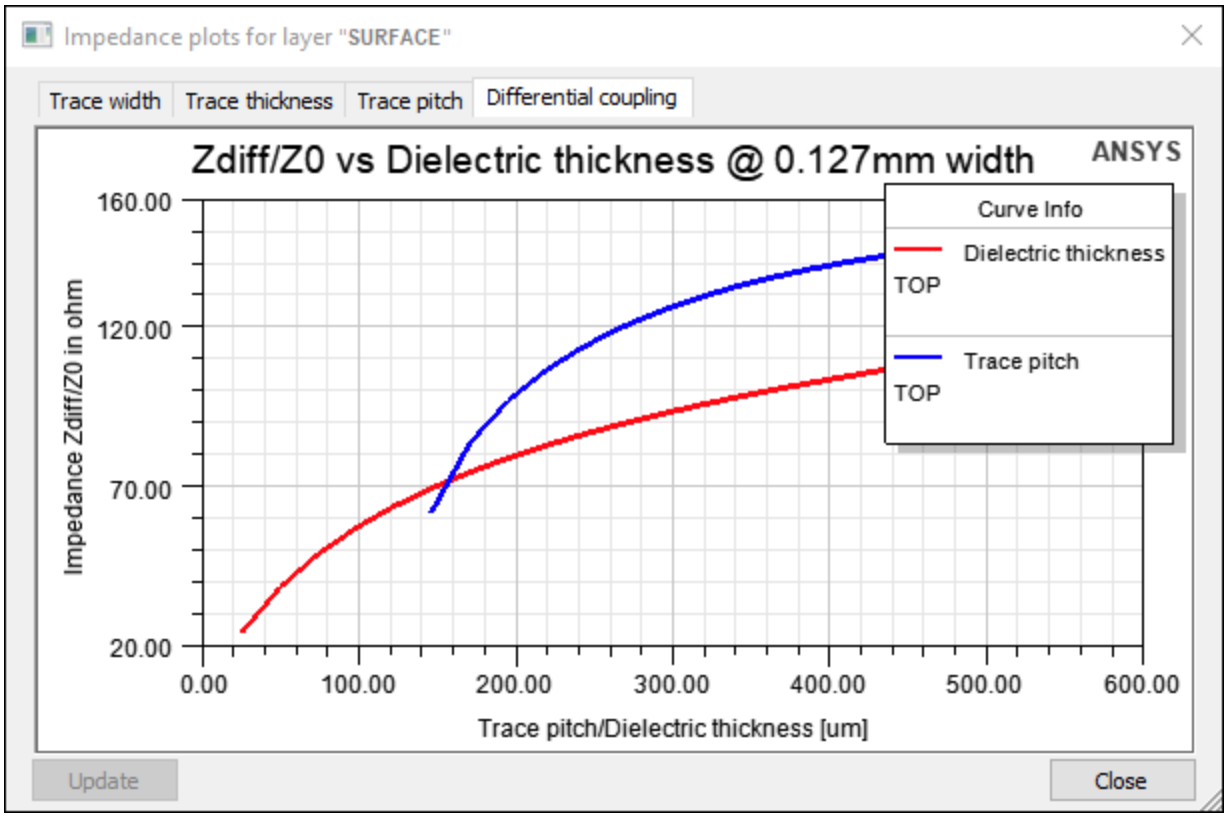

This plot is modeless. Make any change in the Layer Stackup Wizard to enable the **Update** button. For more information about plots in SIwave, see Changing Plot Display Options and Additional Plotting Actions.

From the Layer Stackup Wizard, you can also:

- Calculate trace width and pitch
- Calculate impedance (Z0)
- Calculate differential impedance (Zdiff)
- Export W-element
- Compute insertion/return loss and time domain crosstalk

Adding and Deleting Layers

The position of new layers is relative to the current layer.

Use either Layer Stackup Editor or Layer Stackup Wizard to add new layers above or below the current layer, or to remove existing layers.

In Layer Stackup Editor

To add a new layer above the current layer, click **Add Above Selected Layer**.

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To add a new layer below the current layer, click **Add Below Selected Layer**.

To delete a layer, select it and click **Delete Selected Layer**. You will be asked to confirm the deletion.

To edit a layer's properties, select Edit Layer Properties.

In Layer Stackup Wizard

To add a layer, right-click an existing layer and select one of the following options:

- Insert Signal Layer Above
- Insert Signal Layer Below
- Insert Dielectric Layer Above
- Insert Dielectric Layer Below

To delete a layer, right click it and select **Remove layer**.

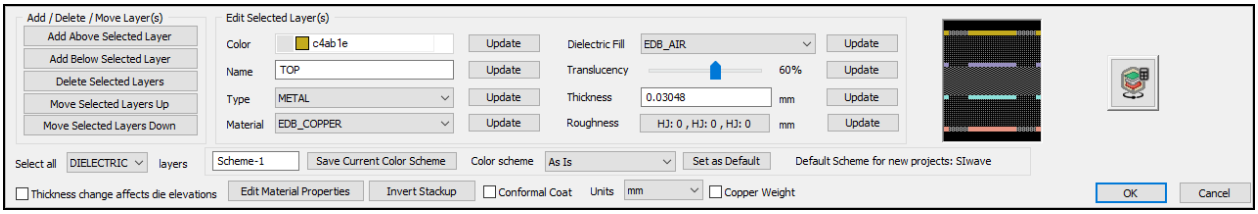
To modify a layer's properties, double-click it.

Editing Layer Properties

Layer properties can be adjusted using Layer Stackup Editor or Layer Stackup Wizard.

Layer Stackup Editor

Layer Stackup Editor is SIwave's tool for making bulk updates to layers. The bottom pane contains the editing controls.



The **Edit Selected Layer(s)** area allows you to select one or multiple layers and edit any of the following:

- **Color**
- **Name**
- **Type** (dielectric, metal, or wirebond)
- **Material** (any existing material; see: Adding a New Material)
- **Dielectric Fill**
- **Translucency**

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- **Thickness** (when thickness is changed, the stackup's elevation is recomputed)
- **Roughness** (metal layers only)

To change any of these layer properties:

1. Select the layer(s).

   > **Note:**
   >
   > To select all layers of a particular type, click the **Select All** drop-down menu and select Dielectric, Metal, or Wirebond.

2. Change a property and click the **Update** button to its right to apply the changes.
3. If appropriate, click the **Edit Material Properties** button to open the **Material Properties** window where you can add, delete or modify materials.
4. If appropriate, click the **Invert Stackup** button to invert the complete set of layers in the stackup.
5. If appropriate, enable the **Conformal Coat** check box to add conformal coat layers. These layers are a set of dielectric layers on the top and bottom of all packages and PCBs in the design. They have a default material of "SolderMask" and a default thickness of 15 microns. They are shown with a Layer Type of "CONFORMAL_COAT".

   > **Note:**
   >
   > If dielectric layers are already present above the top layer and below the bottom layer, their material is changed to SolderMask and the layer type is changed to Conformal Coat.

6. Use the **Units** drop-down menu to select the units for the layer. The display panel in the bottom-right area shows the changes in the layer stackup as they are being made.
7. If needed, enable the **Copper Weight** check box to view the metal layer thicknesses as an equivalent copper weight. 1 oz of copper is used to fill a one foot square up to a height of 35 microns. So, 1 oz. is 0.035 mm, 2oz is 0.07 mm, 3 oz is 0.105 mm and so on.
8. When you're done making changes, click **OK**.

Layer Stackup Wizard

Layer Stackup Wizard is primarily used for trace calculations. However, you can use it to make limited property changes:

- **Thickness** (when thickness is changed, the stackup's elevation is recomputed)
- **Material** (any existing material; see: Adding a New Material)

To change these properties:

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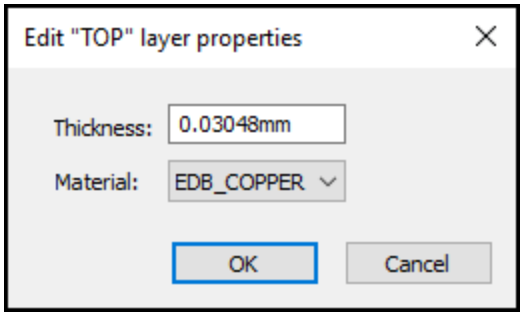
1. Double-click a layer in the stackup. to open the **Edit Layer Properties** window.



2. Change the properties as appropriate and click **OK**.

Editing Surface Roughness

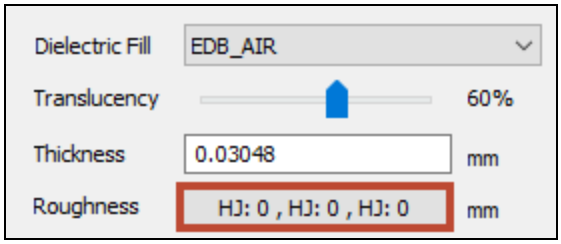
For metal layers, you can choose to specify the surface roughness on the top, bottom, and sides of each layer. For each area, SIwave can use either the Hammerstad-Jensen or the Huray roughness model.

> **Important:**
>
> Previous versions of SIwave supported only top and bottom roughness. When opening these legacy projects, side wall roughness is set to 0 by default.

In Layer Stackup Editor

To specify roughness:

1. Open the Layer Stackup Editor.
2. Click the values in the **Roughness** button to open the **Edit Layer Roughness** window.



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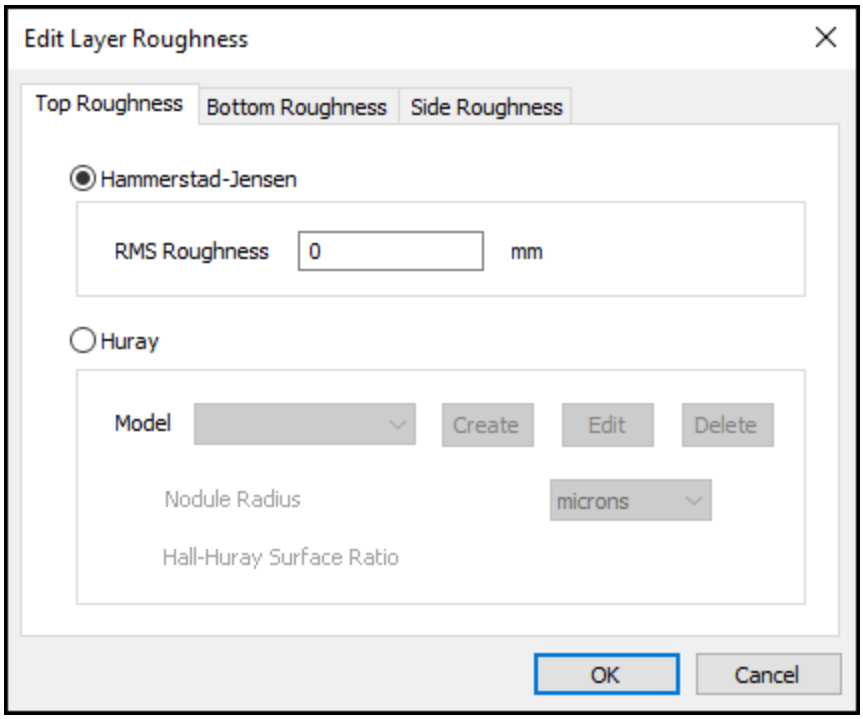

3. Use the **Top Roughness**, **Bottom Roughness**, and **Side Roughness** tabs to select the area whose roughness you want to edit.
4. You can specify the roughness using *either* the **Hammerstand-Jensen** *or* **Huray** model. Use the radio buttons to select one or the other.
   - For the **Hammerstad-Jensen** model, you must enter the **RMS Roughness** value and units. See: Technical Notes.
   - For the **Huray** model, you can either select a system-defined model or create your own.

     There are three system-defined Huray models: Low Loss, Medium Loss and High Loss; all three have r = 0.5 um, and sr values of 1, 3 and 6, respectively.

     To create a new model, click **Create**. The **Edit Huray Roughness Model** window appears. Enter the **Model Name**. Specify the **Nodule Radius** value. This describes the radius of copper spheres that model the surface roughness. Specify the **Hall-Huray Surface Ratio**, a unitless quantity. Click **OK** to return to the **Edit Layer Roughness** model.
5. To edit an existing model, click **Edit**. The **Edit Huray Roughness Model** window appears. Make any changes as needed. Click **OK**.
6. To delete an existing model, click **Delete**. A confirmation window appears. Select **Yes** if you want to delete this model.
7. Similarly, enter the new roughness for the bottom surface in the **Bottom Surface Roughness** tab.
8. Click **OK** to exit the **Edit Layer Roughness** window.

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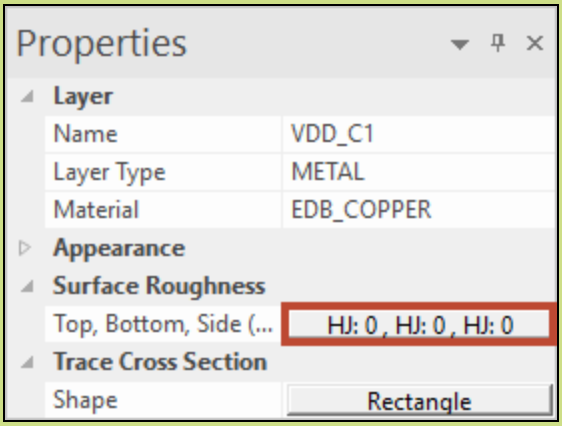
Note:

You can also access the **Edit Layer Roughness** window from the **Properties** workspace. To do this, select a layer in the **Layers** workspace and then click the values in the **Surface Roughness** button:



Importing and Exporting the Layer Stackup

PCB/package designs are often based on the same stackup. Stackup file import/export allows you to define the exact parameters (set materials, layer thicknesses, etc.) for a particular stackup once, and have these assignments be reapplied consistently across different designs. The Layer Stackup can be exported as either an SIwave Layer Stackup File (*.stk) or as an Extensible Markup Language (*.xml) file.

Importing the Layer Stackup

To import a Layer Stackup *.stk file into SIwave:

1. Click **Import** > **Layer Stackup**.
2. Select the file you want to open.
3. Click **Open**.

To import a Layer Stackup *.xml file into SIwave:

1. Click **Import** > **Layer Stackup XML**.
2. Select the file you want to open.
3. Click **Open**.

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> **Note:**
>
> Layer names and layer order in the active design must exactly match those of the stackup file being imported. If discrepancies are detected, no updates will be made.
>
> The only exception is that SIwave can load any layer stack into an *empty* design.

Exporting the Layer Stackup

To export a Layer Stackup *.stk from SIwave:

1. Click **Export** > **Layer Stackup**.

   The **Save As** window appears.

2. Select the directory and file name under which you want to save the file.
3. Click **Save**.

To export a Layer Stackup *.xml from SIwave:

1. Click **Export** > **Layer Stackup XML**.

   The **Save As** window appears.

2. Select the directory and file name under which you want to save the file.
3. Click **Save**.

Calculating Trace Width and Pitch

From the **Trace Computation Settings** area of the Layer Stackup Wizard, you can configure and perform a trace width (or pitch) calculation.

Prerequisites:

- Use the View Pane to select a layer. The **Selected Layer Name** field displays the currently selected layer.
- Use the **Trace Cross Section** button to open the Trace Cross Section editor.
- Use the **Frequency** drop-down menu to select the frequency used for trace width calculations.

To calculate trace width or pitch:

1. Select the **Synthesis** tab.
2. Select the **Single Ended Nets** or **Differential Nets** tab.
3. Use the drop-down menus to select the required impedance or differential impedance (in ohms), as well as reference layers.

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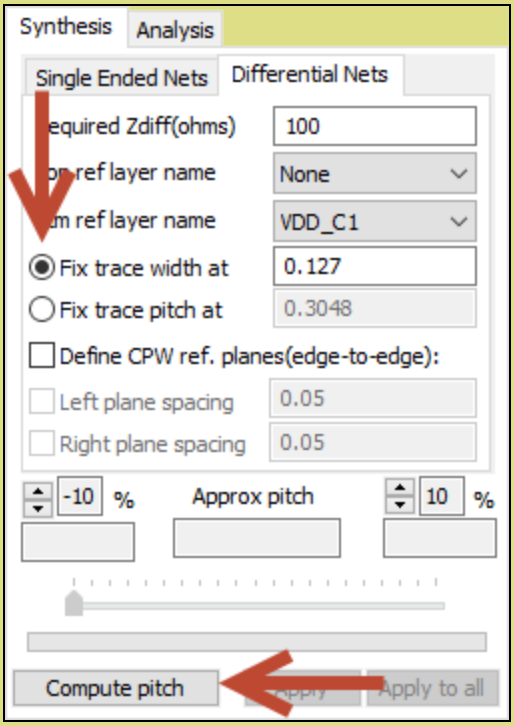
4. If you are using the **Differential Nets** tab, select *either* **Fix trace width at** or **Fix trace pitch at** and enter a value.

   Important:

   By default, **Fix Trace Pitch** is selected. Selecting **Fix Trace Width** changes the calculator so that it computes pitch instead of width.

5. If you wish to define coplane wave reference planes, select **Define CPW ref. planes (edge-to-edge)** to enable additional options.
   - You may select **Left plane spacing**, **Right plane spacing**, or both.
   - For W-element export, selecting **Left plane spacing** means that aggressors may only be added to the right of a victim trace; any traces to the left are removed. Selecting **Right plane spacing** means that aggressors may only be added to the left of a victim trace; any traces to the right are removed.
6. To perform the calculation, click **Compute width**.

   The green progress bar shows the calculation's progress.

   When the calculation is complete, the **Approx width** area updates to show the calculated result.

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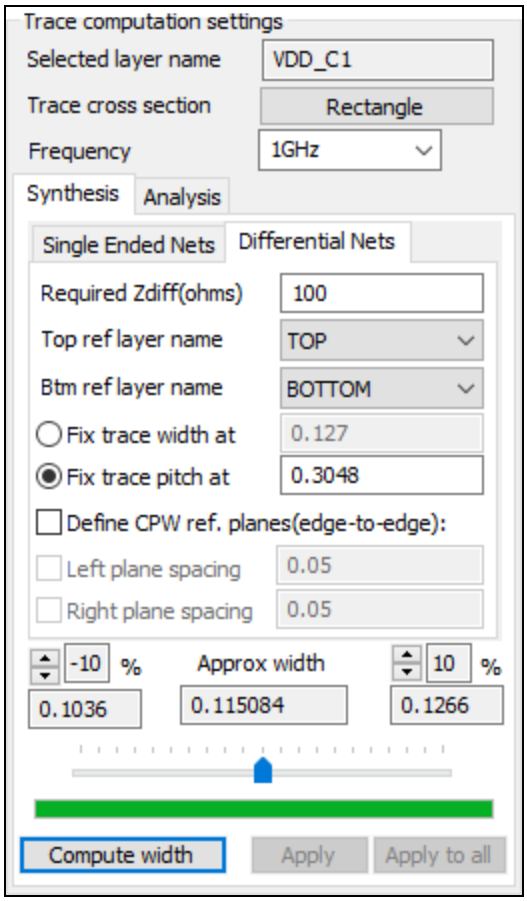

7. Use the slider above the progress bar to update trace width as well as the required Zdiff value.

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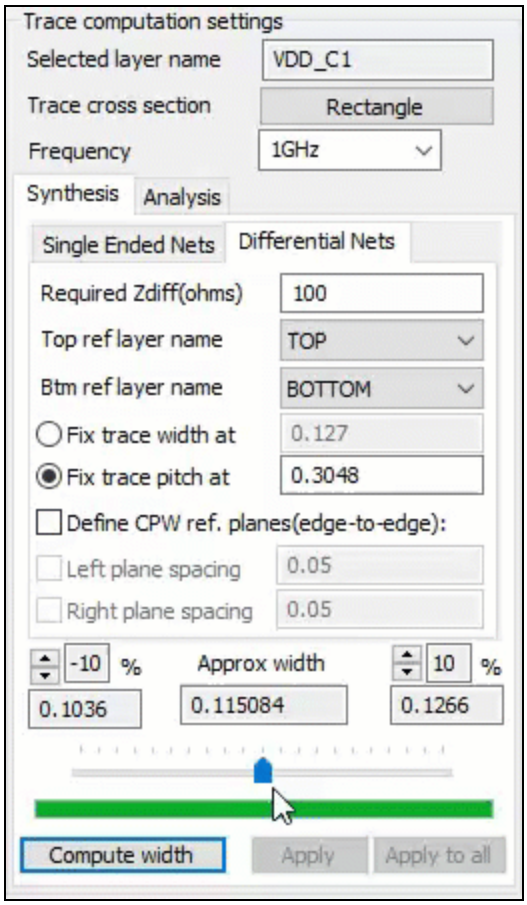

Calculating Impedance (Z0)

From the **Trace Computation Settings** area of the Layer Stackup Wizard, you can configure and perform an impedance calculation.

Prerequisites:

- Use the View Pane to select a layer. The **Selected Layer Name** field displays the currently selected layer.
- Use the **Trace Cross Section** button to open the Trace Cross Section editor.
- Use the **Frequency** drop-down menu to select the frequency.

To calculate impedance:

1. Select the **Analysis** tab.
2. Select the **Single Ended Nets** tab.

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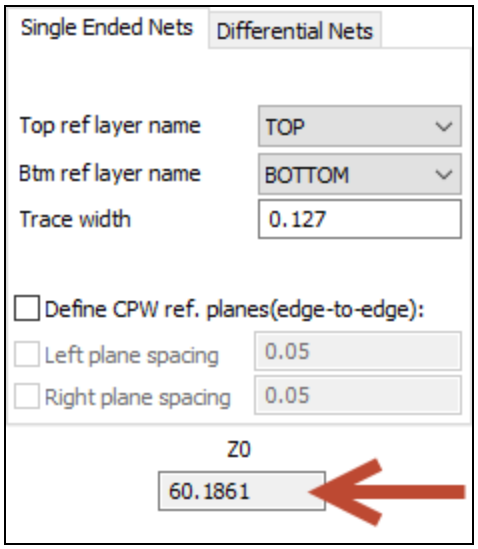
3. Select your reference layers.

> **Note:**
>
> Top and bottom reference layer must be selected in order to use multi-layer features of W-element export.

4. From the **Trace Width** field, enter a trace width.
5. If you wish to define coplanar waveguide reference planes, select **Define CPW ref. planes (edge-to-edge)** to enable additional options.
   - You may select **Left plane spacing**, **Right plane spacing**, or both.
   - For W-element export, selecting **Left plane spacing** means that aggressors may only be added to the right of a victim trace; any traces to the left are removed. Selecting **Right plane spacing** means that aggressors may only be added to the left of a victim trace; any traces to the right are removed.
6. Click **Compute Z0**.
7. The **Z0** field updates to show the result.



8. To apply this setting to one layer or all layers, click **Apply** or **Apply to all**.

Calculating Differential Impedance (Zdiff)

From the **Trace Computation Settings** area of the Layer Stackup Wizard, you can configure and perform a differential impedance calculation.

Prerequisites:

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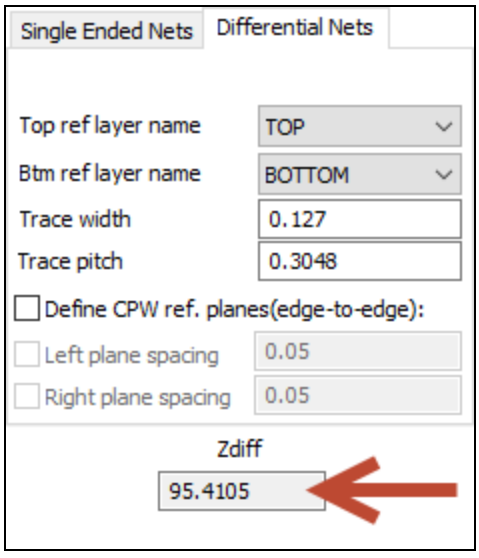
- Use the View Pane to select a layer. The **Selected Layer Name** field displays the currently selected layer.
- Use the **Trace Cross Section** button to open the Trace Cross Section editor.
- Use the **Frequency** drop-down menu to select the frequency.

To calculate differential impedance:

1. Select the **Analysis** tab.
2. Select the **Differential Nets** tab.
3. Select your reference layers.

> **Note:**
>
> Top and bottom reference layer must be selected in order to use multi-layer features of W-element export.

4. From the **Trace Width** and **Trace Pitch** fields, enter a trace width and pitch.
5. If you wish to define coplanar waveguide reference planes, select **Define CPW ref. planes (edge-to-edge)** to enable additional options.
   - You may select **Left plane spacing**, **Right plane spacing**, or both.
   - For W-element export, selecting **Left plane spacing** means that aggressors may only be added to the right of a victim trace; any traces to the left are removed. Selecting **Right plane spacing** means that aggressors may only be added to the left of a victim trace; any traces to the right are removed.
6. Click **Compute Zdiff**.
7. The **Zdiff** field updates to show the result.



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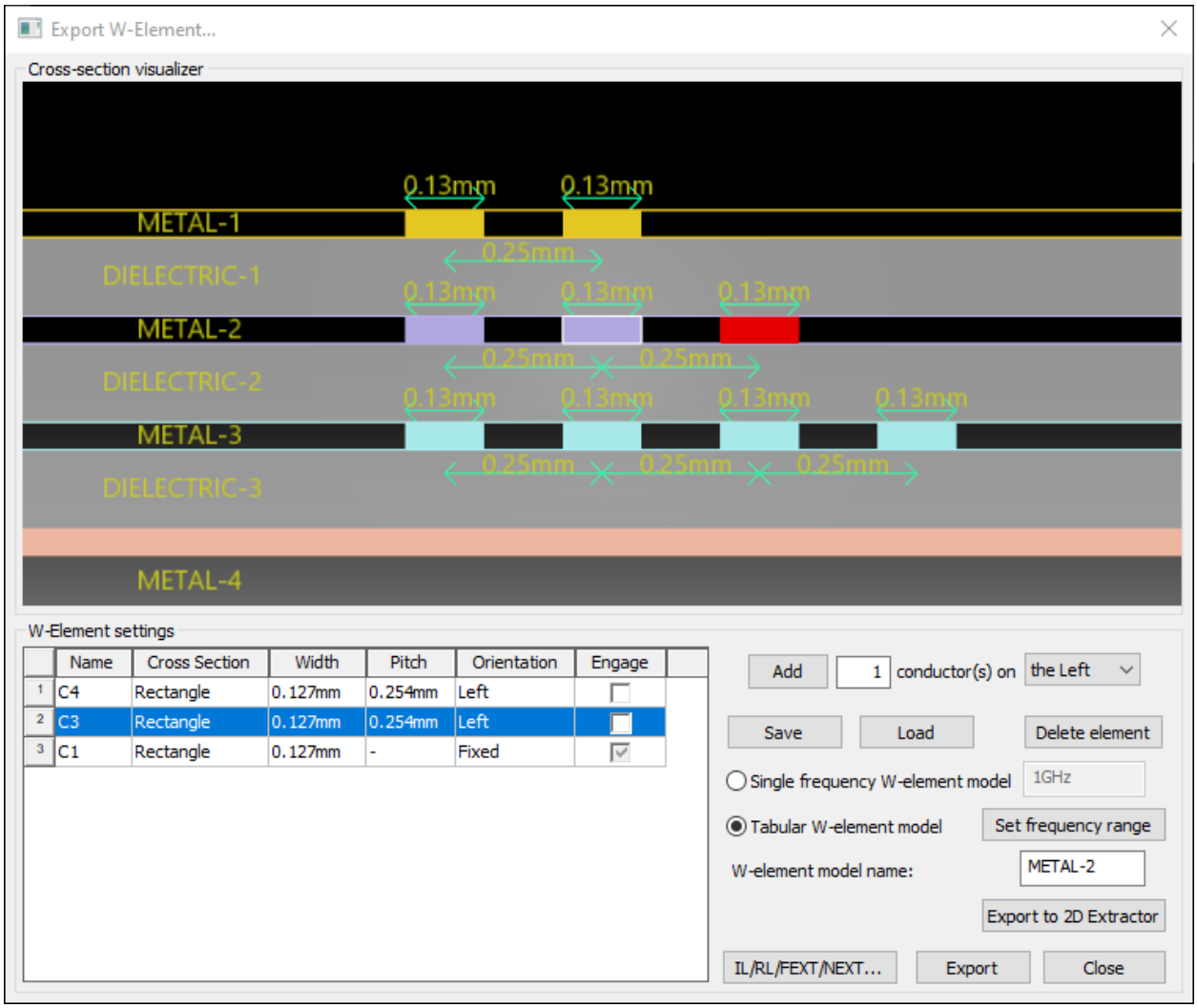
Exporting the W-element

After you have used the Layer Stackup Wizard to calculate impedance, differential impedance, or trace width/pitch, the **Export W-Element** window allows you to set up aggressor traces around a victim trace and export the corresponding w-element.

To configure a w-element export:

1. Access the **Export W-element** window one of two ways:
   - From the **Layer Stackup Wizard**, click **Export W-element**.
   - From the **Advanced** tab, click **W-element Analysis**.

   The **Export W-Element** window appears.



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The **Cross-section Visualizer** displays a graphical representation of the **W-Element Settings**, including dielectric blocks and the top and bottom reference layers.

2. Click a conductor in the visualizer or select it from the list in the **W-Element Settings** area.

   The grid displays the following for each conductor:

   - **Name** – conductor name.
   - **Cross Section** – indicates the shape of the cross section.
   - **Width** – can be edited here directly, or imported from the Layer Stackup Wizard by selecting **Use width/pitch in W-element**.
   - **Pitch** – can be edited here directly, or imported from the Layer Stackup Wizard by selecting **Use width/pitch in W-element**.
   - **Orientation** – fixed, left, or right.
   - **Engage** – enabling this check box engages the conductor in IL/RL/FEXT/NEXT simulations.

   The following options are available:

   - **Add** – Enter the number of aggressors to add, and use the drop-down menu to select whether to add them on the **right**, **left**, or on **both sides**. Then click **Add**.

     > **Note:**
     >
     > If you previously enabled CPW settings during trace width, impedance, or differential impedance calculation, your options will be limited.
     >
     > - If you selected **Left plane spacing**, aggressors may only be added to the right of a victim trace.
     > - If you selected **Right plane spacing**, aggressors may only be added to the left of a victim trace.

   - **Delete Element** – Click to remove an element.
   - **Single Frequency / Tabular Model** – Select **Single frequency** and enter the frequency in Hz, or select **Tabular** and click **Set frequency range** to set up a range of frequencies.
   - **W-Element Model Name** – If appropriate, enter a new model name for the w-element.
   - **Export to 2D Extractor** – generates a VB script to export the selected layer's cross-section to 2D Extractor. Generating this script launches a prompt asking if you want to run the script in Electronics Desktop.

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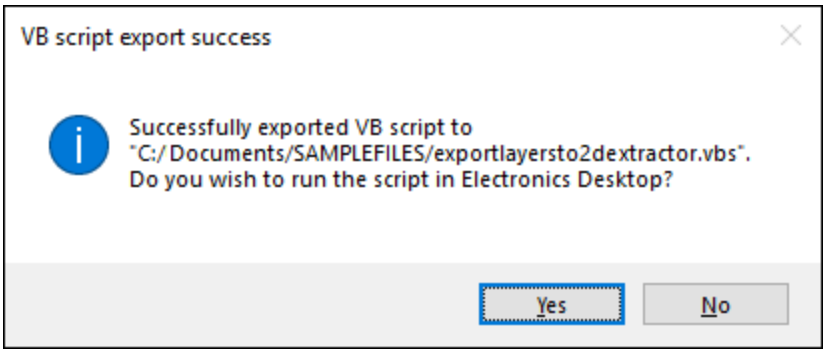

The layer thickness, conductor width, pitch, etching, conformal coat thickness are all defined using design variables.

Consult the Q3D Extractor/2D Extractor help for instructions on running an analysis in 2D Extractor.

3. Click **IL/RL/FEXT/NEXT** to compute insertion/return loss and time domain crosstalk.
4. Make your appropriate selections, then click **Export**.

   The **Select Spice File to Export** window appears.

> **Note:**
>
> If you selected **Tabular W-element model** but did not specify the frequency range, the **Frequency Sweep Dialog** appears. You must specify the frequency range before you can save.

5. Browse to a save location, name your file, and click **Save**.

   The file is saved in Spice (*.sp) format.

Computing Insertion/Return Loss and Time Domain Crosstalk

From the **Export W-Element** window, you can compute and plot insertion loss (IL), return loss (RL), far-end time domain crosstalk (FEXT), or near-end time domain crosstalk (NEXT).

Prerequisites:

- Use the Layer Stackup Wizard to calculate trace width/pitch, impedance, or differential impedance.
- Export W-element.

To calculate and plot IL/RL/FEXT/NEXT:

1. From the **Export W-Element** window, click **IL/RL/FEXT/NEXT**.

   The **Frequency Sweep Dialog** appears.

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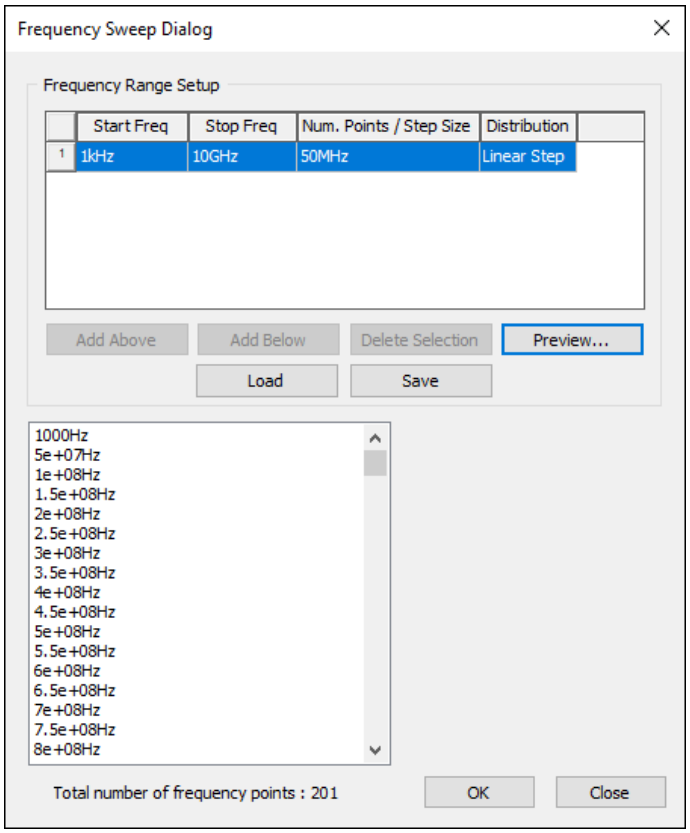

2. Add, remove, and edit frequencies as appropriate. Click **Preview** to preview the number of frequency points.
3. Click **OK**.

   The **IL/RL and Time Domain Crosstalk Plot** window appears, on the **IL/RL** tab. Select the **FEXT/NEXT** tab to view the crosstalk plot instead.

   While the plot computes, a green progress bar displays the progress.

   When it is finished, your selected plot appears.

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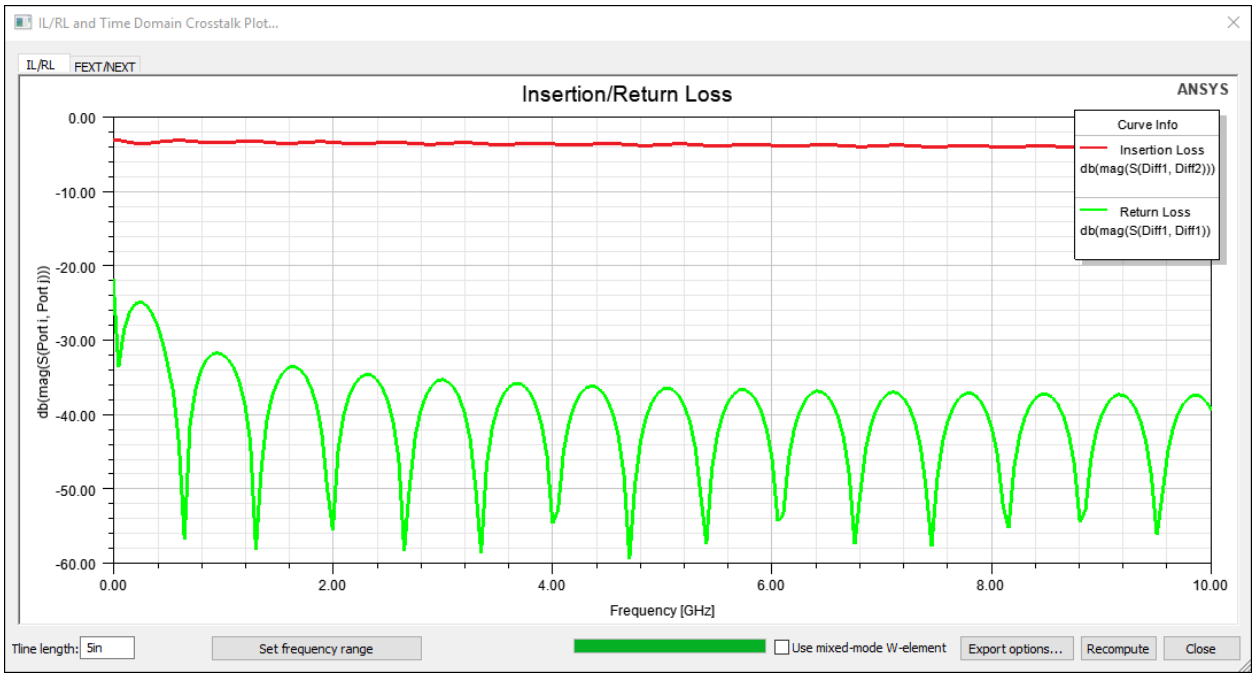

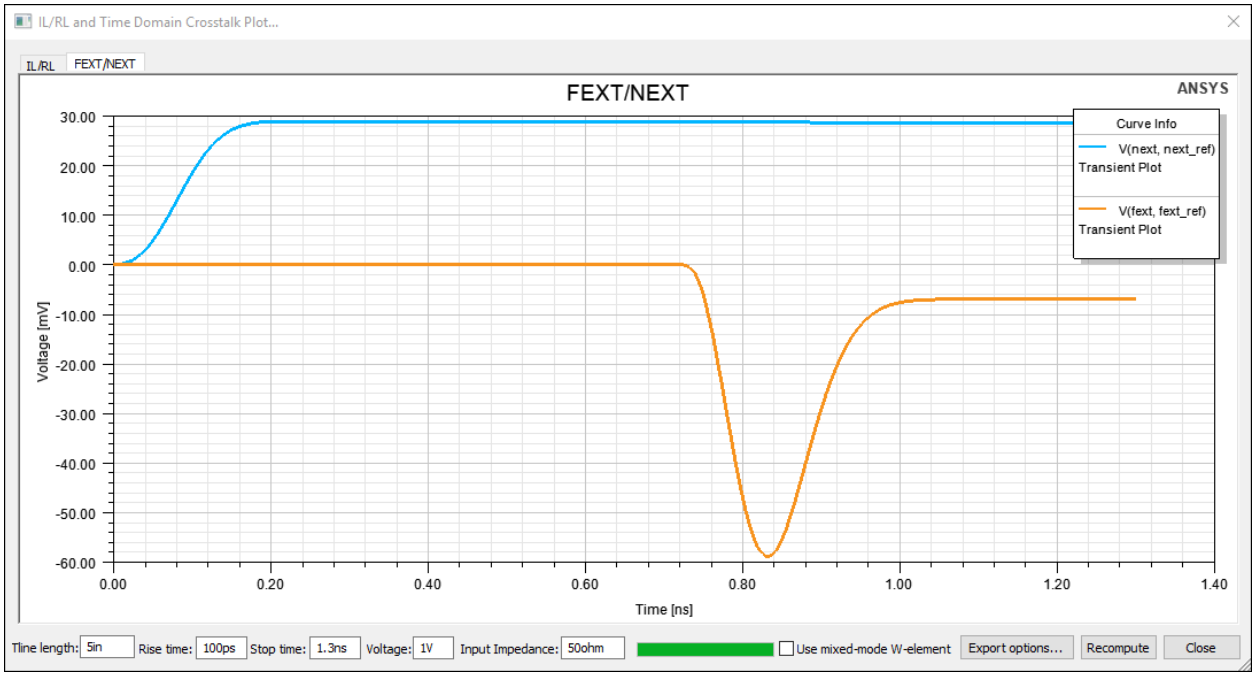

For IL/RL plots, you can adjust the **Length** or click **Set frequency range** to change the frequency range of the plot.

For FEXT/NEXT plots, you can adjust the **Tline length** (trace length); edit the **Rise time**, **Stop time**, and peak **Voltage** of the driver attached to the aggressor net; or modify the

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driver **Input Impedance** value. This impedance is also used to terminate all transmission lines in the specified cross-section.

If you wish to export plot data, click **Export Options**:

- For IL/RL plots, you can choose **Export w-element schematic to circuit** (in *.aedt format) or **Export touchstone file**.
- For FEXT/NEXT plots, you can choose **Export w-element schematic to circuit** (in *.aedt format) or **Export .csv file**.

If you change values and need to regenerate the plot, click **Recompute**.

Right-clicking within the plot enables additional plotting actions.

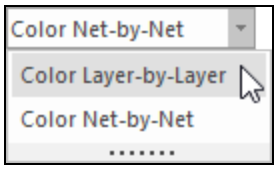
4. Click **Close** to exit the plot window.

Viewing Color by Layers

By default, SIwave displays color on a layer-by-layer basis. You can change this to a net-by-net view.

To return to viewing color by layers:

1. Click **View**.
2. From the **View Options** area, use the **Color Net-by-Net** drop-down menu to change the display mode.



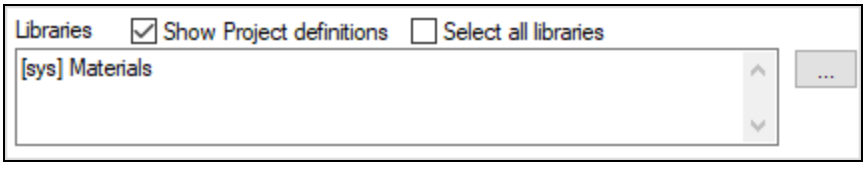
Materials

A material specifies the physical properties of a conducting or dielectric layer of the stackup.

Material Libraries

To view materials in the current project, navigate to the **Home** tab and click **Edit Materials**.

The **Select Definition** window appears, with a section for **Libraries**:



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By default, all materials in the project library display. To display materials from a different library, click the ellipsis (**...**) button and select a library.

Depending on your licensing, available libraries may include:

- ArnoldMagnetics
- Benchmark
- ChinaSteel
- Diamet
- GRANTA Materials Data
- GRANTA Producers Materials Data
- HitachiMetals
- JFE_Steel
- NipponPillar
- NSSMC
- RMxprt
- SCHOTT
- ShinEtsu
- TDK
- Vacuumschmelze

To display all materials in all available libraries, click **Select All Libraries**.

The materials list updates based on your selection:

Name	Location	Origin	Type	Relative Permittivity	Relative Permeability	C
air	SysLibrary	Materials	Dielectric	1.0006	1.0000004	0
Al2_O3_ceramic	SysLibrary	Materials	Dielectric	9.8	1	0
Al_N	SysLibrary	Materials	Dielectric	8.8	1	0
Alnico5	SysLibrary	Materials	Perfect conductor	1	B-H Curve...	2128000
Alnico9	SysLibrary	Materials	Perfect conductor	1	B-H Curve...	2000000
alumina_92pct	SysLibrary	Materials	Dielectric	9.2	1	0
alumina_96pct	SysLibrary	Materials	Dielectric	9.4	1	0
aluminum	SysLibrary	Materials	Perfect conductor	1	1.000021	3800000
aluminum_EC	SysLibrary	Materials	Perfect conductor	1	1.000021	3600000
aluminum_no2_EC	SysLibrary	Materials	Perfect conductor	1	1.000021	3300000
Arlon 25FR (tm)	SysLibrary	Materials	Dielectric	3.58	1	0
Arlon 25N (tm)	SysLibrary	Materials	Dielectric	3.38	1	0
Arlon AD1000 (tm)	SysLibrary	Materials	Dielectric	10.2	1	0

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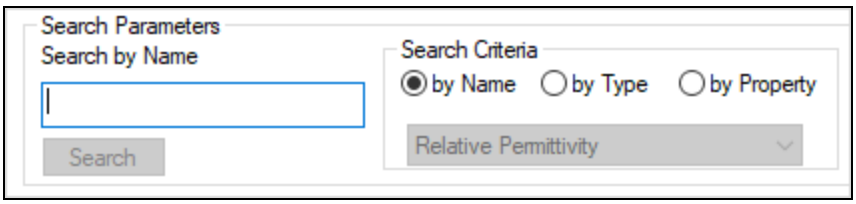
Note:

The **Origin** column shows the library in which the material resides. This is useful when viewing materials from multiple libraries.

Searching and Filtering Materials

To search for a specific material, use the **Search Parameters** field to search by material name, by material type, or by a selected material property. Simply enter a search value, select the **Search Criteria**, and click **Search**.



To filter the materials list, click the **Material Filters** tab. Changes made on this tab immediately appear on the **Materials** tab.

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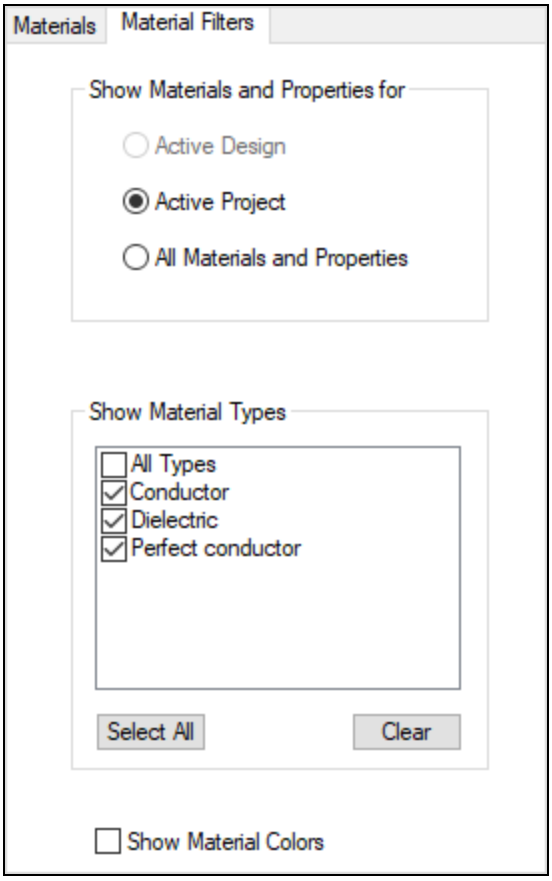

From here, select whether you want to view materials for the **Active Project** or **All Materials and Properties**.

From the **Show Material Types** box, select the types of materials you want to populate the materials list.

If appropriate, select **Show Material Colors** to add a column displaying material colors to the materials list.

From the **Select Definition** window, you can also:

- Add New Materials
- Edit Material Properties
- Edit Frequency-dependent Material Properties
- Assign Thermal and Spatial Modifiers
- Delete Materials

Adding a New Material

You can add a new material to the SIwave Materials Library.

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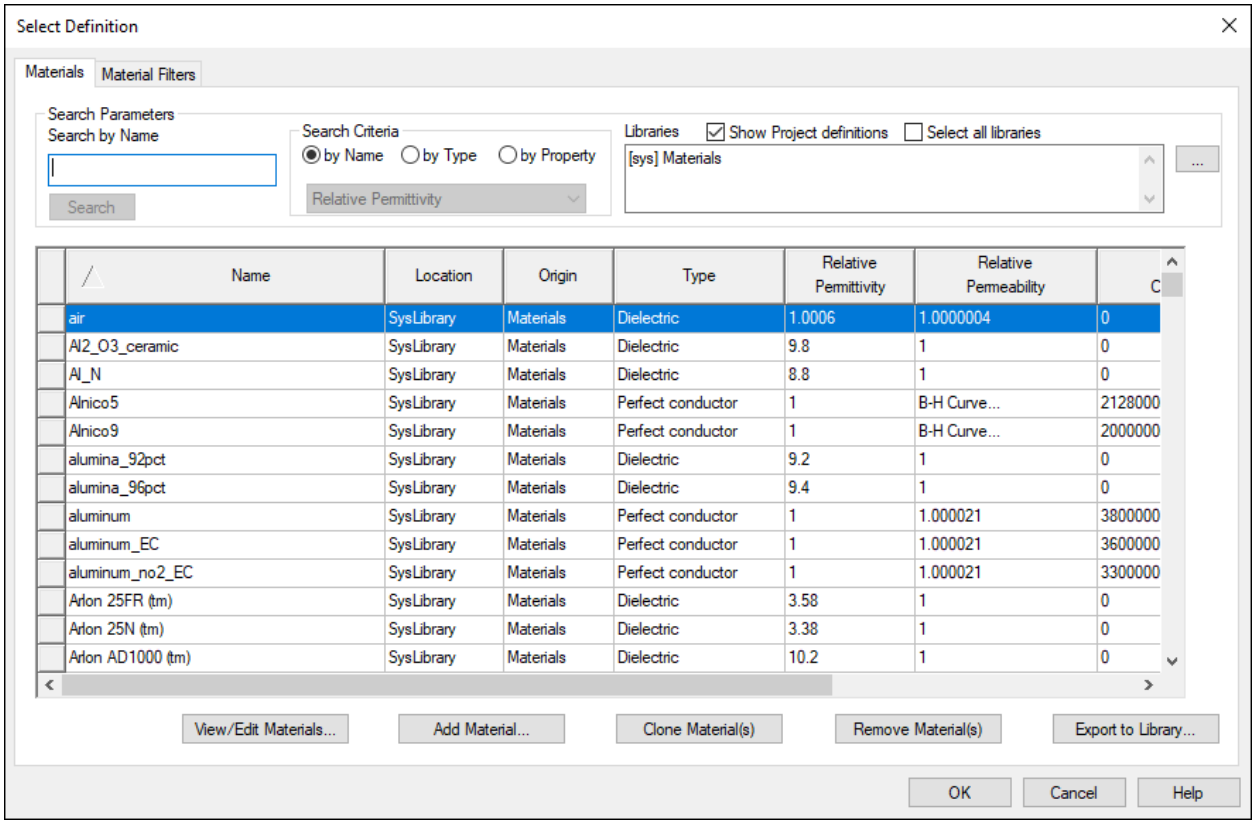
To do so:

1. From the **Home** tab, click **Edit Materials**.

   The **Select Definition** window appears.



2. Click **Add Material**.

   The **View/Edit Material** window appears.

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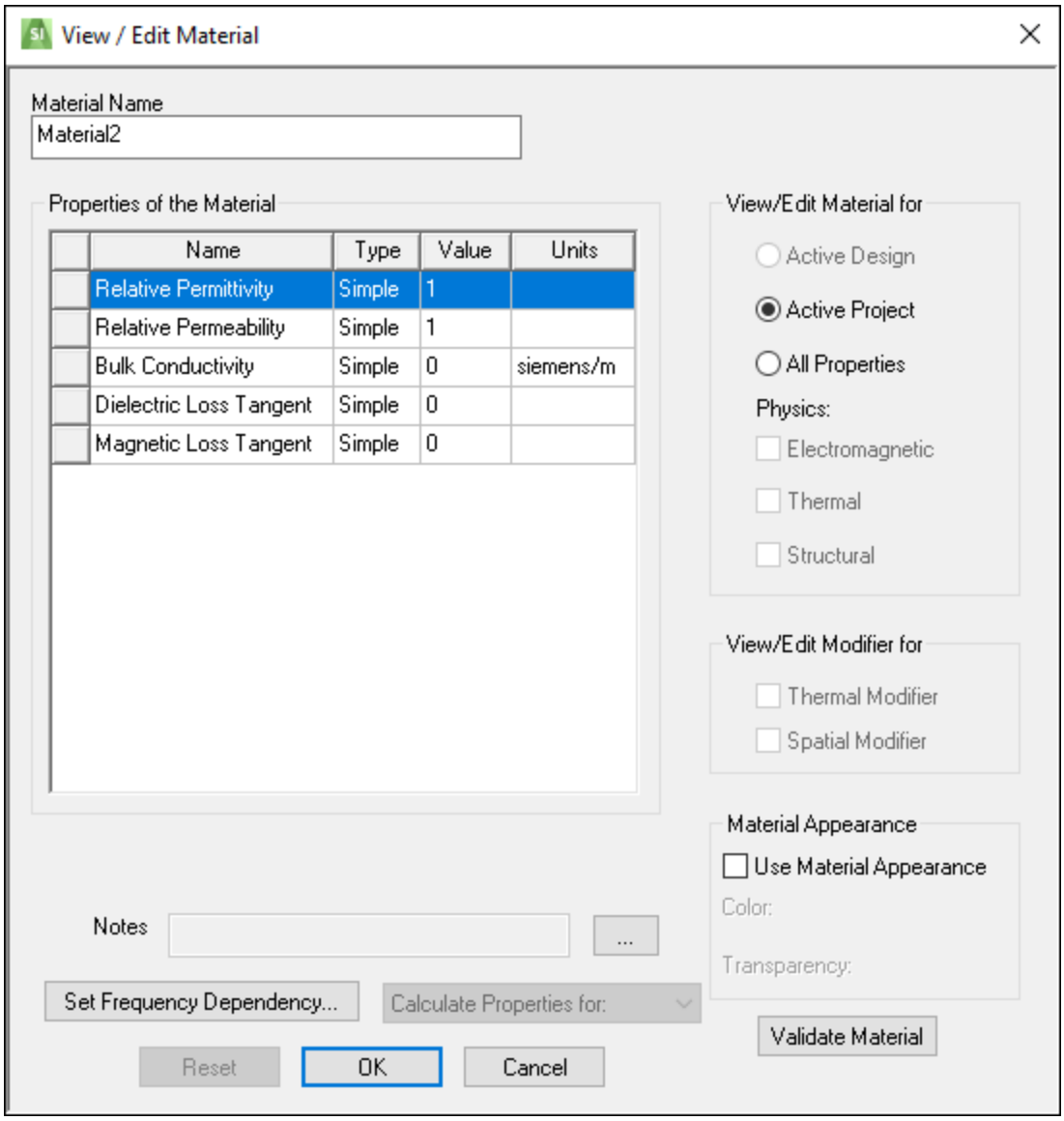

3. Enter a **Material Name**.
4. Under **View/Edit Material for**, select either **Active Project** or **All Properties**. See: Material Properties.
5. From the **Properties of the Material** area, enter values as applicable. See: Material Properties.
6. If appropriate, select **Use Material Appearance** to specify a material color and transparency.
7. Click **Validate Material**. If the material contains valid parameters, a green check mark appears. If the material is invalid, a red X appears.
8. If appropriate, click **Set Frequency Dependency** for frequency-dependent material options. See: Technical Notes.

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> **Note:**
>
> SIwave only supports Djordjevic-Sarkar frequency-dependent dielectric models.

9. If appropriate, use the **Calculate Properties for** drop-down menu to calculate properties for a permanent magnet or permanent electric polarization.
10. Click **OK**.

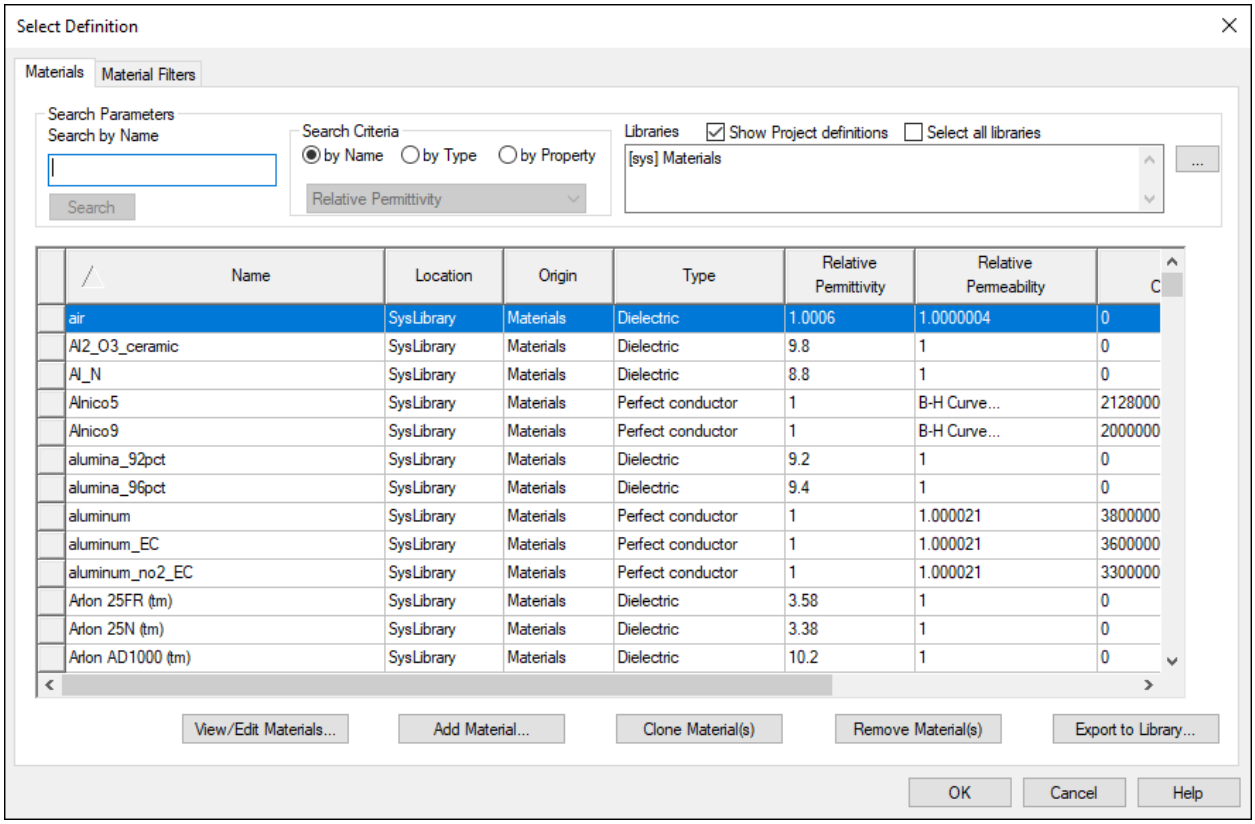
Editing an Existing Material

You can modify any material.

To modify material properties:

1. Click **Home**.
2. From the **Edit Tools** area, click **Edit Materials**.

   The **Select Definition** window appears.



3. Under **Libraries**, click the ellipsis (**...**) button to select the library in which the material resides.

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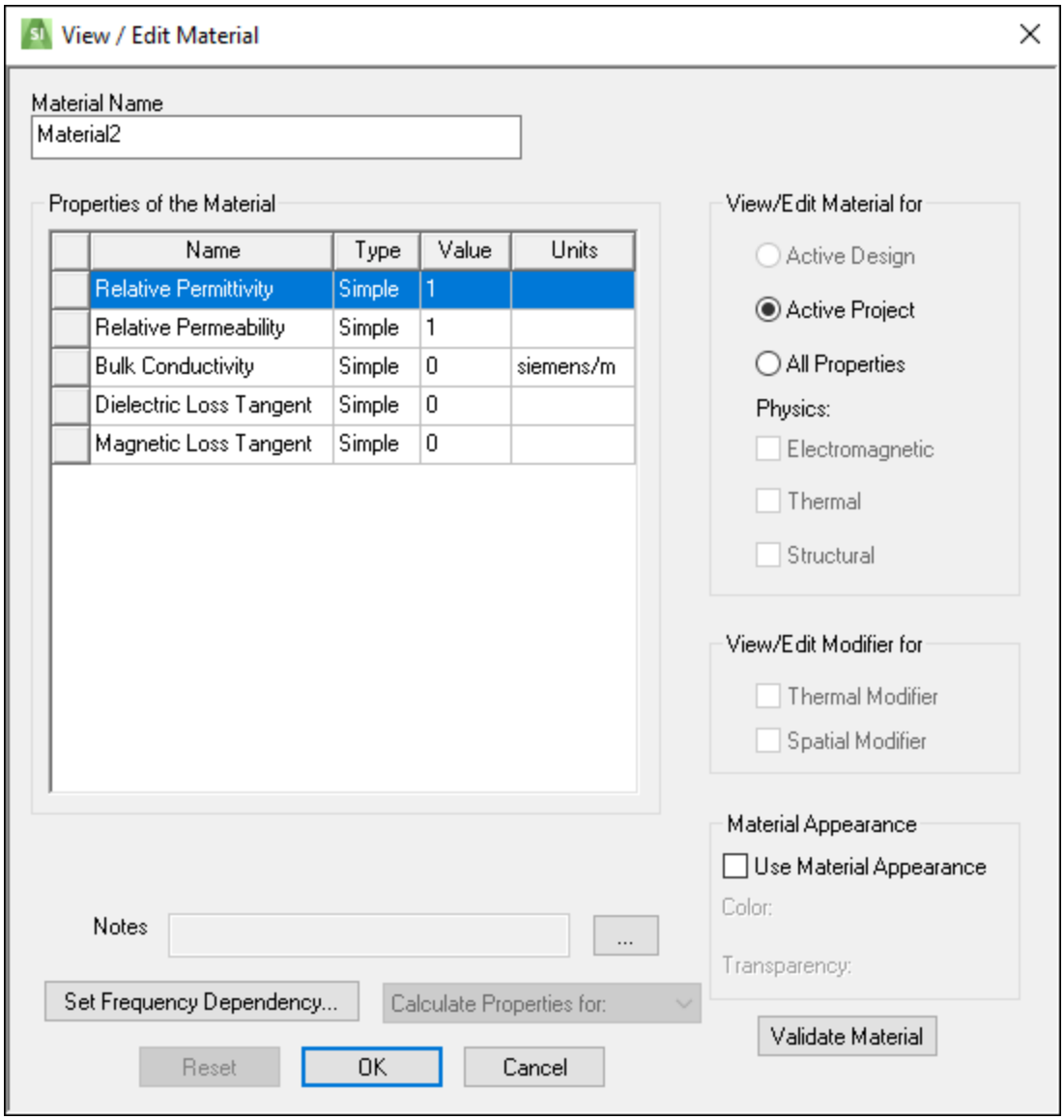
The materials list updates.

4. From the materials list, select the material you want to modify and click **View/Edit Materials**.

   The **View/Edit Material** window appears.



5. If appropriate, enter a new **Material Name**.
6. Under **View/Edit Material for**, select either **Active Project** or **All Properties**. See: Material Properties.
7. From the **Properties of the Material** area, enter values as applicable. See: Material Properties.

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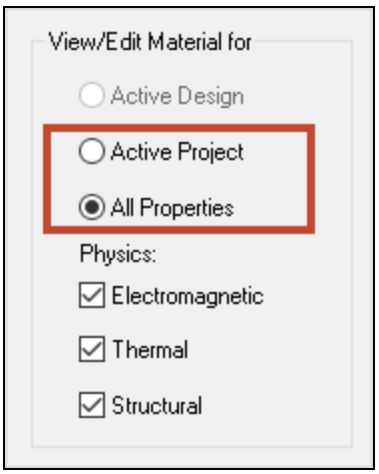
8. If appropriate, select **Use Material Appearance** to specify a material color and transparency.
9. Click **Validate Material**. If the material contains valid parameters, a green check mark appears. If the material is invalid, a red X appears.
10. If appropriate, click **Set Frequency Dependency** for frequency-dependent material options. See: Technical Notes.
11. If appropriate, use the **Calculate Properties for** drop-down menu to calculate properties for a permanent magnet or permanent electric polarization.
12. Click **OK**.

Material Properties

When adding a new material or editing an existing material, the material properties list contains several editable fields.

The editable properties depend on whether you have selected **Active Project** or **All Properties**:



Material Property Types

Each property contains a **Type** field. The type can be one of the following:

- **Simple** – The property takes a simple value.
- **Tensor** – A full 3x3 matrix general tensor, which may or may not be symmetrical.
- **Nonlinear** – The property varies according to a DE, JE, or BH curve.
- **Vector** – The property requires a magnitude and direction.
- **Custom** – Properties that do not fit into one of the these types.

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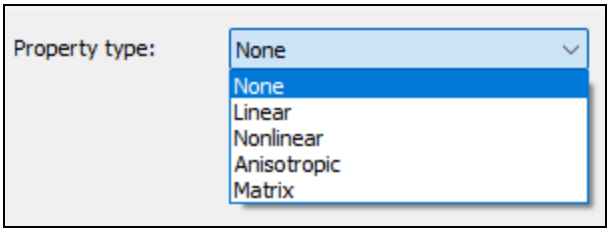
> **Important:**
>
> Anisotropic and Matrix material properties are not compatible with SIwave. The options will be removed in a future release.

Change a property's type by clicking it and using the drop-down menu:



Not all types are available for all properties.

Consult the following topics for more information:

- Defining Tensor Material Properties
- Defining Nonlinear Material Properties
- Defining Vector Material Properties
- Defining Custom Material Properties

Editing Active Project Properties

Most often, you will want to modify a material's properties for the **Active Project**:

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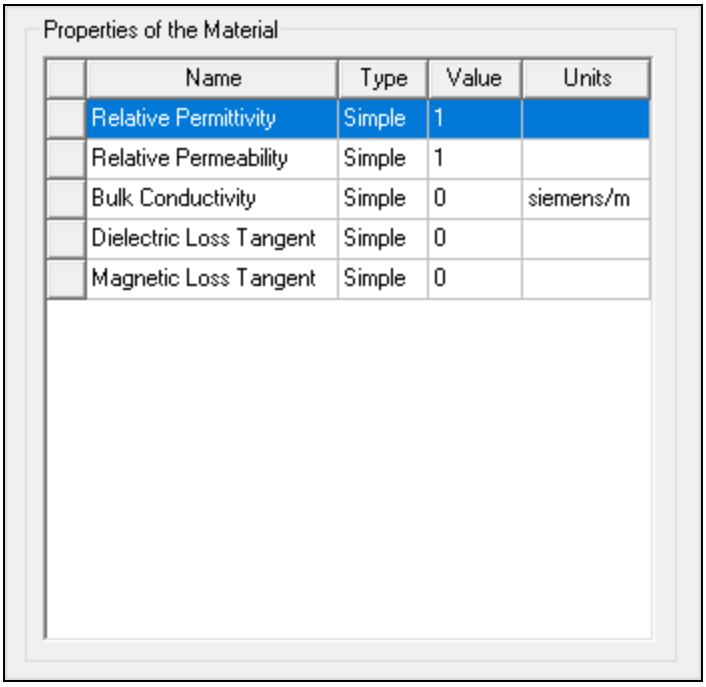

Materials in the **Active Project** have the following properties:

- Relative Permittivity
- Relative Permeability
- Bulk Conductivity
- Dielectric Loss Tangent
- Magnetic Loss Tangent

For conducting materials:

- Specify the bulk conductivity.

For dielectric materials:

- Specify the relative permittivity, relative permeability, and dielectric loss tangent (if applicable). See: Editing Frequency-dependent Material Properties.

Editing All Properties

Selecting **All Properties** allows you to modify the **Electromagnetic**, **Thermal**, and **Structural** physics for a material. Use the check boxes to select the type(s) of properties you would like to edit.

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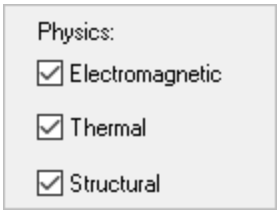

Editable **Electromagnetic** properties include:

- Electric Coercivity
- Magnetic Coercivity
- Magnetic Saturation
- Lande G Factor
- Delta H
- Core Loss Model
- Mass Density
- Composition
- Magnetostriction
- Inverse Magnetostriction

Editable **Thermal** properties include:

- Thermal Conductivity
- Mass Density
- Specific Heat
- Thermal Expansion Coefficient
- Thermal Material Type
- Solar Behavior

Editable **Structural** properties include:

- Mass Density
- Young's Modulus
- Poisson's Ratio
- Thermal Expansion Coefficient

In addition to editing these physics properties, you can view and edit thermal and spatial modifiers.

Editing Frequency-dependent Material Properties

SIwave can define frequency-dependent materials using the Djordjevic-Sarkar Model.

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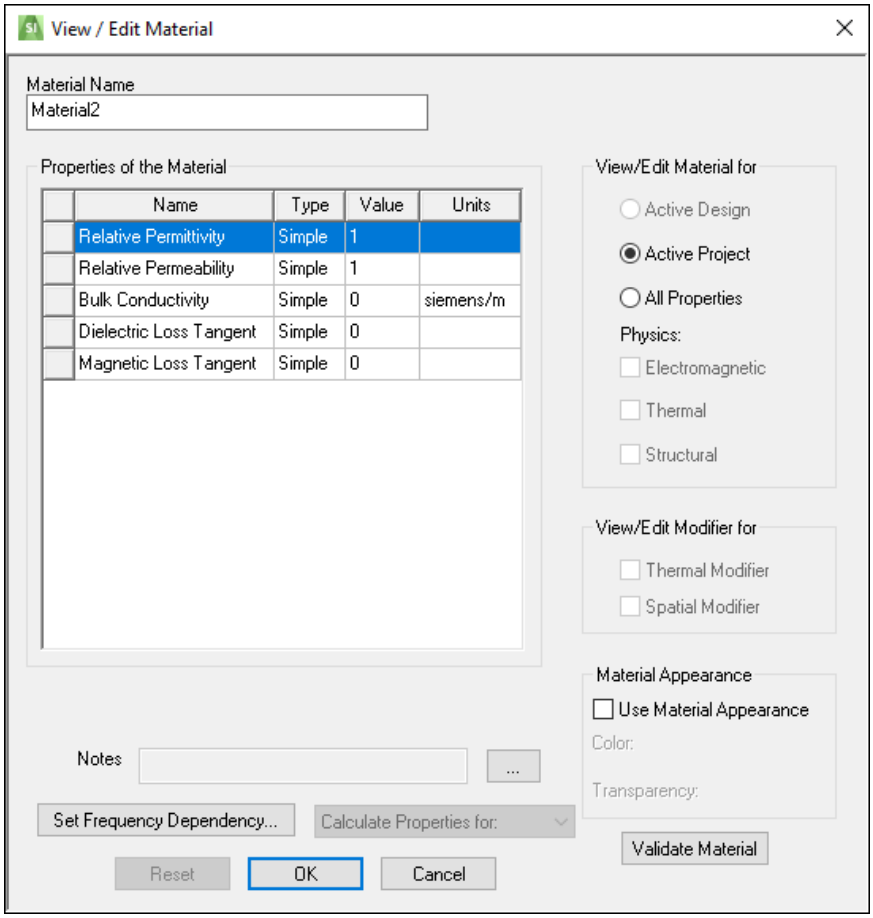
This model uses an infinite distribution of poles to model the frequency response, and in particular the nearly constant loss tangent, of low-loss dielectric materials. The model requires information about the relative permittivity and loss properties of the dielectric at two measurement frequencies: a low frequency and a high frequency. You can provide this information in different ways. The low frequency loss can be specified either as the loss tangent at the low measurement frequency, or by providing the DC conductivity of the dielectric material. The high frequency permittivity can be given either as the permittivity at the high measurement frequency, or the limiting value of the permittivity at optical frequencies. SIwave interpolates or extrapolates the effective permittivity and loss tangent values at other frequencies from this data.

To define a frequency-dependent material:

1. From the **Home** tab, click **Edit Materials**.
2. From the **Select Definition** window, add a material or edit an existing material.

   The **View/Edit Material** window appears.



3. Click **Set Frequency Dependency**.

   The **Djordjevic-Sarkar Model Input** window appears.

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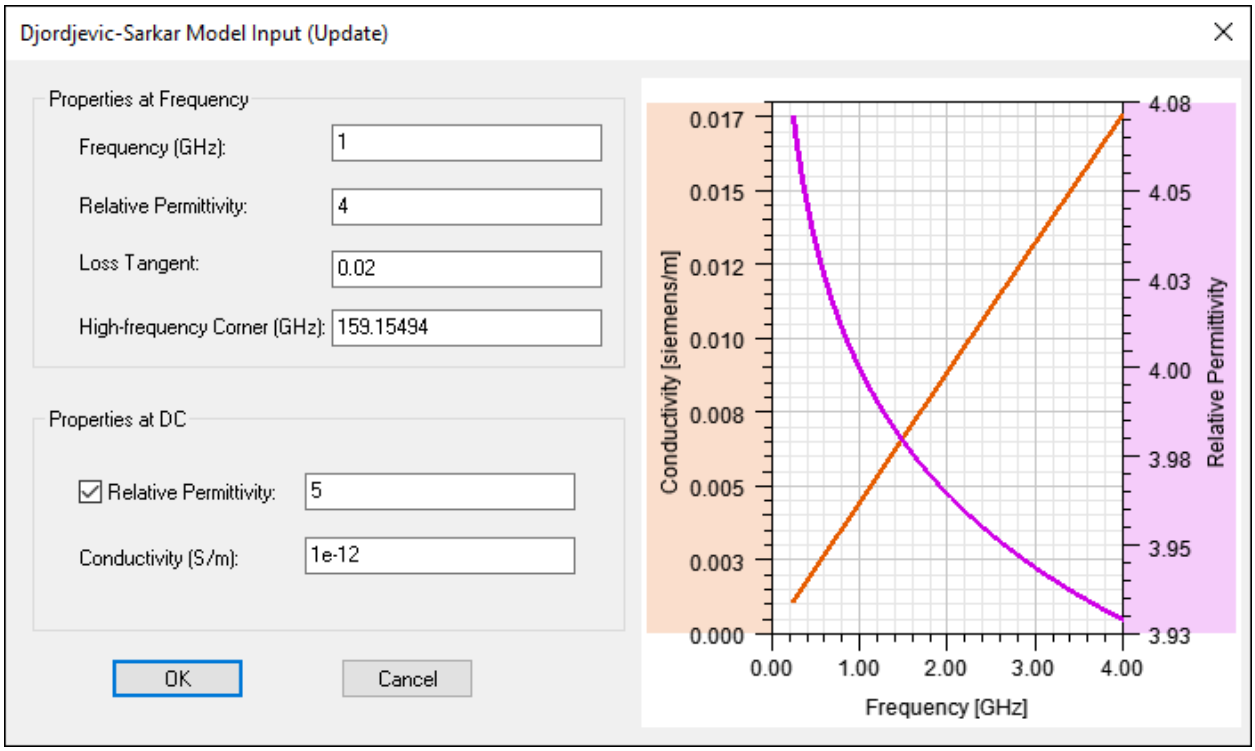

4. Set the options as appropriate:
   - From the **Properties at Frequency** area, enter the **Frequency**, **Relative Permittivity**, **Loss Tangent**, and **High Frequency Corner**.

     Note:

     Ansys recommends a Frequency of 1 MHz or higher and a Loss Tangent less than 0.1. The High Frequency Corner marks the transition frequency; above this frequency, the permittivity quickly approaches its high frequency (optical) limit. The value of the High-frequency Corner should be higher than the Measurement Frequency.

   - From the **Properties at DC** area, select whether or not to specify **Relative Permittivity**. Enter a value for **Conductivity**.
   - The graph on the right previews your input.
5. Click **OK**.

   The **View/Edit Material** window updates with the frequency-dependent information:

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	Name	Type	Value
	Relative...	Sim...	3.74076+0.0255671*ln((2.53303e+...
	Relative...	Sim...	1
	Bulk Co...	Sim...	1e-12+2.84472e-12*Freq*(atan(Fre...
	Dielectri...	Sim...	0
	Magneti...	Sim...	0

6. Click **OK** to save your changes.
7. Click **OK** again to exit the **Select Definition** window.

Assigning Thermal and Spatial Modifiers

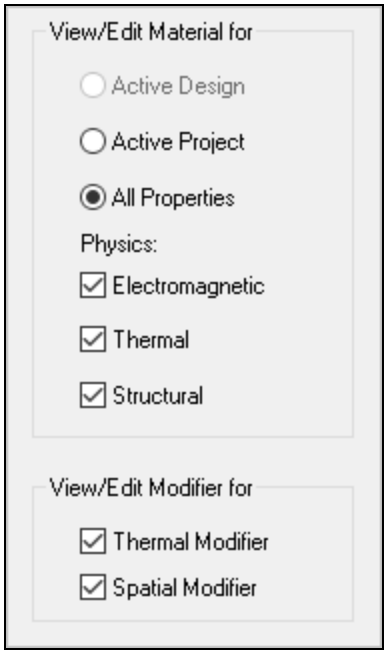
SIwave supports thermal and spatial modifiers for new or existing materials.

Thermal modifiers allow you to assign material properties that change with temperature.

Spatial modifiers allow you to define spatially dependent materials whose properties change over their length, width, or thickness.

To add a thermal or spatial modifier to a property from the **View/Edit Material** window:

1. Select **All Properties**.
2. Select one or more types of physics to modify.
3. Enable **Thermal Modifier** and/or **Spatial Modifier**.



The material properties list updates with a new column for each selected modifier.

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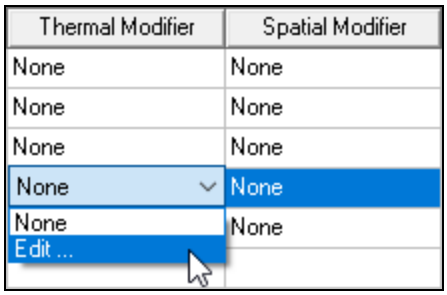

4. To add a modifier, select a cell's drop-down menu and click **Edit**.
   The **Edit Thermal Modifier** or **Edit Spatial Modifier** window appears.
5. Enter the modifier information as described below, and click **OK**.
6. Click **OK** again to exit the **View/Edit Material** window.

Thermal Modifiers

There are three ways to define a thermal modifier.

Select **Expression** to define an equation for the thermal modifier in the **Modifier** field.

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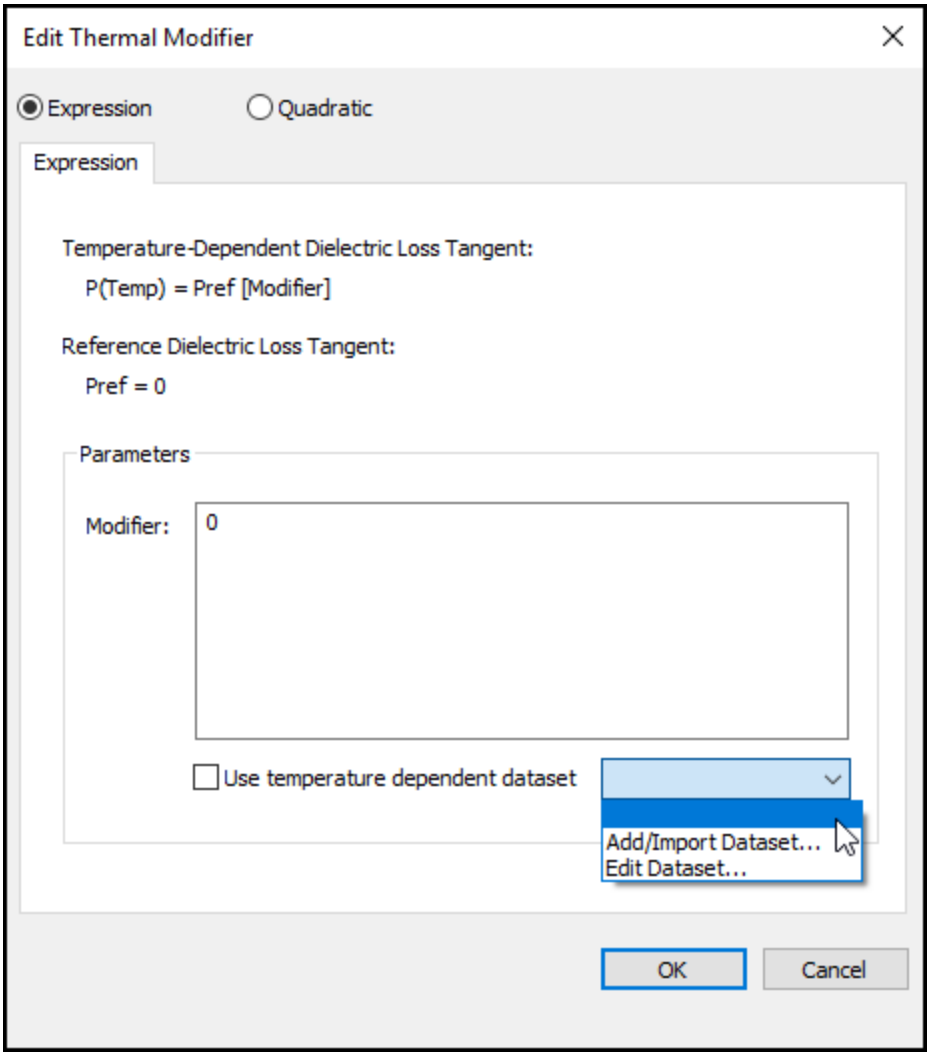

Select **Quadratic** to define either a **Basic Coefficient Set** or an **Advanced Coefficient Set.**

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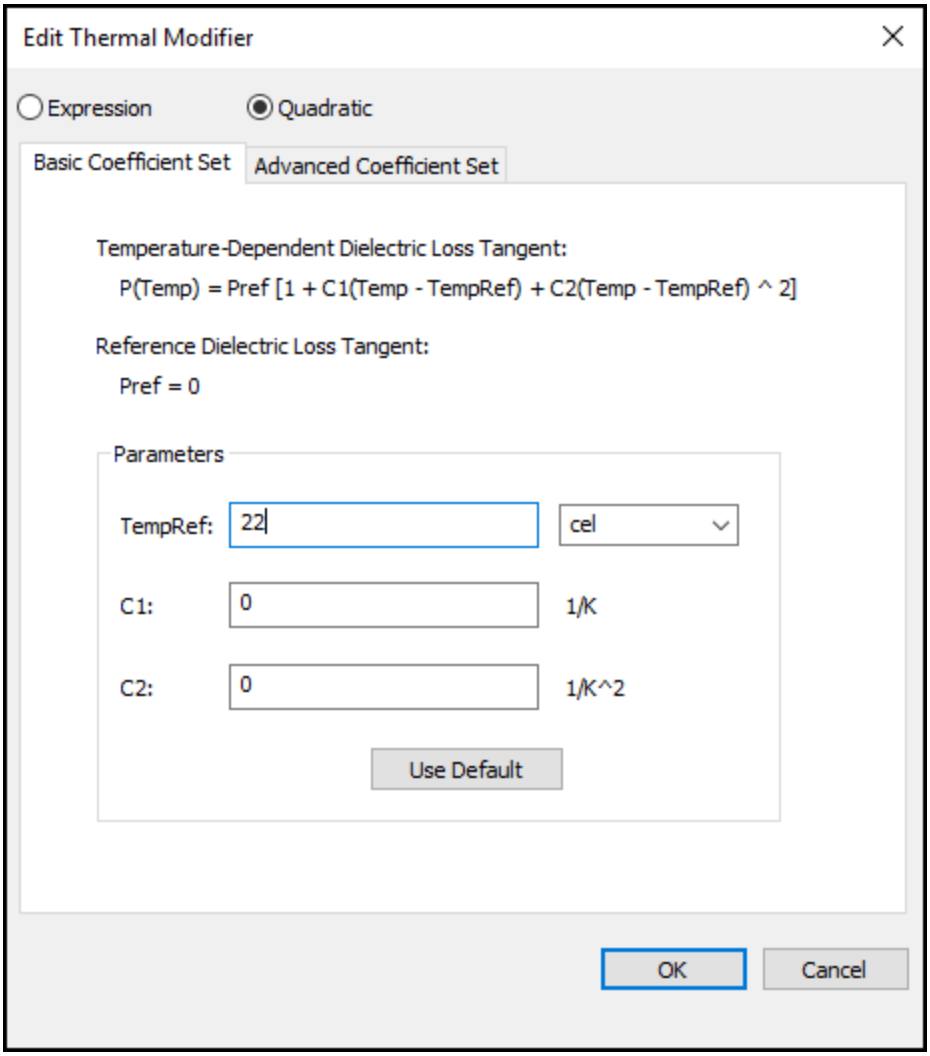

The window displays the formula for temperature-dependent dielectric loss tangent:

$$\mathbf{P\,(Temp) = Pref\left[1 + C1\,(Temp - TempRef) + C2(Temp - TempRef)^2\right]}$$

The **Basic Coefficient Set** allows you to edit the TempRef, C1, and C1 values.

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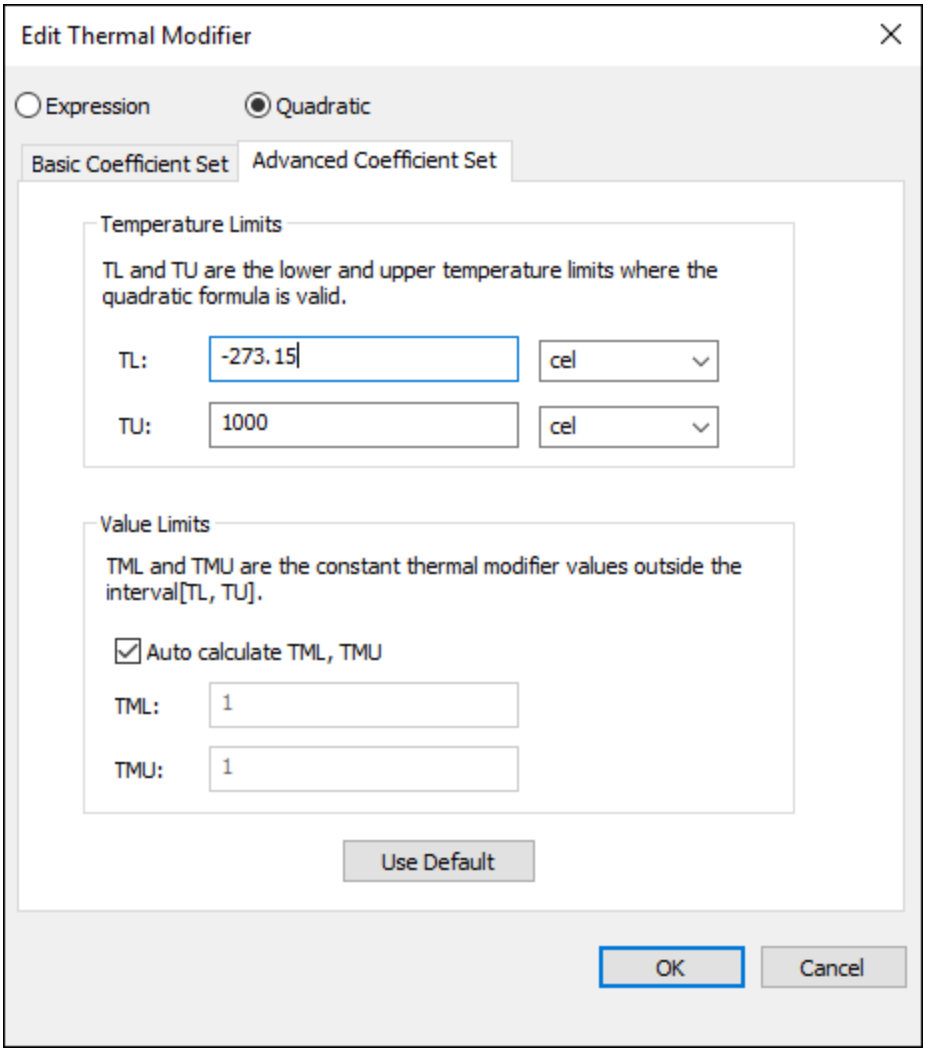

The **Advanced Coefficient Set** allows you to specify the lower (TL) and upper (TU) temperature limits inside which the quadratic formula is valid. It also allows you to specify the lower (TML) and upper (TMU) thermal modifier values outside of the TL and TU.

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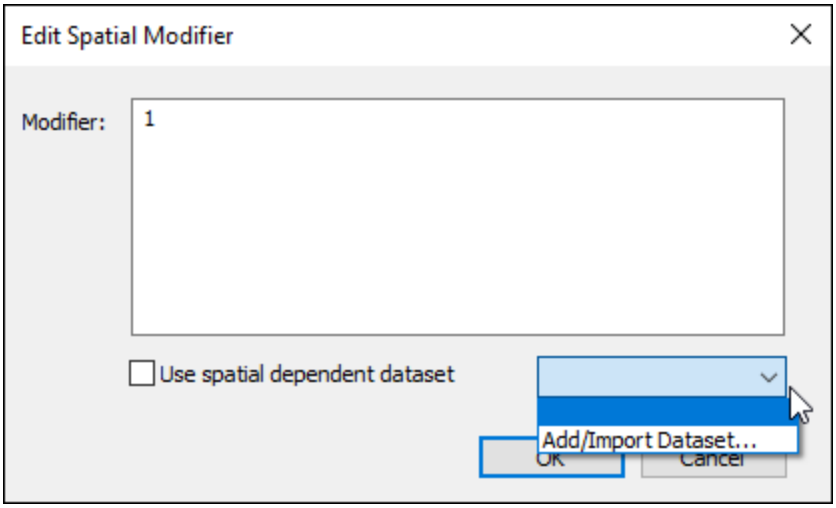
Spatial Modifiers



You can type a value for the spatial **Modifier** as an integer, real number, variable, expression, or dataset in the form "clp($ds1,X,Y,Z)".

Any existing datasets can be selected from the drop-down menu. Otherwise, select **Add/Import Dataset** to open the **Add Dataset** window, where you can specify object coordinates and associated values of the material property:

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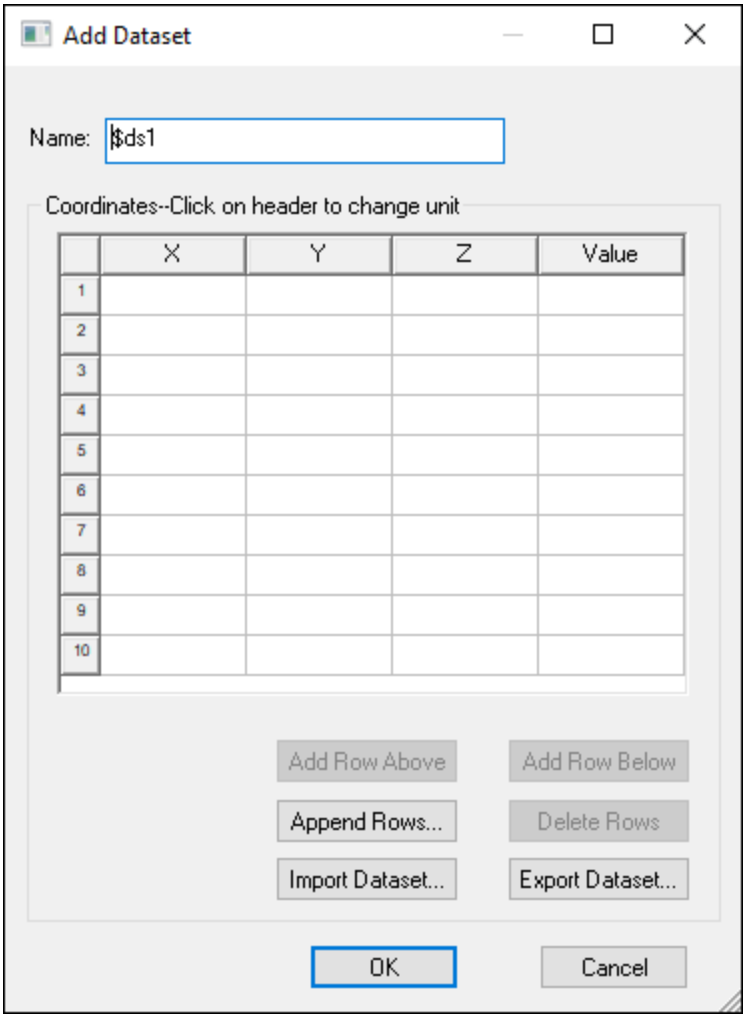

Deleting a Material

You can delete any material.

To do so:

1. Click **Home**.
2. From the **Edit Tools** area, click **Edit Materials**.

   The **Select Definition** window appears.

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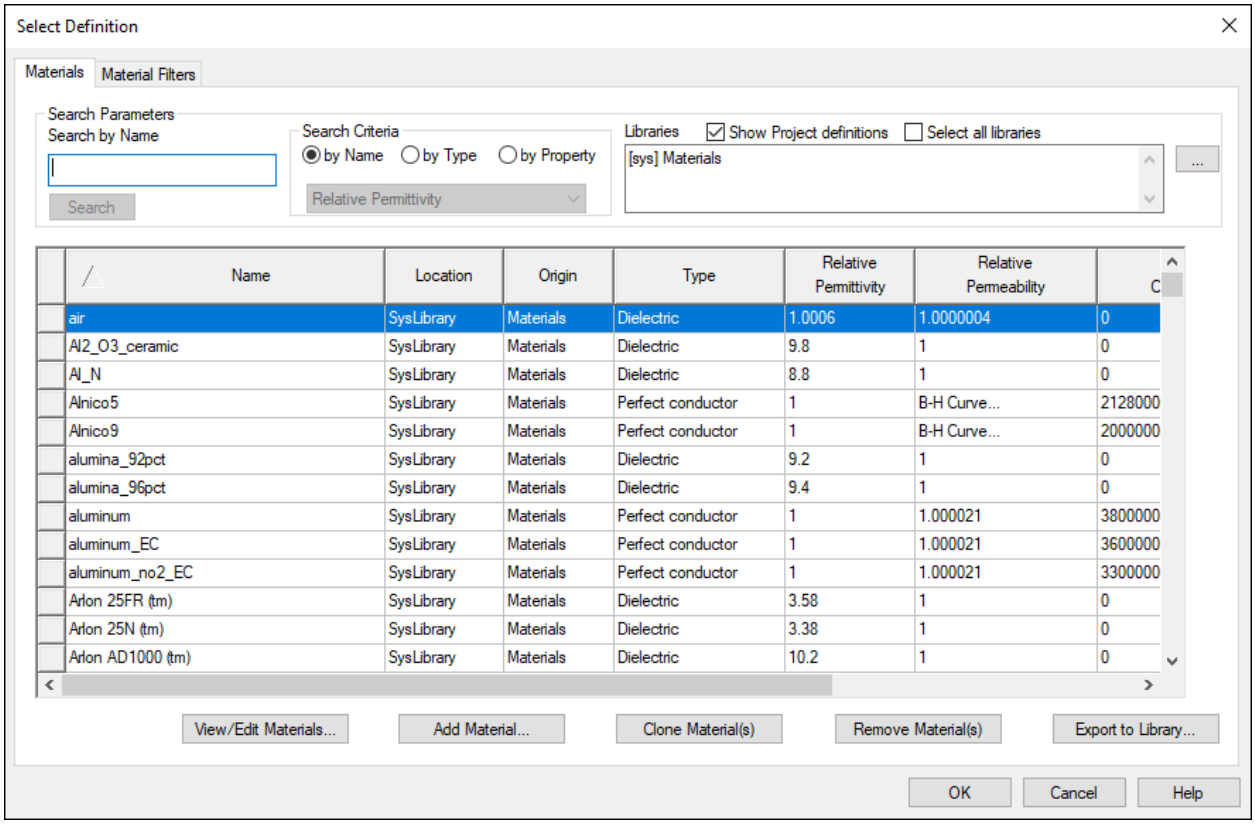

3. Under **Libraries**, click the ellipsis (**...**) button to select the library in which the material resides.

   The materials list updates.

4. From the materials list, select the material you want to modify and click **Remove Material (s)**.

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5 - Modeling PCB Designs

SIwave can work with a single printed circuit board in a given design.

This section explains basic operations that allow you to draw or modify a model using the Modeling Workspace and Components Workspace:

- Drawing a Model
- Adding Circuit Elements
- Working with Traces
- Working with Padstacks and Vias
- Backdrilling

Drawing a Model

Before you can begin drawing a model, you must first choose a layer on which you want to draw.

You can work in various geometry modes, depending on the type of geometry:

- Drawing Mode
- Geometry Selection Mode
- Net Selection Mode

You can also copy the entire Modeling workspace or clip the design to a specified shape.

Geometric Elements

Geometric elements include regions, traces, pads and vias.

- Editing a board
- Editing a plane
- Scaling a plane
- Performing Boolean operations on planes
- Defining region extents

Editing a Board

SIwave allows you to edit board outline(s). The board outlines will be updated when new geometry is added.

To edit a board:

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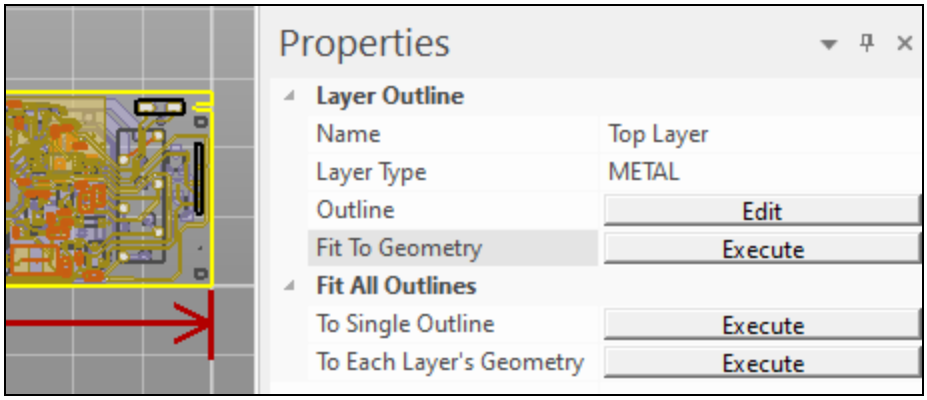
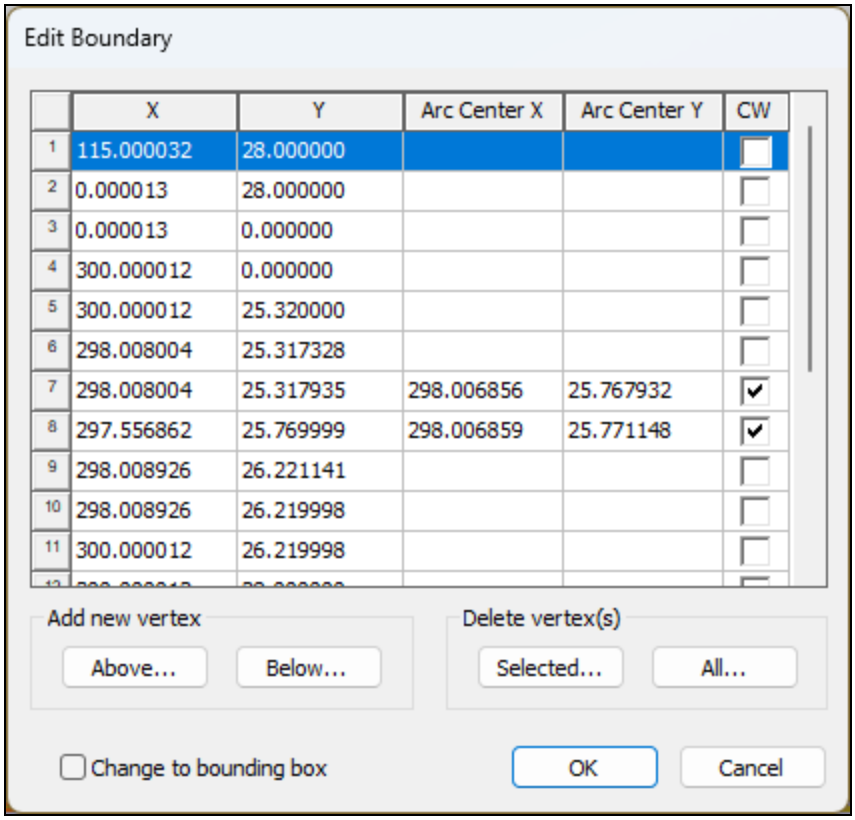
1. Select the board boundary to populate the **Properties** workspace.



2. From the **Properties** workspace, click **Edit** to open the **Edit Boundary** window.



3. If appropriate, edit the board as follows:
   - Modify the **X**, **Y**, **Arc Center X**, or **Arc Center Y** values by double-clicking a cell and entering the new value.
   - Specify that an arc is clock-wise by checking the **CW** box.
   - Add a new vertex above or below an existing vertex using the **Above** and **Below** buttons.

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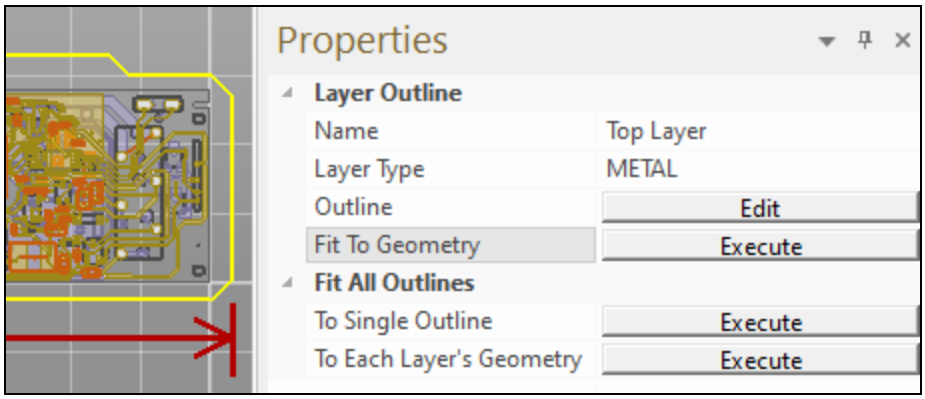
- Delete a vertex by selecting its row and clicking **Selected**
- Delete all vertices by clicking **All**

4. Click **OK** to apply your changes.
5. If appropriate, click **Execute** adjacent to **Fit to Geometry** and the outline will conform to the shape of the design.



6. If appropriate, click **Execute** adjacent to **To Single Outline** or **To Each Layer's Geometry** and the outline will conform to in one single outline or to each layer's separate geometry.

Editing a Plane

To edit a plane:

1. Select the plane you want to edit.
2. Click **Advanced** > **Plane (Boundary/Cutout)**.

   The **Edit Plane's Boundary** window appears.

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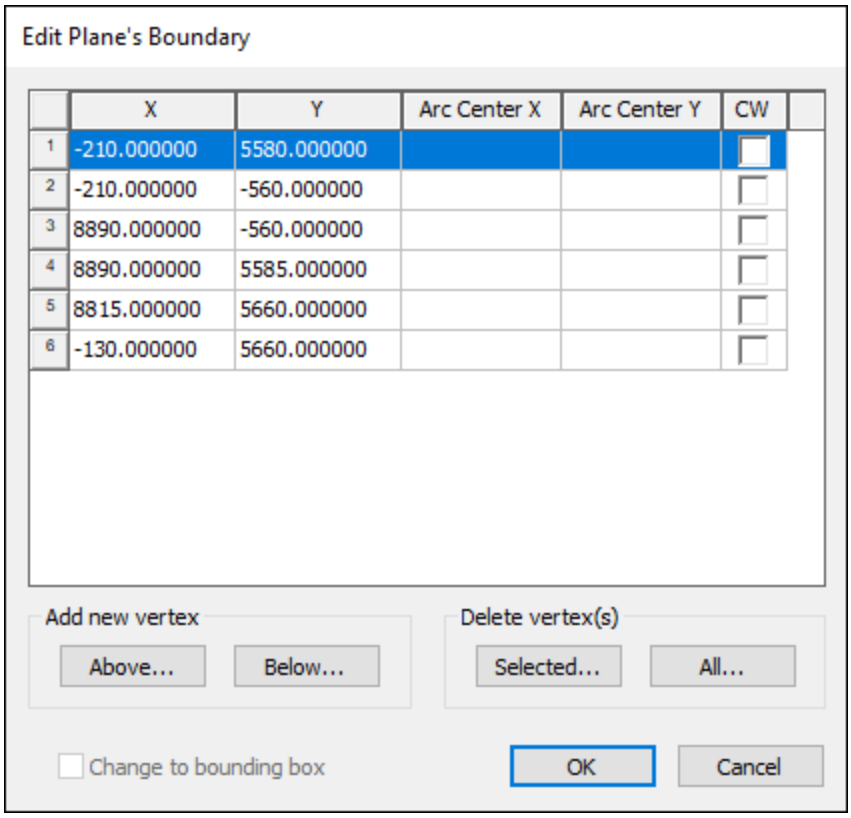

3. If appropriate, edit the plane as follows:
   - Modify the **X**, **Y**, **Arc Center X**, or **Arc Center Y** values by double-clicking a cell and entering the new value.
   - Specify that an arc is clock-wise by checking the **CW** box.
   - Add a new vertex above or below an existing vertex using the **Above** and **Below** buttons.
   - Delete a plane vertex by selecting its row and clicking **Selected**
   - Delete all plane vertices by clicking **All...**
4. Click **OK** to apply your changes.

Scaling a Plane

To expand or shrink a plane:

1. Select the plane you want to resize.
2. Click **Advanced** > **Resize Planes**.

   The **Resize Planes** window appears.

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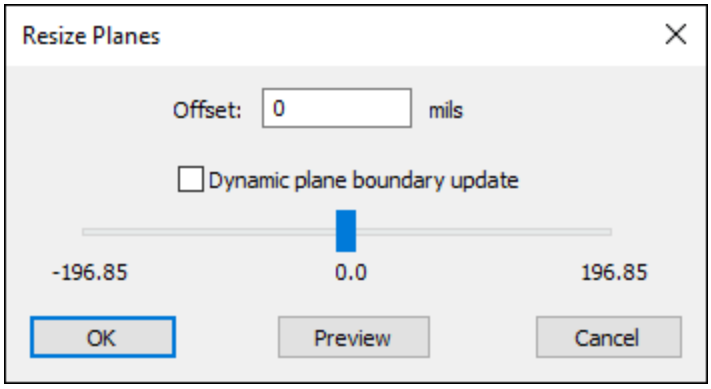

3. Type the **Offset** value, or check the **Dynamic plane boundary update** check box to use the slider.
4. Click **Preview** to see what the change will look like.
5. When you are ready to resize the plane, click **OK** .

Performing Boolean Operations on Planes

Boolean operations can be performed on planes. You can unite, subtract or intersect planes.

Uniting Planes

Uniting two planes merges them into one plane. To unite two planes:

1. Select the two planes that you want to unite. The planes must be on the same layer.
2. Click **Tools**. From the **Transformation Tools** area, click **Unite**.

Subtracting Planes

To subtract one plane from the other:

1. Click **Tools**. From the **Transformation Tools** area, click **Subtract**.

   The **Subtract Planes from Planes** window appears.

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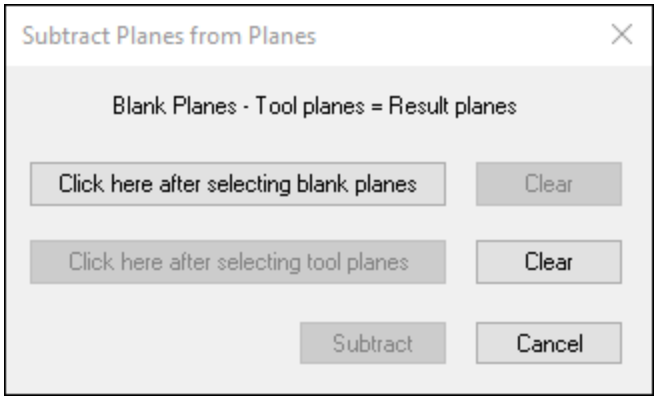

2. Select the first plane, and click **Click here after selecting blank planes**.
3. Select the second plane, and click **Click here after selecting tool planes**.
4. If you make an error, click **Clear** to start over and reselect the planes.
5. Click **Subtract**.

Intersecting Planes

To create the intersection of two planes:

1. Select the two planes that you want to intersect.
2. Click **Tools**. From the **Transformation Tools** area, click **Intersect**.

Defining Region Extents

Region extents determine the shape and size of the area to select for a plane object

To set the shape, click the **Home** tab. Then, from the **Draw Geometry** box, click the icon. The default type is **Simple auto region extents to terminals**.

- To set the resolution, click the icon. Then select **Precise auto region extent**.
- To set the resolution of region extents to terminals, click the icon. Then select either **Simple auto region extent to terminals** or **Precise auto region extent to terminals**.
- To set the distance for region extents, set the distance in the view units of the project.

Importing and Exporting Extents

You can also import and export extents as .pxt files.

To import an existing region extent, click **Import** > **Region Extents** and select a file (*.pxt).

To export a .pxt file for later use, click **Export** > **Region Extents** and select a name and location for your file.

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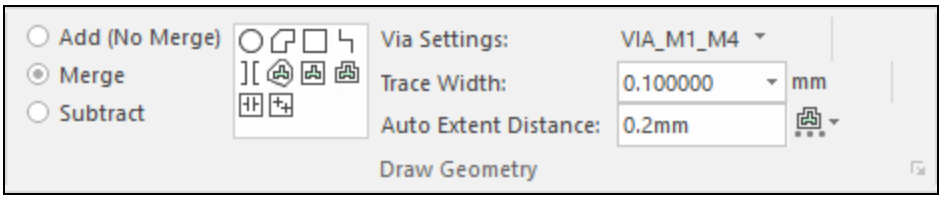
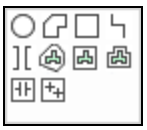
Working in Drawing Mode

Drawing Mode options are located in the Draw Geometry section of the **Home** tab.



The draw box contains elements you can draw:



The radio buttons allow you to decide which option to apply when drawing two or more geometric shapes:

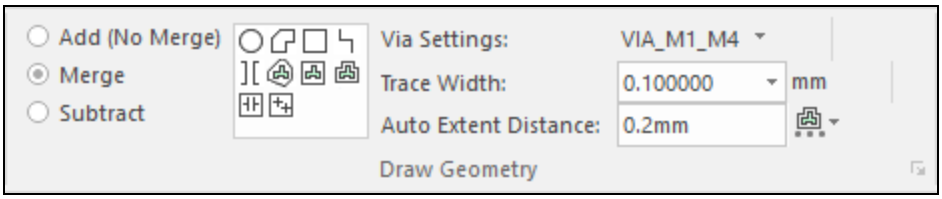
- **Add (No Merge)** – draws and displays multiple objects.
- **Merge** – draws and displays multiple objects as one merged object.
- **Subtract** – modifies an existing geometry by cutting a selected shape from it.

The options on the right apply to vias, traces, and extents.

Drawing a Geometric Shape

To draw any geometry:

Click **Home**. From the Draw Geometry section, select either **Add (No Merge)**, **Merge**, or **Subtract**.



Select the shape you wish to draw.

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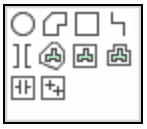
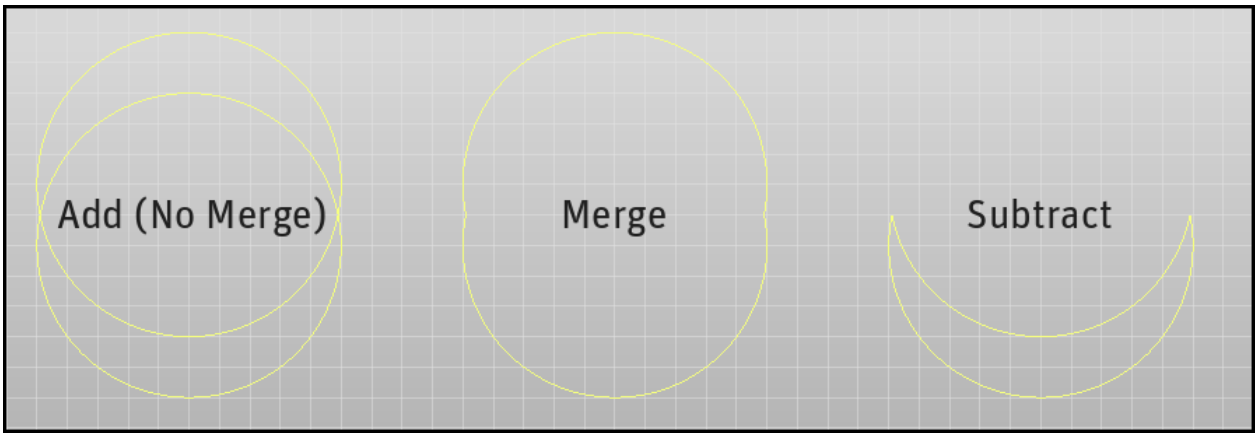


The following image shows the results of Add, Merge, and Subtract. For each, an initial circle was drawn, and a second circle was drawn above it with the indicated mode selected.



More Information:

- Drawing Circles
- Drawing Polygons and Arcs
- Drawing Rectangles
- Drawing Extents

Drawing a Circle

To draw a circle:

1. Click **Home**. From the Draw Geometry section, click the circle icon ( ).
2. Identify the center of the circle, and click at that point.
3. Determine the radius, and drag the mouse to draw a circle.
4. Click to finish.

You now have a circle, at an appropriate location and of an appropriate radius.

Drawing a Polygon

To draw a polygon:

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1. Click **Home**. From the Draw Geometry section, click the polygon icon ( ).
2. Click the point where you wish to start the polygon.
3. Click-and-drag the mouse to draw the shape of the polygon. The lines in the polygon cannot intersect.
4. Click to end each line.
5. Double-click to end the polygon.

To draw arc segments:

1. While drawing the polygon, right-click.

   A menu appears. Select **Arc**.

2. Choose the location of the arc center and click it.
3. Choose the location of the end-point and click it.

Drawing a Rectangle

To draw a rectangle:

1. Click **Home**. From the Draw Geometry section, click the rectangle icon ( ).
2. Choose the location of the starting point and click it.
3. Click-and-drag the mouse to draw the rectangle.
4. Click to finish.

You now have a rectangle at an appropriate location and of an appropriate area.

Drawing Extents

Extents define the area in which you can place components.

To define extents:

1. Click **Home**.
2. From the **Draw Geometry** section, click the Polygonal Extent ( ) or Rectangular Extent ( ) icon.
3. Draw the area.

The Modeling workspace is modified according to the values selected.

You can also automatically generate extents around your design by clicking the Automatic Extent ( ) icon.

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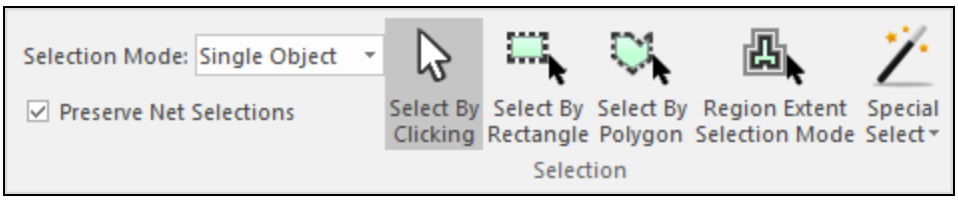
Working in Geometry Selection Mode

After you have drawn a geometry, you can either select a component or select the entire geometry in a particular area.

Selection options appear on the **Home** tab.



To select individual components in a geometry, click **Select By Clicking**.

To select geometry in a defined rectangle:

1. Click **Select By Rectangle.**
2. Click at the starting point to draw a box in which you want to select the geometry.
3. Drag-and-drop to an appropriate box area.

To select geometry in a defined polygonal area:

1. Click **Select By Polygon.**
2. Click at the starting point to draw a polygon in which you want to select the geometry.
3. Click once to create every polygon vertex, and finally double-click to close the polygon.

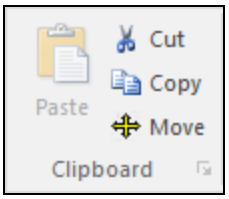
To select an extent:

1. Click **Region Extent Selection Mode.**
2. Click an extent region in the Modeling workspace.

The color of the geometry changes when it is selected. Change the selection color by clicking **View > Selection Color** and selecting a new color.

Working with Selected Geometries

From the **Home** tab, you can also perform clipboard actions on your selection.



Clipboard Options include:

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- **Cut** – removes the selection from the Modeling workspace and places it on the clipboard so that it can be pasted elsewhere.
- **Copy** – places the selection on the clipboard so that it can be pasted elsewhere, but does not remove it from the Modeling workspace.
- **Paste** – places the cut or copied selection in the Modeling workspace.
- **Move** – allows you to change the selection's location in the Modeling workspace.

Copying the Modeling workspace

You can capture an image of what your Modeling workspace looks like.

Right-click in the Modeling workspace, and select **copy image** on the shortcut menu.

You can paste this image into any graphics editor.

Clipping the Design

SIwave allows you to cut out and view a particular region of the design and ignore the rest of the geometry.

To clip a design:

1. Click **Tools**. From the **Transformation Tools** area, click **Clip Design**.

   The **Options For Clipping Design** window appears.

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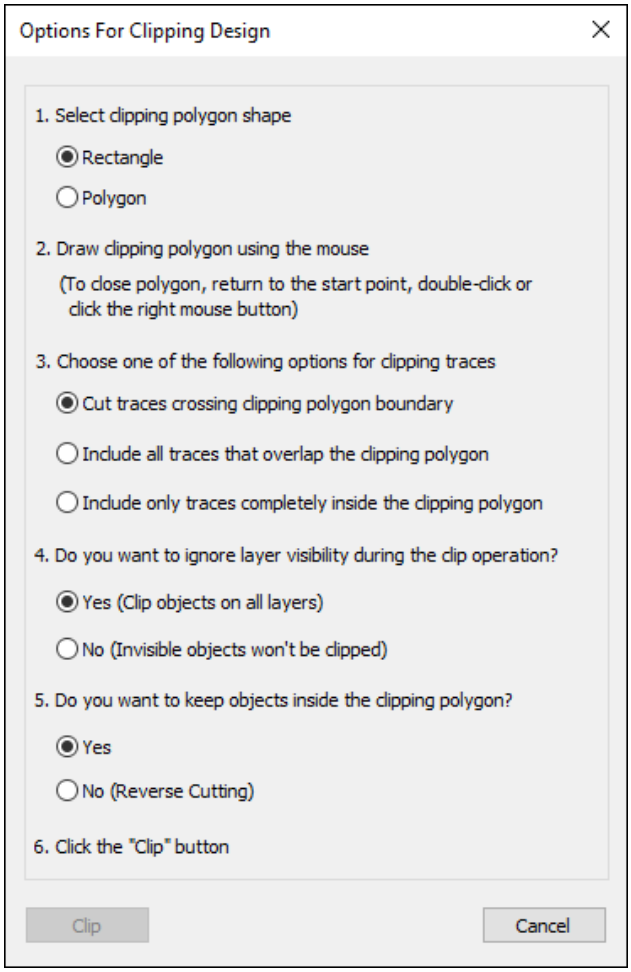

2. Select the shape of the cutting area. You can choose either **Rectangle** or **Polygon**. The **Clip** button is enabled after you select a shape.
3. Draw the cutting area.

   To draw a rectangle:

   a. Choose the location of the starting point and click on it.
   b. Click-and-drag the mouse to draw the rectangle.
   c. Click or double-click to finish. You can also right-click and then select **Done** from the short-cut menu.

   To draw a polygon:

   a. Click on the point where you want to start the polygon.
   b. Click-and-drag the mouse to draw the shape of the polygon. The lines in the polygon cannot intersect.

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c. Click to end each line.
d. Double-click to end the polygon. You can also right-click and then select **Done** from the short-cut menu.

4. Specify the options for clipping traces. You can choose either **Cut traces crossing clipping polygon boundary**, **Include all traces which overlap the clipping polygon**, or **Include only traces completely inside the clipping polygon**.
5. Specify the visibility options. You can choose either **Yes** to clip all objects on all layers or **No** to clip visible objects only.
6. Click **Clip**.

Circuit Elements

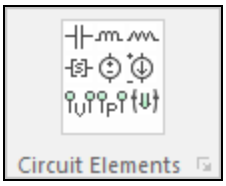
Circuit elements are indivisible components with unique behavior that can be described through a mathematical relationship between voltage and current. They may or may not have a polarity.

Connecting circuit elements in any combination is referred to as wiring a circuit. Points where two or more elements meet at one of their two ends are called *nodes*. After the circuit is wired, its elements form some closed loops. In complex circuits with many loops they form a *mesh* or a *network*.

Passive elements (elements that do not generate power) can be added to your drawing and you can see their influence on the simulation.

Adding Circuit Elements

To add a circuit element, click the **Home** tab and navigate to the **Circuit Elements** area.



The **Circuit Elements** box allows you to perform the following actions:

- Add Capacitor
- Add Inductor
- Add Resistor
- Add S-parameter Circuit Element
- Add Voltage Source
- Add Current Source
- Add Voltage Probe

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- Add Port
- Add Terminal

Adding a Capacitor

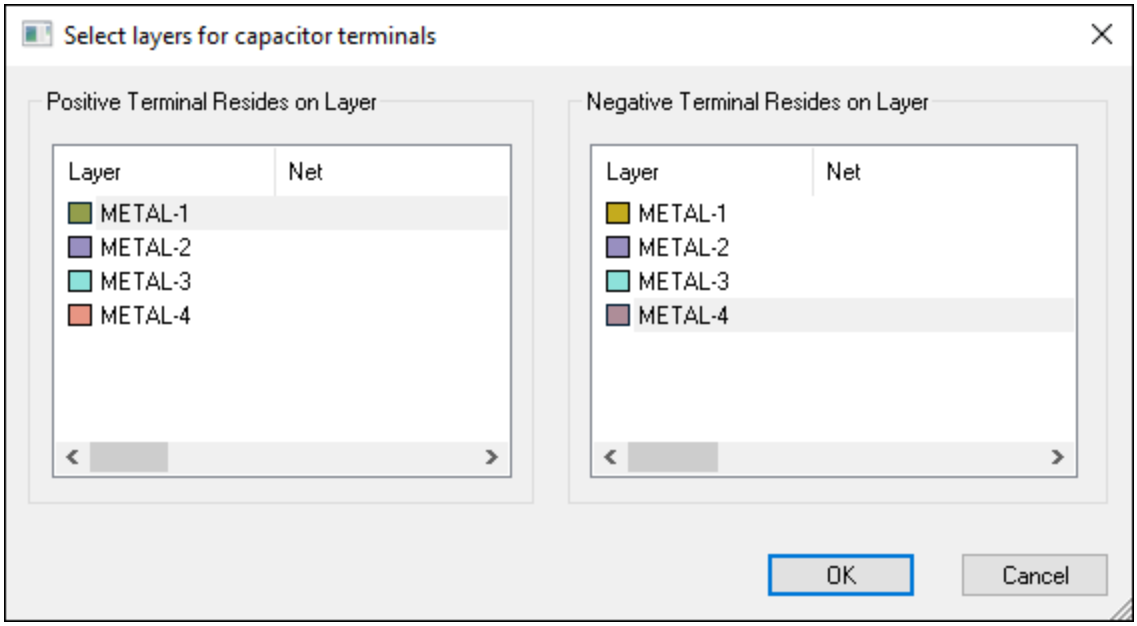
A *capacitor* is an electronic component used to store charge.

To add a capacitor:

1. Click **Home**. From the **Circuit Elements** box, click the **Add Capacitor** icon ( ).
2. Click the location where you want to place the capacitor.
3. Drag the mouse to an appropriate length and direction.
4. Click to finish drawing.

   You have drawn a capacitor, but still need to assign it values such as capacitance, parasitic inductance, and parasitic resistance.

   When you finish drawing the capacitor, the **Select layers for capacitor terminals** window appears.



5. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
6. From the **Negative Terminal Resides on Layer** list, select the layer for the negative end.
7. Click **OK**.

   The **Set Capacitor Parameters** window appears.

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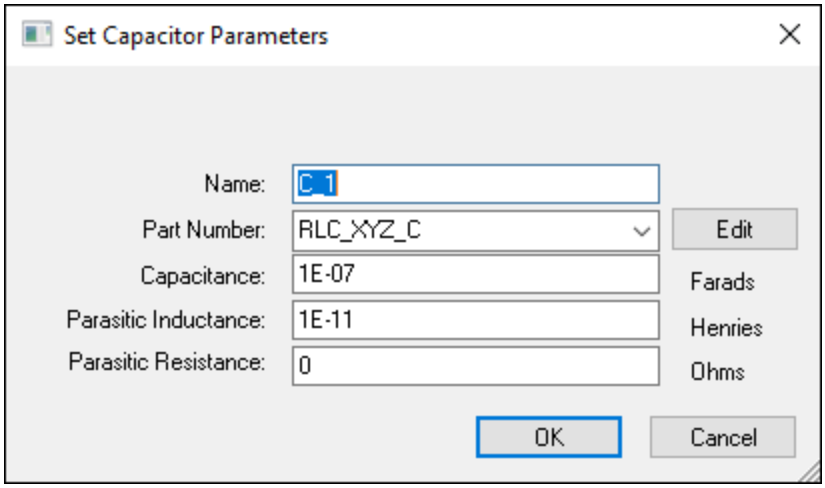

8. From the **Name** field, type a name for the capacitor.
9. From the **Part Number** field, type the manufacturer's part number.
10. From the **Capacitance** field, enter a value in Farads.
11. From the **Parasitic Inductance** field, enter a value in Henries.
12. From the **Parasitic Resistance** field, enter a value in Ohms.
13. Click **OK**.

    You have now added and assigned values to your capacitor. You can also edit the parameters.

Defining Capacitor Mount Dimensions

You can review the mounting dimensions for capacitors by Electronic Industries Alliance (EIA) size. The Capacitor Mount Dimensions window allows you to import and export capacitor mount dimensions as a file (*.mdf). Mounting data can be used by the Capacitor Library Browser and the PI Advisor.

To specify capacitor mount dimensions:

1. Click **Advanced** > **Capacitor Dimension**.

   The **Capacitor Mount Dimensions** window appears.

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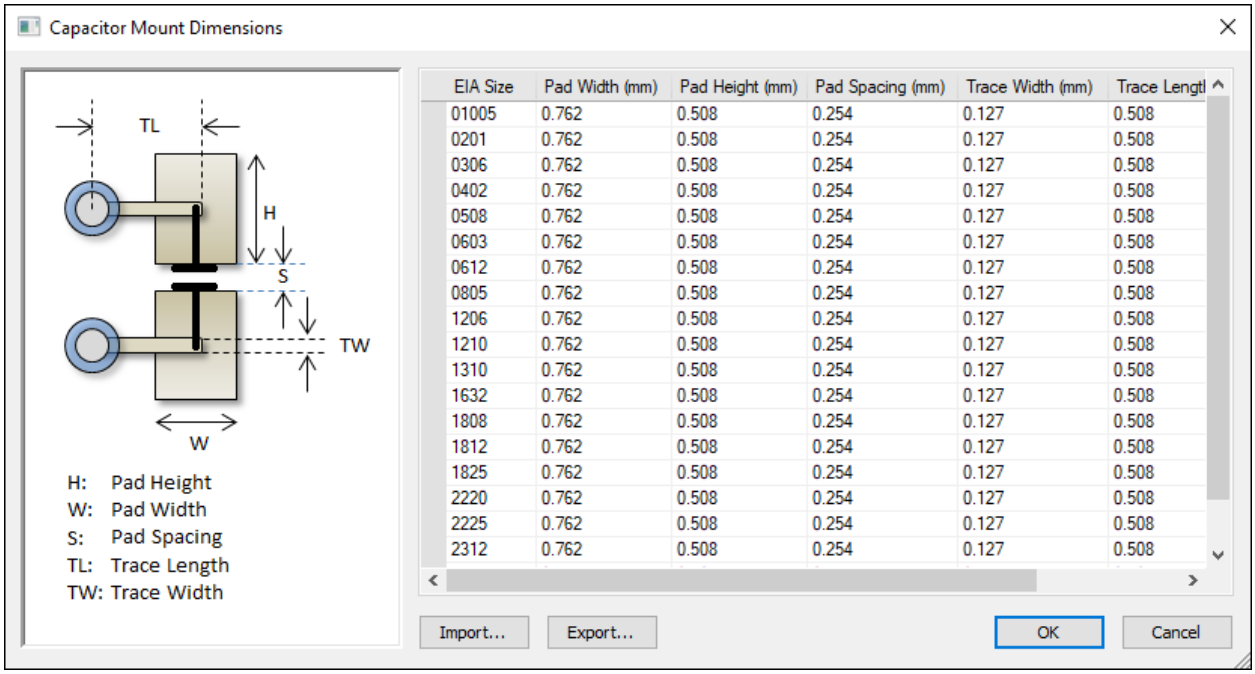


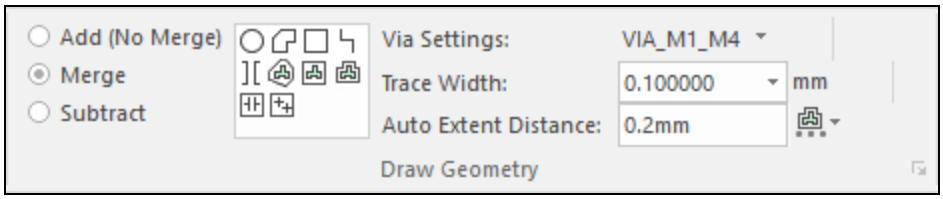
2. Use the **Import...** button to select an .mdf file for import.
3. To manually define dimensions, click a cell and type the new value.
4. Click **OK** to apply changes.
5. If you want to save your settings, click **Export...** to create an.mdf file.

Defining Capacitor Regions

You can define the area in which you will be placing your capacitors.

To define a capacitor region:

1. Click **Home**. From the Draw Geometry section, click the **Define Capacitor Regions...** icon ( ).



The **Define Capacitor Regions** window appears.

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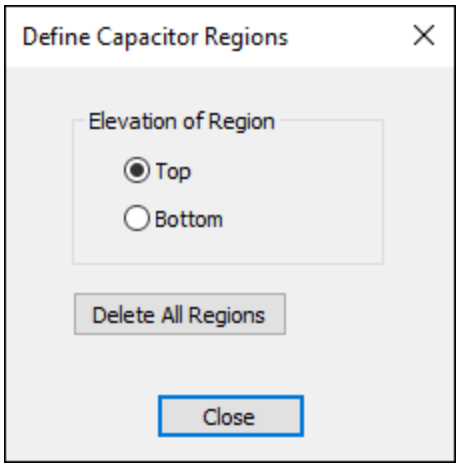

2. Select the elevation to be either the **Top** or **Bottom** of the board.
3. Click an area in the Modeling workspace to draw the rectangle.
4. Click **Close**.

To remove the defined regions, open the **Define Capacitor Regions** window and click **Delete All Regions**.

Using the Capacitor Library Browser

SIwave allows users to define VRM parameters and impedance requirements, automatically select and mount capacitors that meet those requirements, then plot the impedance of various vendor or imported capacitor components versus frequency. Capacitors are mounted within previously defined capacitor regions. Complete the following steps to open and set up the capacitor library.

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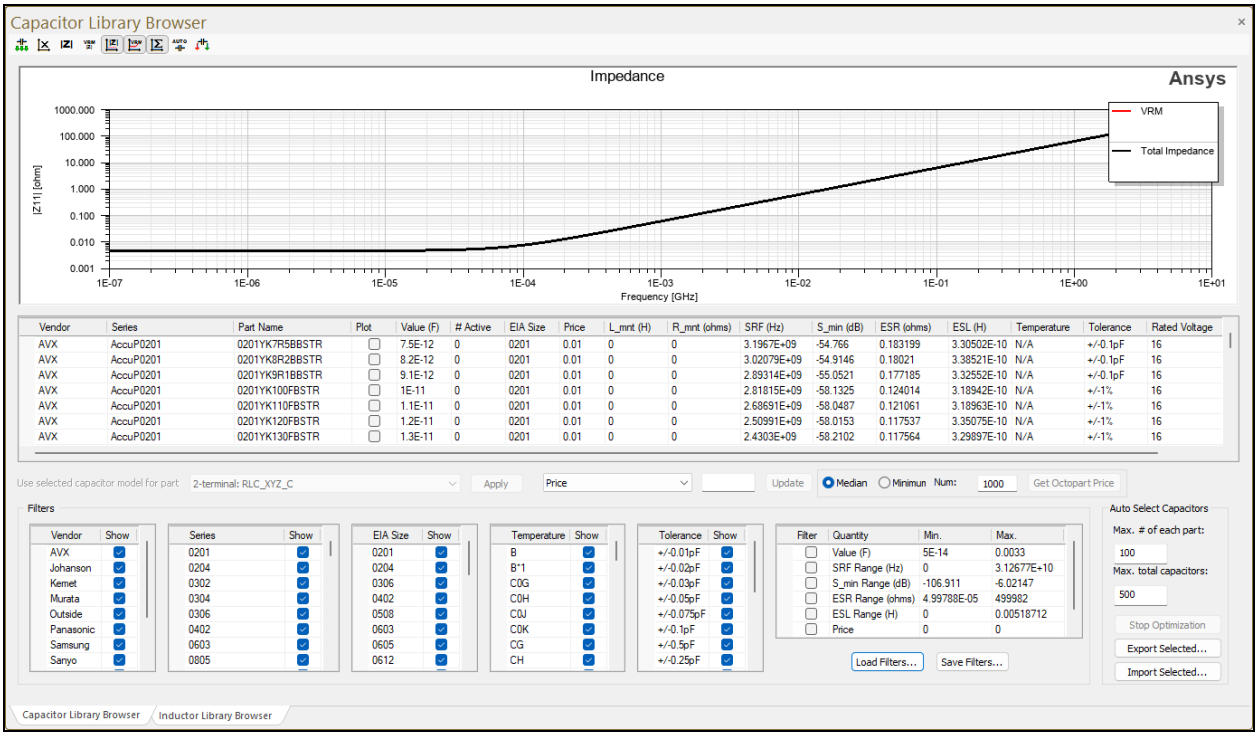
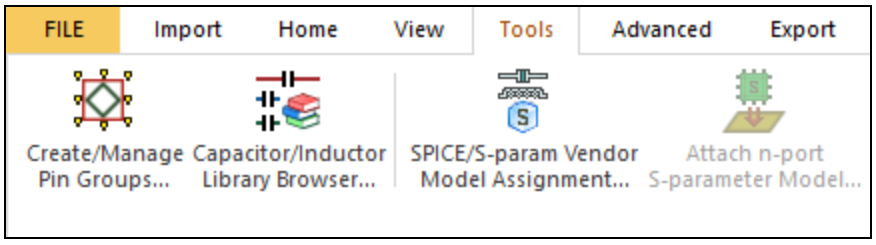


Note:

These instructions are written assuming users make selections from the **Capacitor Library Browser** tab. The **Inductor Library Browser** is available at any time by selecting the **Inductor Library Browser** tab at the bottom-left of the window. Differences are noted in the following text, aside from the most obvious (i.e., assume "inductor" in place of "capacitor").

1. From the **Tools** ribbon, select **Capacitor/Inductor Library Browser** to open the **Capacitor Library Browser** window.



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Note:

Sort the values in the central table by clicking a column title.

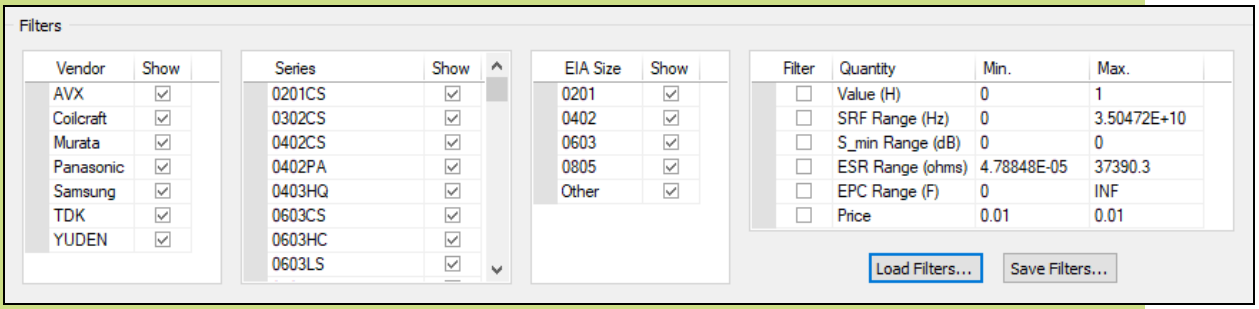
2. To automatically select capacitors that match the defined impedance profile, navigate to the row of buttons in the top-left corner and click **Auto Select** ( ).
3. To manually select a capacitor from the central table, check the **Plot** box. To plot a capacitor's impedance curve, click the **Plot** column heading.
4. Specify filters to dynamically update visible options. Filter by any combination of parameters and across several ranges.

Note:

Filters vary between the **Capacitor Library Browser** tab and the **Inductor Library Browser** tab.

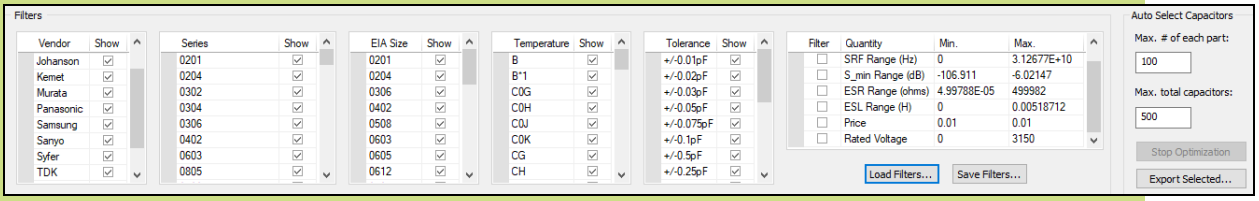
Inductor Library Browser Tab

Filter by **Vendor**, **Series**, and **EIA Size**, as well as across most of the available ranges (i.e.**Value**, **SRF Range**, **S_min Range**, **ESR Range**, **ESL Range**, **Price**.



Capacitor Library Browser Tab

All of the same filters and ranges are available, as well as additional filters for **Temperature** and **Tolerance**, and an additional value range (i.e., **Rated Voltage**).



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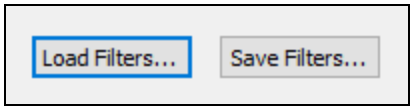
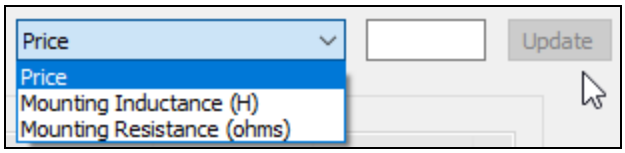
5. If appropriate, do either of the following:



   - To import filter settings click **Load Filters**. Then navigate to an appropriate **Capacitor filter criteria** (i.e., **.cff**) file and click **Open**.
   - To save the current filter settings, click **Save Filters**. Then navigate to an appropriate directory, name the output **.cff** file, and click **Save**.

6. To update a value for multiple capacitors, select a value from the drop-down menu above the **Filters** area. Then enter a value in the text field and click **Update**.



7. To import a capacitor model from a **Touchstone** file, do the following:
   a. Navigate to the row of buttons in the top-left corner and click **Import** ( ) to open the **Import S-parameter Component** window.

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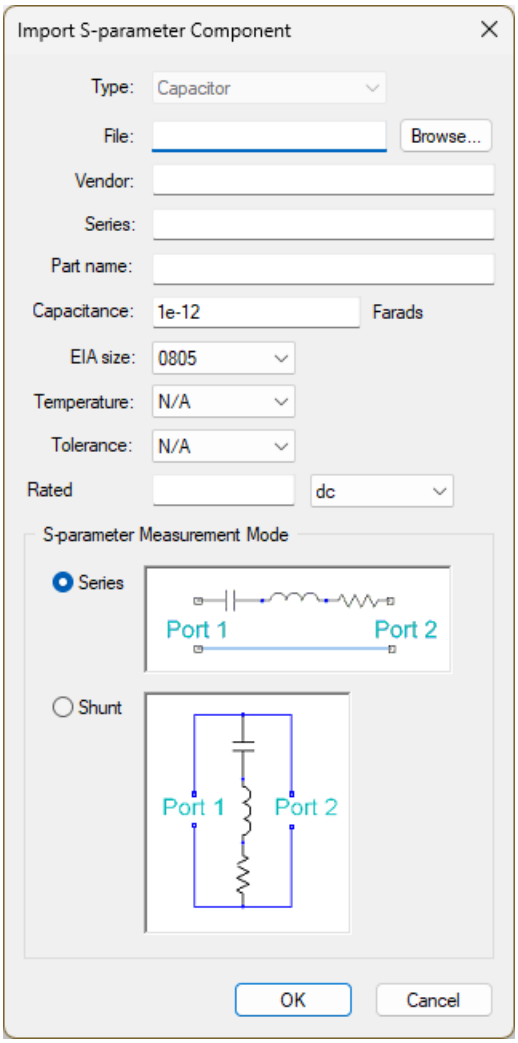

b. Specify the component details then click **OK**.

8. To remove all capacitor impedance curves that have been selected, navigate to the row of buttons in the top-left corner and click **Remove all impedance curves from plot** ( ).
9. To define impedance requirements, do the following:
   a. Navigate to the row of buttons in the top-left corner and click **Define Impedance Requirements** ( ) to open the **Define Impedance Mask** window.

> **Note:**
>
> The **Define Impedance Mask** window and **Define VRM Parameters** window (i.e., step 10 are functionally similar to options available at the PI Advisor Wizard - Step 1 window.

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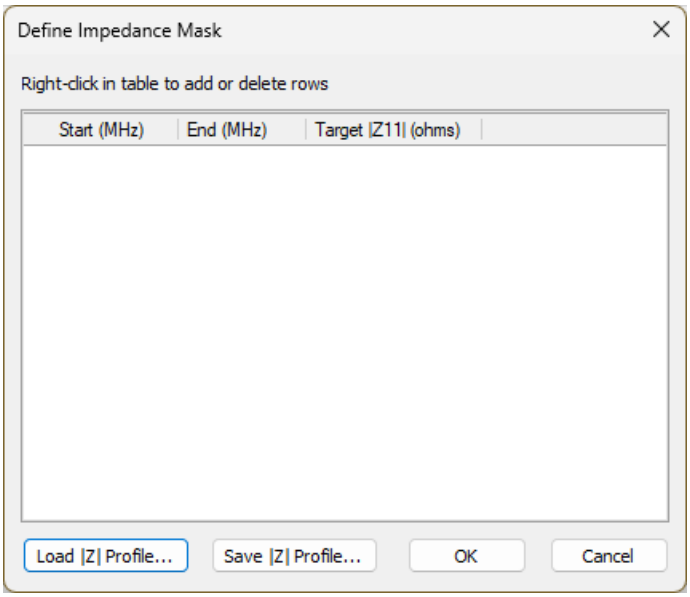
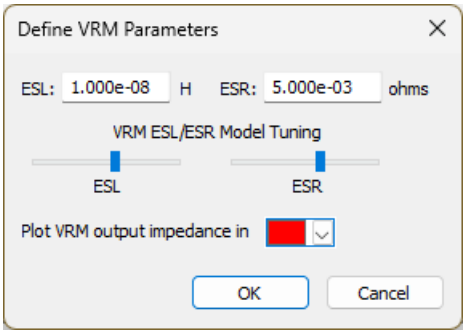


b. From the **Define Impedance Mask** window, right-click in the table and click **Add Row** to begin creating an impedance profile.

c. Click **OK**.

10. To define VRM parameters, do the following:

a. Navigate to the row of buttons in the top-left corner and click **VRM** ( ) to open the **Define VRM Parameters** window.



b. Specify **ESL** and **ESR** by either entering new parameters in the appropriate fields or click+dragging the slides.

c. Select the plot color from the **Plot VRM output impedance in** drop-down menu.

d. Click **OK**.

11. To change the display options, navigate to the row of buttons in the top-left corner and click **display impedance mask** ( ), **VRM output impedance curve** ( ), or **aggregate output impedance curve** ( ), as appropriate.

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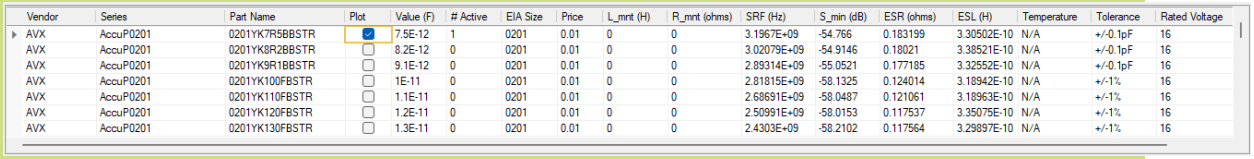
12. To mount the active capacitors, do the following:

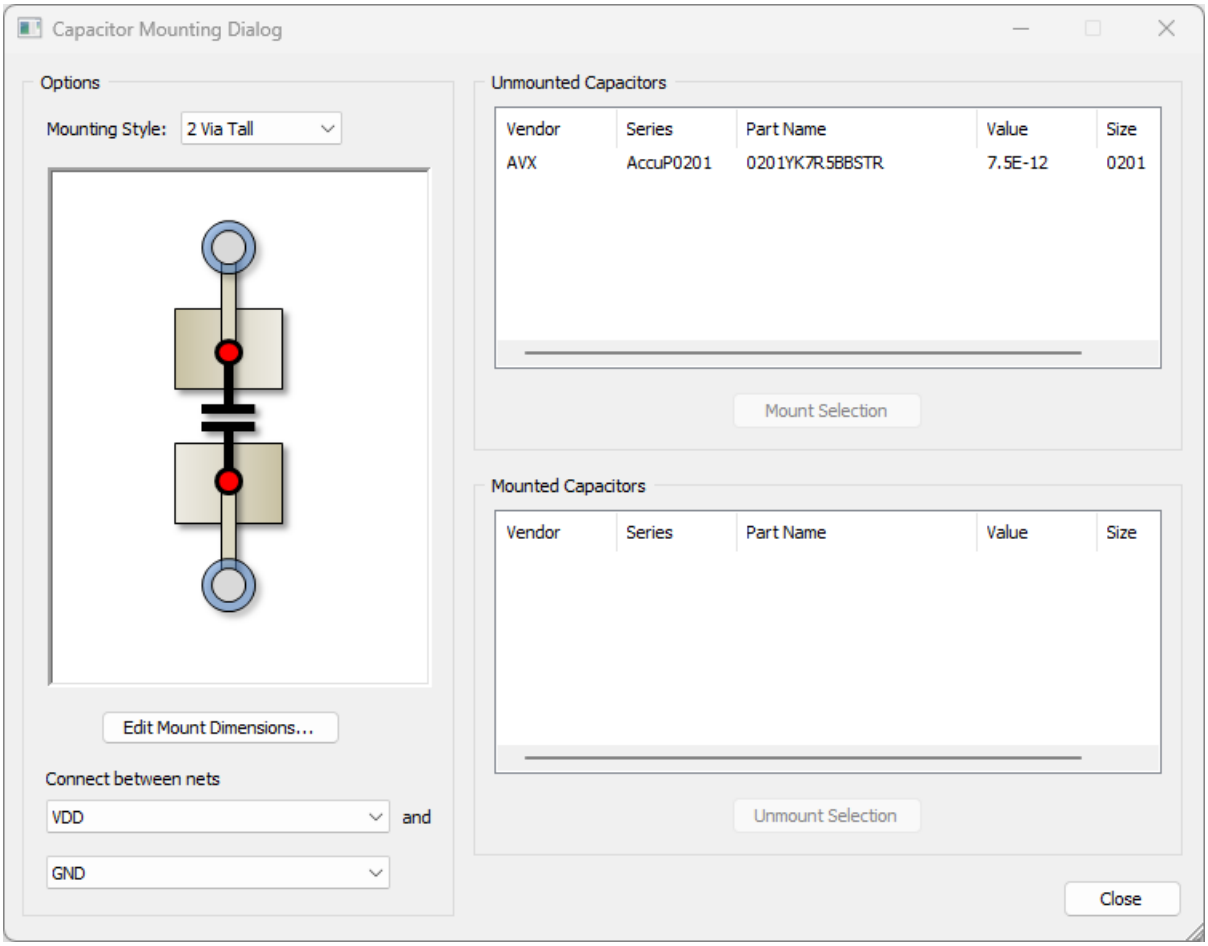
Note:

At least one capacitor must be selected in the **Capacitor Library Browser**.



Vendor	Series	Part Name	Plot	Value (F)	# Active	EIA Size	Price	L_mnt (H)	R_mnt (ohms)	SRF (Hz)	S_min (dB)	ESR (ohms)	ESL (H)	Temperature	Tolerance	Rated Voltage
AVX	AccuP0201	0201YK7R5BBSTR	☑	7.5E-12	1	0201	0.01	0	0	3.1967E+09	-54.766	0.183199	3.30502E-10	N/A	+/-0.1pF	16
AVX	AccuP0201	0201YK8R2BBSTR	☐	8.2E-12	0	0201	0.01	0	0	3.02079E+09	-54.9146	0.18021	3.38521E-10	N/A	+/-0.1pF	16
AVX	AccuP0201	0201YK9R1BBSTR	☐	9.1E-12	0	0201	0.01	0	0	2.89314E+09	-55.0521	0.177185	3.32552E-10	N/A	+/-0.1pF	16
AVX	AccuP0201	0201YK100FBSTR	☐	1E-11	0	0201	0.01	0	0	2.81815E+09	-58.1325	0.124014	3.18942E-10	N/A	+/-1%	16
AVX	AccuP0201	0201YK110FBSTR	☐	1.1E-11	0	0201	0.01	0	0	2.68691E+09	-58.0487	0.121061	3.18963E-10	N/A	+/-1%	16
AVX	AccuP0201	0201YK120FBSTR	☐	1.2E-11	0	0201	0.01	0	0	2.50991E+09	-58.0153	0.117537	3.35075E-10	N/A	+/-1%	16
AVX	AccuP0201	0201YK130FBSTR	☐	1.3E-11	0	0201	0.01	0	0	2.4303E+09	-58.2102	0.117564	3.29897E-10	N/A	+/-1%	16

a. Navigate to the row of buttons in the top-left corner and click **Mount Active Capacitors** ( ) to open the **Capacitor Mounting** window.



b. Select one of the capacitor regions.

c. Click **Mount Selection**.

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d. If appropriate, unmount a capacitor by selecting it in the **Mounted Capacitor** list, and then clicking **Unmount Selection**.
e. Click **Close**.

13. Select a value from the **Use selected capacitor model for part** drop-down menu to reassign it as a vendor capacitor part.
    a. To update the value for multiple capacitors, do the following:
    b. Select an appropriate value from the drop-down menu.
    c. Enter a new value for all the selected capacitors in the text box.
    d. Click **Update**.

Decoupling Capacitors

In SIwave, decoupling capacitors can be specified by one of the following methods:

1. RLC equivalent model - an RLC capacitor model has the R, L, and C elements connected in series. You can specify their values as needed.
2. S-parameter data supplied by the different manufacturers of discrete components.

See Adding a Circuit Element from the Component Database.

Adding an Inductor

An *inductor* is a passive electronic component that stores energy in the form of a magnetic field.

To add an inductor:

1. Click **Home**. From the **Circuit Elements** box, click the **Add Inductor** icon ( ).
2. Click the location where you want to place the inductor.
3. Drag the mouse to an appropriate length and direction.
4. Click to finish drawing.

   When you finish drawing the inductor, the **Select layers for inductor terminals** window appears.

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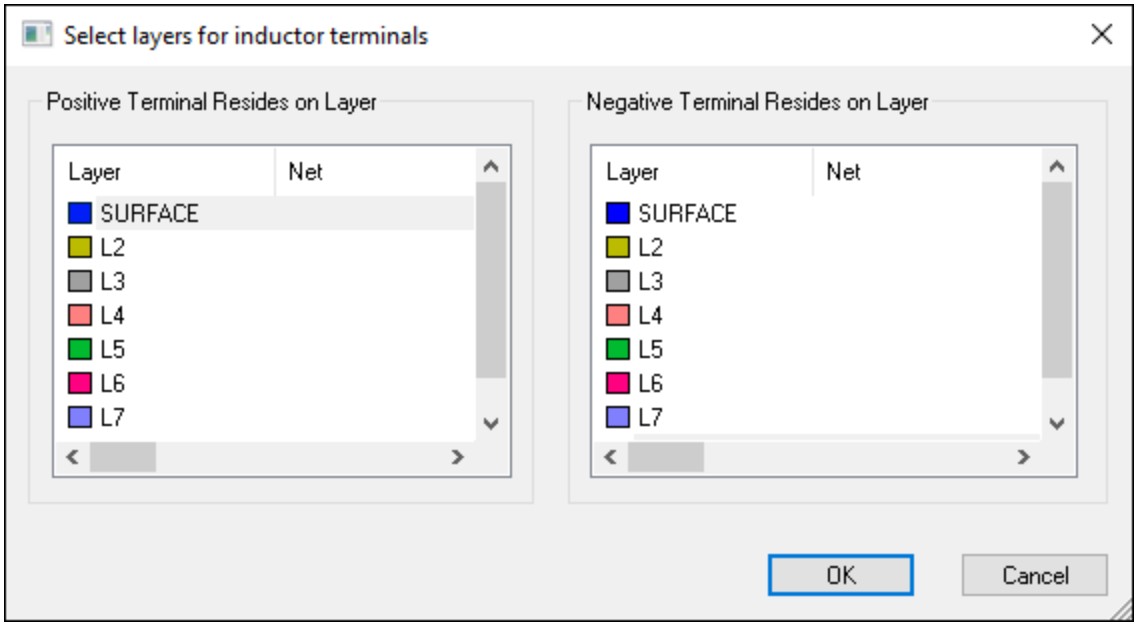
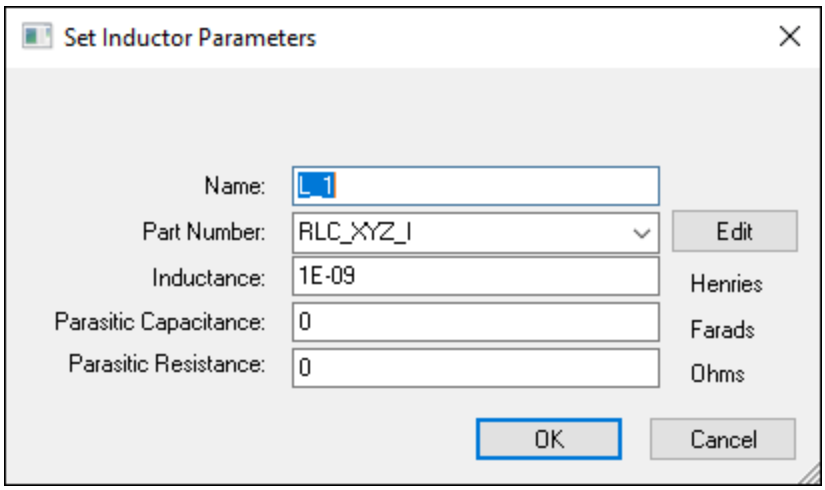


5. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
6. From the **Negative Terminal Resides on Layer** list, select the layer for the negative end.
7. Click **OK**.

   The **Set Inductor Parameters** window appears.



8. From the **Name** field, type a name for the inductor.
9. From the **Part Number** field, type the manufacturer's part number.
10. From the **Inductance** field, enter a value in Henries.
11. From the **Parasitic Capacitance** field, enter a value in Farads.
12. From the **Parasitic Resistance** field, enter a value in Ohms.

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13. Click **OK**.

    You have now added and assigned values to your inductor. You can also edit the parameters.

Decoupling Inductors

In SIwave, decoupling inductors can be specified by one of the following methods:

1. RLC equivalent model - an RLC inductor model has the L and R elements connected in series and a C element connected in parallel. You can specify their values as needed.
2. S-parameter data supplied by the different manufacturers of discrete components.

See Adding a Circuit Element from the Component Database.

Adding a Resistor

A *resistor* is an electrical component that limits or regulates the flow of electrical current in an electronic circuit.

To add a resistor:

1. Click **Home**. From the **Circuit Elements** box, click the **Add Resistor** icon ( ).
2. Click the location where you want to place the resistor.
3. Drag the mouse to an appropriate length and direction.
4. Click to finish drawing.

   When you finish drawing the resistor, the **Select layers for resistor terminals** window appears.

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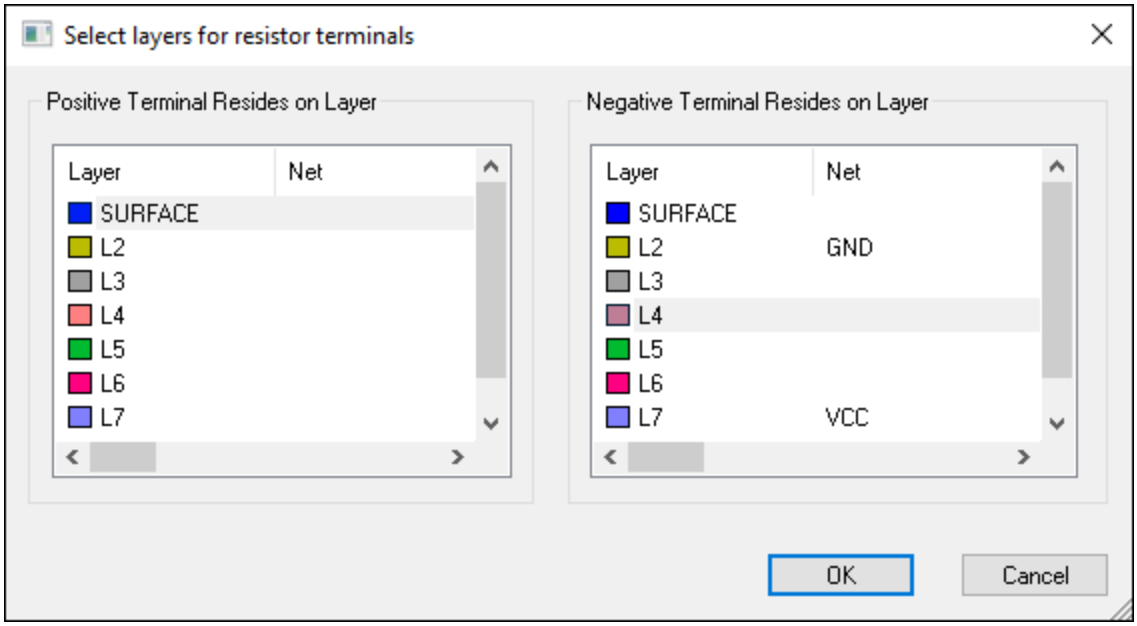
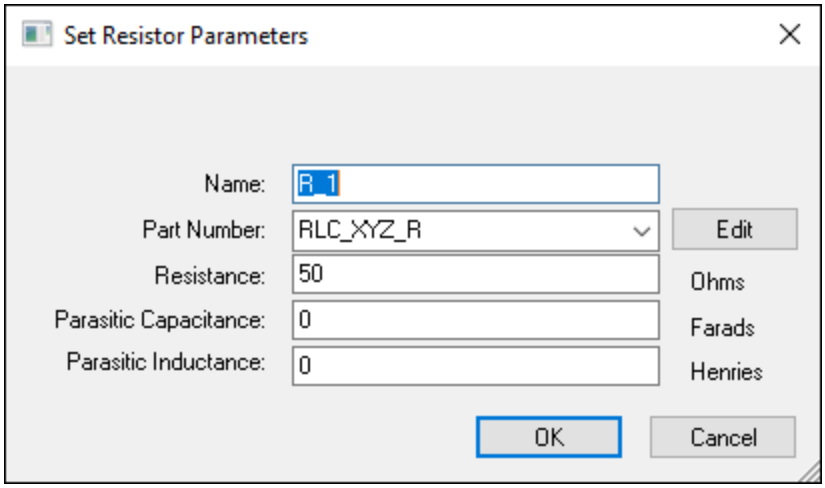


5. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
6. From the **Negative Terminal Resides on Layer** list, select the layer for the negative end.
7. Click **OK**.

   The **Set Resistor Parameters** window appears.



8. From the **Name** field, type a name for the resistor.
9. From the **Part Number** field, type the manufacturer's part number.
10. From the **Resistance** field, enter a value in Ohms.
11. From the **Parasitic Capacitance** field, enter a value in Farads.
12. From the **Parasitic Inductance** field, enter a value in Henries.

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13. Click **OK**.

    You have now assigned values to your resistor. You can also edit the parameters.

Adding a Circuit Element from the Component Database

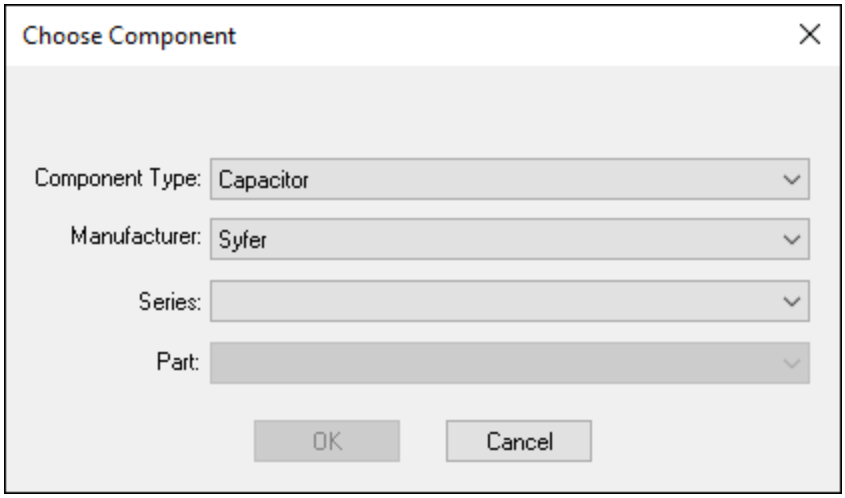
SIwave comes with hundreds of preset components from manufacturers like Murata and TDK.

You can add these components to your design, or map your local components to these global ones.

To add an s-parameter circuit element:

1. Click **Home**. From the **Circuit Elements** box, click the **Add S-Parameter Circuit Element** icon ( ).

   The **Choose Component** window appears.



2. From the **Component Type** drop-down menu, select Capacitor, Inductor, or Resistor.
3. From the **Manufacturer** drop-down menu, select the part manufacturer.
4. Use the **Series** and **Part** drop-down menus to select your part.
5. Click **OK**.
6. From the Modeling workspace, click the location where you want to place the part.
7. Drag the mouse to an appropriate length and direction.
8. Click to finish drawing.

   When you finish drawing the part, the **Select layers for <part type> terminals** window appears.

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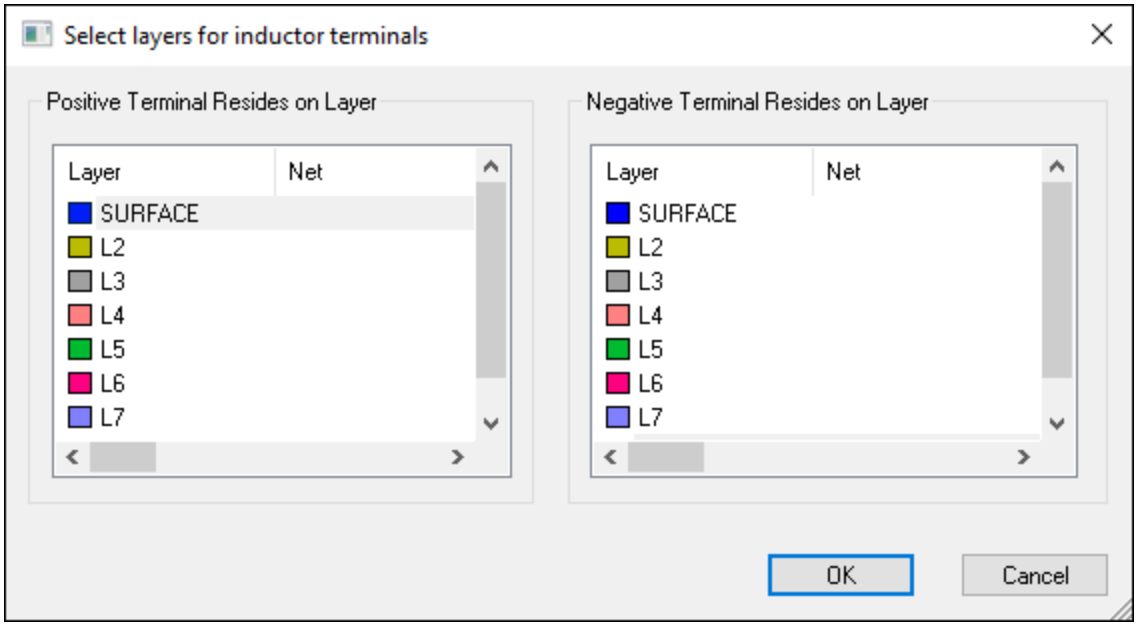

9. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
10. From the **Negative Terminal Resides on Layer** list, select the layer for the negative end.
11. Click **OK**.

Editing the Component Database

You can edit the manufacturer's component database in three ways:

- Importing new components
- Removing user-created or unlocked components
- Mapping components to your local part numbers based on part names and/or component values

To edit the database:

1. Click **Tools** > **SPICE/S-parameter Model Assignment**.

   The **S-parameter Component Management Dialog** window appears. All parts belonging to your project are displayed in the table.

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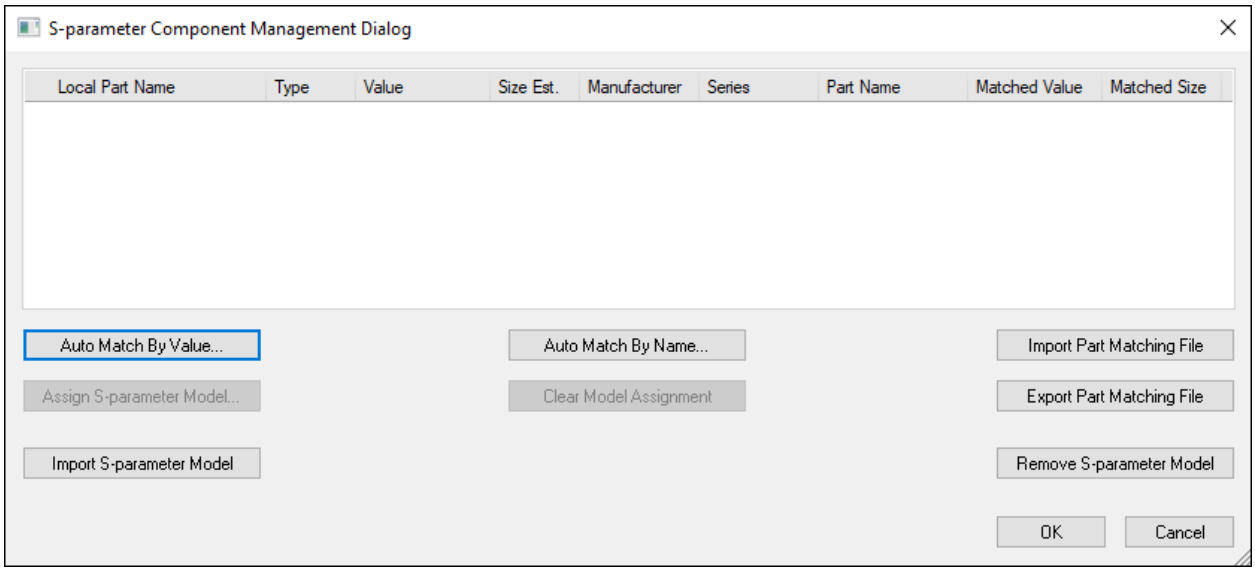

2. There are three ways to map components:
   - Select one or more local part names. Click **Assign S- Parameter Model**. The **Select S-Parameter Component** window appears. Select the filter criteria and click **Filter**. Select the global part from the list, and click **OK**.
   - Click **Part Matching File**. Select an SIwave Partname Mapping File (*.pmap). Click **OK**.

     You can associate the internal part name with manufacturer part name using a file. Specific part names can be converted to a certain manufacturer type. The syntax for specifying parts is:

     ```
     <localpartName> <CompType><ManufName> <seriesName>
     <ManufPartName>
     ```

     > **Note:**
     >
     > Any line beginning with # is treated as a comment.

     Click **Auto Match By Value** or **Auto Match By Name**.

     If you click **Auto Match By Value**, SIwave compares the local and global components based on the part value, and places the local component under the first matching global component (e.g., if the design contains a 1uF capacitor, the **Component Management window** maps that capacitor to the first 1uF capacitor it finds in the **Global Capacitor Database**).

     Auto Match By Value looks for parts whose capacitance/inductance match. If a part is found whose value and name matches the local parts, that part is chosen for mapping; otherwise, the global part with a matching value and the highest available quality will be selected.

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Auto Match By Name tries to match local components with global components based on the part name. For example, if the design contains capacitors whose part name is *08020059A*, the **Component Management window** maps that capacitor to the first capacitor named *08020059A* in the **Global Capacitor Database**.

If the global part name is not found then the part is left unmatched.

3. To unmap local part names, select one or more local part names, click **Clear Model Assignment**.
4. To export a file from the specified mappings: Click **Export Part Matching File** to open the **Save As** window. Browse to the directory where the project will be saved, and enter the name of the file (.**pmap** suffix) for the exported project. Click **Save**.
5. To import new components: Click **Import S-parameter Model**. The **Import S-Parameter Component** window appears. Select the component details, and click **OK**.

> **Note:**
>
> If you frequently encounter permissions errors while importing S-parameter models, change the component library directory to a directory to which you have access. Alternately, you can use Windows to change the SIwave program properties to always run in administrator mode. Consult Microsoft documentation for more information about using administrator mode in your version of Windows.

6. To delete an unlocked global part: click **Remove S-parameter Model**. The **Select S-Parameter Component** window appears. Select the **Manufacturer, Series** and **Part** to delete. Click **OK**.
7. Click **OK**.

   The part name is listed under the selected component. You can manually change the position if required.

Editing Touchstone Port Properties

Touchstone is a standard format for n-port S parameter data. It allows you to import the S-parameters into third-party simulation tools.

To configure the options while exporting a touchstone file:

1. Click **Advanced** > **Touchstone Port Names**.

   The **Touchstone Port Naming Configuration** window appears.

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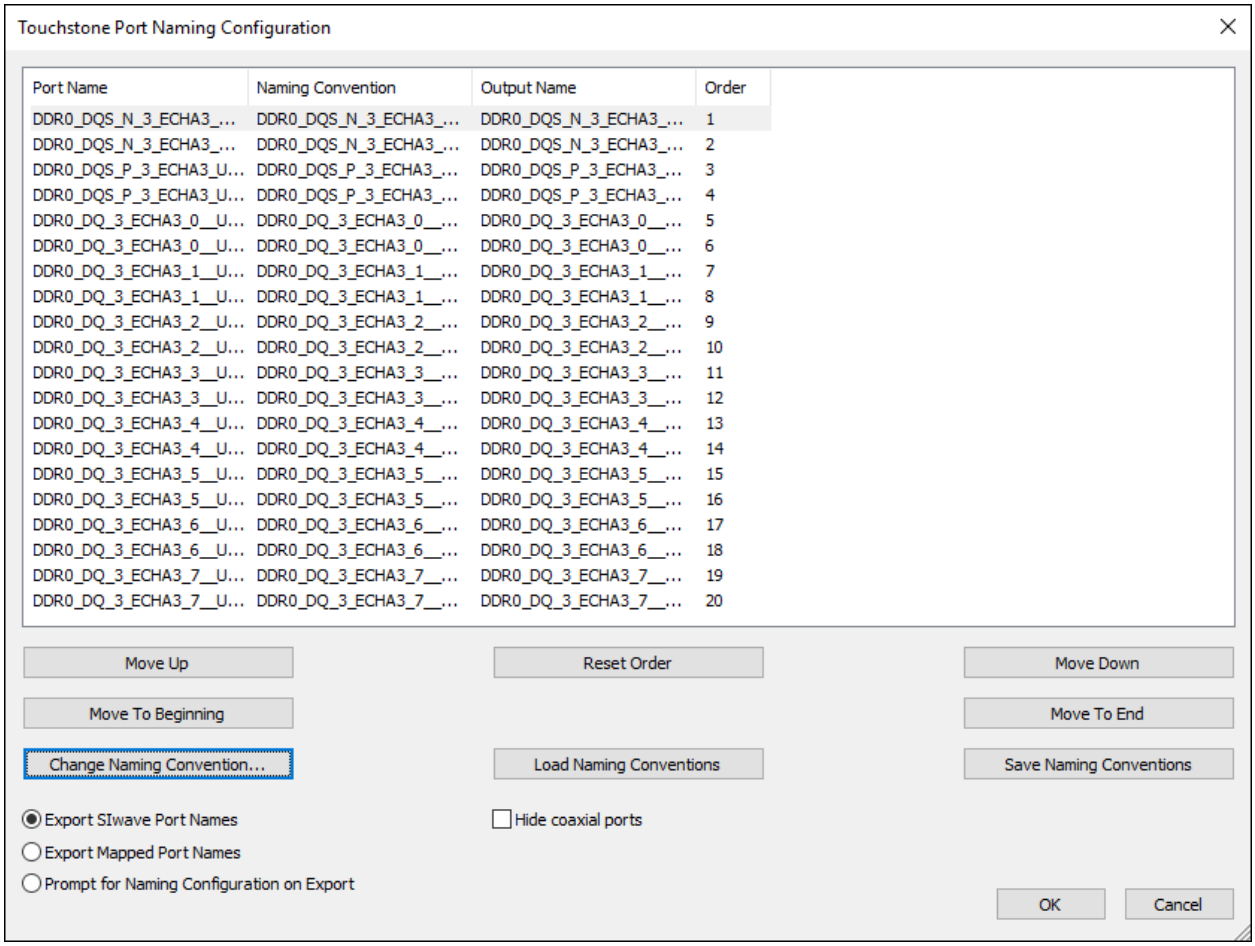

Note:

This window also contains coaxial ports created for HFSS 3D Layout simulations. You can hide these by selecting **Hide coaxial ports**.

The **Move Up**, **Move Down**, **Move to Beginning**, and **Move to End** buttons allow you to move rows in order to change port ordering in the output file. To return to the default settings, click **Reset Order**. The order is used for sorting, but does not necessarily indicate the absolute position of a port in the touchstone file since some ports may not be included in the results (e.g., inactive ports or coaxial ports not included in the simulations). You can also change the Touchstone port order via script.

The radio buttons offer three options for export:

- **Export SIwave Port Names** – the exported file will retain the original SIwave port names.
- **Export Mapped Port Names** – the exported file will use the newly defined names.

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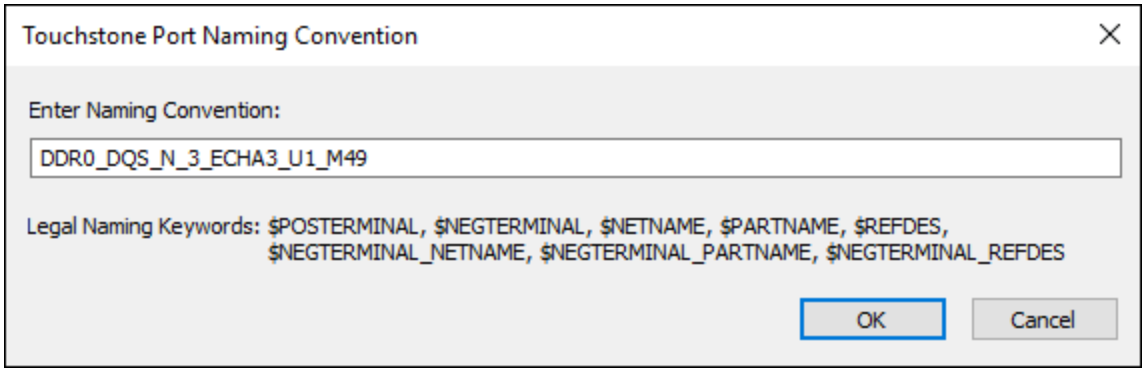
- **Prompt for Naming Configuration on Export** – you will be prompted to choose one of the these options at the time of export.

To change the export naming convention:

1. Select one or more ports and click **Change Naming Convention**.

   The **Touchstone Port Naming Convention** window appears.



2. Click **OK**.
3. If you want to save your naming configuration for later, click **Save Naming Conventions** to save a *.pnc file. You can later click **Load Naming Conventions** to use a saved configuration.

Viewing a Component's Capacitance-Temperature-DC Voltage Bias Plot

Capacitor effectiveness is impacted by operating conditions, particularly the DC bias voltage across their terminals and the ambient temperature at their physical location. SIwave can extract capacitor DC bias values from an associated DC IR simulation and extract capacitor temperatures from an associated Icepak simulation. If such simulation data is not available, SIwave can import and apply a "derating" table, a simple CSV file containing temperatures and DC bias values for capacitors in the design. See SIwave Simulation Options and Computing DC IR Simulations.

For certain components, you can view a surface plot of the model's capacitance as a function of DC bias voltage and temperature:

1. Navigate to the Components workspace.
2. Expand the Components tree to an appropriate Murata-SPICE component.
3. Right-click to open a pop-up menu and select **Examine Component Properties**.

   The **Capacitance-Temperature-DC Voltage Plot** window appears.

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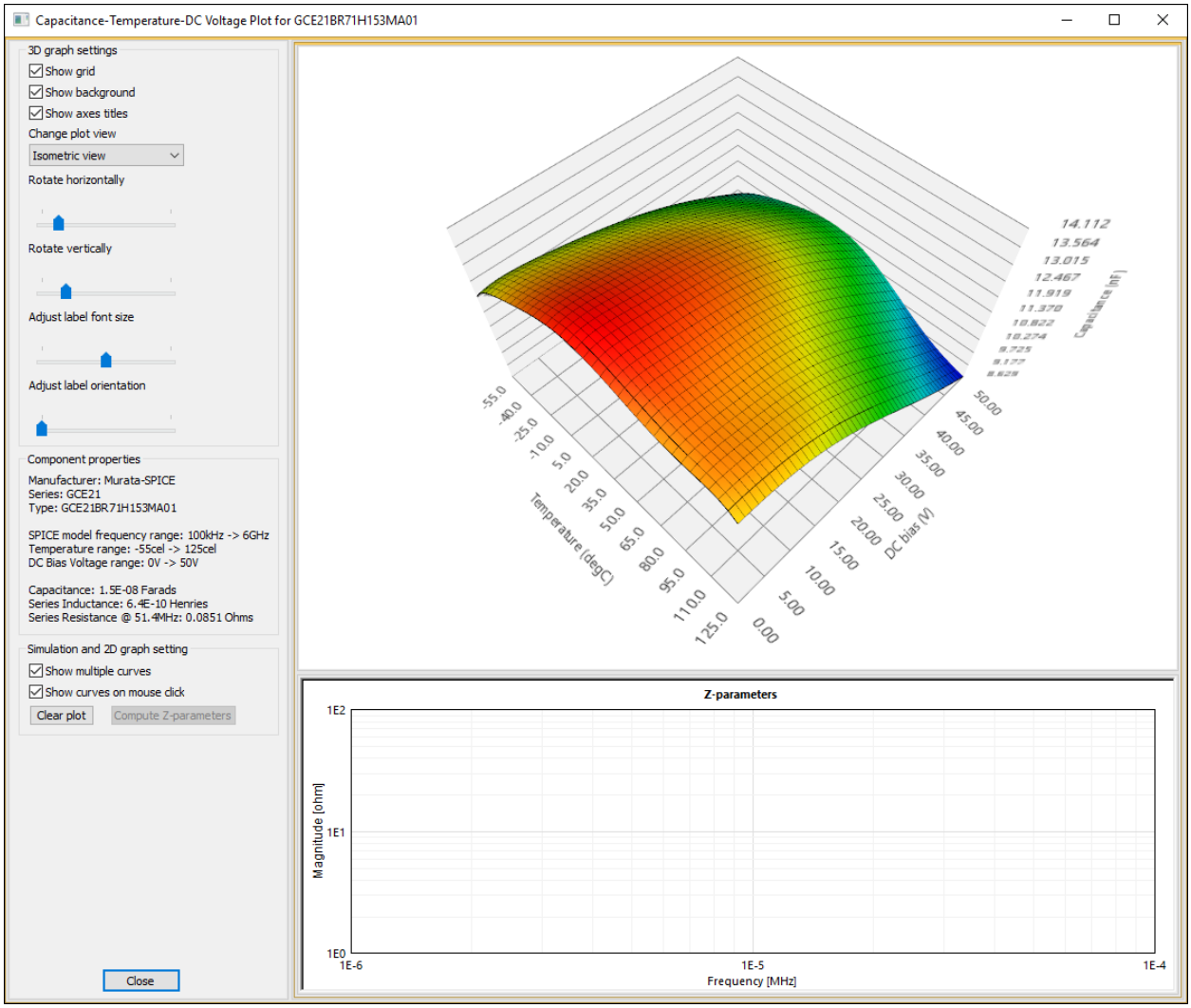

The 3D graph displays Capacitance, Temperature, and DC Voltage Bias. Component properties are displayed to the left.

4. From the **3D Graph Settings** area, use the check boxes and sliders to alter the display. You can change the background, grid, and titles, as well as rotate the graph.
5. Click any point on the 3D graph to view the plotted Z-parameters. If you want to disable this function, uncheck the **Show curves on mouse click** check box.

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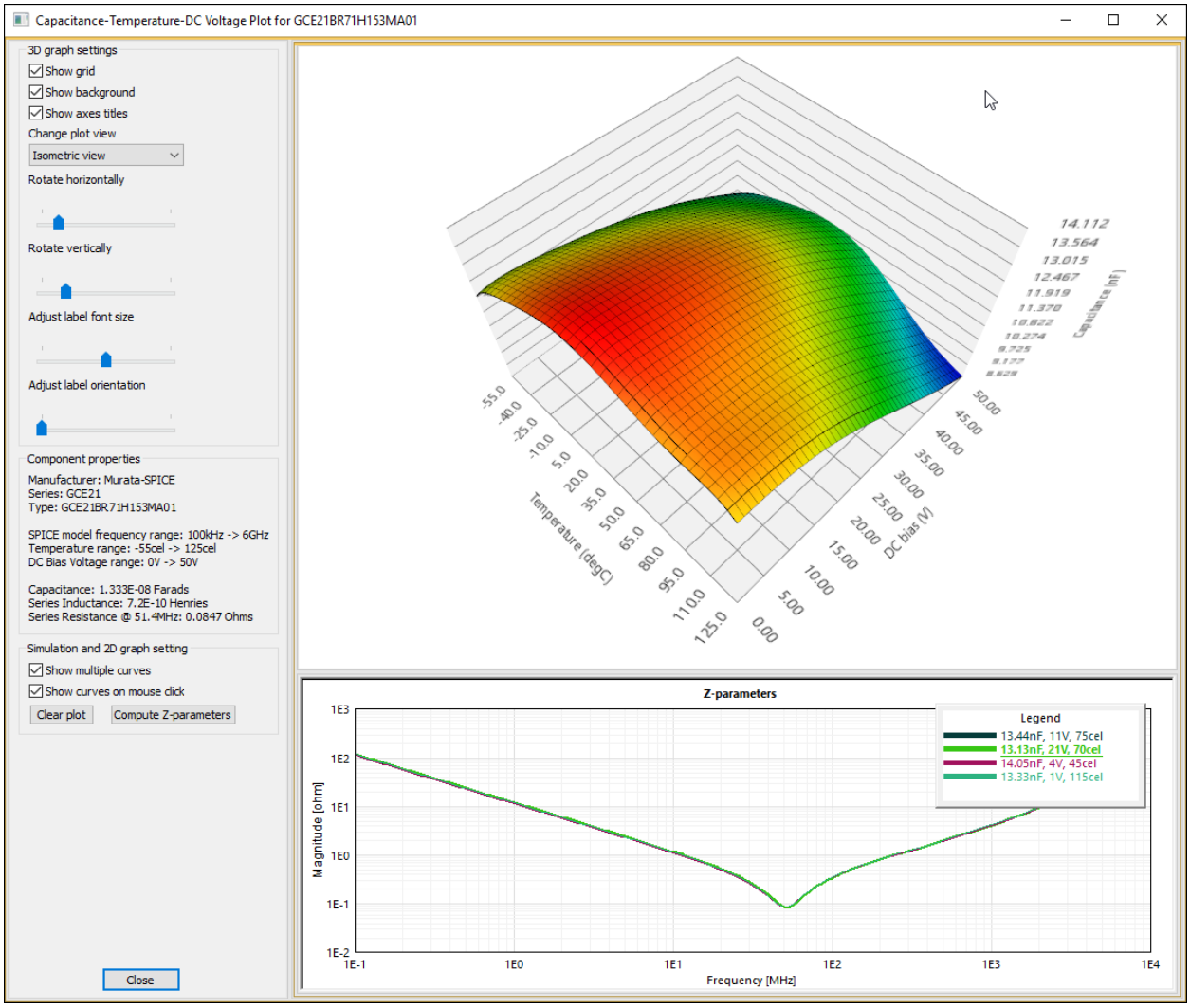

6. From the **Simulation and 3D Graph Setting** area, you can select whether to show multiple curves on the Z-parameter chart and whether curves are automatically selected on mouse click. You can also clear the plot.
7. Click **Close** to exit.

Adding a Voltage Source

To add a voltage source:

1. Click **Home**. From the **Circuit Elements** box, click the **Add Voltage Source** icon ( ).
2. Click the location where you want to place the voltage source.
3. Drag the mouse to an appropriate length and direction.
4. Click to finish drawing.

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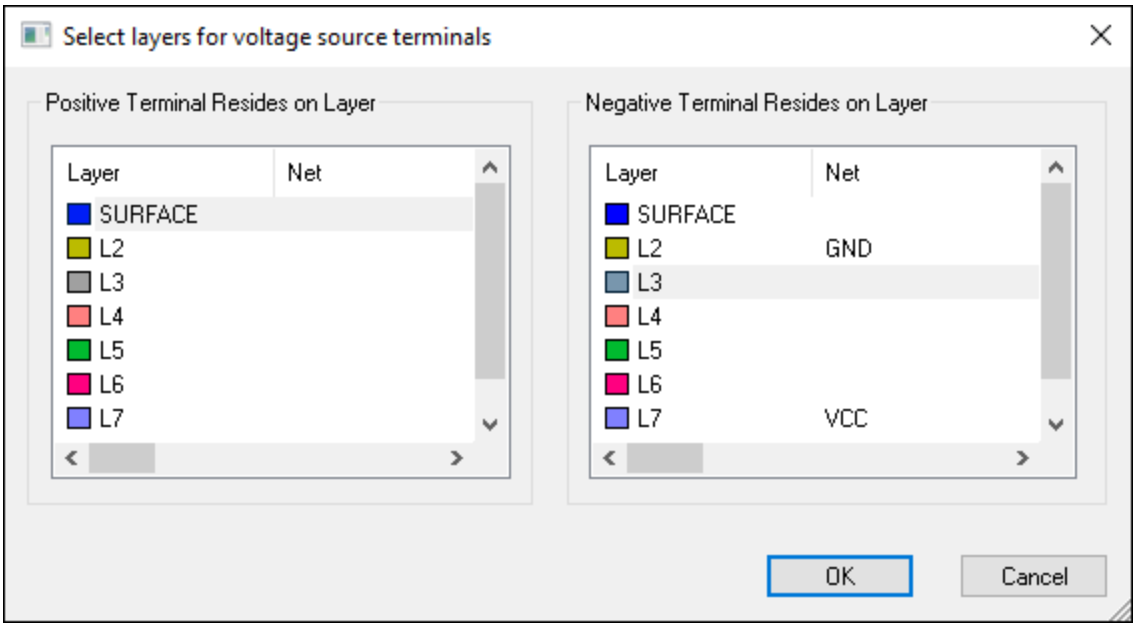
When you finish drawing the voltage source, the **Select layers for voltage source terminals** window appears.



5. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
6. From the **Negative Terminal Resides on Layer** list, select the layer for the negative end.
7. Click **OK**.

   The **Set Voltage Source Properties** window appears.

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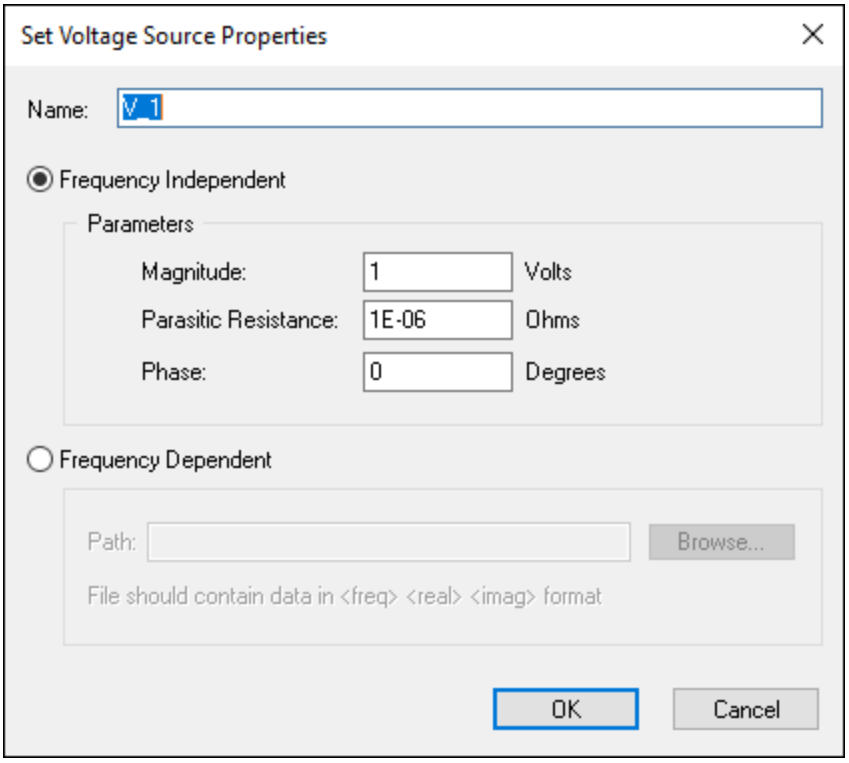

8. From the **Name** field, type a name for the voltage source.
9. Use the radio buttons to specify whether the voltage source is **Frequency Independent** or **Frequency Dependent**.
10. If the source is Frequency Independent, enter its parameters.
11. If the source is Frequency Dependent, select a data file with the format *<freq><real><imag>*.
12. Click **OK**.

You have now added and assigned values to your voltage source. You can also edit the parameters.

Adding a Current Source

To add a current source:

1. Click **Home**. From the **Circuit Elements** box, click the **Add Current Source** icon ( ).
2. Click the location where you want to place the source.
3. Drag the mouse to an appropriate length and direction.
4. Click to finish drawing.

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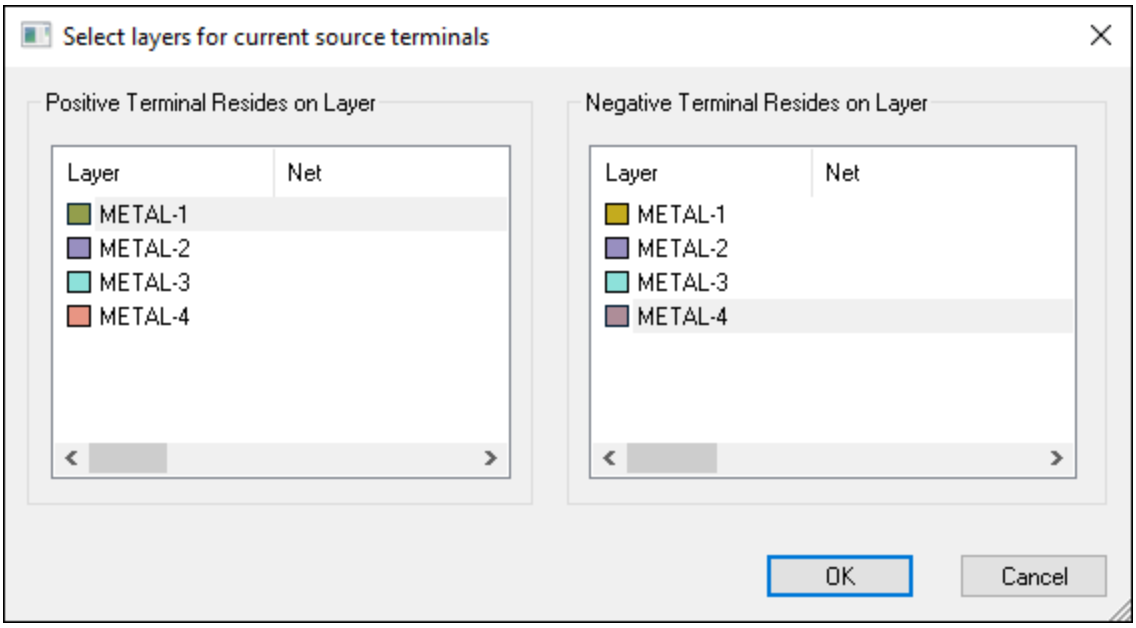
When you finish drawing the voltage source, the **Select layers for current source terminals** window appears.



Current flows from the positive to the negative terminal through the source.

5. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
6. From the **Negative Terminal Resides on Layer** list, select the layer for the negative end.
7. Click **OK**.

   The **Set Current Source Properties** window appears.

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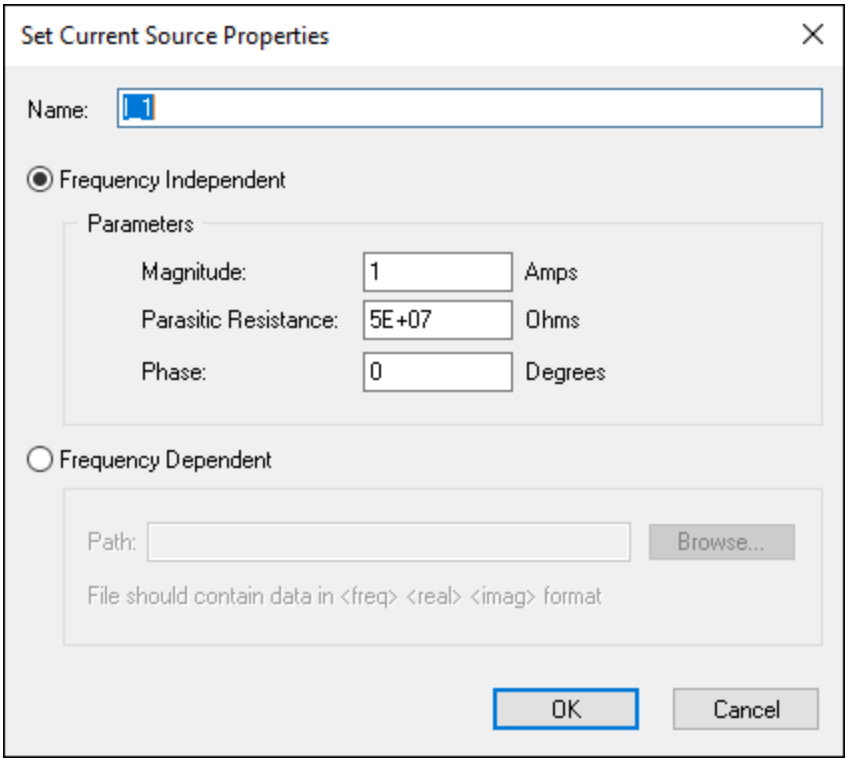

8. From the **Name** field, type a name for the current source.
9. Use the radio buttons to specify whether the voltage source is **Frequency Independent** or **Frequency Dependent**.
10. If the source is Frequency Independent, enter its parameters.
11. If the source is Frequency Dependent, select a data file with the format *<freq><real><imag>*.
12. Click **OK**.

You have now added and assigned values to your current source. You can also edit the parameters.

Adding a Voltage Probe

A probe specifies the two terminals across which a potential difference is computed. This voltage can also be plotted using Ansys Electronics Desktop. The voltage is probed as a function of frequency at a fixed location. A probe is used only for frequency sweep computations.

To add a voltage probe:

1. Click **Home**. From the **Circuit Elements** box, click the **Add Voltage Probe** icon ( ).
2. Click the location where you want to place the probe.
3. Drag the mouse to an appropriate length and direction.

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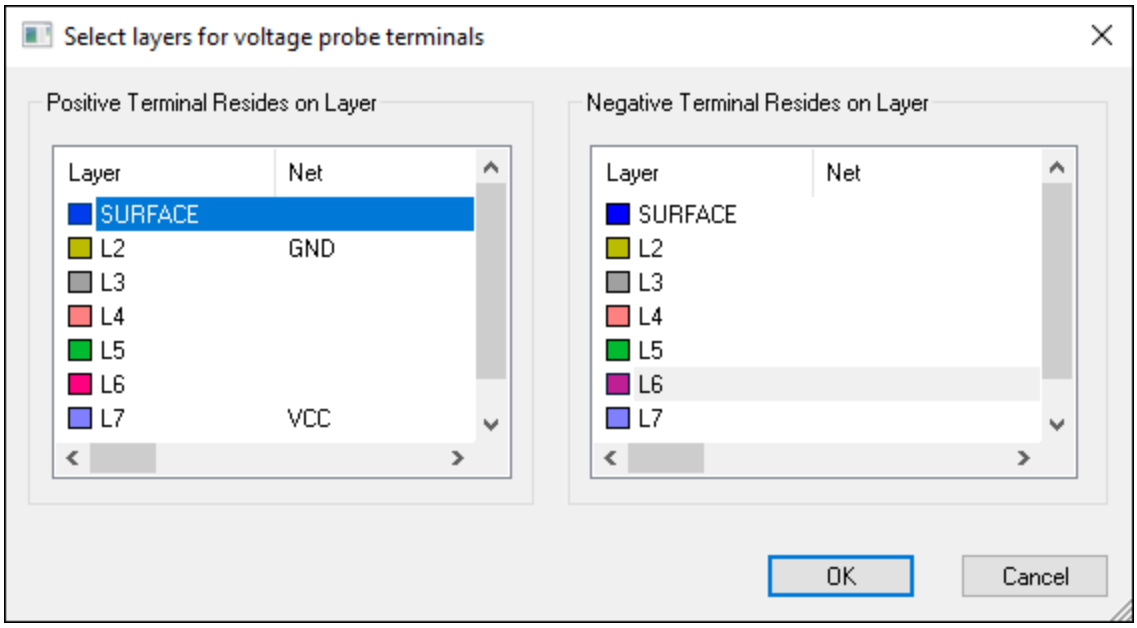
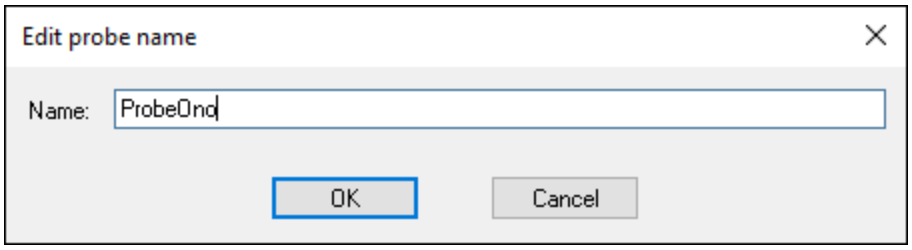
4. Click to finish drawing.

   The **Select layers for voltage probe terminals** window appears.



5. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
6. From the **Negative Terminal Resides of Layer** list, select the layer for the negative end.
7. Click **OK**.

   The **Edit Probe name** window appears.



8. From the **Name** field, enter a name for the probe.
9. Click **OK**.

   You have now added a voltage probe. You can also edit its parameters.

Adding a Terminal

A terminal is generated for every mouse click in the Modeling workspace. If there is a net on the active layer, the terminal will be attached to that net.

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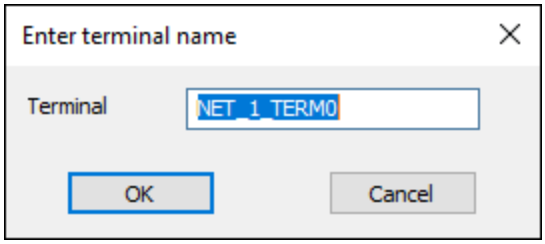
To add a terminal:

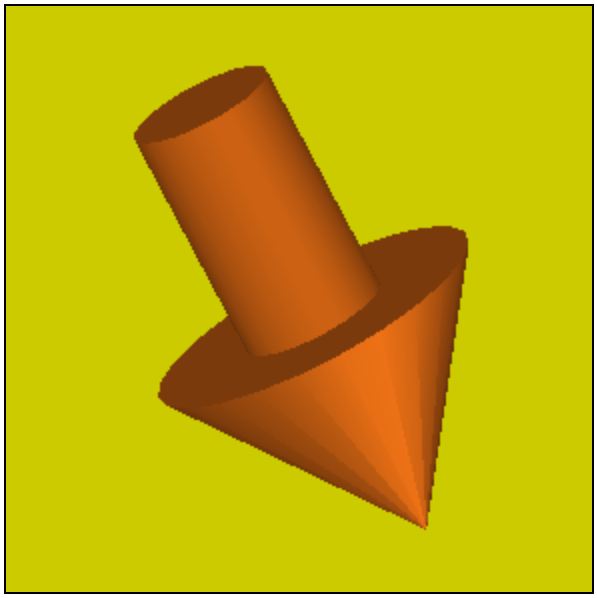
1. Click **Home**. From the **Circuit Elements** box, click the **Add Terminal (Source/Sink)** icon ( ).
2. Click the location where you want to place the terminal.

   The **Enter Terminal Name** window appears.



3. Enter a name and click **OK**.

   The terminal appears in the Modeling workspace, and is listed in the **Components** workspace under **Terminals**.



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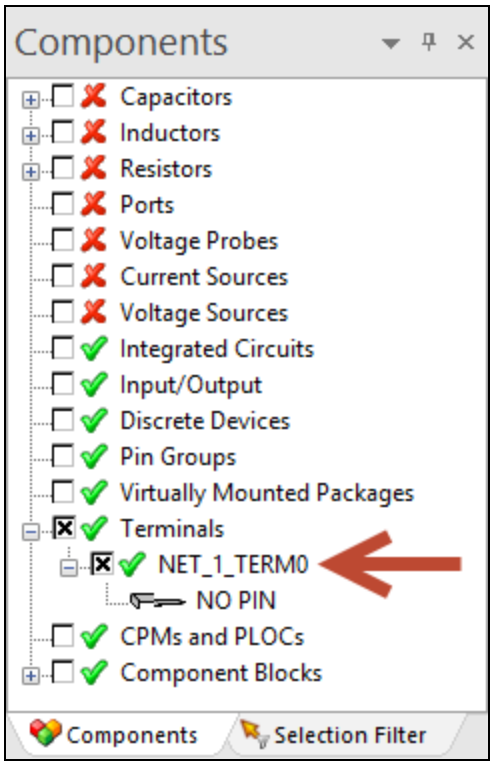

You can modify the terminal's parameters at any time.

Attaching Terminals to Pins and Pin Groups

DC terminals can also be attached to pin groups or pins. Select a pin group or pin, then click the Terminal icon. A DC terminal is generated on each selected item that does not already have an associated terminal of some kind.

Adding a Port

Ports represent the external nodes and specify an external access point in the circuit. When an SIwave design is exported or cosimulated, ports define the externally visible nodes.

A new naming convention uses keywords, such as $PARTNAME and $REFDES, to define ports.

To add a port:

1. Click **Home**. From the **Circuit Elements** box, click the **Add Port** icon ( ).
2. Click the location where you want to place the port.
3. Drag the mouse to an appropriate length and direction.

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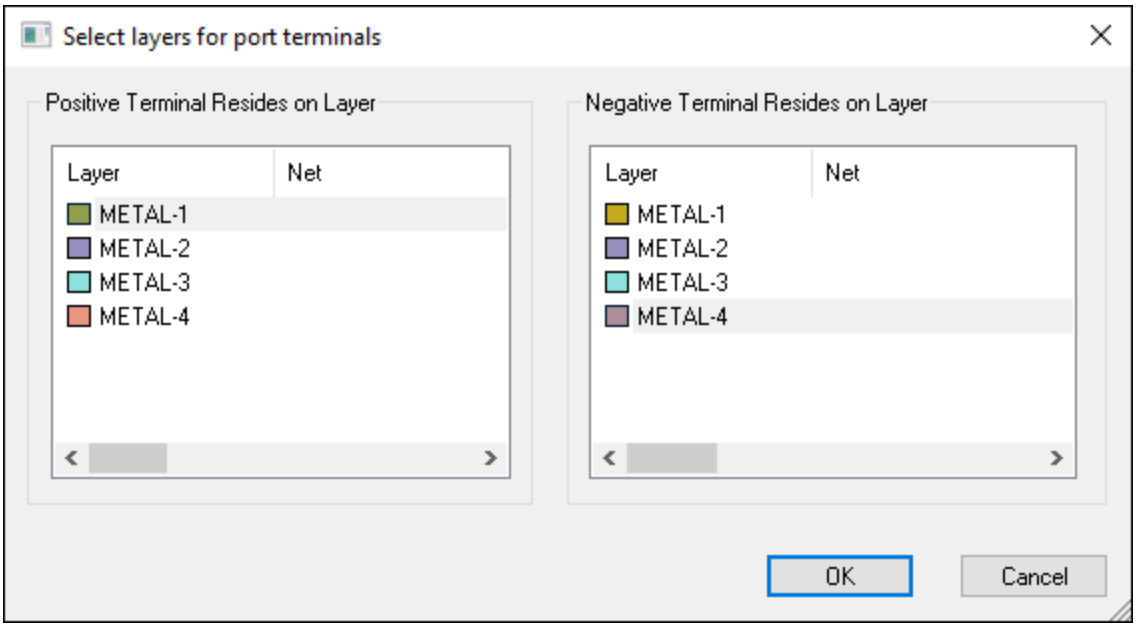
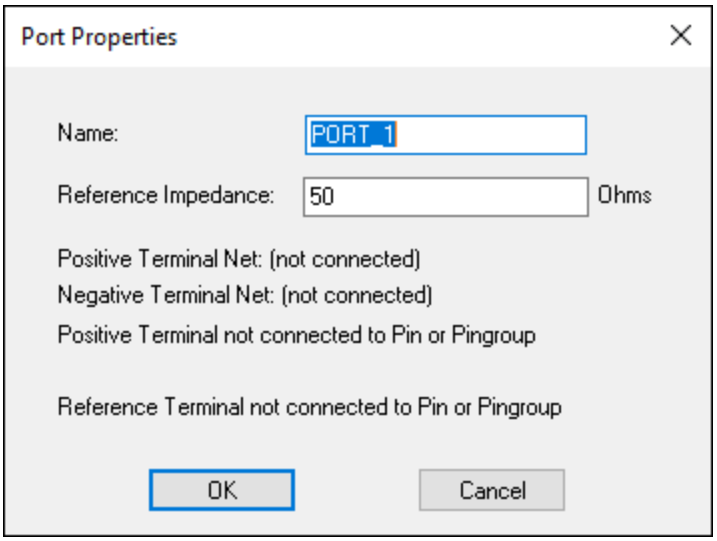
4. Click to finish drawing.

   The **Select layers for port terminals** window appears.



5. From the **Positive Terminal Resides on Layer** list, select the layer for the positive end.
6. From the **Negative Terminal Resides on Layer** list, select the layer for the negative end.
7. Click **OK**.

   The **Port Properties** window appears.



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8. From the **Name** field, type a name for the port.
9. From the **Reference Impedance** field, type a value in Ohms. This value is used as the normalization when calculating s-parameters.
10. Click **OK**.

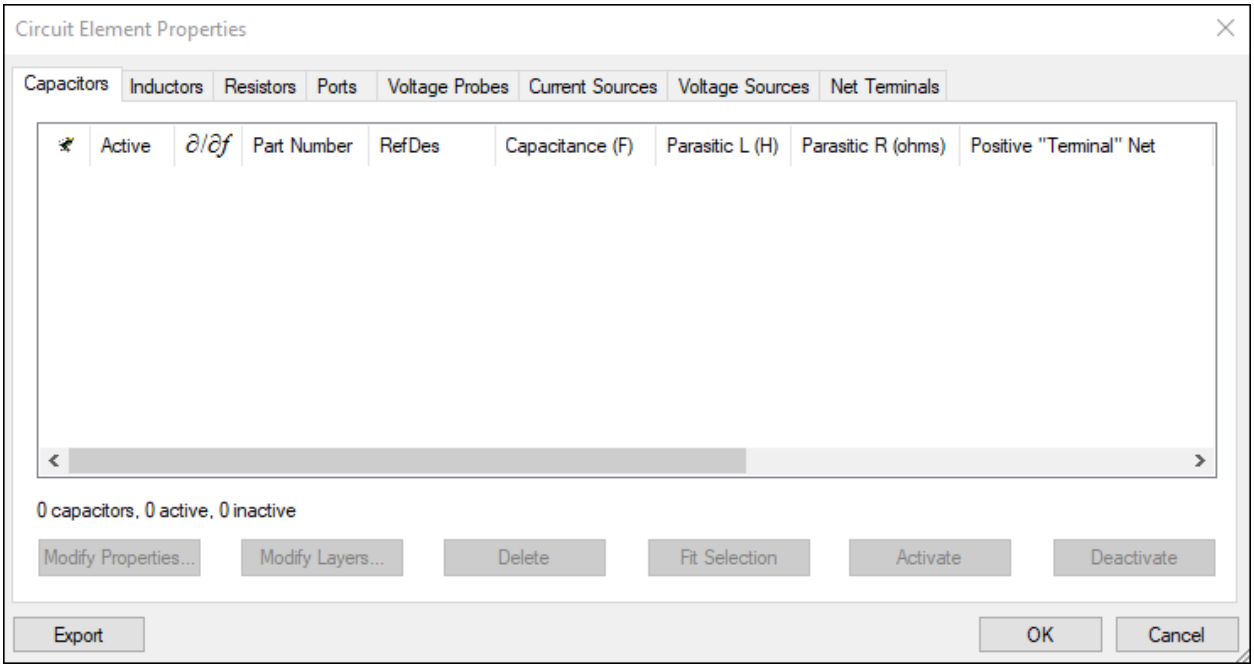
You have now added a port. You can also edit its parameters.

Modifying Circuit Element Parameters

You can edit the parameters of any circuit element. If required, you can also delete an element.

To edit the parameters, click **Home** > **Circuit Element Parameters**.

The **Circuit Element Properties** window appears. This windows lists all circuit elements in your layout: capacitors, inductors, resistors, ports, voltage probes, current sources, voltage sources, and net terminals.



To view a specific type of circuit element, click its tab. All elements of that type are listed, and can be sorted by any column header.

To modify a circuit element, double-click it. Alternatively, select the element and click **Modify Properties**. To modify sensitivity computation for capacitors, inductors and inductors, select the value in the partial derivative ($\partial/\partial f$) column.

The relevant, editable details for that element display.

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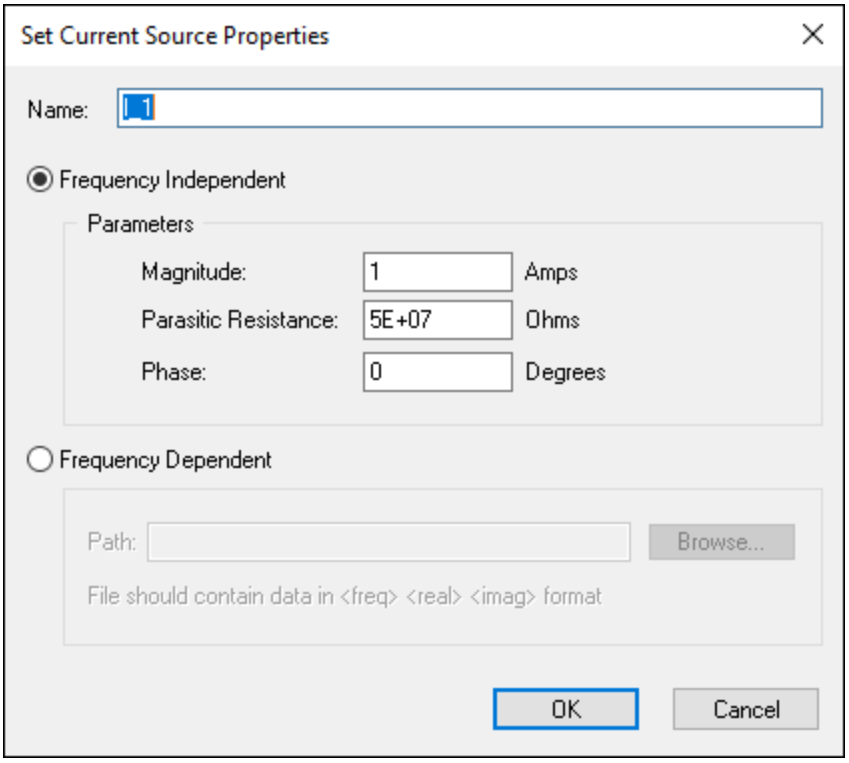
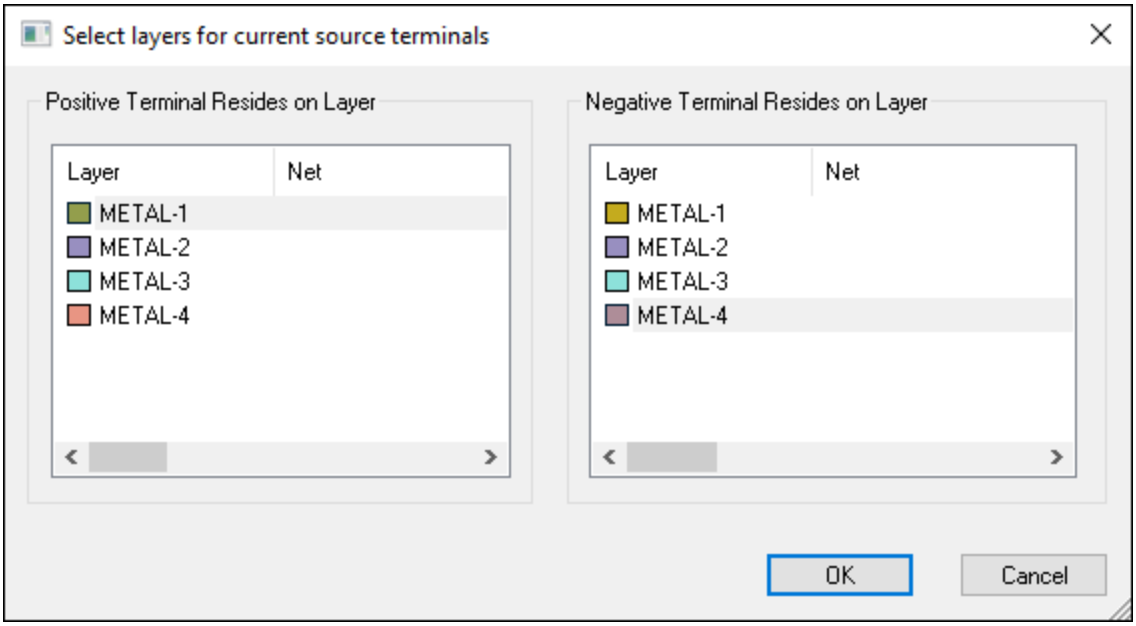


To modify the positive and negative layers of a circuit element, click **Modify Layers**.

The **Select layers for <circuit element>** window opens.



To delete a circuit element, select it and click **Delete**.

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To fit a circuit element in the selected area, click **Fit Selection**.

To activate or deactivate an element, click **Activate** or **Deactivate**.

To export the circuit element table data, click **Export**. You can save the information as a .ce file.

Resizing Circuit Elements

To change the radius of a circuit element:

1. Select the circuit element.
2. Click **View**.
3. Use the **Circuit Element Size** slider to resize the element. You can choose any discrete scaling factor between -11 and +11.

Simplifying Circuit Elements

To speed up the rendering of a very large or complicated layout, SIwave allows you to represent circuit elements as simple line segments. When a circuit element is simplified, only its visual representation is affected, and not the manner in which it is electrically represented by the solver.

To simplify circuit elements:

1. Click **View**.
2. Check the **Simplify Circuit Elements** check box.

The following image shows a Voltage Source before and after being simplified.

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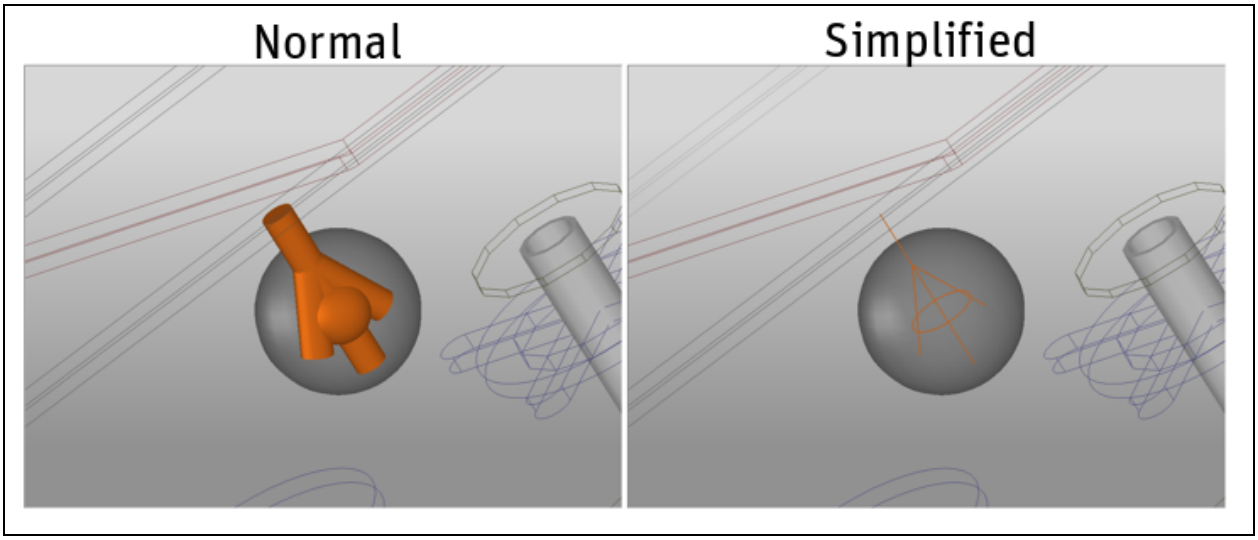

Generating Circuit Elements

To generate circuit elements:

1. Click **Tools** > **Generate Circuit Element on Components**.

   The **Circuit Element Generation Dialog** window appears.

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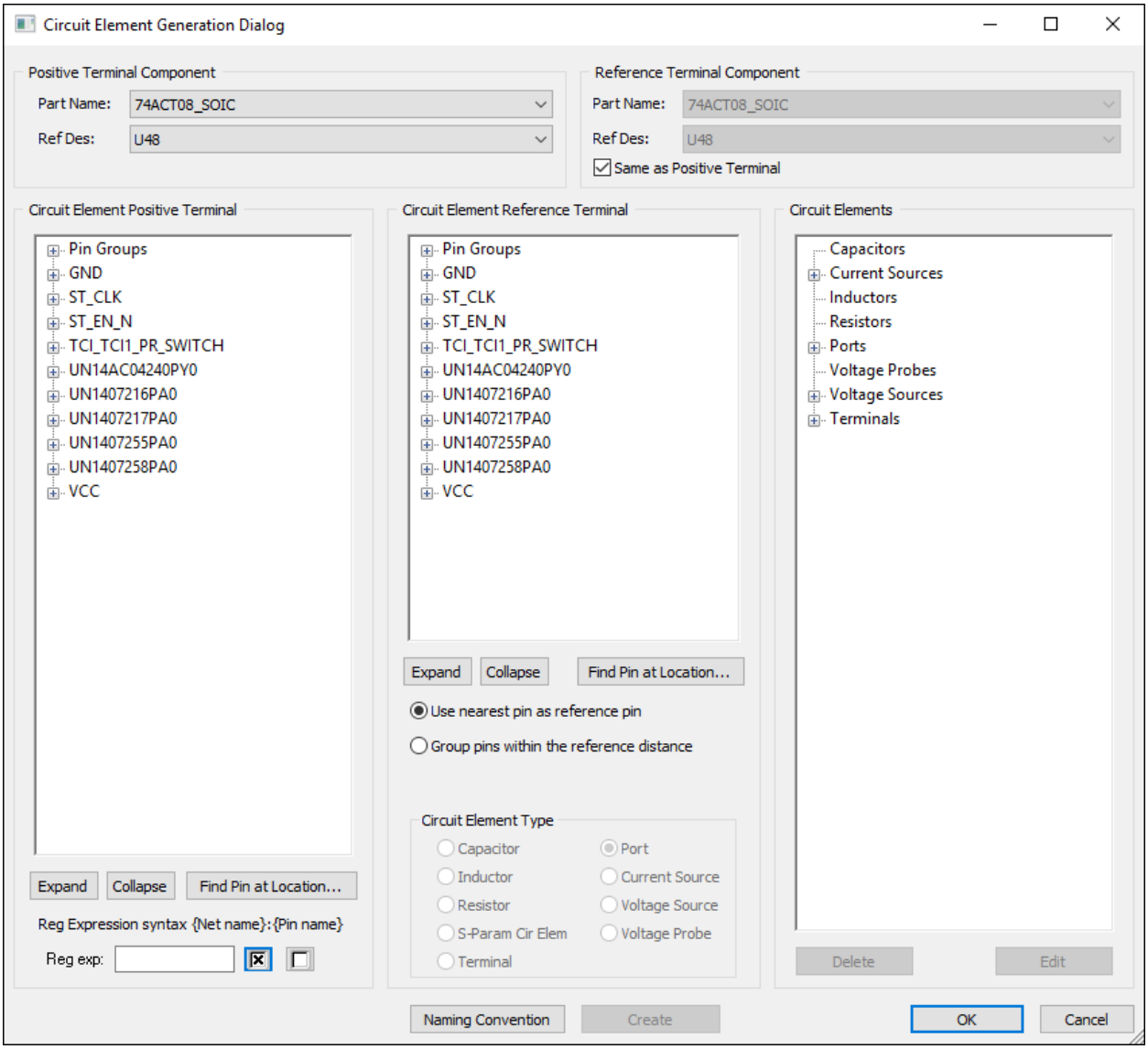

2. From the **Positive Terminal Component** area, use the **Part Name** and **Reference Designator** drop-down menus to select the positive component.
3. From the **Reference Terminal Component** area, use the **Part Name** and **Reference Designator** drop-down menus to the select the reference component. Alternatively, check the **Same as Positive Terminal** check box to select the same component.
4. From the Circuit Element Positive Terminal area, select the pins or nets you want to set as the positive terminals. Expand and collapse items in the tree using the plus signs (+), or use the Expand and Collapse buttons. If you want to find a pin using its X and Y coordinates, click Find Pin at Location. You can also select pins for the positive terminal using regular expressions.

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If you select a net as the positive terminal, a circuit element is created for each pin in the positive terminal.

5. From the **Circuit Element Reference Terminal** area, select the pins you want to set as negative terminals. Expand and collapse items in the tree using the plus signs (+), or use the **Expand** and **Collapse** buttons. If you want to find a pin using its X and Y coordinates, click **Find Pin at Location**.
6. The radio buttons allow you to select distance options. You can **Use nearest pin as reference pin**, or **Group pins within the reference distance**.

   If you select **Group pins within the reference distance**, you must specify distance and units. Distance is assumed to be from pin center to pin center. A pin group will be created with all pins within that distance. A port will be created with this pin group as the negative terminal. If no pins are found within that specified distance, you will be prompted to increase the distance.
7. From the **Circuit Elements** area, select the circuit element you want to generate.
8. From the **Circuit Element Type** area, select the circuit element's type.
9. If you want to specify the naming conventions, click **Naming Convention**. Otherwise, the default for that element's type will apply.
10. Click **Create**.

    The new element is listed in the **Circuit Elements** box. For each selected pin or pin group in the **Circuit Element Positive Terminal**, a port is created. The ports are visible in the Modeling workspace; positive terminals are displayed in red, while negative terminals are displayed in green.

To delete a generated circuit element:

1. From the **Circuit Elements** area, select the element you want to delete.
2. Click **Delete Selection**.

To modify a generated circuit element:

1. From the **Circuit Elements** area, select the element you want to modify.
2. Click **Edit**.

   A properties window appears with options specific to the circuit element type.

Using Regular Expressions to Select Pins

The syntax for regular expressions is *net name:pin*.

To use regular expressions, enter the name of the nets and pins you want to select in the **Reg exp** field, using wild cards when appropriate.

The following regular expressions are supported:

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*	Matches any sequence of characters.
?	Matches any character.

These match a text pattern and use special constructions to represent strings or single characters. Examples:

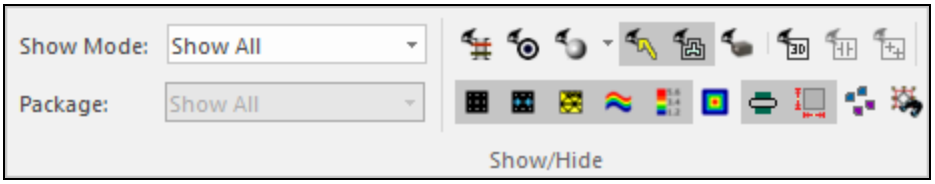
net* selects all pins in nets that start with "net"

net*:1* selects pins with names starting in "1" within nets starting with "net"

A*:3? selects pins 31, 32, 33, 34,... in nets A1, ACC, AGND, AGND2,...

Viewing Circuit Elements

Your design can contain a number of circuit elements (capacitors, inductors, resistors, etc.). By default, all components are visible. You can choose to make all elements invisible, make all elements of a certain type invisible, or make an individual element invisible. Most of this is done in the **Show/Hide** area on the **View** tab.



Use the **Show Mode** drop-down menu to show all objects or only those currently selected.

Each icon on the right side of the **Show/Hide** area toggles the visibility of a certain element. Hover over the icons to see their associated actions. In order (from left to right, top to bottom), the icons are:

- View Non-Functional Pads
- View Antipads
- View Solderballs
- View Bondwires
- View Region Extents
- View Icepak Cabinet
- View 3D Regions
- View Capacitor Regions
- View Equipotential Regions
- Toggle Grid
- Toggle Grid Snap
- Display Mesh

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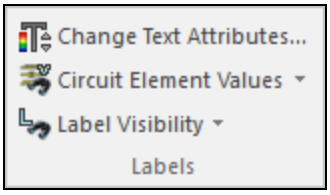
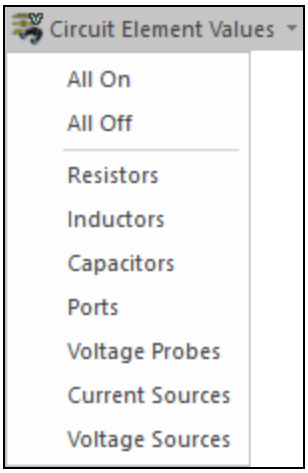
- Display Surface Plot
- Display Color Scale
- Temperature Plots
- View Dielectric Layers
- View Dimension Marker
- View Coupled Structures
- View Pin Groups

Also on the **View** tab, the **Labels** section allows you to toggle visibility of labels and circuit element values.



Use the **Circuit Element Values** drop-down menu to select the elements for which you would like to view values. Select **All On** to apply values to all circuit elements, and **All Off** to remove values from all circuit elements.



Use the **Label Visibility** drop-down menu to select the elements for which you would like to view labels. Select **All On** to apply labels to all circuit elements, and **All Off** to remove labels from all circuit elements.

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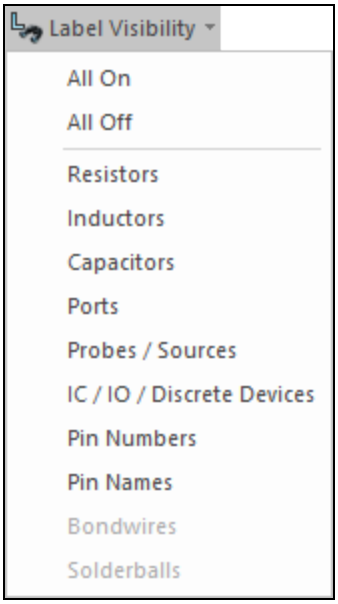

Grouping Pins

You can create pin groups for various components. During analysis, grouped pins are treated as if they are electrically connected. You can also connect circuit elements (ports, sources, RLCs) to any generated pin groups. Consult the Technical Notes for a brief walkthrough.

Pin groups can be created multiple ways:

- From the Tools tab
- From the Modeling workspace
- From the CPA setup window (Hotspot Die Pin Group Generation)

Grouping Pins from the Tools Tab

To create a pin group:

1. From **Tools**, select **Create/Manage Pin Groups** to open the **Create/Manage Pin Groups**>window.

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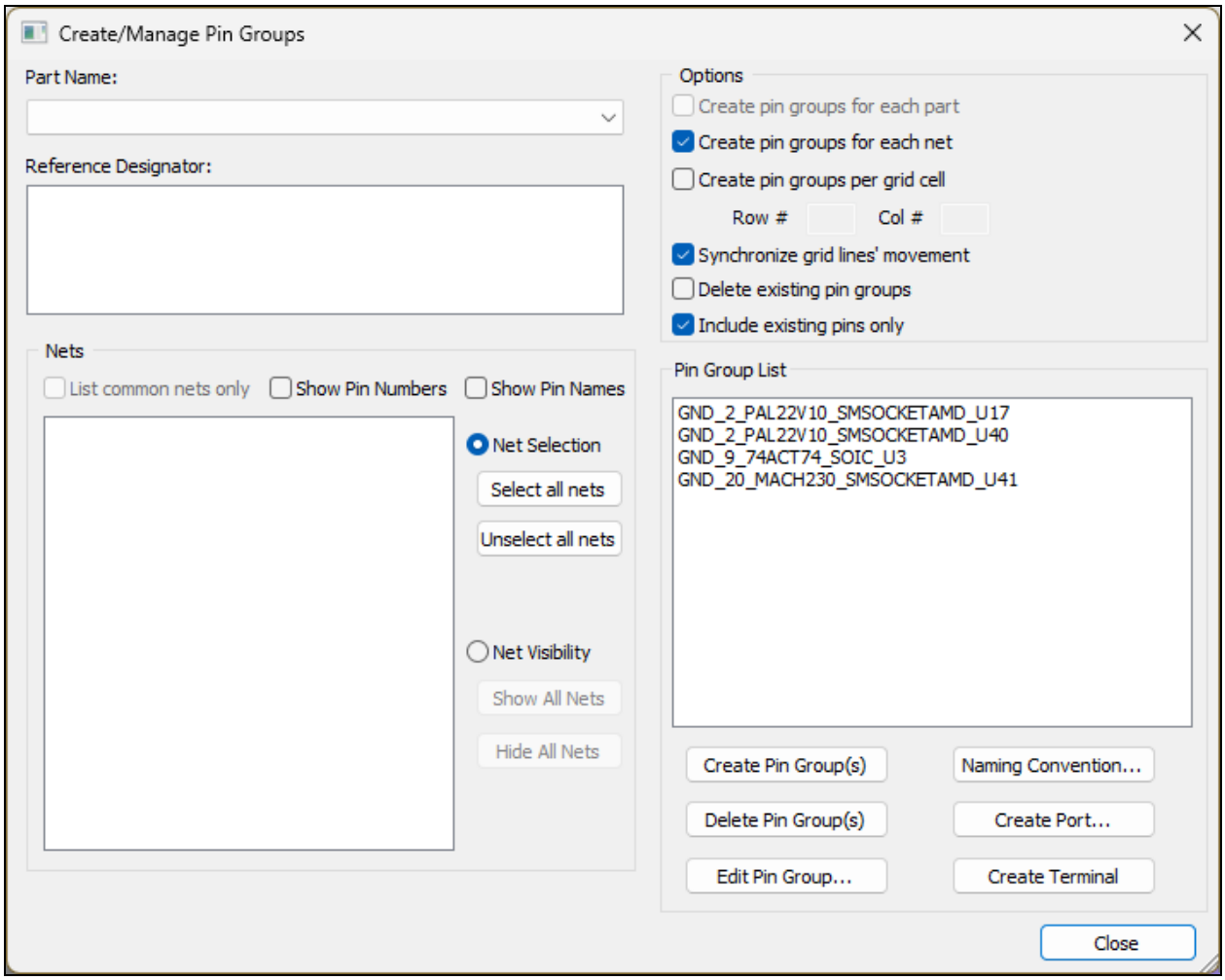

2. From the **Part Name** drop-down menu, select a part. To display all pin groups in the design, select **DON'T KNOW**.
3. The **Reference Designator** area will populate. Make your appropriate selection(s).
4. From the **Nets** area, use the radio buttons to select either **Net Selection** or **Net Visibility**.
   - To select all the nets, click **Net Selection** and then click **Select all nets**. The pins associated with the selected nets will be grayed.
   - To show all the nets in the Modeling workspace, click **Net Visibility** and then click **Show All Nets**.
5. Also in the **Nets** area, use the check boxes to narrow your search by listing common nets only, or decide whether to show pin numbers and names.
6. Select the Nets you want to include in the pin group.
7. From the **Options** area, select the settings for your pin group:
   a. **Create pin groups for each part** – Use this option if the selected part contains multiple reference designators and you want to create identical pin groups for each of them.

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b. **Create pin groups for each net** – Use this option if multiple nets are selected and you want to generate multiple pin groups (one for each selected net).
c. **Create pin groups per grid cell** – Use this option if you know the grid location where you'd like to create the pin group. Enter the row and column number to update the Modeling workspace.
d. **Synchronize grid lines' movement** – Use this option to synchronize the movement of grid lines.
e. **Delete existing pin groups** – Use this option to delete existing pin groups when creating a new group. Existing groups display in the **Pin Group List**.
f. **Include existing pins only** – Use this option to only include existing pins in the selection when creating or editing pin groups.

8. Optionally, click **Naming Convention** to change the naming convention for circuit elements.
9. Optionally, use the **Create Port** and **Create Terminal** buttons to create ports and terminals for inclusion in your group.
10. Click **Create Pin Group(s)**.

    The created groups display in the **Pin Group List**.

    To delete a pin group:

    a. From the **Pin Groups** area, select the group you want to delete.
    b. Click **Delete Pin Group(s)**.

    To edit a pin group:

    a. From the **Pin Groups** area, select the group you want to edit.
    b. Click **Edit Pin Group** to open the **Pin Group Editor** window. From the **Pin Group**

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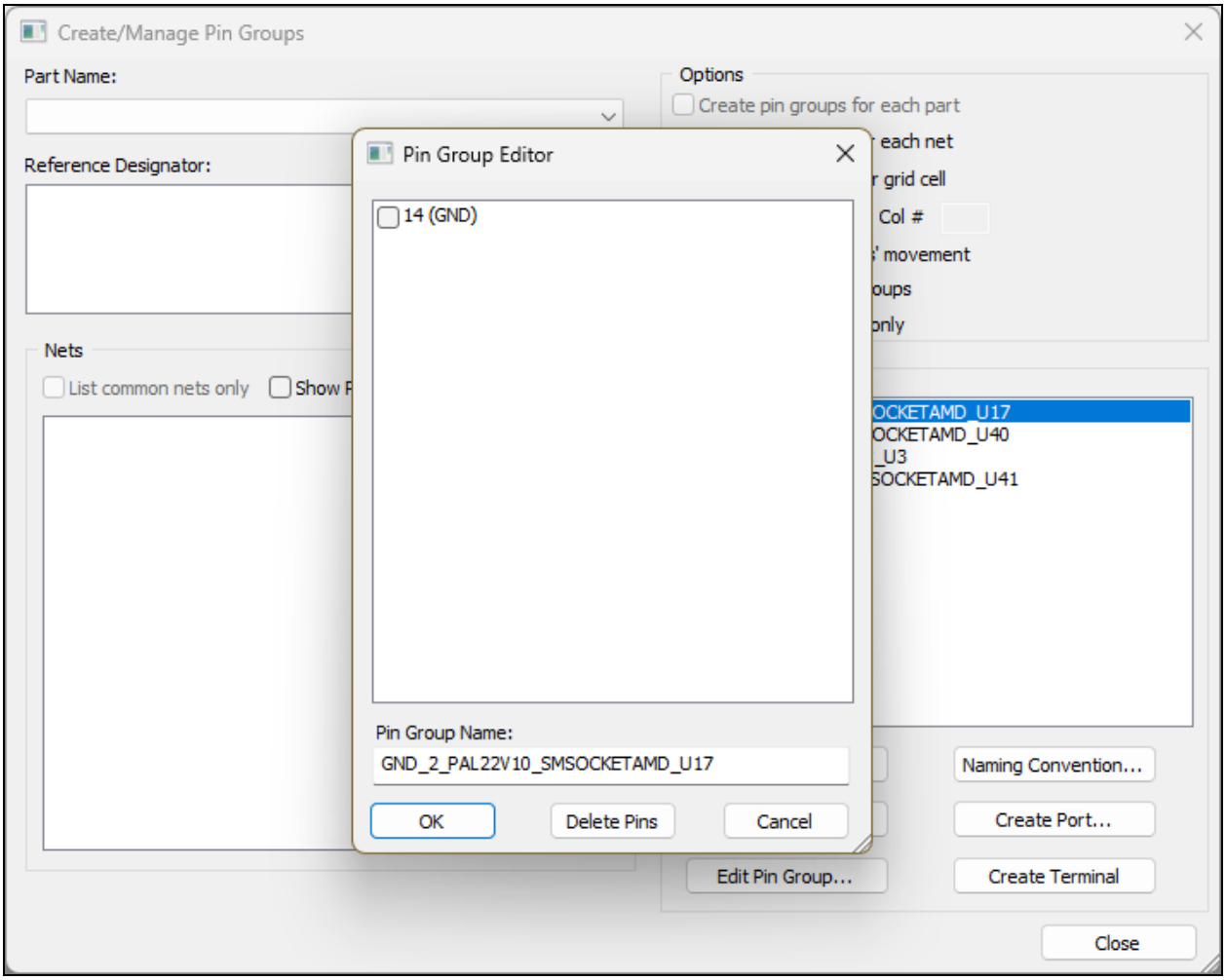
Editor window, rename the group or delete pins.



Grouping Pins Quickly in the Modeling Workspace

As an alternative to the preceding instructions you can group pins without opening the Create/Manage Pin Groups window.

To do this:

1. **Ctrl+click** to select pins in the Modeling workspace.

   You can also select pads and vias.

   If a subset of the selection is already part of an existing single component, SIwave will add selected pads/vias that do not have pin assignments to this existing component.

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If a subset of the selection belongs to more than one component, pads/vias without pin assignments will be added to the parent component of the first selected pin and a pin group spanning these different components will be created.

If none of the pads and vias have pin assignments, a new component is created to act as the parent for the new pins.

> **Important:**
>
> A pin group containing pins from multiple components will not work in CPA.

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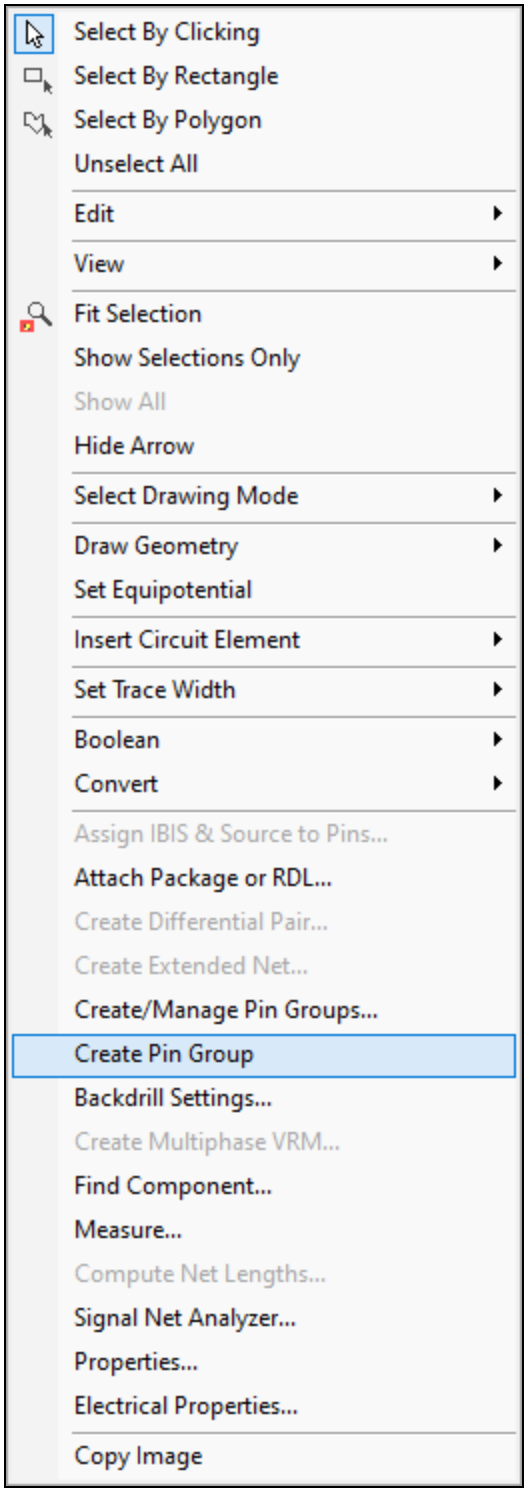
2. Right-click to open the options menu.



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3. Click **Create Pin Group**.

   The pins are grouped, and the pin group properties display in the Properties workspace.

> **Note:**
>
> - Pin groups on the die side are treated as sources while pin groups on the ball side are sinks. If you only have pin groups defined on the ball side, the resulting matrix will contain individual terminals for the die side sources.
> - Pin groups should be defined on signal nets. Pin groups created on nets that are defined as power/ground are not included in the resulting matrix.

Grouping Pins from CPA (Smart Pin Groups)

For CPA RLGC extraction, you can generate pin groups based on hotspots. This is more efficient than extracting every pin.

To generate pin groups automatically:

1. Click **Simulation**.
2. From the **CPA** area, click **Compute RLGC** to open the **Launch CPA** window.
3. Select **CPA Channel Setup**.

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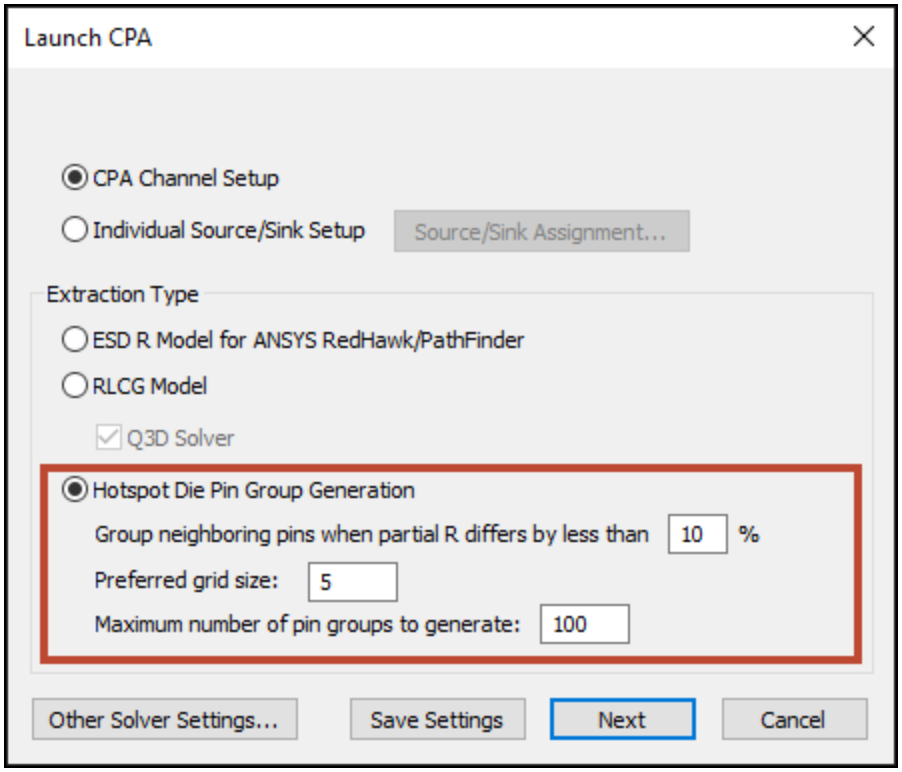
4. From the **Extraction Type** area, select **Hotspot Die Pin Group Generation**.



5. Enter a percentage value to group neighboring pins when their partial resistance differs by less than that percentage from the nominal value. The default is 10%. Pins that fall outside this range are put into single pin groups (extracted individually).
6. Enter a **Preferred grid size**. The default is 5. Pins with partial resistance within the specified range are further put into a grid of 5x5 (default), and are grouped by net.
7. Enter a value for the maximum number of pin groups to generate.

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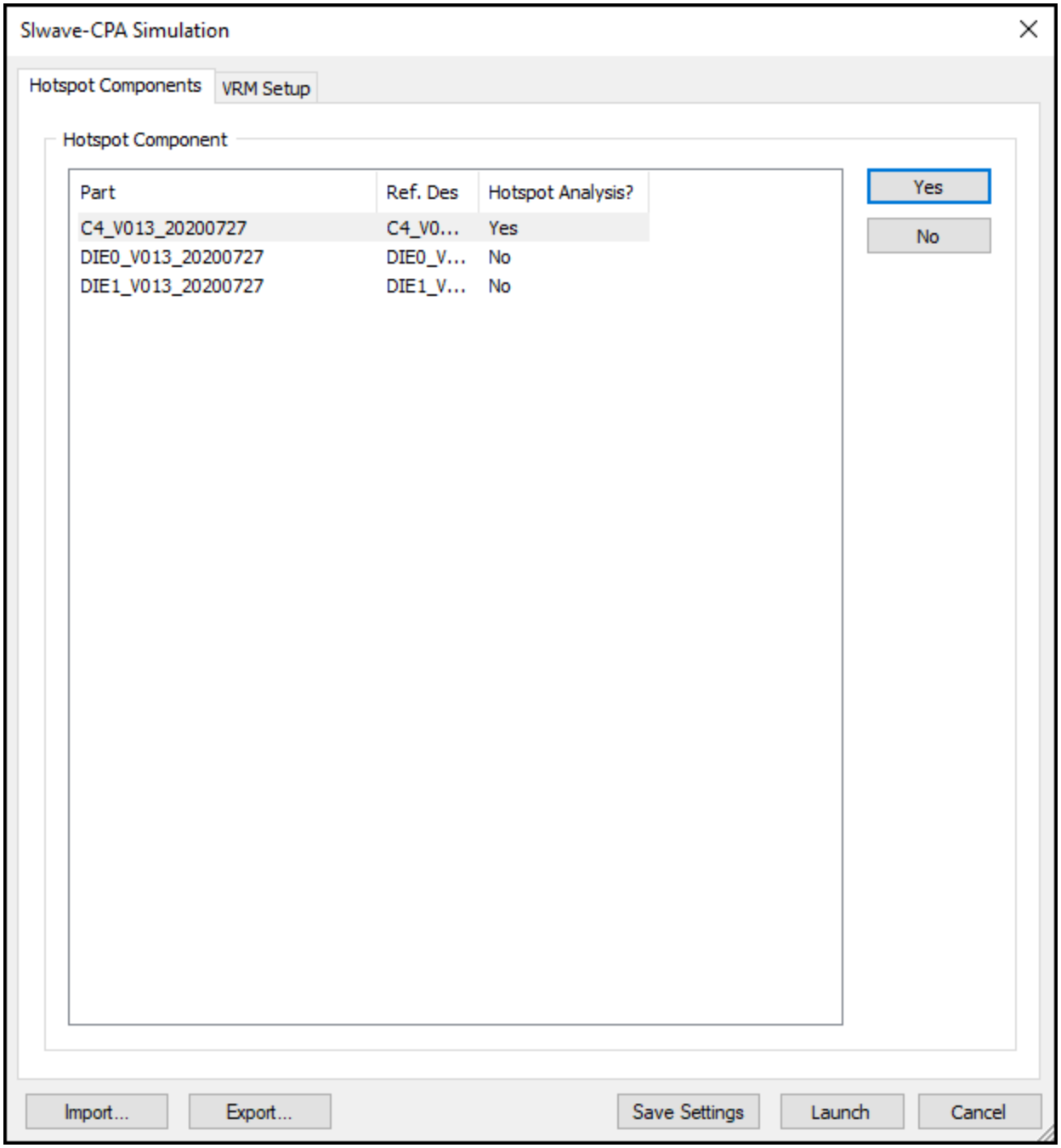
8. Click **Next** to open the **SIwave-CPA Simulation** window, with Hotspot-specific options.



9. Select parts and use the **Yes** and **No** buttons to assign whether or not they will be part of the Hotspot grouping. Parts are set to "No" by default.
10. Select the **VRM Options** tab and choose options as appropriate.
11. Click **OK** and the **Messages** window updates with a progress bar. When the progress bar is finished, the pin groups are created and listed in the **Components** window. Pin groups

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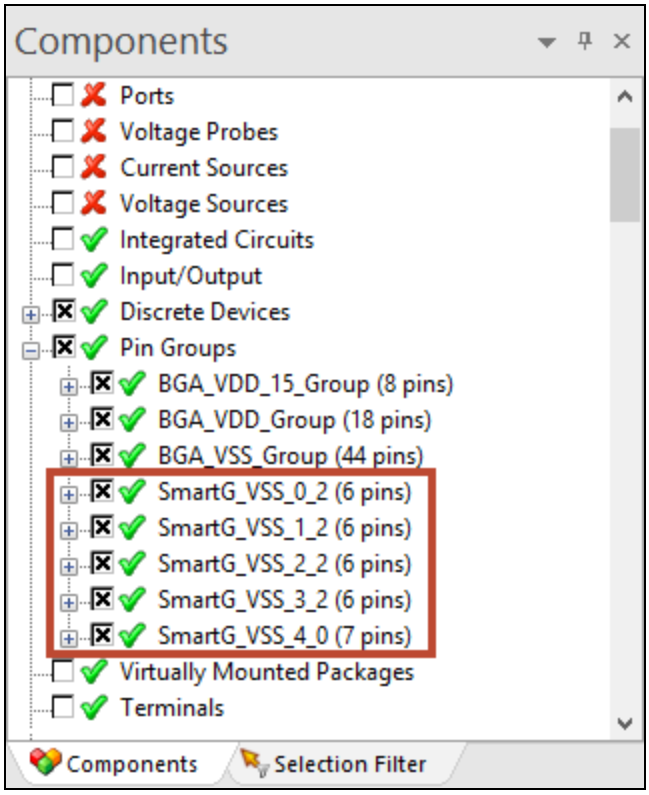
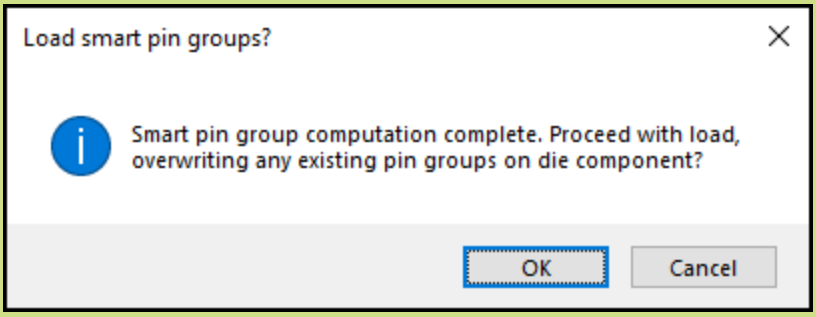
created using smart grouping begin with the prefix 'SmartG'.



Note:

If there are existing pin groups on a die component, SIwave will prompt you to determine whether to overwrite the existing groups.



Click **OK** to overwrite the pin groups. Click **Cancel** to abort.

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Traces

Traces are separate conducting lines that make up an important part of the PCB layout.

- Drawing a trace
- Editing an existing trace
- Modifying the width of the trace
- Converting an existing trace into a plane
- Converting an existing plane into a trace
- Cleaning up overlapping traces
- Modifying the cross-section of all traces on a given layer
- W-element analysis
- Calculating trace width/pitch

Drawing a Trace

To draw a trace:

1. Click **Home**. From the **Draw Geometry** box, click the **Draw Trace** icon (┐).
2. Click the point where you want to start the trace.
3. Drag the cursor to an appropriate length and direction of the trace.
4. Click to end each line.
5. Double-click to end the trace.

To view additional options, right-click while drawing a trace.

A menu appears.

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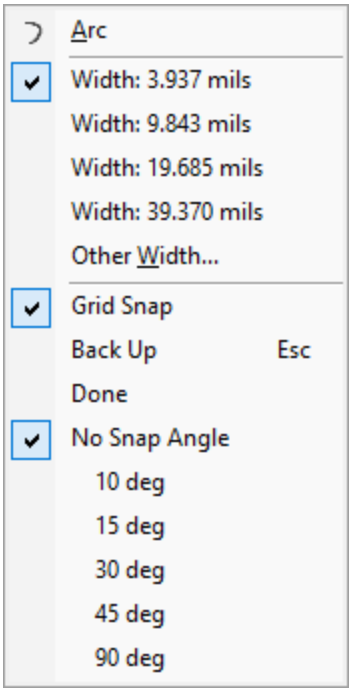

This menu allows you to select an arc and also modify the trace width.

To create an arc:

1. Select **Arc**.
2. Choose the location of the arc center and click it.
3. Choose the location of the arc's end point and click it.
4. Finish drawing the trace.

Editing Traces

Complete these steps to edit an existing trace.

1. Click **Advanced** > **Trace/Bondwire**. to open the **Edit Trace** window.

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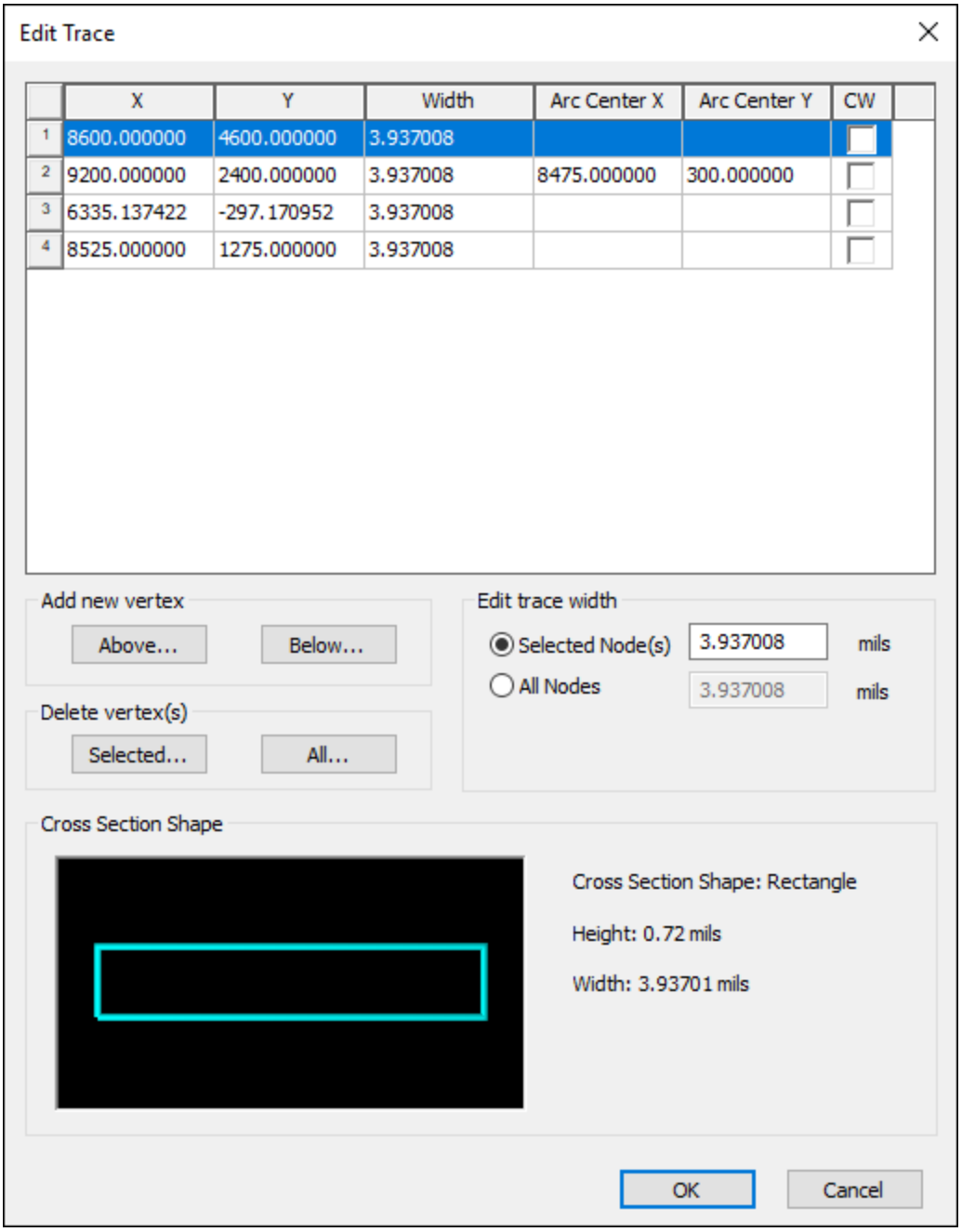

2. Double-click a cell to modify the **X**, **Y**, **Width**, **Arc Center X** and **Arc Center Y** values. Use the **CW** check box to specify the trace as clockwise.
3. From the **Add new vertex** section, click **Above** or **Below** to add a vertex above or below the selected row.
4. From the **Delete vertex(s)** section, you can delete the selected row(s) or all rows.

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5. From the **Edit trace width** section, use the radio buttons to select either the **Selected Node (s)** or **All Nodes**. You can then change the width in mils.
6. Click **OK** to save your changes.

Setting Trace Width

You can use the Edit Trace window to modify trace width. However, additional methods of doing so exist.

To change trace width:

1. Click **Home**.
2. Use the **Trace Width** drop-down menu to select a width (in mils), or type a value directly into the field.

Alternatively, right-click in the Modeling workspace and use the **Set Trace Width** submenu.

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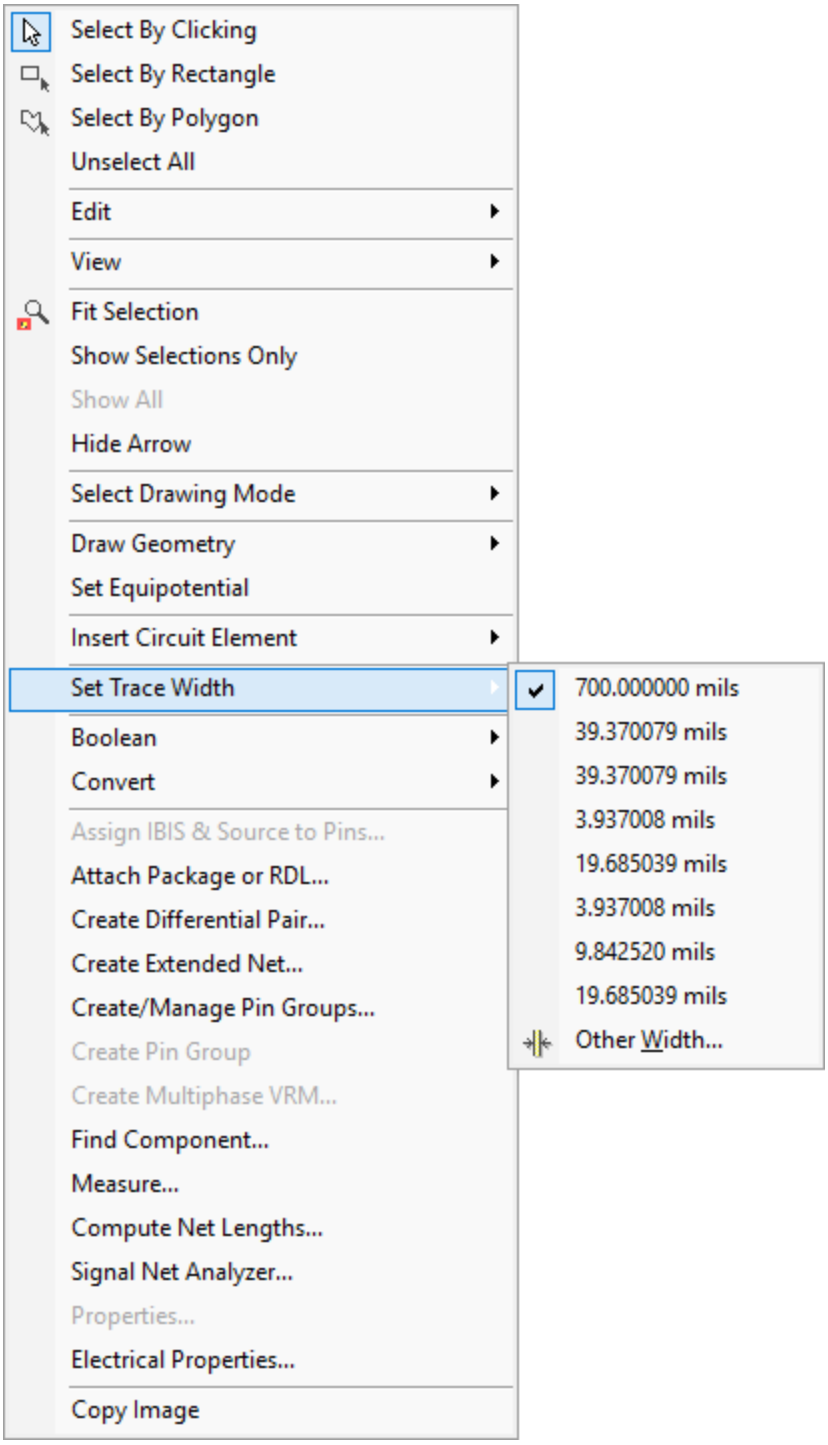

Converting Traces to Planes

To convert a trace into a plane:

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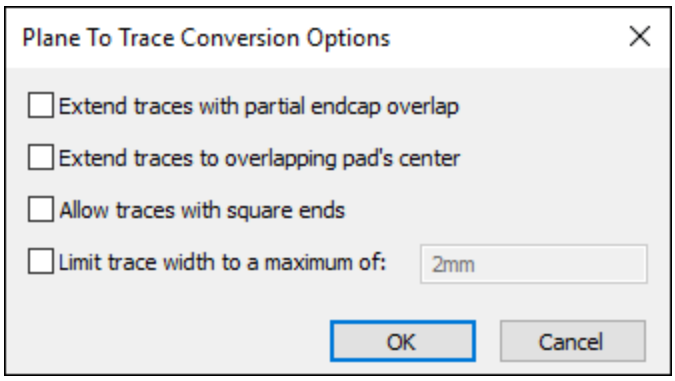
1. Select the trace.
2. Click **Tools**. From the **Transformation Tools** area, click **Convert Traces to Planes**.

The trace is converted into a plane and you can edit its boundary points.

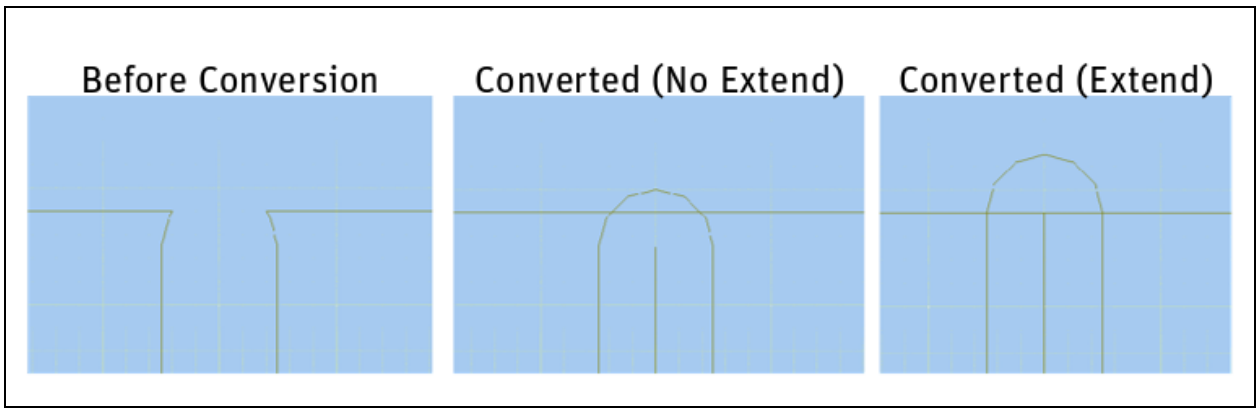
Converting Planes to Traces

To convert a plane into a trace:

1. Select the plane.
2. Click **Tools**. From the **Transformation Tools** area, select the **Convert Planes to Traces** drop-down menu and click **Options**. The **Plane to Trace Conversion Options** window opens.



If the round endcap of a trace overlaps a plane, but the center line of the trace does not intersect the plane, select the **Extend traces with partial endcap overlap** option. This lengthens the trace so that the center line touches the bound of the plane, and fixes misalignment issues. However, if there is other geometry in the small gap that gets filled, it can introduce DC shorts.



3. Select an appropriate options and click **OK**.

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4. Click **Tools**. From the **Transformation Tools** area, click **Convert Planes to Traces** > **Convert Planes to Traces**.

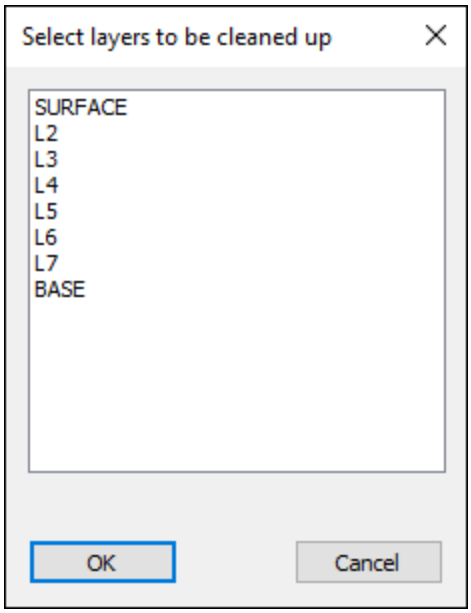
The selected planes are converted into traces.

Cleaning up Overlapping Traces

Optionally, you can clean up overlapping traces. The traces will automatically get converted to planes. This process takes some time, and you have the option to undo the results, if required.

1. Click **Advanced** > **Clean Up Overlapping Traces**.

   The **Select layers to be cleaned up** window appears.



2. Select the layers in which you want to clean up traces. You can select multiple layers using the **Ctrl** and **Shift** keys.
3. Click **OK**.

All traces in the selected layers are converted to planes.

Modifying the Cross Section of Traces

Complete these steps to modify the trace cross-section.

1. Click **Advanced** > **Trace Cross Section** to open the **Trace Cross Section Shape Editor** window.

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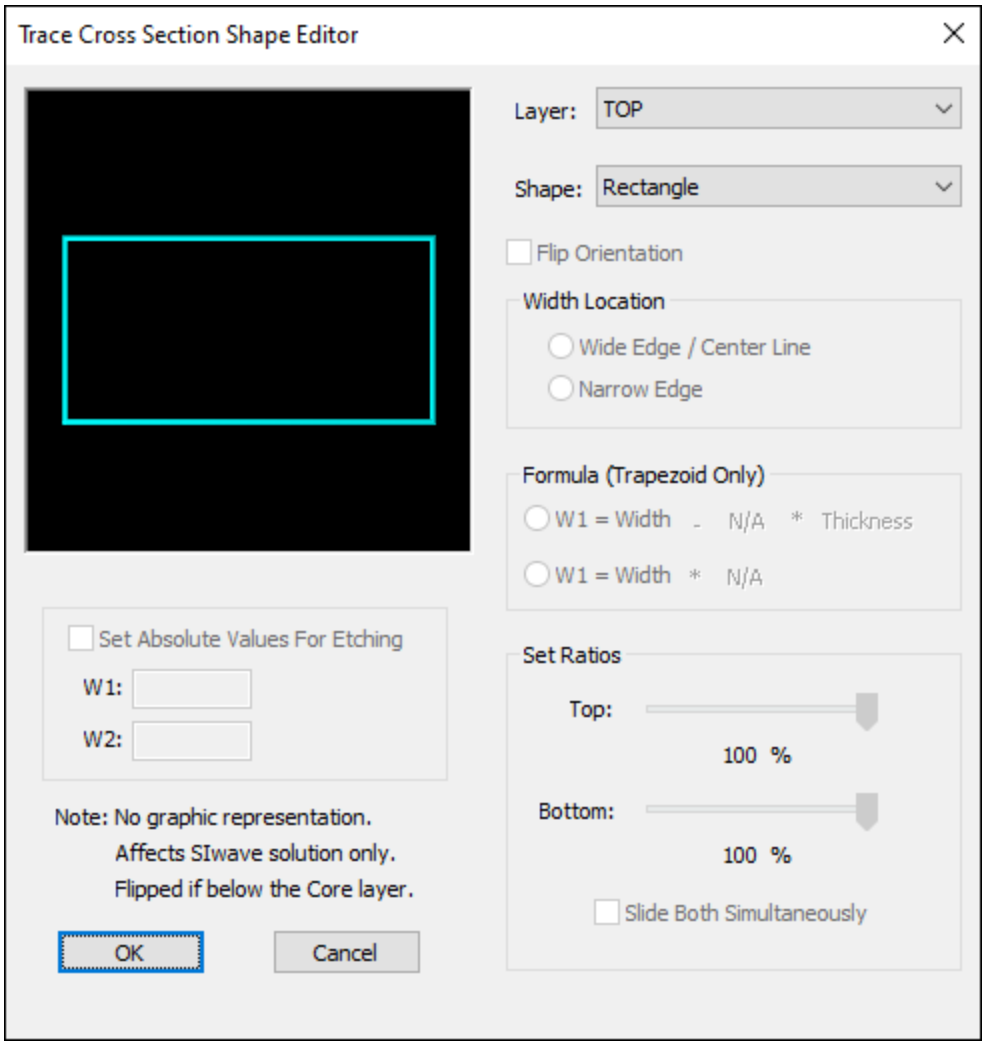

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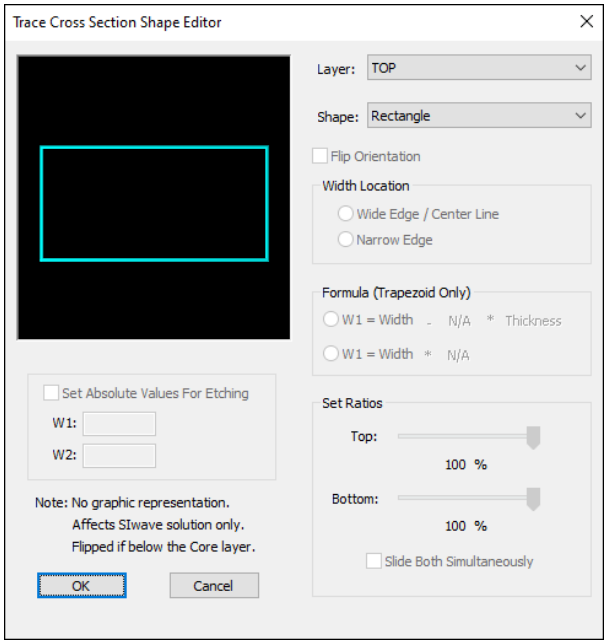

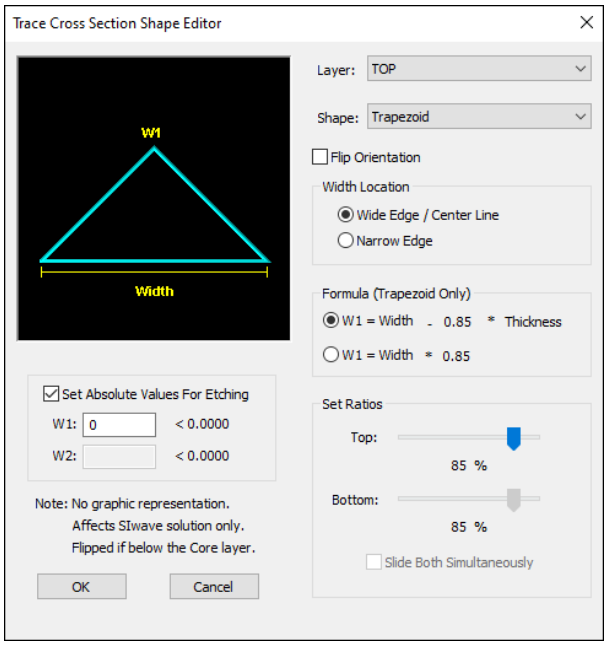

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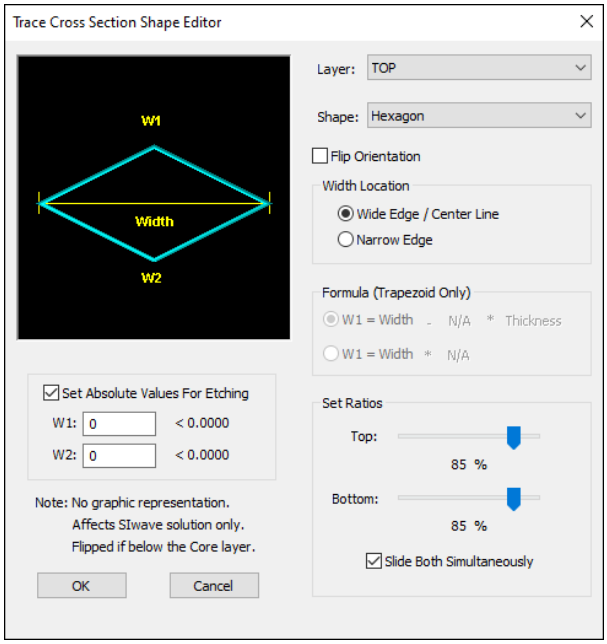

The window contains the following options:

- **Layer** – select a layer to clean up traces.
- **Shape** – select a shape to assign to the trace (rectangle, trapezoid, hexagon).

> **Note:**
>
> The shape selected determines which options are available in the rest of the window.

- **Flip Orientation** – flips the orientation of the trace cross section. *Available for trapezoid and hexagon only.*
- **Width Location** – Available for trapezoid and hexagon only.
- **Formula** – Select one of two trapezoid-calculating formulas. *Available for trapezoid only.*
- **Set Ratios** – Use the sliders to set ratios for your shape. Enable the **Slide Both Simultaneously** check box to slide both sliders at the same time. *Available for trapezoid and hexagon only*.
- **Set Absolute Values for Etching** – Enter widths for the cross sections in the **W1** and **W2** fields. *Available for trapezoid and hexagon only.*

2. Change the settings as appropriate. The graphic updates to show your changes.
3. Click **OK** to close the window and save changes, which are reflected in the Layer Stackup Editor and Trace Editor.

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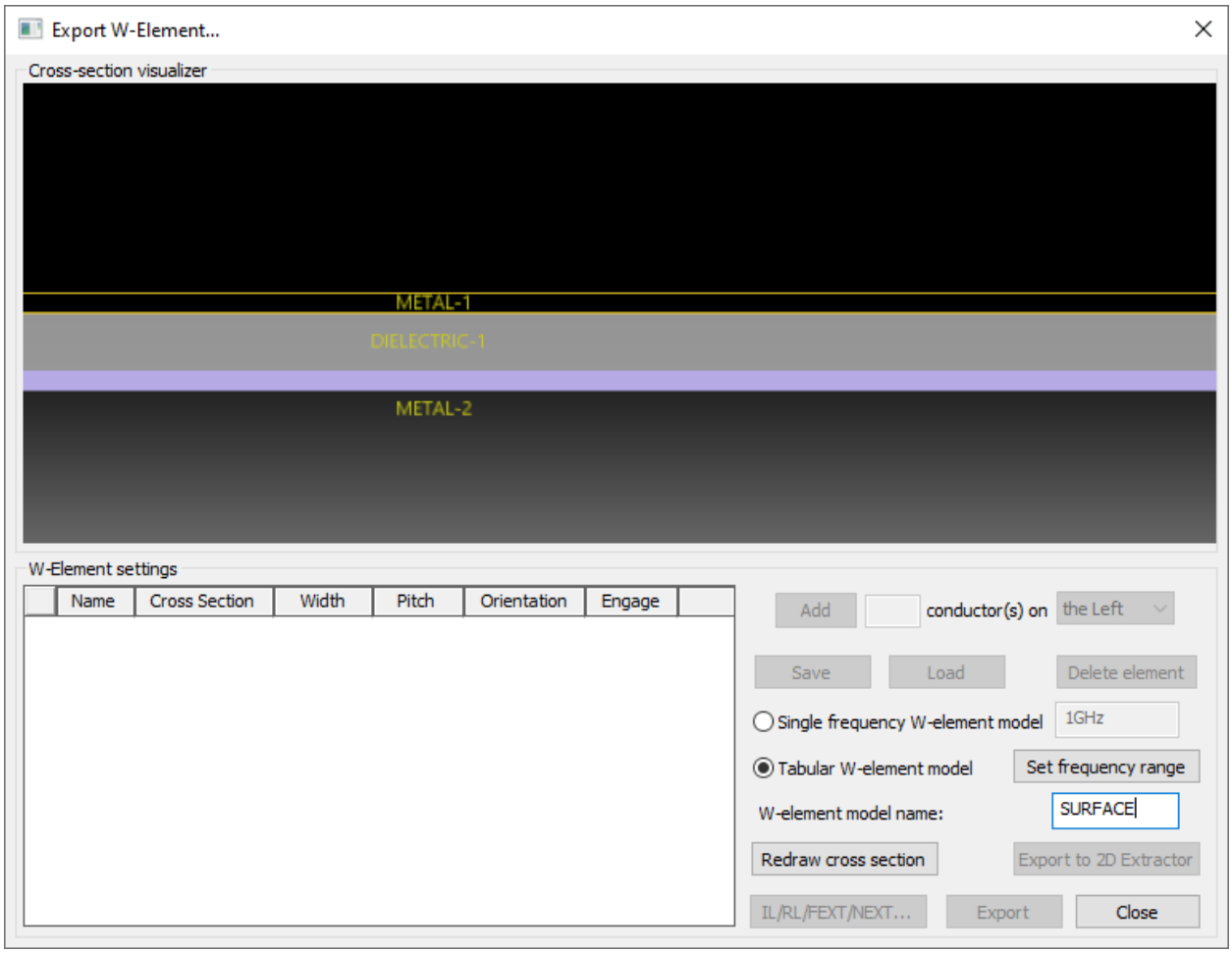
W-element Analysis

W-elements are a distributed model for transmission lines used in certain HSPICE-compatible circuit simulators. For designs containing traces and planes, SIwave can export the W-element in either single frequency or tabular format.

To export the W-element in SIwave:

1. Open a project containing traces and planes.
2. Select the layer containing the trace you want to analyze.
3. Select the trace.
4. Click **Advanced** > **W-element Analysis**.

   The **Export W-element** window appears.



5. Leave the **Export W-element** window open and click in the Modeling workspace to draw a cross-section over the trace.

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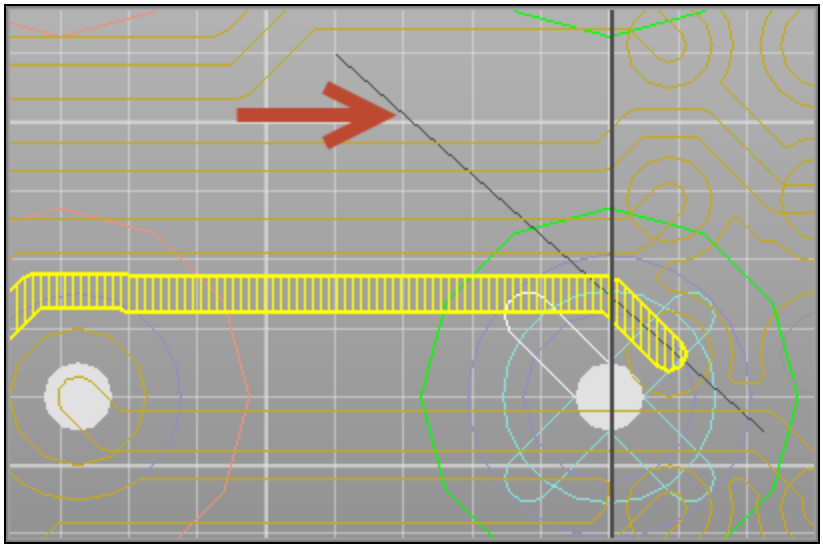
From the following image, the trace is highlighted in yellow and the cross-section is the line intersecting it (indicated by a red arrow).



If you make a mistake, you can click **Redraw cross section** to retry.
Click **OK**.

Using the cross-section you entered, the **Cross-section visualizer** updates, and the list of conductors populates:

	Name	Cross Section	Width	Pitch	Orientation	Engage
1	C4	Rectangle	0.127mm	0.254mm	Left	☐
2	C3	Rectangle	0.127mm	0.254mm	Left	☐
3	C1	Rectangle	0.127mm	-	Fixed	☑

The grid displays the following for each conductor:

- **Name** – conductor name.
- **Cross Section** – indicates the shape of the cross section.
- **Width** – can be edited here directly, or imported from the Layer Stackup Wizard by selecting **Use width/pitch in W-element**.

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- **Pitch** – can be edited here directly, or imported from the Layer Stackup Wizard by selecting **Use width/pitch in W-element**.
- **Orientation** – fixed, left, or right.
- **Engage** – enabling this check box engages the conductor in IL/RL/FEXT/NEXT simulations.

From here, you can:

- Edit the **Width** and **Pitch** values directly in the table.
- **Add** aggressor(s) to the left, right, or on both sides of a selected victim element.
- Delete an element by selecting it and clicking **Delete element**.
- Export the W-element:
  - Select **Single frequency W-element model** and enter a frequency for export, or select **Tabular W-element model** and click **Set frequency range**.
  - Click **Export** to save the W-element as a Spice (*.sp) file, or click **Export to 2D Extractor** to save the W-element as a VB script (*.vbs) and run it in 2D Extractor. Generating this script launches a prompt asking if you want to run the script in Electronics Desktop. Consult the Q3D Extractor/2D Extractor help for instructions on running an analysis in 2D Extractor.
- Compute insertion/return loss and time domain crosstalk.

6. Click **Close** to exit the **Export W-element** window.

> **Note:**
>
> You can also access the **Export W-element** window from the Layer Stackup Wizard.

Padstacks and Vias

Padstacks describe the stacking structure of shapes associated with pads and vias. They enable different shapes on different layers. You can easily create and edit padstacks across all board types. Changes to the saved format and functionality are minimal, since the padstacks are independent of the number of layers in the design.

Padstacks consist of:

- Drill information
- Plane layer information – used for calculating the heat and iso shapes used on plane layers.
- Inner layer information – used for assigning different shapes for used/unused component pads.

Vias consist of a hole cut in the PCB to route a trace vertically from one layer to another, as well as the vertical pieces of conductor that make connections between layers. If a via is too big, it

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does not have sufficient room to route signal traces. If vias are made smaller, more traces can be drawn.

Consult the following topics:

- Configuring Padstacks
- Adding and Deleting Padstacks
- Converting Padstacks to Planes
- Drawing Vias
- Editing Via Properties
- Translucent Via Rendering

Configuring Padstacks

To configure padstacks:

1. Click **Home** > **Edit Padstacks**.

   The **Padstack Editor** window appears.

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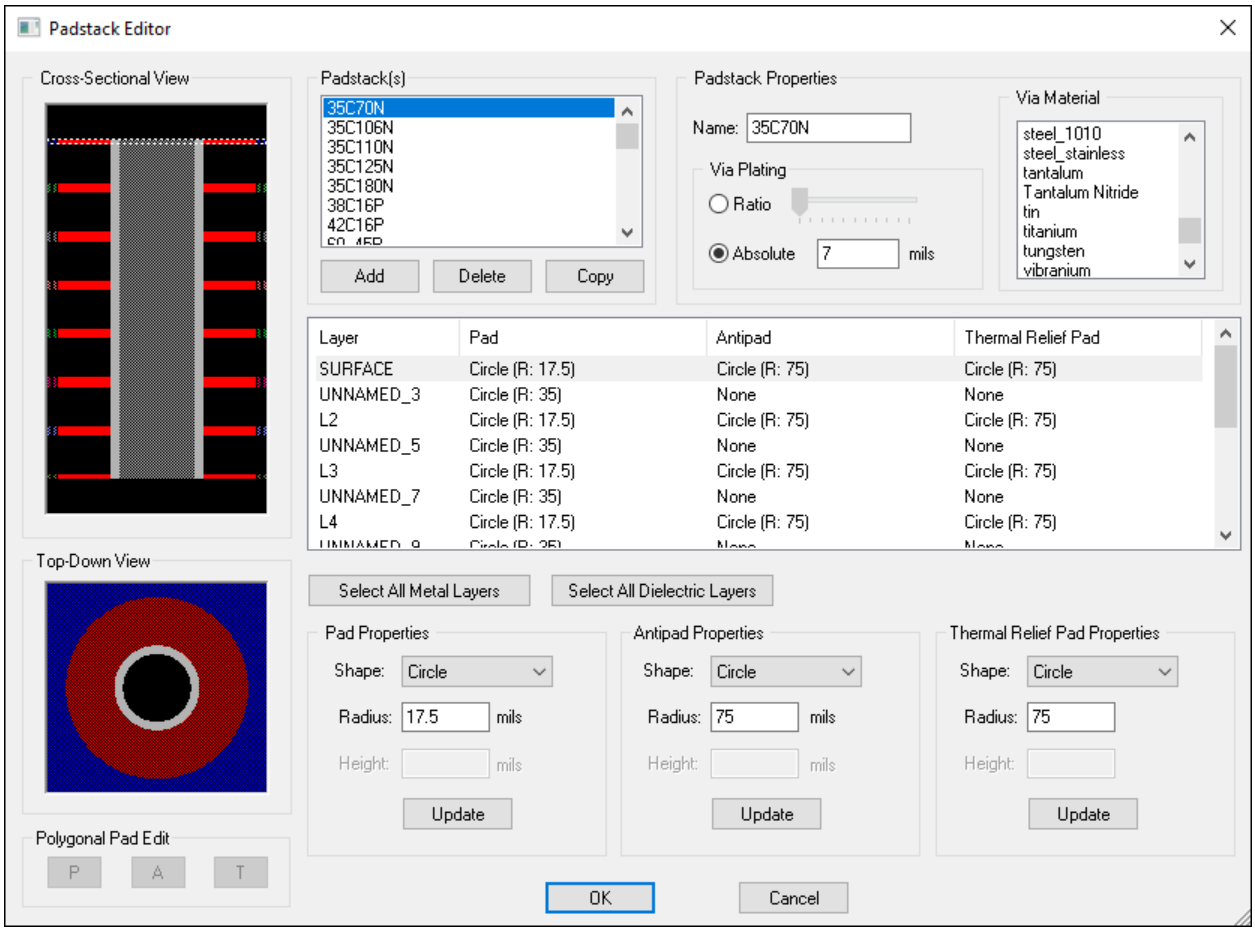

2. From the **Padstack(s)** area, select a padstack.
3. From the layer selection box, select any metal or dielectric layer to modify the properties. If you want to apply the same properties to all metal or dielectric layers, click **Select All Metal Layers** or **Select All Dielectric Layers**.
4. From the **Name** field, rename the padstack.
5. From the **Via Material** list, select a material.
6. From the **Via Plating** area, specify the thickness of the via shell using a **Ratio** or **Absolute** thickness, in mils.

   The **Cross-Sectional View** area updates to show the vertical cross-section of the layer stackup.

To update pad properties:

1. Select the layer on which you want to modify the padstack. You can also draw the padstack between two layers.
2. From the **Pad Properties** area, use the **Shape** drop-down menu to select a shape for the pad, or choose **None** if there is no pad on that layer of the padstack. The options below will

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change, depending on the shape selected (e.g., if you choose a Circle, you must then choose the radius).

3. Click **Update** to apply changes to the pad.

   From the **Cross-Sectional View**, the innermost gray area shows the thickness of the via passing through the center of the pad. Metal colors are selected from the Edit layer properties window and the colors are proportionate to the dimensions of the pad.

To update antipad properties:

1. Select the layer on which you want to modify the padstack. You can also draw the padstack between two layers.
2. From the **Antipad Properties** area, use the **Shape** drop-down menu to select a shape for the pad, or choose **None** if there is no antipad on that layer of the padstack. The options below will change, depending on the shape selected (e.g., if you choose a Circle, you must then choose the radius).
3. Click **Update** to apply changes to the antipad.

   From the **Cross-Sectional View** and **Top-Down** view, the black area represents the antipad.

To update thermal relief pad properties:

1. Select the layer on which you want to modify the padstack. You can also draw the padstack between two layers.
2. From the **Thermal Relief Pad Properties** area, use the **Shape** drop-down menu to select a shape for the pad, or choose **None** if there is no thermal relief pad on that layer of the padstack. The options below will change, depending on the shape selected (e.g., if you choose a Circle, you must then choose the radius).
3. Click **Update** to apply changes to the thermal relief pad.

From the **Cross-Sectional View** and **Top-Down** view, the red area represents the thermal relief pad.

From the Padstack Editor, you can also add or delete a padstack.

Adding and Deleting Padstacks

From the **Padstack Editor**, you can add a new padstack to the stackup.

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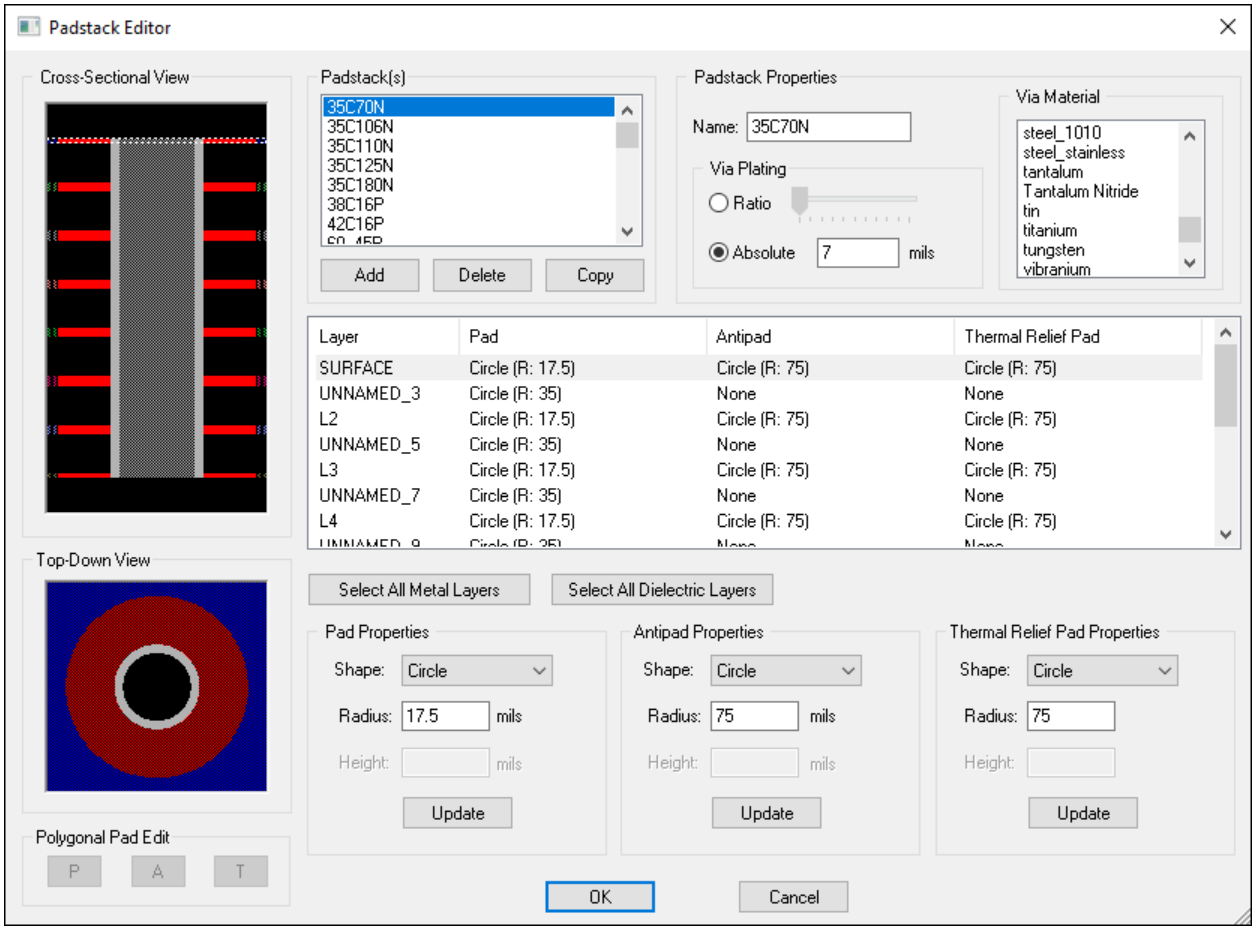
1. Click **Home** > **Edit Padstacks**.



To add a new padstack:

1. From the **Padstack(s)** area, click **Add**.

   The new padstack is given the default name NEW_PADSTACK and is positioned alphabetically in the padstack list. You can then rename and configure the padstack.

To delete a padstack:

1. From the **Padstack(s)** area, select the padstack you want to delete.
2. Click **Delete**.

   An alert window appears, asking you to confirm deletion. Note that any vias referencing the padstacks will also be deleted.

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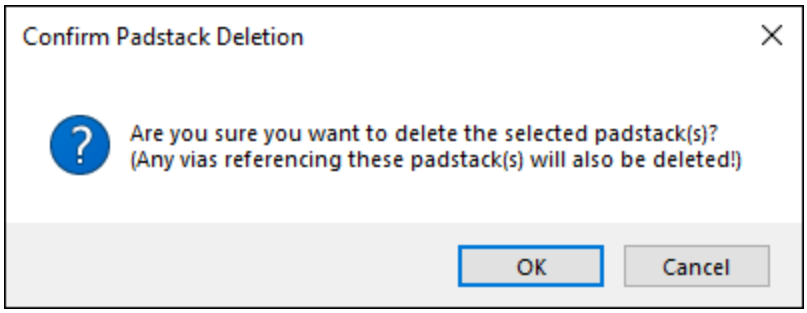

3. Click **OK** to proceed with the deletion.

   The padstack is removed.

Converting Pads to Planes

Pads above a certain fraction of the design bounding box area are automatically converted to planes. This fraction can be set using the **SIWAVE_PAD_CONVERSION_FACTOR** environment variable. The default value is 500. So if the bounding box area is 60E+3 mm^2, all pads with area more than 120 mm^2 (== 60E+3/500) will be modeled as planes. In addition, SIwave automatically identifies pads overlapping plane geometry, converts these pads into planes (irrespective of their size) and unites them with the overlapping plane(s). The automatic conversion of pads to planes is done only during solver input file generation, with no changes to the layout (the geometry in the Modeling workspace does not change).

> **Note:**
>
> Rectangular pads with a height greater than twice their width will be automatically converted to traces when the connection configuration allows. This conversion enables impedance calculation for these pads. Non-rectangular pads remain unconverted and do not display impedance results.

To manually select pads in the Modeling workspace and convert them into planes:

1. Select the pad.
2. Click **Tools**. From the **Transformation Tools** area, click **Convert Pads to Planes**.

   The pads are converted to planes and the layout is changed.

Small circular pads are better off not being modeled as planes. The solver is able to accurately compute capacitance between such pads and any surrounding planes when they are modeled implicitly. Larger pads, especially those that are non-circular, result in improved accuracy when represented as planes.

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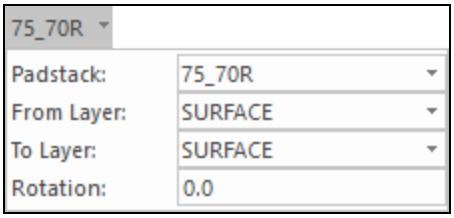
Drawing Vias

To draw a via:

1. Select the padstack on which you want to draw the via.
2. Click **Home**. From the **Draw Geometry** box, click the **Drop Via** icon ( ) .
3. Click the location where you want to draw the via.

A via is placed at the specified location.

Alternately, use the **Via Settings** drop-down menu on the **Home** tab to make changes to the via's padstack, layers, and rotation.



You can also simplify how the via is displayed.

Editing Via Properties

To edit via properties:

1. Select one or more vias.
2. Click **Advanced** > **Via**, or right-click a via in the **Modeling workspace**, and select **Properties** from the shortcut menu.

   The **Via Properties** window appears.

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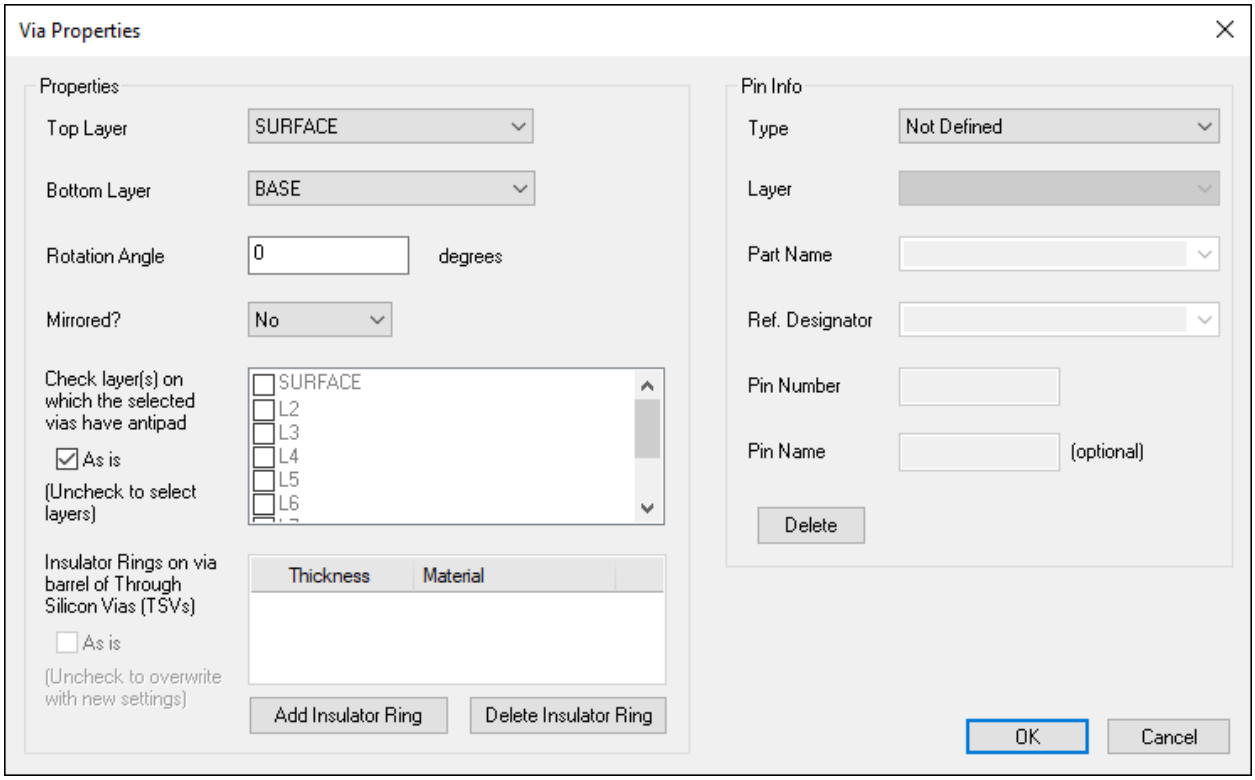

3. Use the **Top Layer** and **Bottom Layer** drop-down menus to select the via layers.
4. From the **Rotation Angle** field, type an angle in degrees to rotate the via in the XY plane. The rotation angle is specified from the orientation in the padstack and is counter-clockwise.
5. Use the **Mirrored?** drop-down to specify whether the via layers are mirrored.

   If your design has an even number of layers and you mirror those layers, the layers are mirrored in the following order: top layer is mirrored with the bottom layer and (top-n) layer is mirrored by the (bottom-n) layer

   If you have an odd number of layers, the middle layer is mirrored around itself and the other layers are mirrored like even layers.

   The graphic below shows the difference in mirroring for an even number of layers (top) and an odd number of layers (bottom).

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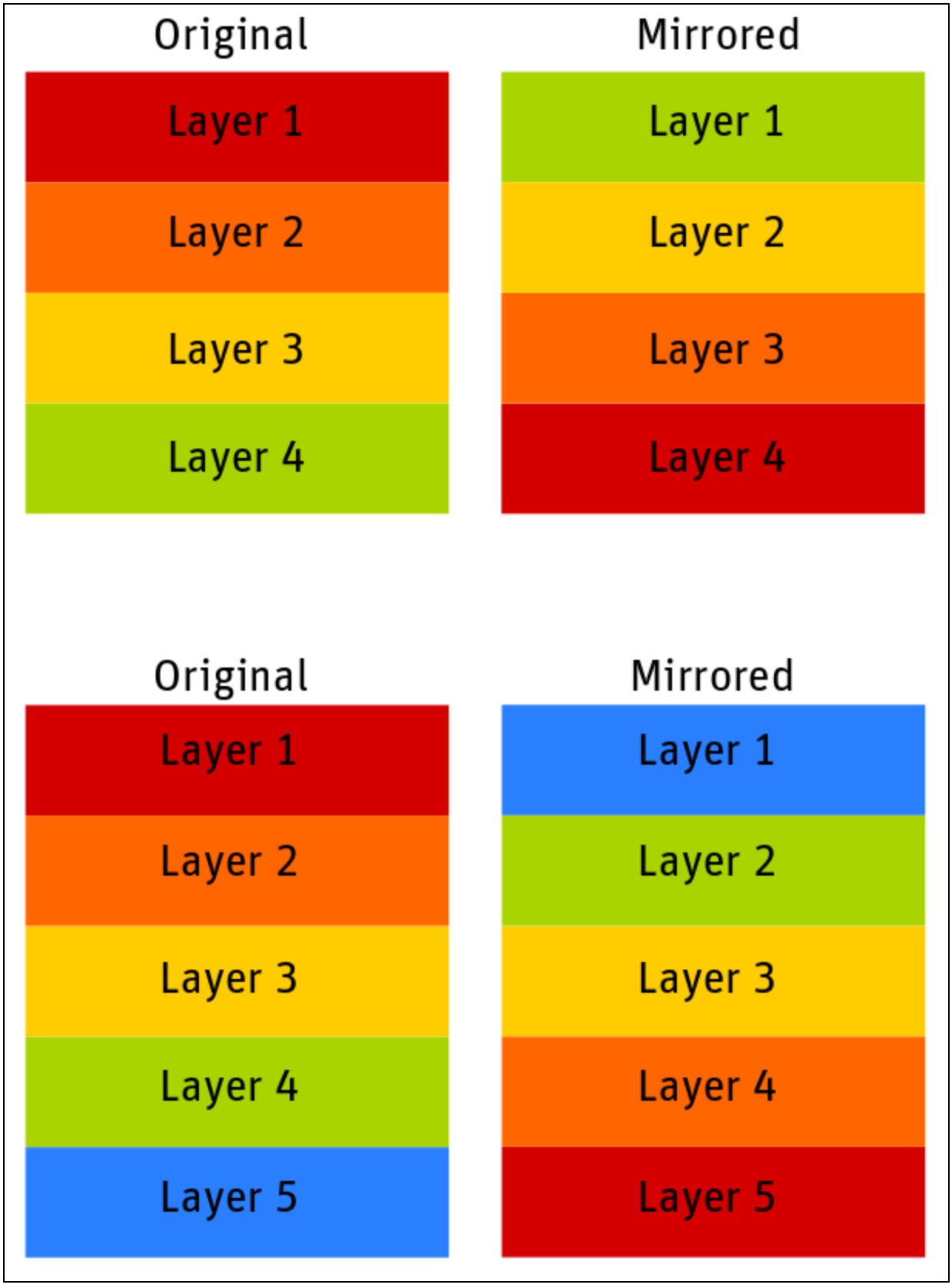

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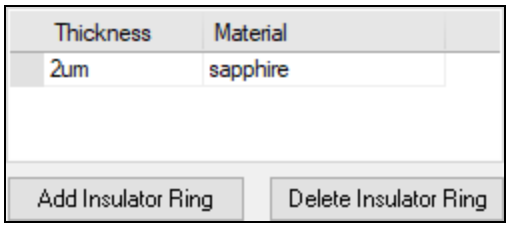
6. From the **Check layer(s) on which the selected vias have antipad**, you can enforce antipad definition. By default, if a via is part of a net and crosses through a plane that it also part of that net, no antipad will be created regardless of the antipad definition in the padstack. This option forces selected layers to get an antipad, even if the via net is the same as the plane net that it is passing through. When multiple vias are selected, an **As is** option appears here, which leaves antipads as defined.
7. Use the **Add Insulator Ring** and **Delete Insulator Ring** buttons as appropriate, or check **As is** to not change insulator rings. When an insulator ring is created, you can type the **Thickness** and select the **Material** of each ring. Only insulator materials are listed.



> **Note:**
>
> TSVs (Through Silicon Vias) are vias that can pass through semi-conductor layers, such as silicon. They require insulator rings along the via barrel to prevent any electrical contact between the barrel and the semi-conductor layers through which they pass.
>
> Simulation of TSVs is only supported in the PSI & CPA solvers within SIwave. If TSV rings exist on any via when another solver is run, a warning about TSV not being supported appears. You can acknowledge and proceed, or abort the simulation.

8. From the **Pin Info** area, you can reassign pin names. Use the drop-down menus to select an appropriate pin and rename it using the **Pin Name** field. Click **Delete** to clear pin information.
9. Click **OK** to accept the changes, or click **Cancel** to exit without making any changes.

Translucent Via Rendering

Vias can be rendered as either opaque or translucent.

To change this setting:

1. Click **View**.
2. Use the **Translucent Vias** check box to toggle between translucent and opaque.

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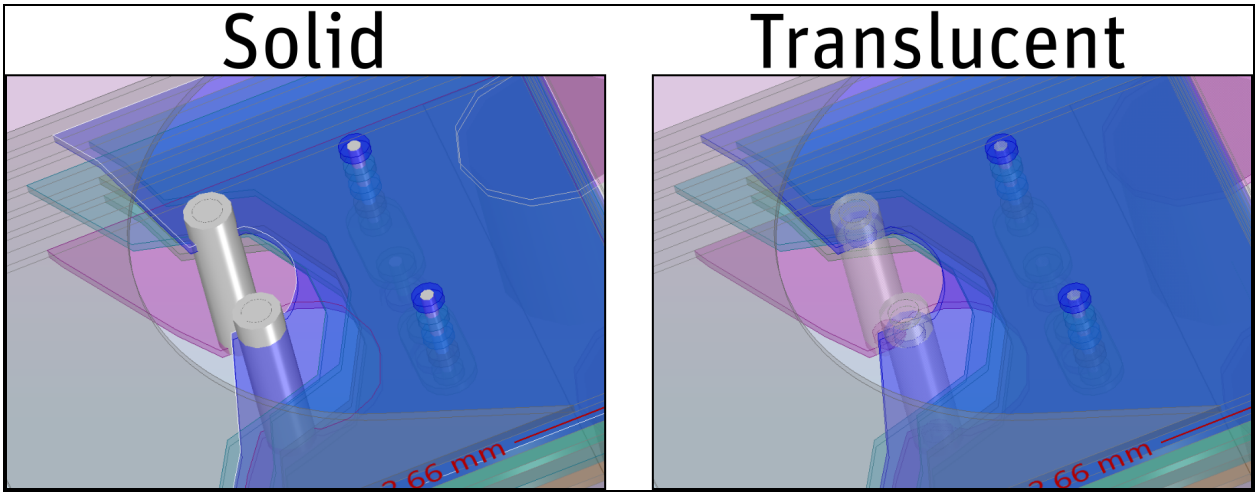
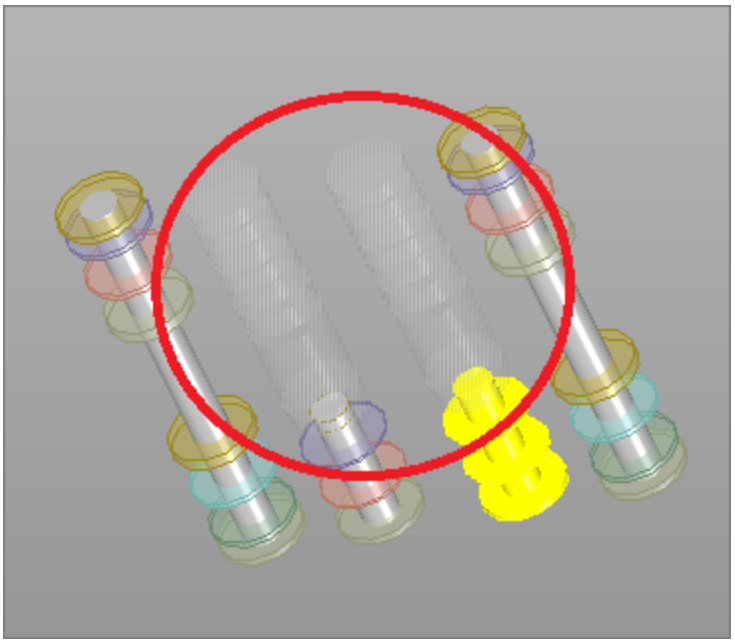


Backdrilling

Unused portions of vias (known as "stubs") can create significant signal integrity disturbances. Backdrilling is a technique that removes these stubs.

From the Modeling workspace, backdrills appear as transparent via stubs:



If a selected via has a backdrill, its properties display in the Properties window:

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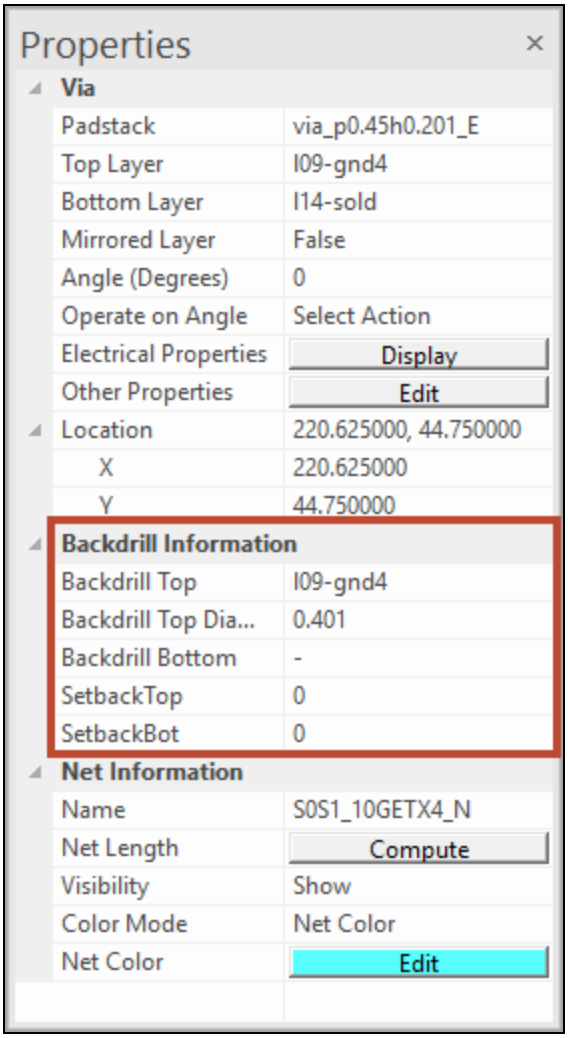

Changing Backdrill Settings

To open the **Backdrill Settings** window, click **Advanced** > **Backdrill Settings**.

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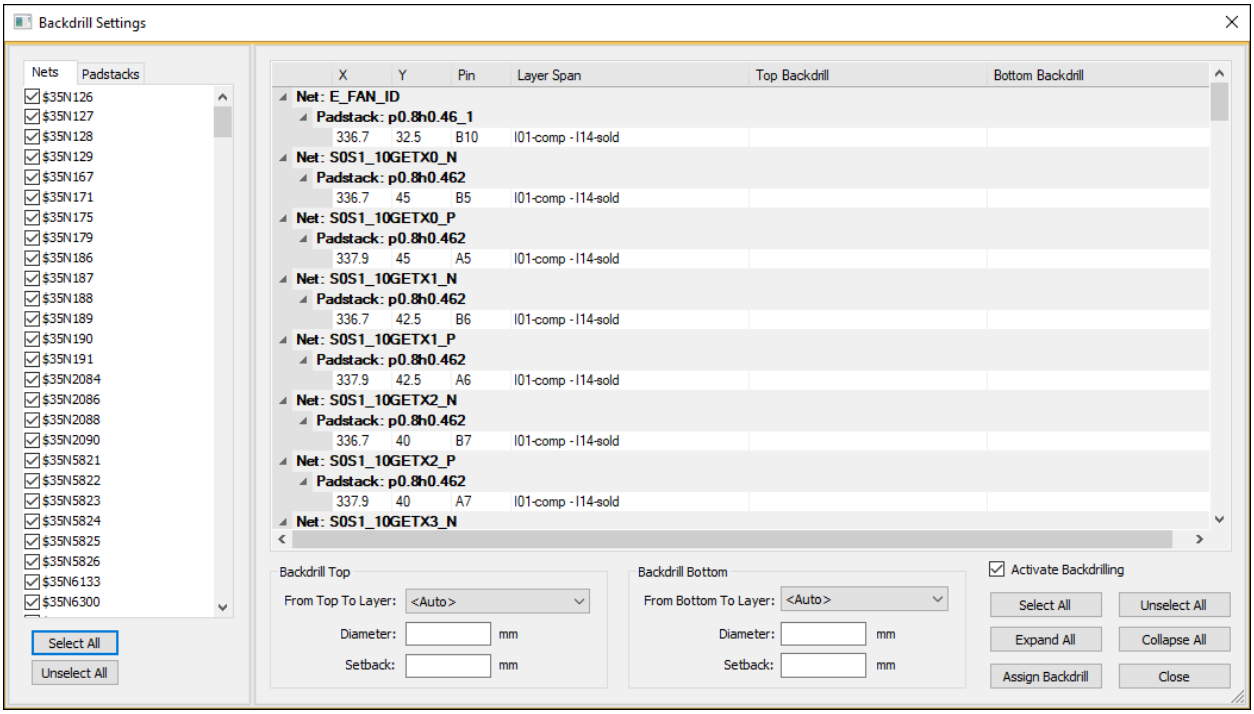
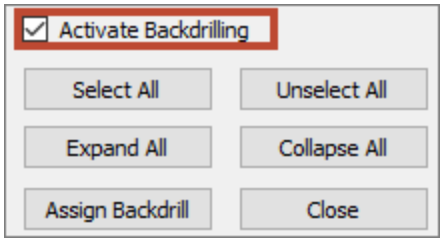


The left pane allows you to select or deselect nets and padstacks. The right pane displays vias associated with your selection.

Selecting a single backdrill via causes the modeling workspace to zoom in on it. When more than one via is selected, nothing is zoomed.

To enable or disable backdrilling project-wide:

- Select or clear the **Activate Backdrilling** check box.



To assign a backdrill to one or more vias:

1. Use the filters in the left pane to find the via(s) to which you want to add backdrills.
2. Select the via(s) from the list on the right. Use **Ctrl+click** to select more than one via, or use the **Select All** button to select all vias in the list.

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3. From the **Backdrill Top** and **Backdrill Bottom** areas, enter the information for your backdrill:
   - **From Top to Layer** – when creating a top backdrill, the backdrill begins at the top layer and ends at the layer you select. The **Auto** setting identifies the stub and selects an appropriate layer.
   - **From Bottom to Layer** – when creating a bottom backdrill, the backdrill begins at the bottom layer and ends at the layer you select. The **Auto** setting identifies the stub and selects an appropriate layer.
   - **Diameter** – the diameter of the backdrill.
   - **Setback** – the diameter required at the top or bottom layer.
4. Click **Assign Backdrill**.

   The via list updates with the new backdrill information.
5. Click **Close**.

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6 - Packages and ICs

The Package design flow is needed when a PCB design does not include all the packages to be mounted on the PCB.

Package models and models of integrated circuits or chips require special handling.

- Packages
- Integrated Circuits

Packages

Packages can be drawn as models, or can be imported and attached to an existing PCB design.

- Importing a Package
- Adding Solderballs

Importing a Package

Usually, SIwave automatically finds a proper PCB part and reference designator and the correct orientation to match pins between the imported package and the PCB component. However, Ansys recommends selecting a PCB component from the main graphic window before opening the **Attach Package** window.

To import a package, after opening a PCB:

1. Click **Tools** > **Attach Package or RDL**.

   The **Attach Package or RDL** window appears.

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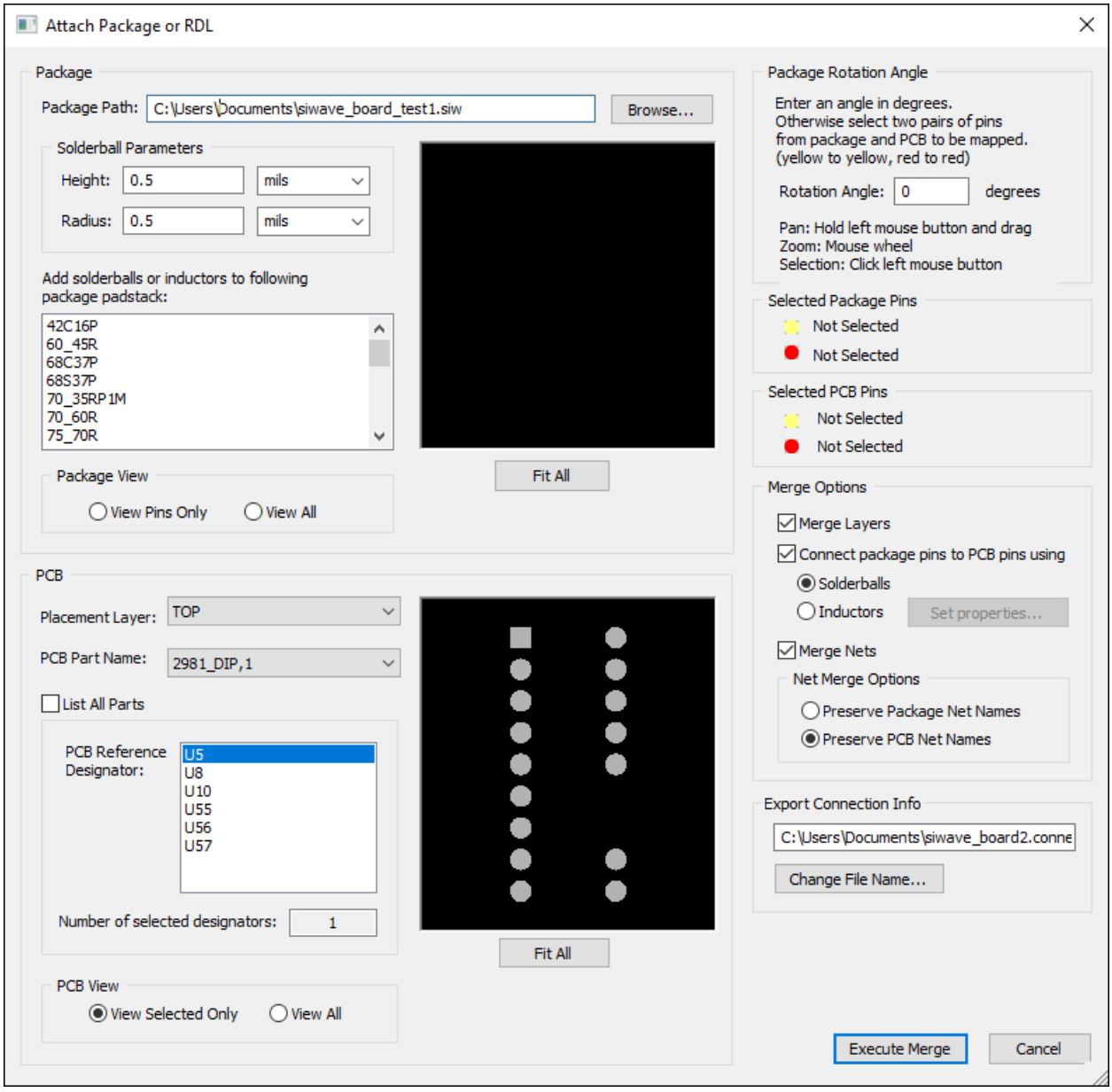

2. From the **Package Path** field, click **Browse** to locate the package file.

To place the package:

1. From the **PCB** area, use the **PCB Part Name** drop-down menu to select a part. Specify the **Placement Layer** as **Top** to place the package above the top layer, or **Bottom** to place it below the bottom layer.
2. Select the **PCB Reference Designator**. **Ctrl+click** to make multiple selections.

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3. From the **Merge Options** area, check the boxes and make selections as applicable:
   a. **Merge Nets** – Use if there are overlapping nets. Select the naming convention you prefer.
4. From the **Export Connection Info** area, click **Change File Name** to select a file name and location to save your settings.
5. Use the **Package** and **PCB** view areas (shown with a black background) to select one pair of pins from the imported package and one pair from the PCB. As you select pins, the first selection highlights in red and the second selection highlights in yellow. The red pin in the package is mapped to the red pin on the PCB, and the yellow pin in the package is mapped to the yellow pin on the PCB. The rotational angle is determined from the locations of the mapped pins.

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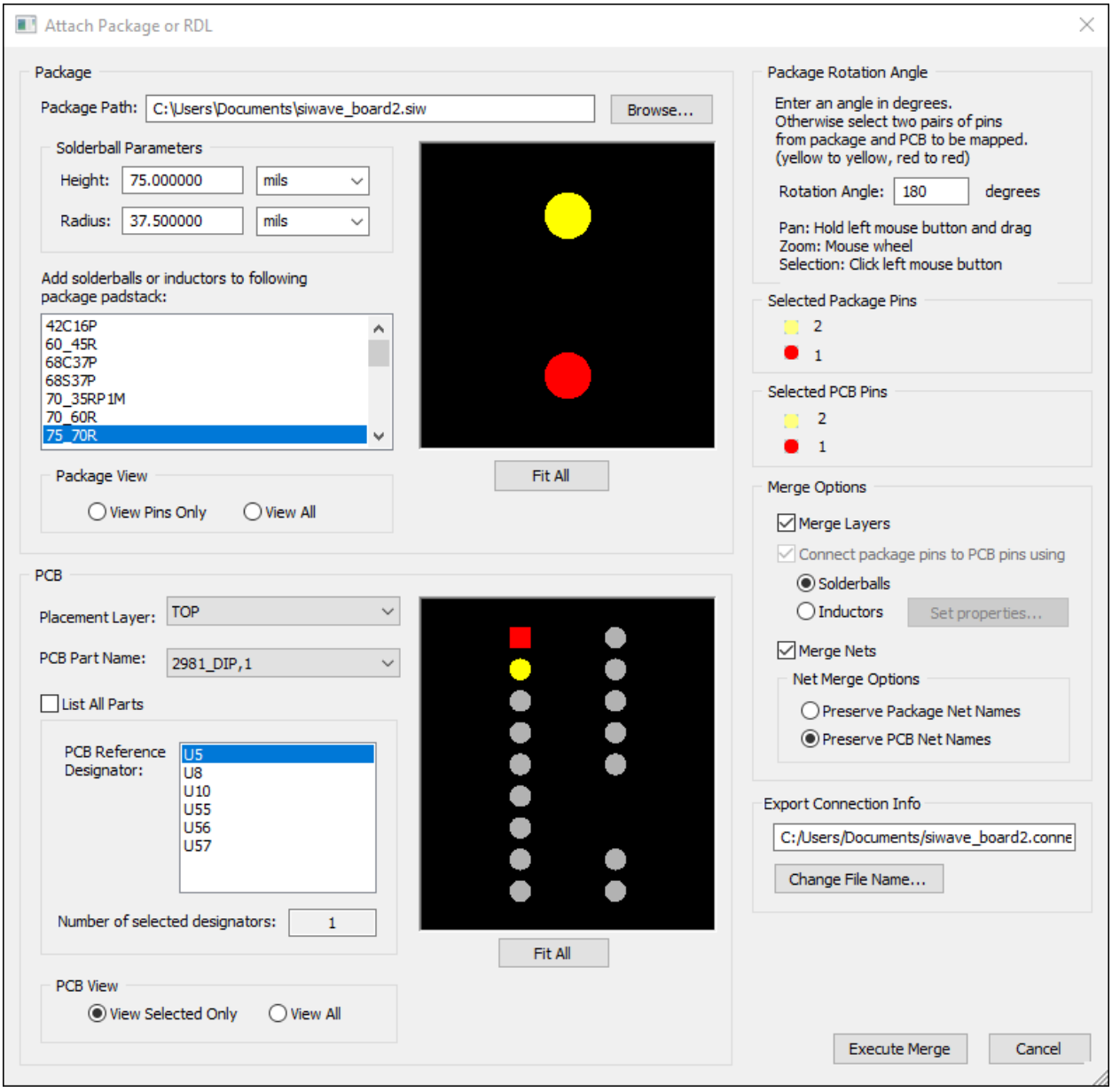

6. Click **Execute Merge**.

   You can see the project updated in the Modeling workspace. All layers and padstacks that are merged have *_pkg* after their name.

Adding Solderballs to a Package

Solderballs connect a BGA type package to the PCB at a designated reference designator location.

To create a solderball:

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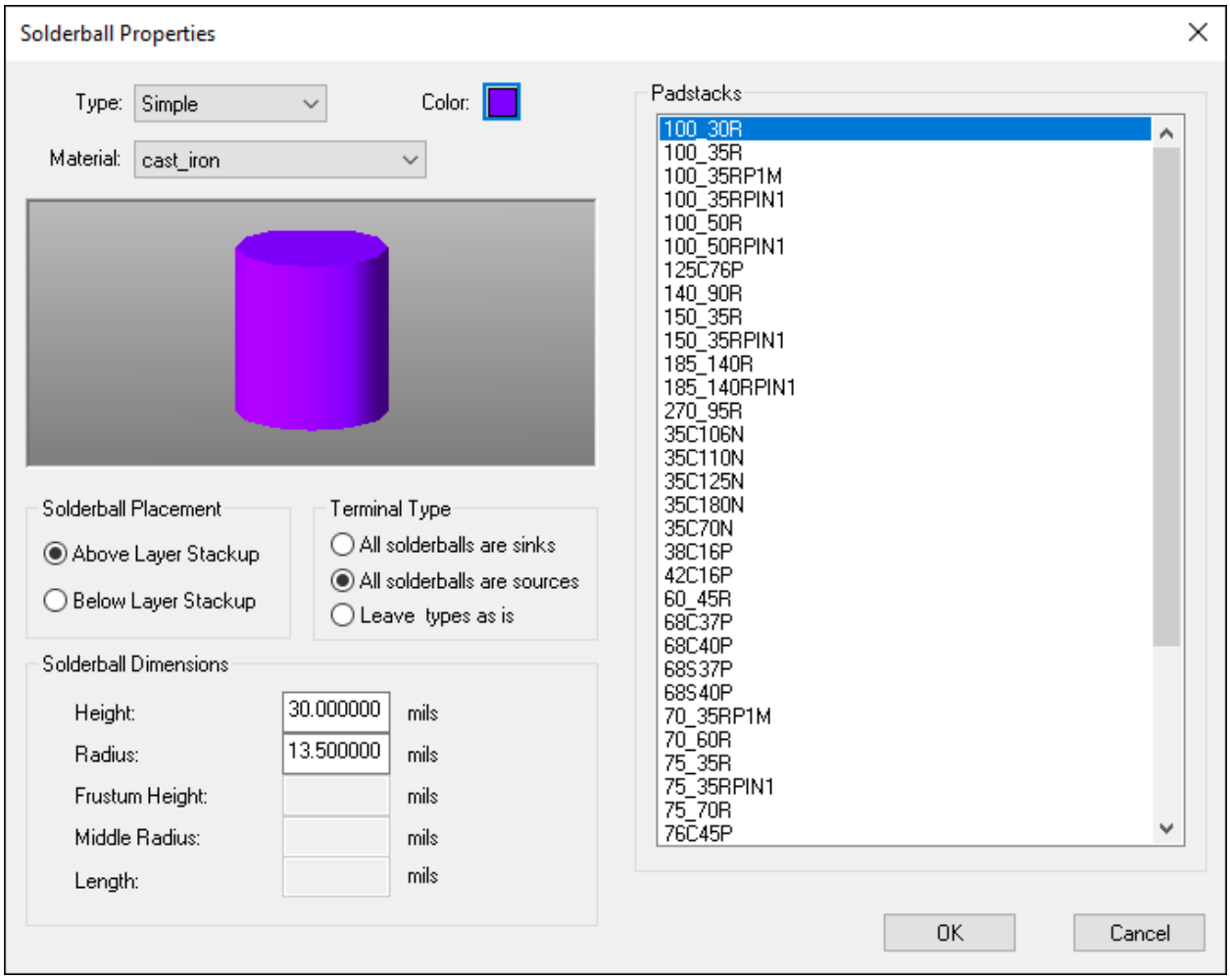
1. Click **Home** > **Solderball Properties**.

   The **Solderball Properties** window appears.



2. From the **Padstacks** area, select a padstack to define solderballs.
3. From the **Type** drop-down menu, select **Simple**, **Complex**, or **Oblong**. The **Solderball Dimensions** section updates to reflect required fields.
4. From the **Material** drop-down menu, select a material for the solderball.
5. Click the **Color** swatch to select a color for the solderball(s). The default is gray.
6. From the **Solderball Placement** area, use the radio buttons to place the solderball either **Above Layer Stackup** or **Below Layer Stackup**.
7. From the **Terminal Type** area, use the radio buttons to set solderballs as sinks or sources globally, or to leave types as is.

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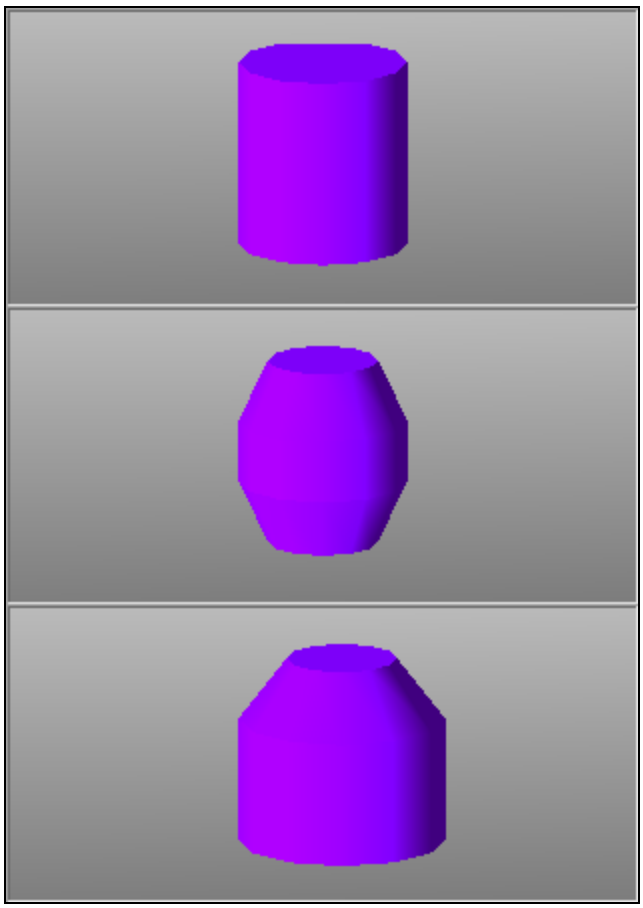
8. From the **Solderball Dimensions** area, enter the applicable dimensions, in mils. As you make changes, the new shape of the solderball previews in the window. A simple, complex, and oblong solderball are shown below.



9. Click **OK**.

Solderballs are added to every instance of the specified padstacks in the layout.

Integrated Circuits

Integrated circuits can be represented with IC dies or with CPM/PLOC/Voltus die power models.

See:

- Importing CPM/PLOC/Voltus Files
- Remapping a Package Netlist
- Editing IC Die Properties
- Creating an IC Die network
- Adding Bondwires

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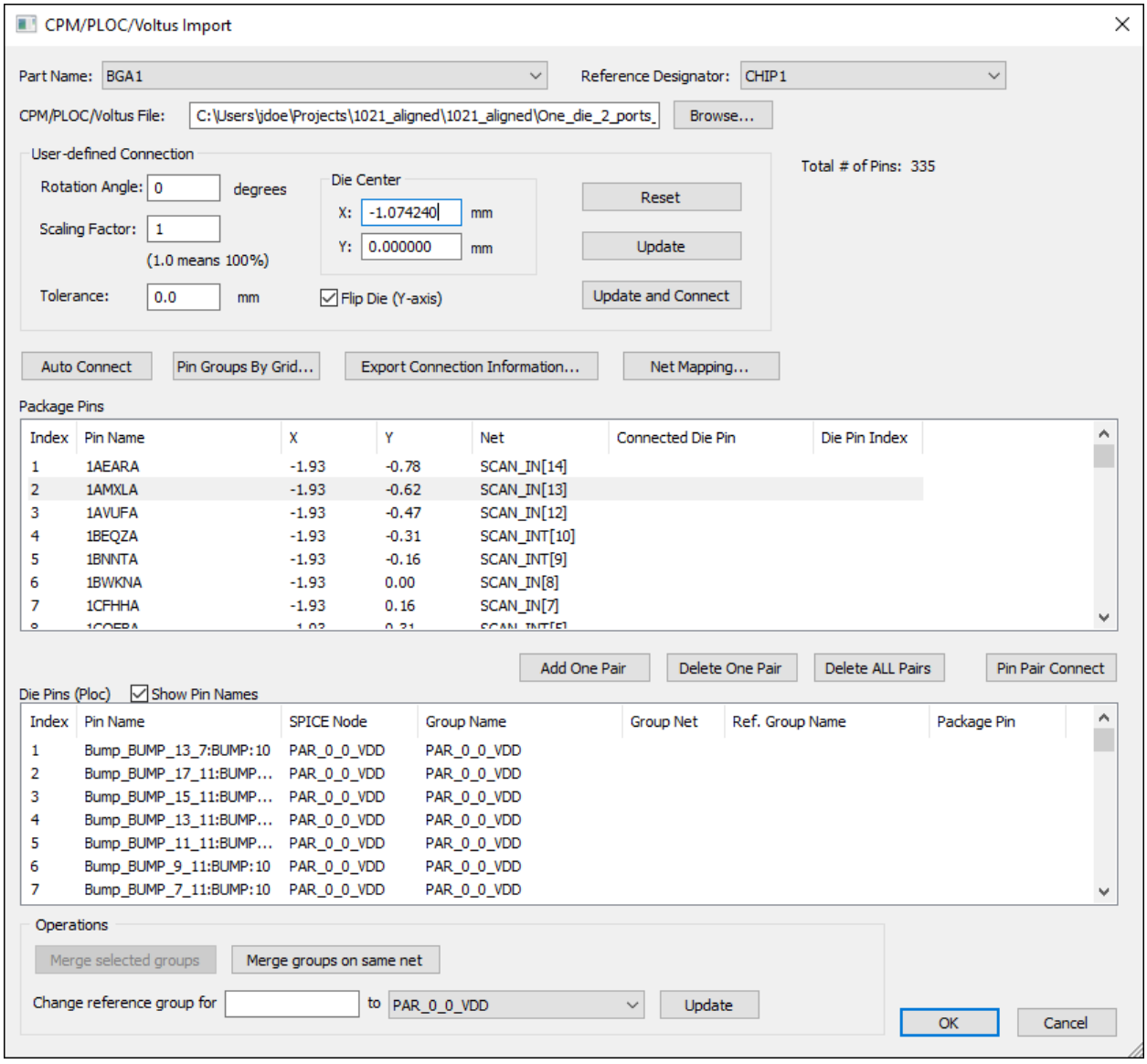
Importing CPM/PLOC/Voltus Files

CPM, PLOC, or Voltus files (*.sp, *.ploc, *.isrc) contain the IC die power model. The Chip Package Protocol (CPP) header on the CPM file supplies the coordinates and groupings for the IC die pin locations. This information, which other SPICE files generally do not include, enables SIwave to automatically align and connect the IC die pins and the package pins.

To import a CPM/PLOC/Voltus file into SIwave:

1. Click **Import** > **CPM/PLOC/Voltus File**.

   The **CPM/PLOC/Voltus Import** window appears.



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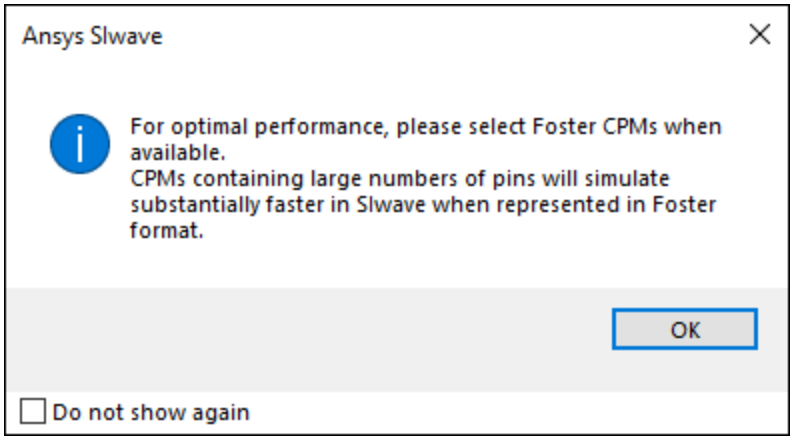
2. Use the **Part Name** and **Reference Designator** drop-down menus to select the package that will receive the IC die.

   The **Package Pins** list populates.

3. To fill the **CPM/PLOC/Voltus File** field, click **Browse**.

   An alert window appears, advising you to select Foster CPMs for best performance.



4. Click **OK** to close the alert.
5. From the file browser, locate and select a CPM/PLOC/Voltus file for import. Then click **OK**.

   The **Die Pins** list populates. The values and check box under **User-defined Connection** populate based on the information in the file. To define your own connection parameters, specify the **Rotation Angle**, **Scaling Factor**, **Tolerance**, **Die Center**, and whether or not to **Flip Die**. Then click **Update and Connect**.

6. Map package pins to die pins one of the following ways:
   - Click **Auto Connect** to update the **Package Pins** and **Die Pins** lists to show connections.
   - Click **Pin Groups by Grid**.
   - Click **Net Mapping** to open a window summarizing connections. From this window, you can easily identify P/G shorts or nets not connected to their proper domains as well as disconnect any unwanted net mappings.

   The lists of **Package Pins** and **Die Pins** update to show connections.

   The upper-right area of the window displays the number of **Pins mapped** and the number of **Pins unmapped**.

7. If appropriate, click **Export Connection Information**.
8. Click **OK**.

   A prompt appears with two options.

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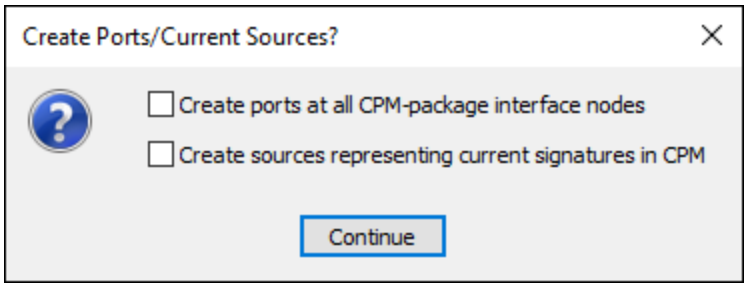

If you'd like to create ports at all CPM-package interface nodes and/or create sources representing current signatures, select an appropriate check box(es).

9. Click **Continue**.

   The **Components** list updates and SIwave marks the location of the IC die on the package with an 'X' to indicate that the CPM/PLOC/Voltus import was successful. If you elected to create ports and/or current sources, those also appear. Full details are available in the **Circuit Element Parameters** window.

   Current signatures are imported into SIwave as current sources (IPWL sources are averaged and represented as constant current sources in SIwave). Such sources can be used as the basis for DC IR drop, frequency sweep, and near/far field simulations.

Remapping a Package Netlist

SIwave can map a previously extracted package netlist into the footprint of a new chip.

For instructions on exporting a PLOC file, see: Exporting CPA RLGC Results.

Requirements:

- The model has been extracted using an old PLOC file and needs to be remapped into a new PLOC file.
- There is a preexisting adsCPA folder. The new PLOC will be mapped to and update the annotated and ASCII PLOC files in this folder.
- The number of nets in the new PLOC matches that of adsCPA.
- The preexisting package has been extracted using an M x N grid, with Channel setup

Remapping Commands:

Remapping is performed from the command line, using speng.exe:

```
speng.exe <path_to_adsCPA_folder\adsCPA\> <path_to_config_file\ploc_
remap_config.txt> <path_to_new_ploc_file\newplocfile.ploc> -reassign_
ploc_gridbased
```

The command window will track remapping progress.

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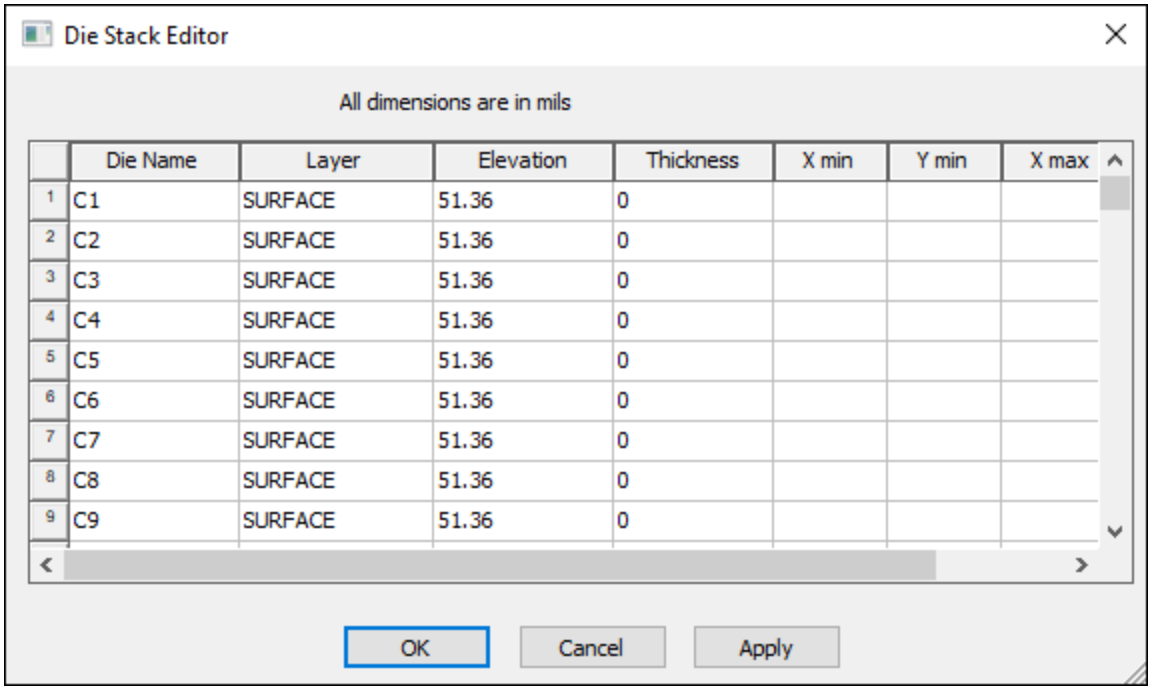
The adsCPA folder is expected to contain a file named cpa_annotated.ploc. Once remapping has finished, cpa_annotated.ploc will be overwritten. A copy of the original file will be available as cpa_annotated_old.ploc.

Editing IC Die Properties

You can view and modify the thickness and elevation of a die:

1. Click **Advanced** > **Die Stackup**.

   The **Die Stack Editor** window appears.



2. To modify the name, elevation, thickness, or X and Y minimums and maximums of a particular die, click a cell and enter the new information.
3. Click **OK**.

The **Modeling workspace** is modified according to the values entered. You can save the ANF for future use.

Creating an IC Die Network

If your design contains a set of pins representing connection points for an IC die, you can create an IC Die Network. Such a network consists of resistive and/or capacitive elements that model the on-chip power distribution (e.g., VDD and GND net) interconnect parasitics.

You can place a series resistance and shunt capacitance to ground at chip bumps.

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To create an IC Die Network:

1. Click **Tools** > **Create IC Die Network**.

   The **IC Die Network Generation window** appears.

2. Select the **IC Part Name** from the drop-down menu.
3. Select the reference designator from the **Reference Designator** drop-down menu.
4. Select the power rail net you want to use in the network, from the **Net** drop-down menu.
5. Enter a name for this network in the **Network Name** field.
6. To generate a network that models the on-chip power rail interconnect parasitic resistance:
   a. Select the **Generate Series Resistance** check box.
   b. Enter a value for each resistor in the network in the **Resistance** field.
   c. Select the number of neighbors for the power rail die pin. If you choose **Star Pattern**, each power rail die pin is connected to 8 of its nearest neighboring pins on the same net. For **Grid Pattern**, the pin is connected to 4 of its neighboring pins. This distribution of uniform resistive elements serves as a reasonable approximation of the on-chip power rail resistance.
7. To generate a network that models the on-chip capacitance between the power rail interconnect and the ground rail interconnect:
   a. Select the **Generate Bypass Capacitance (Per Bump)** check box.
   b. Enter a value for each capacitor in the network in the **Capacitance** field.
   c. Optionally, enter a value for the equivalent series resistance (ESR) assigned to each capacitor in the **ESR** field.
   d. Select the name of the ground rail net from the **To Net** drop-down menu.

   A capacitor of the specified value is introduced between each power rail pin and the nearest ground rail pin.

8. Click **Generate**.

   The network is listed in the **Existing RC Networks** box.

9. Optionally, to delete a network, select it from the **Existing RC Networks** box, and then click **Delete Selection**.
10. Click **OK**.

Adding Bondwires between Package and IC

Bondwires connect the integrated circuit to pads on the package.

- Creating Bondwires
- Selecting Bondwires
- Relocating Bondwires

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Creating a Bondwire

SIwave analyzes bondwires using a Method of Moments (MoM) field solver. This solver derives a lumped RLC model (wherein mutual inductance is fully captured, but mutual capacitance—which tends to be small for most bondwire structures—is not). The hybrid field solver then uses this model. It is important that bondwires have a homogenous ground plane to ensure optimal levels of accuracy. Also, to ensure the lumped RLC approximation is valid, the bondwires should be electrically "small". Working within these constraints, this approach provides an extremely fast and accurate electrical description of bondwires.

> **Note:**
>
> When the utmost accuracy is required, you may want to consider a full 3D solution in Ansys HFSS. This is especially useful when bondwires have multiple reference planes (non-homogeneous ground) and become electrically large (electrical wavelength should be about 8 times greater than the physical size of the bondwire being solved).

Bondwire models can be assigned to bondwires. Each bondwire has its own bondwire model.

This command is active only when at least one layer has the type WIREBOND. You can edit the layer properties to change the layer type.

Because bondwires are modeled as traces in SIwave, you first need to draw a trace before creating a bondwire. You can also edit the start and end point of the trace from the top-down view.

To define the bondwires:

1. Click **Home** > **Bondwire Model Editor**.

   The **Bondwire Editor** window appears.

2. Type a model name in the text box. Click the button **Create New Model**. A new bondwire model is created.
3. Select the model type from the **Model** drop-down menu. You can choose from None,JEDEC 4, or JEDEC 5.

   The cross-section for the selected model appears below the **Model** menu.

4. Enter the parameters for the model, using the cross-section as a guide.
5. Select the **Flip Profile About XY-Plane** option if you want to view the bondwire upside-down. This option is not available if the **None** model type is selected.
6. Select the **Static Diagram** option to view a figure defining the model's parameters. This option is not available if the **None** model type is selected.

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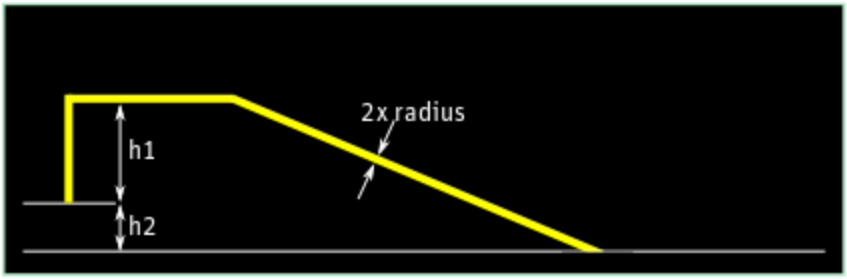
7. Select the **Reverse Pkg & Die** option if you want to switch the position of the package and die points. This option is not available if the **None** model type is selected.
8. Click **OK** to create the bondwire.

Excluding a Bondwire Layer (Model Type None)

Since WIREBOND layers have a thickness of zero, they cannot be excluded by setting their thickness. Choose a model type of **None** if you want to exclude a WIREBOND layer from being exported.

Bondwire Layer Model Type JEDEC 4

Defines the layer as a JEDEC 4-point bondwire model.



The following parameters are available for JEDEC 4 models:

Radius	The radius, in microns, of the bondwire.
h1	The height between the IC die I/O pad and the top of the wire bond loop.
h2	The height of the IC die I/O pad above the lead frame (a negative value if the I/O pad is below the lead frame).

Bondwire Layer Model Type JEDEC 5

Defines the layer as a JEDEC 5-point bondwire model.

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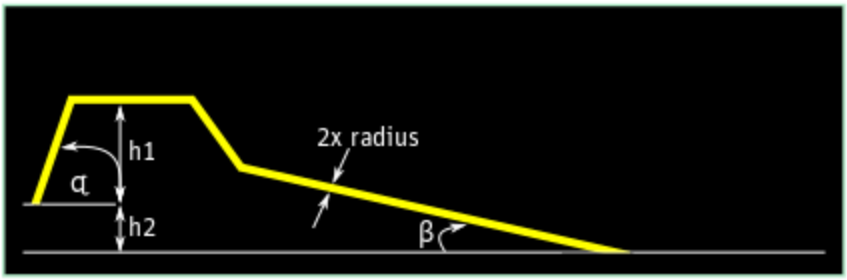

The following parameters are available for JEDEC 5 models:

Radius	The radius, in microns, of the bondwire.
h1	The height between the IC die I/O pad and the top of the wire bond loop.
h2	The height of the IC die I/O pad above the lead frame (a negative value if the I/O pad is below the lead frame).
alpha	The angle in degrees between the xy plane and the wire bond at the IC die I/O pad.
beta	The angle in degrees between the xy plane and the wire bond at the lead frame.

Selecting Bondwires

You can select bondwires on a model-by-model basis. When you check the **Select Bondwires** box in the **Bondwire Model Editor** window, all bondwires with the currently selected model are selected.

Relocating Bondwires

SIwave allows you to change the destination layer of bondwires. You can either relocate selected bondwires or specify the length restrictions to select bondwires.

You may need to move bondwires to different layers to avoid collisions and the resultant electrical shorts. SIwave allows you to assign unique bondwire profiles only on a per-layer basis. When SIwave detects colliding bondwires during a validation check, you can delete the nets that are not critical for your project, or you can relocate them to another layer. To change a bondwire profile to prevent it from colliding with another on the same layer, move (relocate) the bondwire to a different layer and then change that layer's bondwire profile.

To relocate specific bondwires:

1. Select the bondwires in the Modeling workspace.
2. Click **Tools** > **Relocate Bondwires**.

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The **Relocate Bondwires** window appears.

3. Click the **Relocate Selected Bondwires** radio button.
4. Select the **Destination Layer**.
5. Click **OK**.

To relocate bondwires based on length:

1. Click **Tools** > **Relocate Bondwires**.

   The **Relocate Bondwires** window appears.

2. Click the **Relocate Bondwires By Length** radio button.
3. Enter the minimum and maximum values for the **Length Criteria**. Any bondwires with a length between these values will be relocated.
4. Select the **Destination Layer**.
5. Click **OK.**

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7 - Nets

A net is a set of electrically connected traces and pins.

Topics in this section:

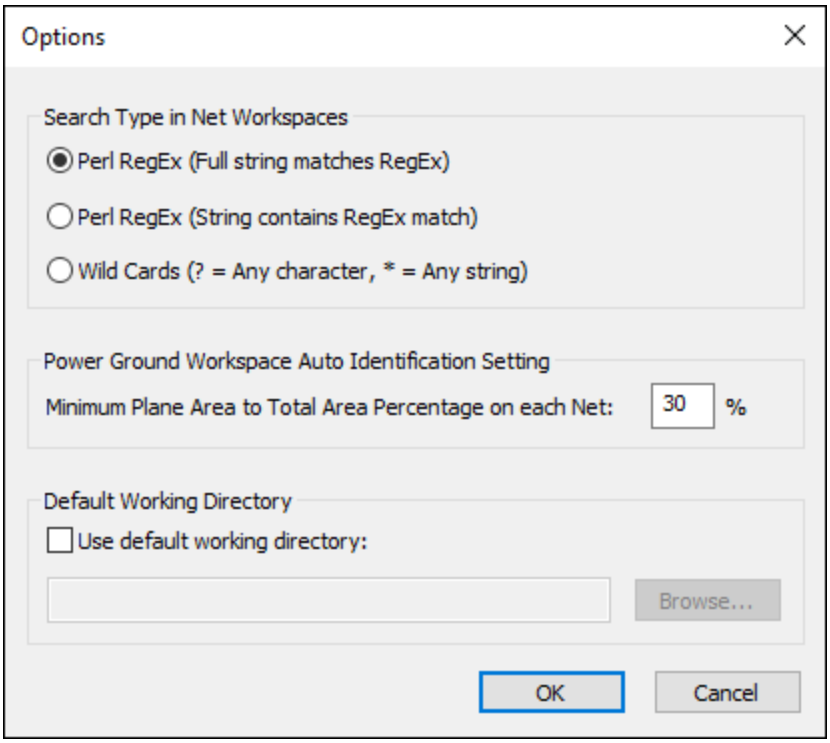
- Net Options
- Working with Nets

Net Options

To set the net options:

1. Click **Home** > **Options**.

   The **Options** window appears.



2. From the **Search Type in Net Workspaces** area, select between **Perl RegEx** (full string matches RegEx), **Perl RegEx** (string contains RegEx match), and **Wild Cards**.
3. From the **Power Ground Workspace Auto Identification Setting** area, select the minimum plane area to total area percentage on each net. The default is 30%.
4. Click **OK**.

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Working with Nets

You can perform various operations on nets:

- Select Nets
- Merge Nets
- Check for DC Short Connections
- Check for Disjoint Nets
- Separate Disjoint Parts of a Net
- Correct Net Misalignments
- Change Net Names
- Compute Net Length
- View Color Modes for Nets
- Use Special Selection between Nets or Components

Working in Net Selection Mode

You can select an individual net by clicking it in the Nets workspace. You can also select a net in the Modeling workspace.

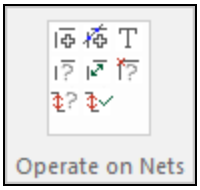
To select an existing net from the Modeling workspace:

1. Click **Home**.
2. From the **Selection Mode** drop-down menu, choose **Net**.
3. Click a net to select it. To select multiple nets, hold the Ctrl key and select the nets.

   The net(s) are highlighted, and properties display in the Properties workspace.

Merging Nets

You can merge two or more nets together using the **Net Operations** toolbox on the **Tools** tab.



You can either force selected nets to merge into one destination net, even if the nets are disconnected electrically, or merge nets into groups based on their electrical connections.

Merging Selected Nets

To merge selected nets:

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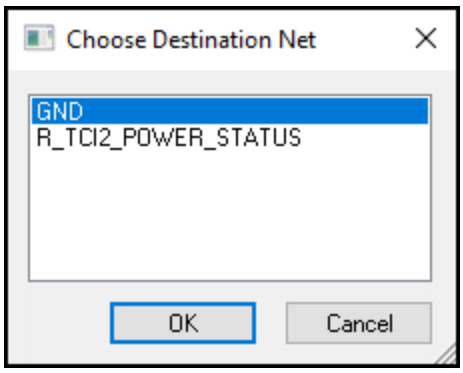
1. From the **Nets** workspace, select the nets you want to merge. Selected nets display with checked boxes.
2. Click **Tools**. From the **Net Operations** box, click the **Merge Selected Nets** ( ) icon.

   The **Choose Destination Net** window appears.



3. Select the net you want to be the destination, and click **OK**.

   SIwave automatically merges all electrically connected nets in the set, typically resulting in a smaller set of nets after merging.

Merging Connected Nets

To merge connected nets:

1. From the **Nets** workspace, select the nets you want to merge. Selected nets display with checked boxes.
2. Click **Tools**. From the **Net Operations** box, click the **Merge Connected Nets** icon ( ).

   SIwave automatically merges all electrically connected nets in the set into a single net. The destination net is chosen arbitrarily. The Messages window displays information about the merged and destination nets.

Checking DC Short Connections

To check the DC short connections:

1. From the **Nets** workspace, select the nets for which you want to check connections. Selected nets display with checked boxes.
2. Click **Tools**. From the **Net Operations** box, click the **Check for DC Short** icon ( ).

If there are no shorts, an alert window states such.

If there are shorted areas, the coordinates are displayed in the Messages window. Click the line showing the XY coordinates to zoom in on the short in the Modeling workspace.

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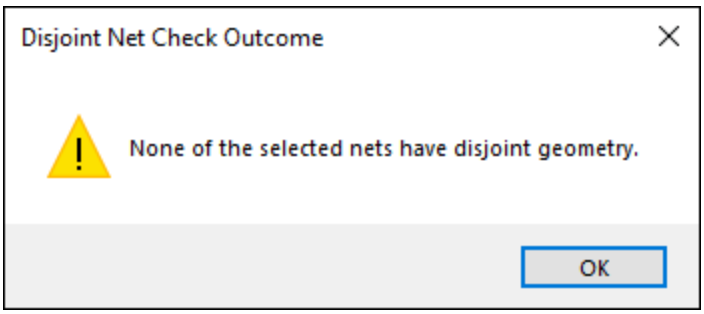
Checking for Disjoint Nets

To check for disjoint nets:

1. From the **Nets** workspace, select the nets you want to check. Selected nets display with checked boxes.
2. Click **Tools**. From the **Net Operations** box, click the **Check if Disjoint** icon ( ).

The **Disjoint Net Check Outcome** window appears, showing the results.



Separating Disjoint Parts

To separate disjoint parts of a net:

1. From the **Nets** workspace, select the nets with parts you want to separate. Selected nets display with checked boxes.
2. Click **Tools**. From the **Net Operations** box, click the **Separate Disjoint Parts** icon ( ).

The **Separate Nets** window appears, showing the results.

Correcting Net Misalignments

If your design has traces whose center lines are not connected to any planes or pads or to the center lines of other traces, you must first validate your project. The Validation Results will include a warning. You can have SIwave automatically fix any misalignment issues from the Validation Results window itself.

Alternatively, to correct misalignments manually, you must clear the **Auto-fix** check box in **Validation Results** (or cancel the **Validation Results** window).

These steps can be performed only after a Validation Check has been run.

To check for misaligned nets:

1. From the **Nets** workspace, select the nets you want to analyze. Selected nets display with checked boxes.

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2. Click **Tools**. From the **Net Operations** box, click the **Check for Misalignment** icon ( ).

   The **Messages Window** shows a list of misaligned nets.

To correct the misalignments:

1. Click **Tools**. From the **Net Operations** box, click the **Correct Misalignment** icon ( ) .

   SIwave adds a small trace segment to previously misaligned areas.

Renaming Nets

You can modify the name of a net.

To rename a net:

1. From the **Nets** workspace, select the net you want to rename. Selected nets display with checked boxes.
2. Click **Tools**. From the **Net Operations** box, click the **Change Net Name** icon ( ).

   The **Enter New Net Name** window appears.

3. Type a new **Net Name** and click **OK**.

   The name of the selected net is changed.

Computing Net Length

You can compute the lengths of all possible paths in a net and calculate the distance between any two net nodes.

To compute net length:

1. From the **Nets** workspace, select the net(s) whose length you want to compute. Selected nets display with checked boxes.
2. Click **Tools**. From the **Inspection Tools** area, click **Compute Net Lengths**.

> **Note:**
>
> Note: You will receive a warning if the signal nets contain planes.

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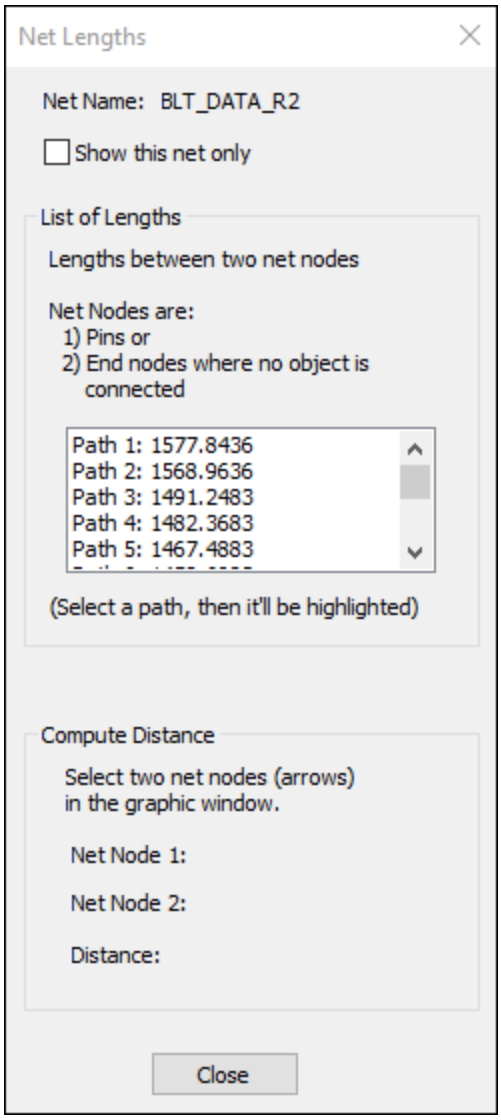
The **Net Lengths** window appears.



The **List of Lengths** displays paths in the net, with the longest net at the top. Click a listed path to highlight it in the Modeling workspace.

From the **Net Lengths** window, you can also compute the distance between two nodes.To do so, select two nodes in the Modeling workspace.

The path between the nodes is highlighted, and the **Compute Distance** field updates to display the distance between the nodes.

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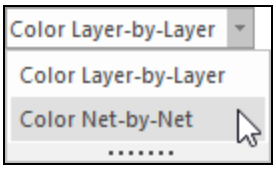
Viewing Color by Net

By default, SIwave displays color on a layer-by-layer basis. You can change this to a net-by-net view.

1. Click **View**.
2. From the **View Options** area, use the **Color Layer-by-Layer** drop-down menu to change the display mode.



Special Selection between Nets or Components

SIwave can automatically select:

- Nets routed between two or more selected components
- Nets that are connected through RLC elements
- Active capacitors, inductors, or resistors between nets

SIwave also allows you to generate summary reports of net connectivity in HTML format.

To perform automatic selections:

1. Select two or more nets (or components, if you are searching for nets routed between components).
2. Click **Home**.
3. From the **Selection** area, use the **Special Select** drop-down menu to make your selection.

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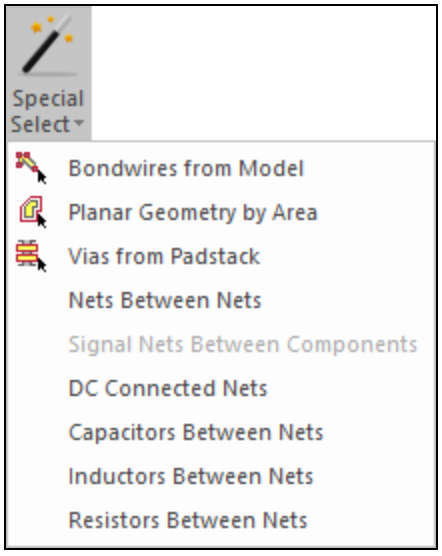

The relevant nets or components are selected, and highlighted in the Modeling workspace.

To generate a net connectivity report:

1. Select a net.
2. Click **Advanced**. From the **Other Edit Tools**, click **Export Connection Report**.

   The **Save As** window opens. You can name and save the HTML file.

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8 - Simulation Setup

SIwave enables you to compute and view the results of analyses such as resonant modes and frequency response.

Earlier topics have covered how to draw or import the components for each layer, specify their material characteristics, and identify sources and vias. The system uses this information to generate an appropriate current solutions.

This section covers actions appropriate to perform successful simulations:

- Auto-Identify Power and Ground Nets
- Define IBIS Models for Pins
- Add Ports
- Add a Voltage Probe
- Define Equipotential Regions
- Detect Close Edges
- Sanitize Layout
- Perform a Validation Check

Identifying Power and Ground Nets

Before starting a simulation of any kind, you must identify the power and ground nets. SIwave can make the identification for you, based on the names of the nets in the design.

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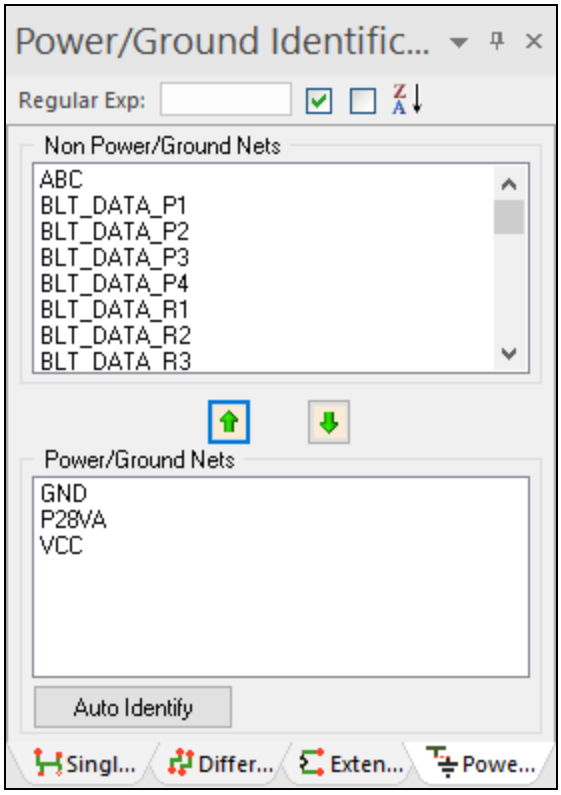
1. From the **Nets** workspace, click the **Power/Ground Identification** tab.



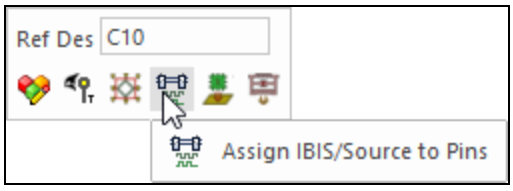
2. Click **Auto Identify** to have SIwave find power and ground nets by name.

Defining IBIS Models for Pins

As a preliminary step before running the Signal Net Analyzer or the SIWizard, you need to specify the IBIS buffer models to use for any pins that will be analyzed or cosimulated. IBIS buffer models are selected from the library of available models.

To define the IBIS buffer model:

1. Select a component to view its mini toolbar. Click **Assign IBIS/Source to Pins**.



   This menu option can also be found on the **Advanced** tab.

   The **Assign IBIS Model & Excitation Source to individual pins** window appears.

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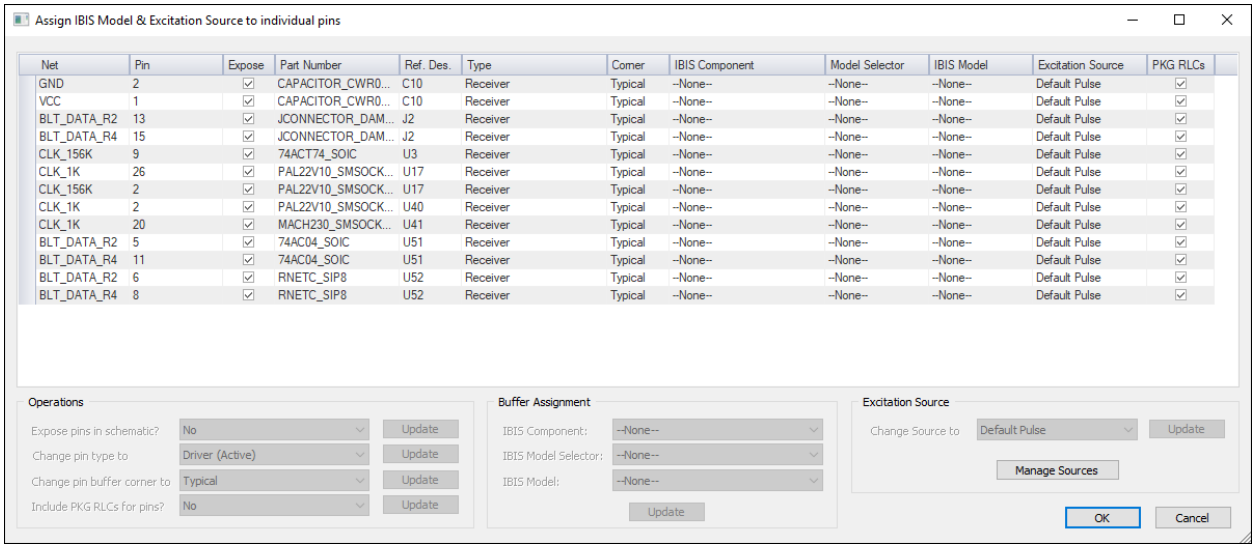

2. Under **Default Buffer Models,** set the **Class** to **IBIS**.
3. Set the buffer **Type** to the Driver or Receiver type that matches the component.
4. Set the **Corner** behavior to Minimum, Typical, or Maximum (Typical is the default).
5. Use the menu in the **Component** field to select the IBIS model.

> **Note:**
>
> IBIS buffer models are located under the buflib\IBIS directory in the AnsysEM install directory. You can change the buflib directory in SIwave Options.

For most components, this completes the IBIS buffer assignment. If the IBIS file is well-documented, the buffer models are automatically assigned based on the pin names. Steps 6-8 are for exceptions.

6. Use the **Model Override** menu to select a particular driver or receiver model from those available.
7. Use the **Override For** field to specify the pins that will use the override model rather than the default. Generally, override involves **Only Unmatched Pins**.
8. Use the **Individual Pin Overrides Edit** button or click **Edit > Assign IBIS/Source to Pins** to assign models for pins on a pin-by-pin basis.

   The **Assign IBIS Model & Excitation Source to individual pins** window appears. You can also directly assign excitations on a pin-by-pin basis. You can see the nets with pins identified, and can also specify the IBIS component and buffer model to use for the ports on the nets.

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a. Click on any column heading (e.g., **Ref. Des.**) to sort the table using the elements in that column).
b. Check the **Expose** check box for any pin that is to be an external connection to the Ansys Electronics Desktop circuit.
c. Click on the **Type** field for a net to select the IBIS buffer type—Driver (active), Driver (inactive), Receiver, Receiver (with termination), Passive termination.
d. Click on the **Corner** field to select the range for parameters (typical, minimum, maximum).
e. Click on the **IBIS Component** field to select a component from the library of IBIS buffer elements. The choice of **Component** determines the available models and model selectors for each buffer type.
f. When the buffer type includes model selectors, the **Model Selector** field is populated. In his case, you must choose a model selector, then a model from the ones available for that model selector. If no model selectors have been defined, leave the field at the default - none.
g. Click on the **IBIS Model** field to select the model from the listing. The available models depends on the model selector, if any.
h. Click on the **Excitation Source** field to select the source for the input excitation to the net. Optionally, click the Manage Sources button to view the available sources, change the parameters of existing sources, or define new sources.
i. Check the **PKG RLCs** check box to include the RLC Package model for the buffer model.
j. Select the **Excitation Source**. To add or delete sources, click **Manage Sources**. The **Manage Sources** window appears. You can **Add New Source** or **Delete Selected Sources**. Then, click **OK** to return to the **Assign IBIS Model & Excitation Source to individual pins** window.

Defining Equipotential Regions

The DC IR drop solver uses equipotential regions to force equal voltage across a specified region, including specified pads.

To define equipotential regions:

1. Click **Home**. From the **Draw Geometry** box, click the Define Equipotential Regions icon ( ).

   The **Define Equipotential Regions** window appears.

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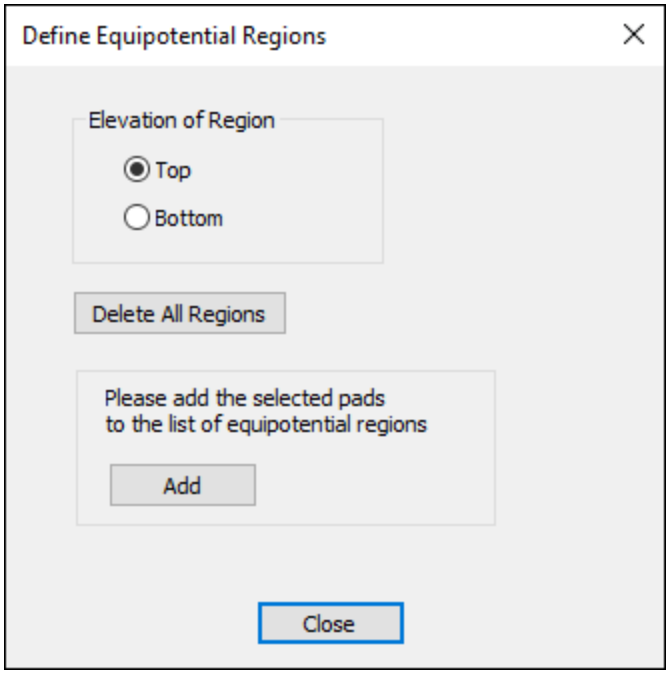

The cursor is activated to draw a rectangle.

2. From the **Elevation of Region** area, choose whether to draw the region at the **Top** or **Bottom**.
3. If appropriate, click **Delete All Regions** to erase any previously defined regions.
4. If appropriate, click **Add** to add selected pads to the list of equipotential regions.
5. Click **Close** to end the definition.

Detecting Close Edges

To have SIwave check for edges of selected nets and layers, or of selected objects:

1. Click **Advanced**.
2. Click **Detect Close Edges**.

   The **Close Edge Detector** window appears.

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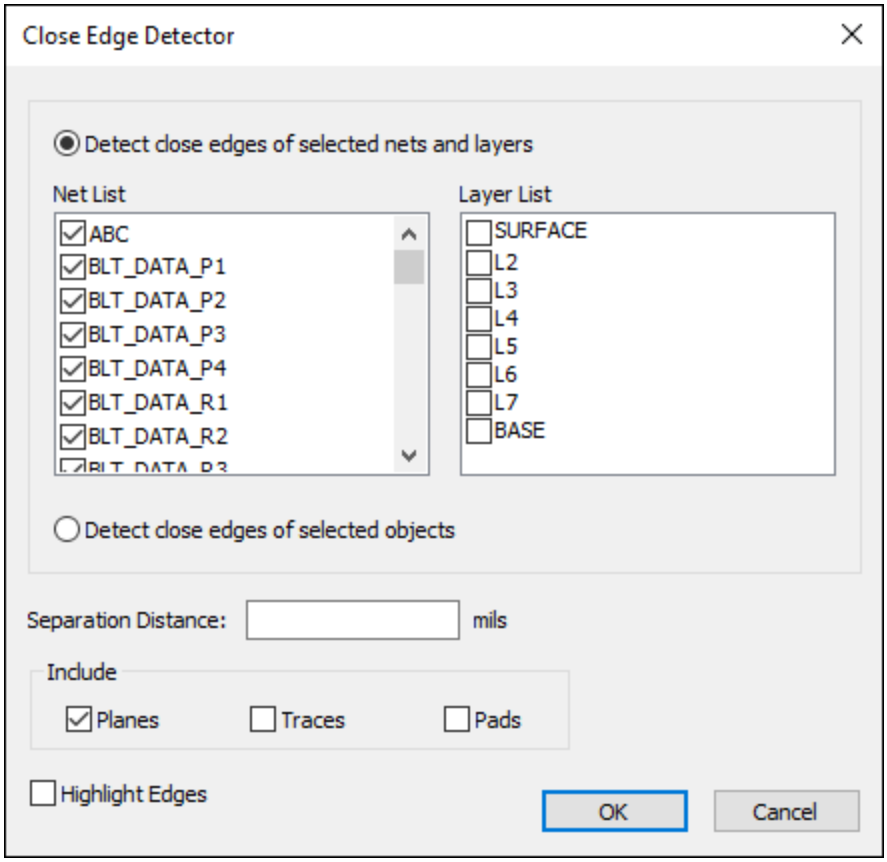

3. If no objects have been selected, the **Detect close edges of selected nets and layers** radio button is selected. Use the check boxes to select one or more nets and layers.
4. If you have already selected objects in the Modeling workspace, the **Detect close edges of selected objects** radio button is selected.
5. Enter a **Separation Distance** in the specified unit.
6. Use the check boxes to decide whether to include planes, traces, and/or pads.
7. If appropriate, check the **Highlight Edges** check box to highlight edges in the Modeling workspace.
8. Click **OK**.

   The check locates edges that are closer than the separation distance.

   The check does not detect violations of the separation distance for trace gaps, trace-to-trace, or trace-to-plane.

Sanitizing Layout

Sanitize Layout is an operation for cleaning power and ground nets in order to fix certain alignment problems as well as complexities that may slow down simulation. It works by uniting

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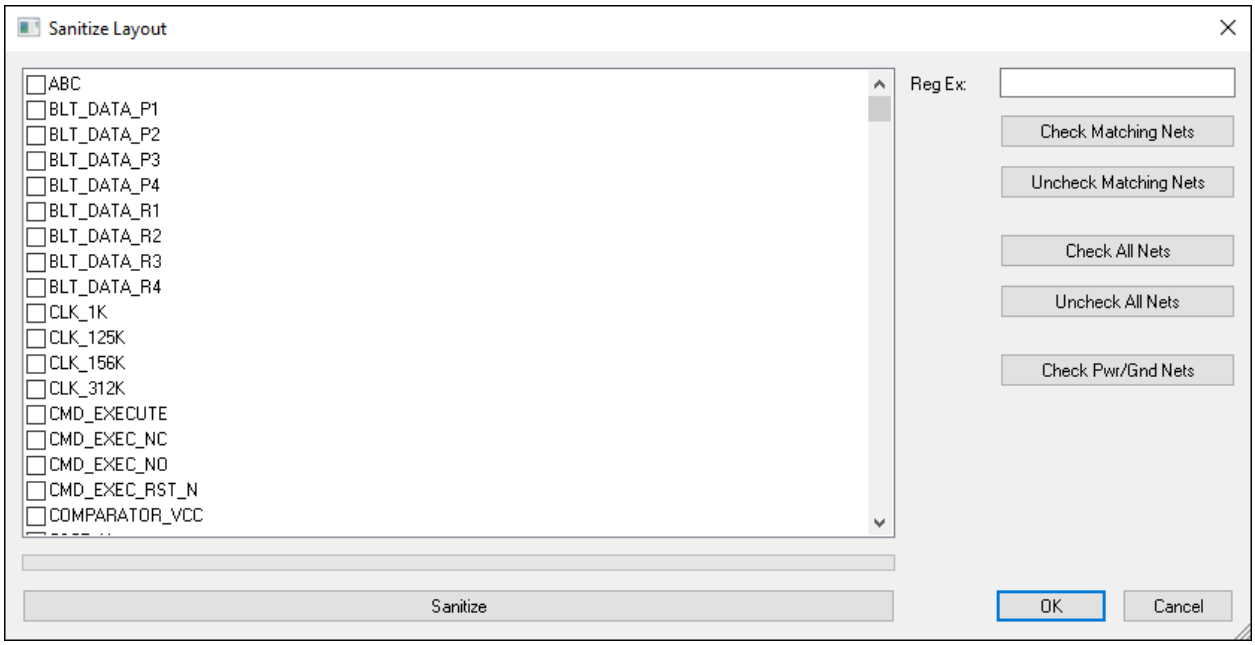
the planes and traces for each net to be cleaned. Once the united planes are formed, portions that display trace-like properties are converted into traces. Under certain conditions, these traces are extended in order to improve their connection with vias, pads, and the remaining planes. Lattices originally formed from multiple traces become planes with cutouts after the sanitization process.

To sanitize the layout in the active project:

1. Click **Tools**.
2. From the **Inspection Tools** area, click **Sanitize Layout...** Alternatively, open the SIwave Workflow Wizard and click **Sanitize Layout for Simulation**.

   The **Sanitize Layout** window opens, with all power and ground nets selected.



3. You can add nets directly from this window.
   - **Check All Nets** – click to select all nets.
   - **Uncheck All Nets** – click to deselect all nets.
   - **Check Pwr/Gnd Nets** – click to select power and ground nets only. This is the default selection.
   - **Reg Ex** – use this field to type a regular expression and search for nets. Click **Check Matching Nets** to select matches, or click **Uncheck Matching Nets** to deselect matches.
4. Click **Sanitize** to run Sanitize Layout on the selected nets.
5. Click **OK**.

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Performing a Validation Check

Before running an analysis on a model, it is important to first perform a validation check on the project. During this process, SIwave runs a check on all the setup details of the project to verify that all appropriate steps have been completed and that their parameters are reasonable.

Note:

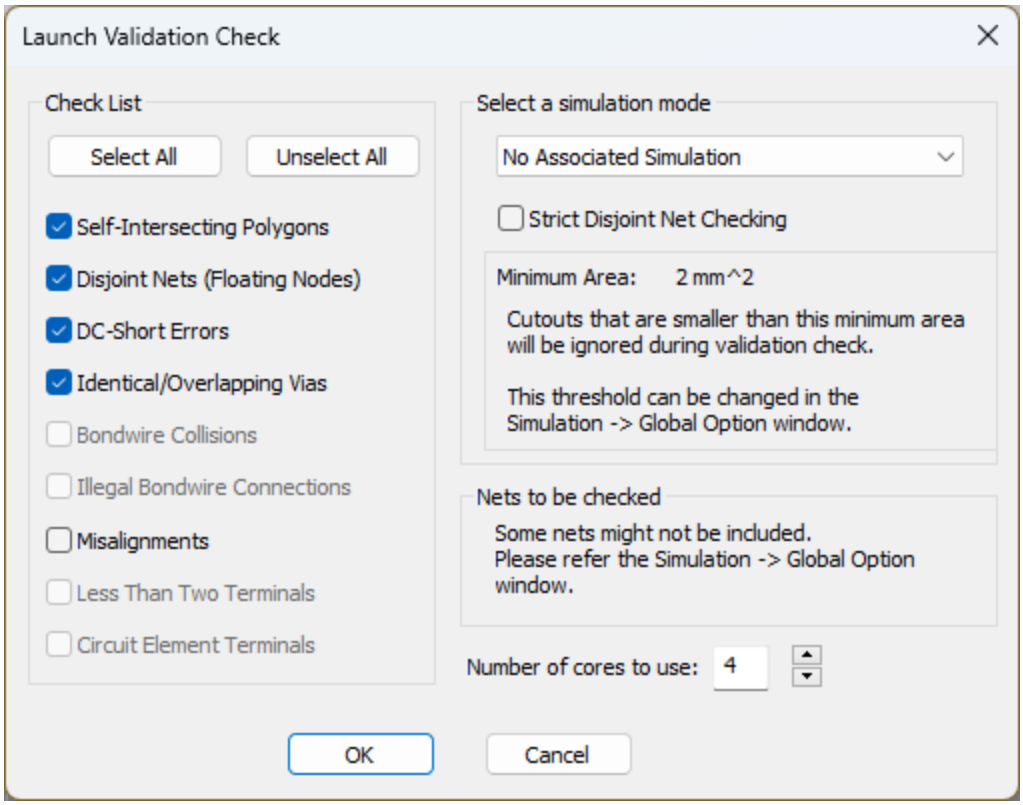
To improve response time when SIwave is run over a remote desktop:

- Informational tool tips do not appear.
- Dynamic zoom is deactivated.
- Faster transformation is activated.

To perform a validation check on the active project:

1. Click **Tools**.
2. From the **Inspection Tools** area, click **Validation Check**.

   The **Launch Validation Check** window appears.



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3. Select the type of simulation you are preparing to perform from the **Select a simulation mode** drop-down menu.
4. The **Select a simulation mode** and **Nets to be checked** areas give further information about the simulation.
5. Use the **Check List** to select errors to check.
   - **Self-Intersecting Polygons** – checks for duplicating planes and intersecting edges, and whether voids intersect plane boundaries.
   - **Disjoint Nets (Floating Nodes)** – checks for any nets that are not completely connected.
   - **DC-Short Errors** – checks for overlapping nets.
   - **Identical/Overlapping Vias** – checks for identical vias, or vias that overlap on the same nets.
   - **Bondwire Collisions** – checks for duplicate or overlapping bondwires.
   - **Illegal Bondwire Connections** – checks for vias with a greater inner radius than that of the bondwire, and for bondwires that extend through their pad.
   - **Misalignments** – checks for trace intersect issues (with planes and traces), and pad/via intersect issues (with planes and traces).
   - **Less Than Two Terminals** – flags traces with fewer than two terminals. This field is only active for the legacy TPA solution simulation mode (can be enabled through environment variable).
   - **Circuit Element Terminals** – flags circuit element terminal connection errors. This field is only active for CPA Solutions.

   In addition to the previous checks mentioned, two checks are always performed, regardless of the simulation mode selected:
   - **Traces-Inside-Traces** – flags and automatically corrects traces completely contained within another trace.
   - **Floating Planes** – provides the locations of floating planes or vias. If there are any floating planes, there are disjoint nets.
6. Select the **Number of cores to use**. This number should be the same as that on the **Multiprocessing** tab of **SIwave Options**.
7. Click **OK**.

   The **Validation Check Results** window appears, listing errors and warnings.

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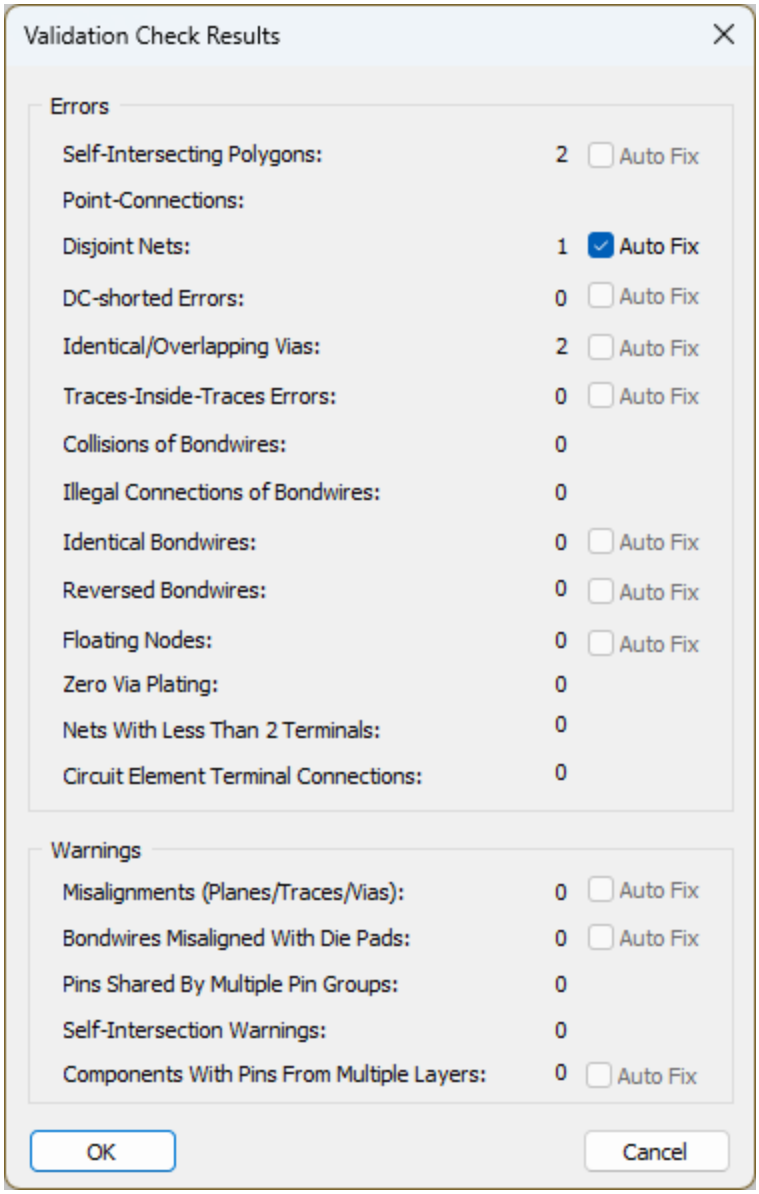

Items that SIwave can fix automatically have **Auto Fix** check boxes. To allow SIwave to fix these, select the **Auto Fix** check box and click **OK**.

Running EMI Scanner

Ansys EMI Scanner identifies design issues that might result in electromagnetic interference problems during operation. Such problems can stem from a compromised power delivery network or from improperly shielded signal nets. This feature, which is based on geometric rule checks, scans complete layouts quickly and can be used to identify subsections of the design requiring more rigorous analysis using the SIwave or HFSS finite element-based solvers.

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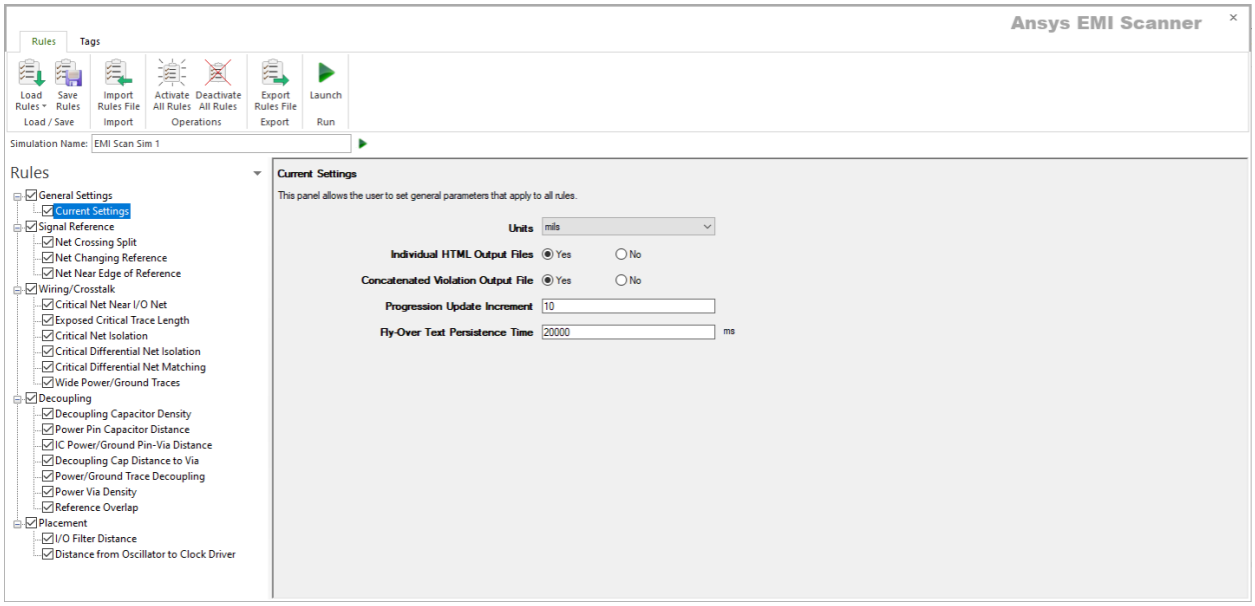
To launch EMI scanner:

1. Click **Simulation** > **EMI Scanner**.

   The **Ansys EMI Scanner** window appears, on the **Rules** tab.

2. If appropriate, use the **Simulation Name** field to rename the scan.
3. Set rules, as appropriate.
4. Select the **Tags** tab.

   The **Tags** tab displays.

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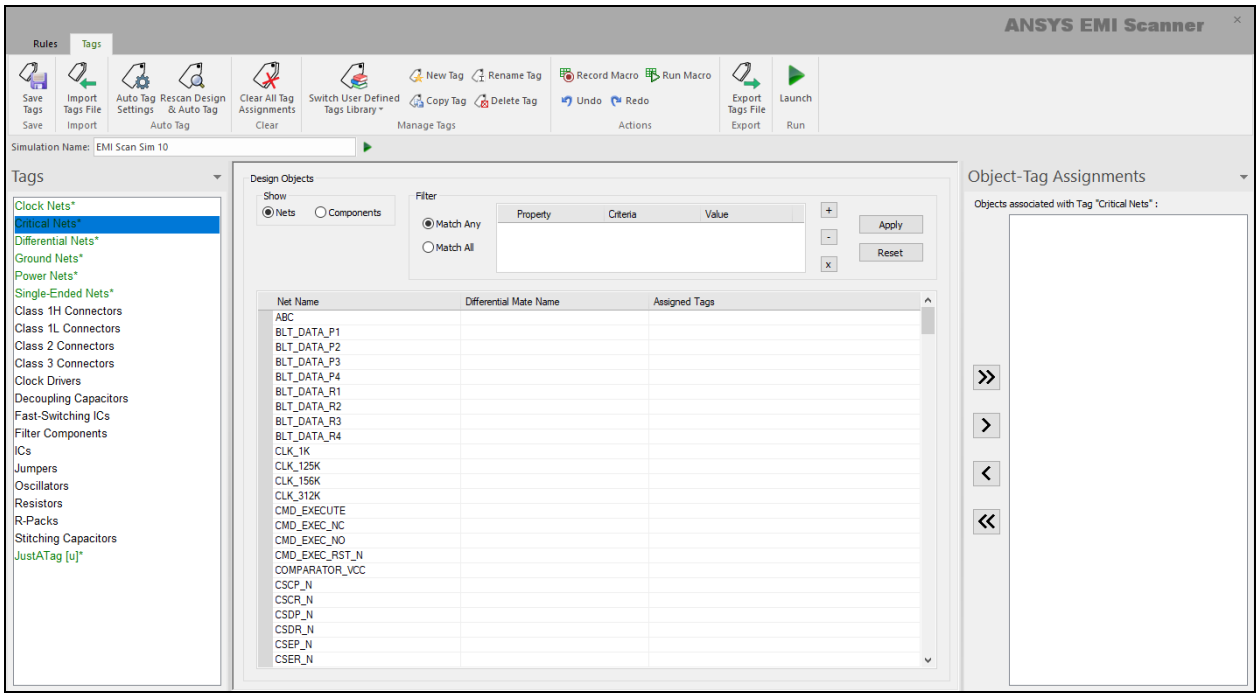
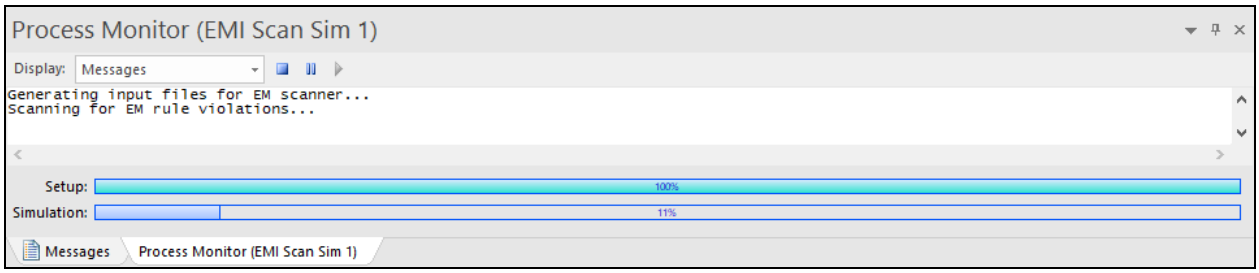


5. Assign tags, as appropriate.
6. Click **Launch**.

   The **Messages** window updates to show EMI Scanner progress.



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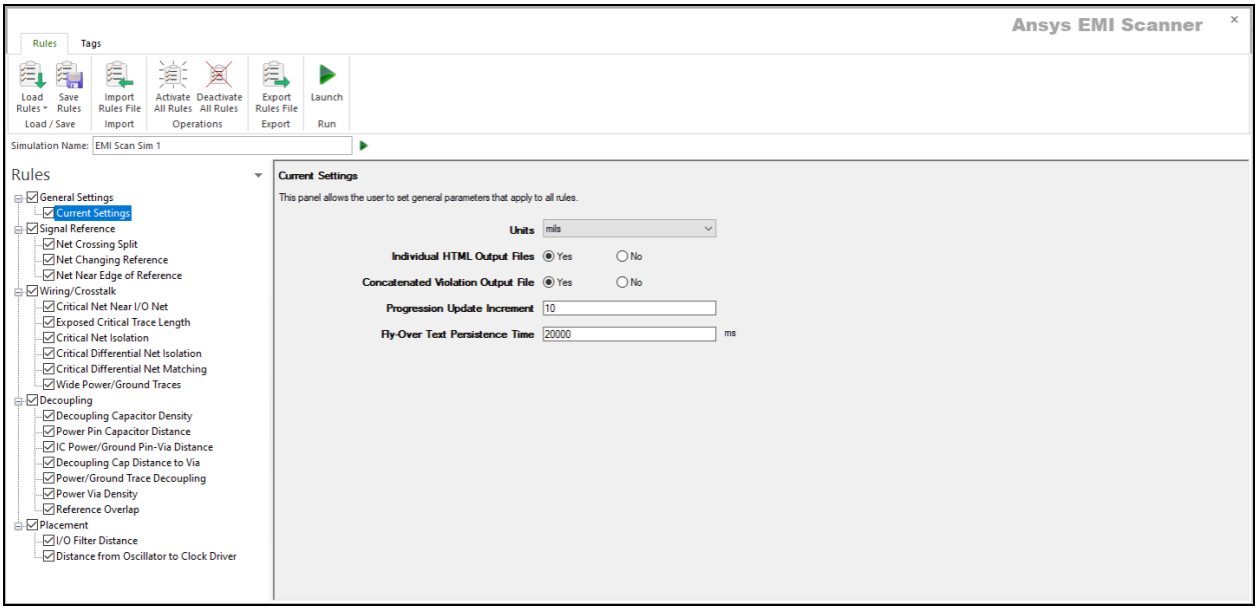
Setting Rules in EMI Scanner



The EMI Scanner **Rules** tab contains the following buttons:

- **Load Rules** – allows you to select from a series of pre-defined rule sets to load into the Rules pane:
  - **Default EM Rules Profile** – contains the basic rule set for analyzing electromagnetic interference.
  - **Default SI Rules Profile** – contains the basic rule set for analyzing signal integrity.
  - **Default EM+SI Rules Profile** – contains all rules from both the Default EM Rules Profile and the Default SI Rules Profile.
  - **Default Rules Profile (0 - 100MHz)** – contains the recommended rule set for frequencies ranging from 0 - 100MHz.
  - **Default Rules Profile (100MHz - 500MHz)** – contains the recommended rule set for frequencies ranging from 100 - 500MHz.
  - **Default Rules Profile (500MHz - 1000MHz)** – contains the recommended rule set for frequencies ranging from 500 - 1000MHz.
  - **Default Rules Profile (1GHz+)** – contains the recommended rule set for frequencies 1GHz and above.
- **Save Rules** – applies changes to the rule profile.
- **Import Rules File** – allows you to import rules via an XML file.
- **Activate All Rules** – selects all check boxes in the Rules pane.
- **Deactivate All Rules** – deselects all check boxes in the Rules pane.

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- **Export Rules File** – allows you to export the current rule settings in XML format.
- **Launch** – begins the EMI scan.

To set rules for an EMI Scan:

1. Use the **Load Rules** drop-down menu to select a pre-defined rules profile, or click **Import Rules File**.

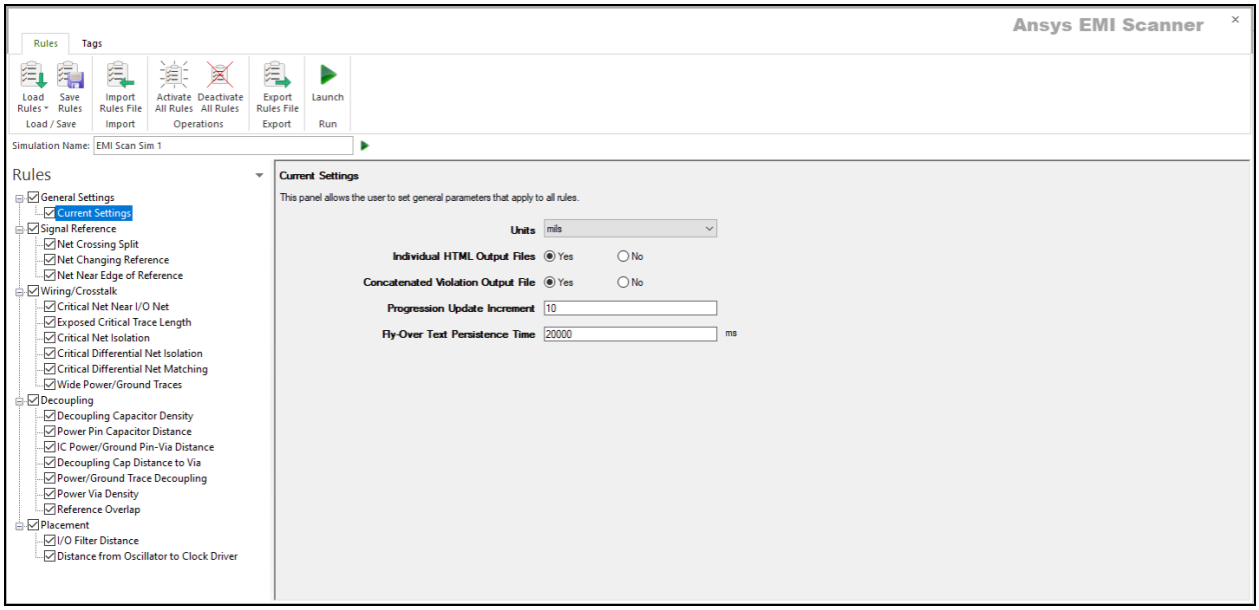
   The **Rules** pane updates to show all applicable rules for the selected profile.
2. From the **Rules** pane, use the check boxes to activate and deactivate rules, as appropriate. You can also **Activate All Rules** or **Deactivate All Rules**.
3. Change the General Settings, as well as settings for Signal Reference, Wiring/Crosstalk, Decoupling, Placement, Net Integrity, Via Integrity, and Power Integrity rules, as appropriate.

Applying EMI Scanner General Settings

To change EMI Scanner General Settings:

1. Launch EMI Scanner.

   The **EMI Scanner** window appears, on the **Rules** tab.



2. The **Current Settings** display by default. If they do not, in the Rules pane, select **General Settings > Current Settings**.

   The **Current Settings** display.

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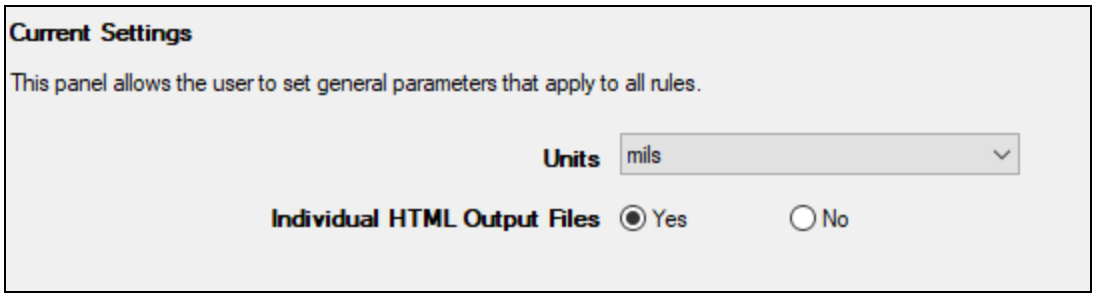


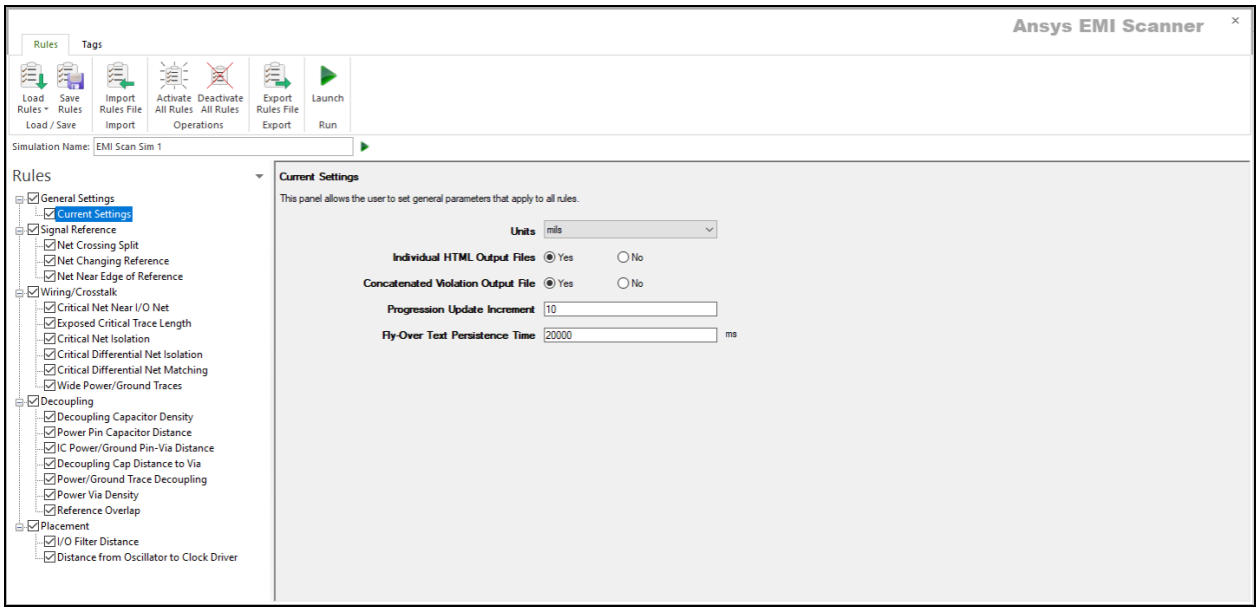
3. From this screen, you can set the following:
   - **Units** – selects the unit in which other rules are measured.
   - **Individual HTML Output Files** – selects whether to export EMI Scanner results as one large, combined HTML file or as individual HTML files. See Exporting EMI Scanner Results.
4. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

Applying Signal Reference Rules

To change EMI Scanner Signal Reference rules:

1. Launch EMI Scanner.

   The **EMI Scanner** window appears, on the **Rules** tab.



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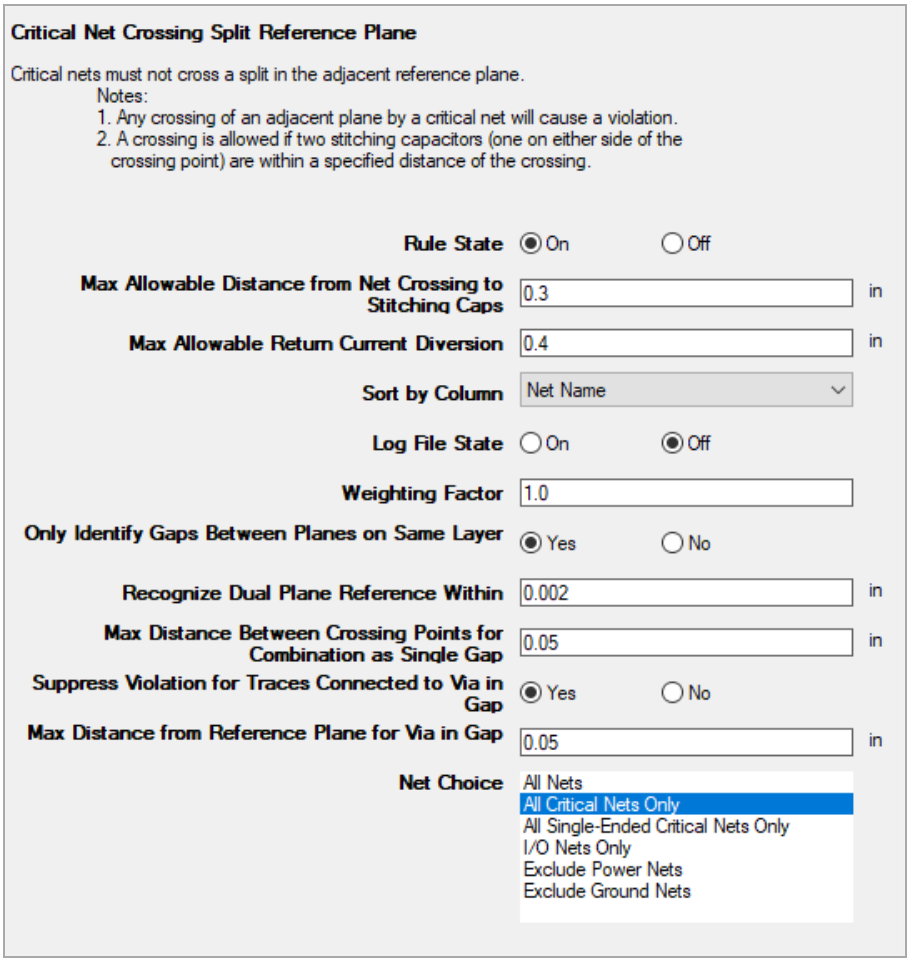
2. From the Rules pane, select one of the three subcategories under **Signal Reference**:
   - **Net Crossing Split** – displays **Critical Net Crossing Split Reference Plane** rule configuration.



This rule states that critical nets must not cross a split in the adjacent reference plane. A cross is allowed only if two stitching capacitors are within a specified distance of the crossing.

From here, you can set the following:

- **Rule State** – toggles Net Crossing Split rules on or off.
- **Max Allowable Distance from Net Crossing to Stitching Caps** – sets the maximum distance from the point where the net crosses a split in its reference plane. Two stitching capacitors must be found within this distance.
- **Max Allowable Return Current Diversion** – sets the maximum distance for a return current diversion. If a signal's return current can divert itself around the gap in the reference plane, the total distance of the diversion must be less than this value.
- **Sort by Column** – specifies the column by which results are sorted.

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- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Only Identify Gaps Between Planes on Same Layer** – determines whether gaps are only between planes on the same layer or not. When the rule tries to pair up nearby plane boundary crossing points and identify gaps, this parameter enables or disables a check for layer commonality.
- **Recognize Dual Plane Reference Within** – instructs EMI Scanner to consider both planes as a reference when checking for gap crossing when the distance difference to each plane is less than the specified distance. This allows recognition of both planes as references for strip line traces when the trace is offset from the exact center by a small amount (normally for manufacturing reasons).
- **Max Distance Between Crossing Points for Combination as a Single Gap** – sets the maximum distance for combining crossing points into a single violation (e.g., the entrance and exit of a gap between planes). Too large a value can cause the algorithm to pair up unrelated crossing points, and too small a value can prevent crossing points from being paired up, resulting in more violations. It is recommended to set the value to a reasonable distance based on the board design technology being used (e.g., slightly larger than the typical plane separation within a layer).
- **Suppress Violation for Traces Connected to Via in Gap** – determines whether to ignore trace crossing split/gap when connected to a via within that gap.
- **Max Distance from Reference Plane for Via in Gap** – sets the maximum distance for which via violations within a gap will be suppressed. If the trace extends greater than this distance from the edge of the reference plane to the via, its violation will not be suppressed.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Net Changing Reference** – displays **Critical Net Changing Reference Plane** rule configuration.

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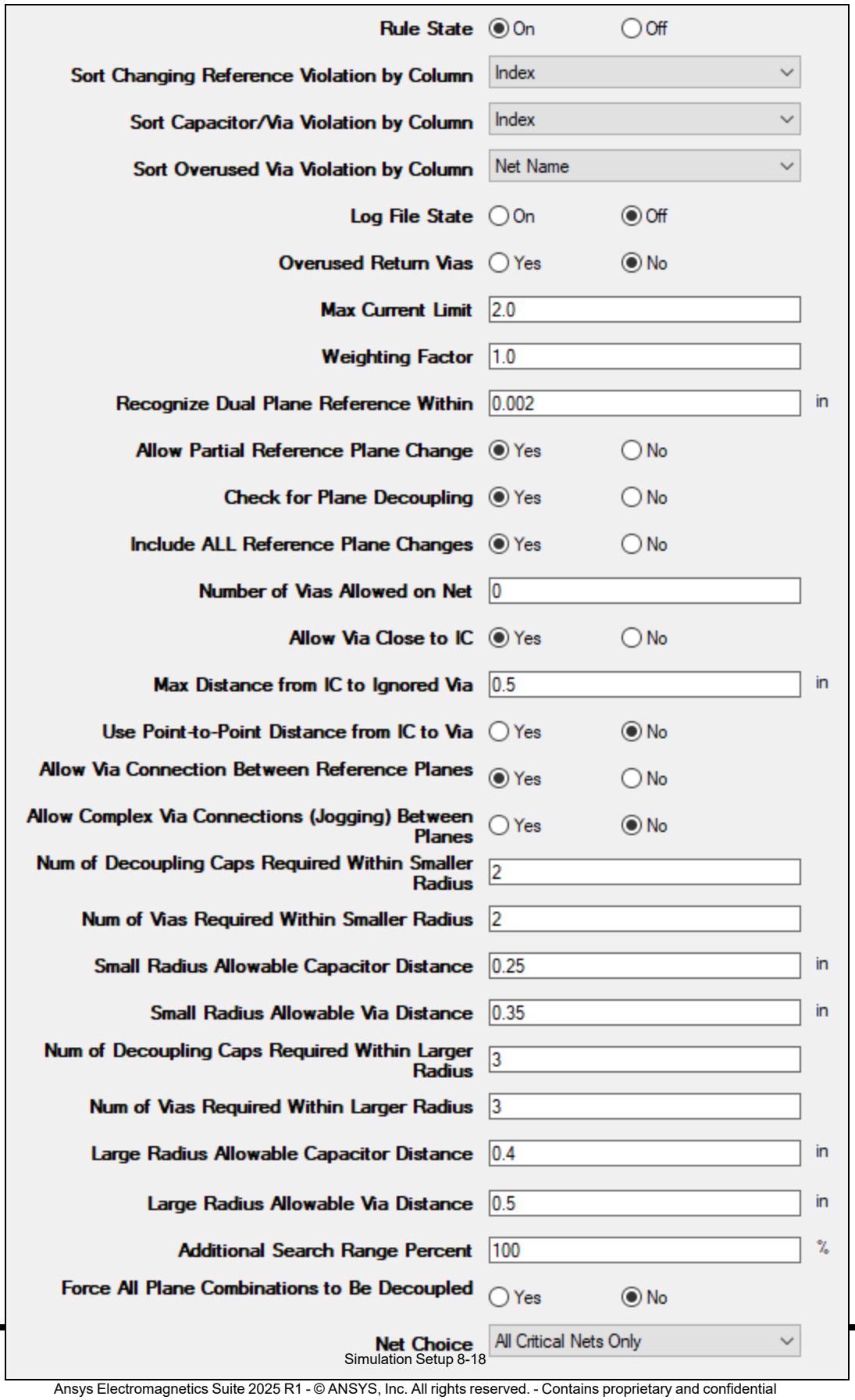

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This rule states that critical nets must not change reference planes.

> **Note:**
>
> 1. Any change in the reference plane for a critical net will cause a violation.
> 2. Reference plane changing is allowed if two decoupling capacitors (or vias if the planes share the same net name) are within a specified radial distance from the signal via where the signal changes reference planes.
> 3. Reference plane changing is allowed if three decoupling capacitors (or vias if the planes share the same net name) are within a specified radial distance from the signal via where the signal changes reference planes.
> 4. Reference plane changing can be ignored when the initial via is within a specified distance from its IC pin (transmit or receive).

From here, you can set the following:

- **Rule State** – toggles Net Changing Reference rules on or off.
- **Sort Changing Reference Violation by Column** – specifies the column by which Changing Reference Violation results are sorted.
- **Sort Capacitor/Via Violation by Column** – specifies the column by which Capacitor/Via Violation results are sorted.
- **Sort Overused Via Violation by Column** – specifies the column by which Overused Via Violation results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Overused Return Vias** – determines whether EMI Scanner checks for overused return vias.
- **Max Current Limit** – specifies the maximum number of signal currents that a via should carry. Use in conjunction with **Overused Return Vias**.
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Recognize Dual Plane Reference Within** – instructs EMI Scanner to consider both planes as a reference when checking for gap crossing when the distance difference to each plane is less than the specified distance. This allows recognition of both planes as references for strip line traces when the trace is offset from the exact center by a small amount (normally for manufacturing reasons).
- **Allow Partial Reference Plane Change** – instructs EMI Scanner to ignore a violation if one of the two reference planes remains a reference plane on both sides of the via transition.

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- **Check for Plane Decoupling** – instructs EMI Scanner to ignore a violation if a decoupling capacitor exists between the two reference planes (entering reference plane and leaving reference plane) and is within a specified distance of the signal via (see additional settings below).
- **Include ALL Reference Plane Changes** – instructs EMI Scanner whether to display all reference plane changes. When there are two associated reference planes for the entry to the via, and two different associated reference planes for the trace leaving the via, selecting 'yes' will show two violations for this transition. If 'no' is selected and a decoupling capacitor exists between one of the entering reference planes and one of the leaving reference planes (within the specified distance), no violation will be reported, even though the two other reference planes do not have any connection.
- **Number of Vias Allowed on Net** – specifies the number of via reference plane changes that are allowed on critical nets. If no vias are appropriate except the 'escape' via close to the IC, set this parameter to zero, and set **Allow Via Close to IC** to 'yes'.
- **Allow Via Close to IC** – determines whether to ignore vias that are close to the IC and are required to get a trace from the surface to an inner layer.
- **Max Distance from IC to Ignored Via** – specifies the maximum distance between IC and via at which vias are ignored.
- **Use Point-to-Point Distance from IC to Via** – if 'yes' is selected, the actual trace path length is NOT calculated. This option allows EMI Scanner to check rules faster, but may cause violations to be ignored incorrectly.
- **Allow Via Connection Between Reference Planes** – allows a via to be used to connect reference planes (to provide return current path) when the two reference planes share the same net name.
- **Allow Complex Via Connections (Jogging) Between Planes** – allows a set of vias (e.g., 'blind' vias that do not extend through all layers) to be used to connect reference planes (to provide return current path) when the two reference planes share a net name. This advanced checking requires extra processing time because all vias found in the larger via radius are considered as potential paths.
- **Num of Decoupling Caps Required Within Smaller Radius** – when **Allow Partial Reference Plane Change** is selected, a return current path (when a critical net changes reference planes) may be provided with either capacitors or vias. This setting specifies the number of capacitors required within the smaller radius.
- **Num of Vias Required Within Smaller Radius** – when **Allow Partial Reference Plane Change** is selected, a return current path (when a critical net changes reference planes) may be provided with either capacitors or vias. This setting specifies the number of vias required within the smaller radius. A via between planes is a lower impedance/inductance connection then a decoupling capacitor, so you may want to specify a different setting.
- **Small Radius Allowable Capacitor Distance** – specifies the smaller radius used with the **Num of Decoupling Caps Required Within Smaller Radius** setting.

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- **Small Radius Allowable Via Distance** – specifies the smaller radius used with the **Num of Vias Required Within Smaller Radius** setting.
- **Num of Decoupling Caps Required Within Larger Radius** – if a smaller radius is not specified, this allows specification of a larger radius for a larger number of decoupling capacitors.
- **Num of Vias Required Within Larger Radius** – if a smaller radius is not specified, this allows specification of a larger radius for a larger number of vias. A via between planes is a lower impedance/inductance connection then a decoupling capacitor, so you may want to specify a different setting.
- **Large Radius Allowable Capacitor Distance** – specifies the larger radius used with the **Num of Decoupling Caps Required Within Larger Radius** setting.
- **Large Radius Allowable Via Distance** – specifies the larger radius used with the **Num of Vias Required Within Larger Radius** setting.
- **Additional Search Range Percent** – specifies an additional search range beyond the larger radius for additional capacitors. For example, if the larger radius is set to 500mils and the Additional Search Range Percent is 100%, EMI Scanner will report capacitors within 1000mils when a violation occurs.
- **Force All Plane Combinations to Be Decoupled** – determines whether to decouple all reference plane combinations. See Technical Note.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Net Near Edge of Reference** – displays **Critical Net Near Edge of Reference Plane** rule configuration.

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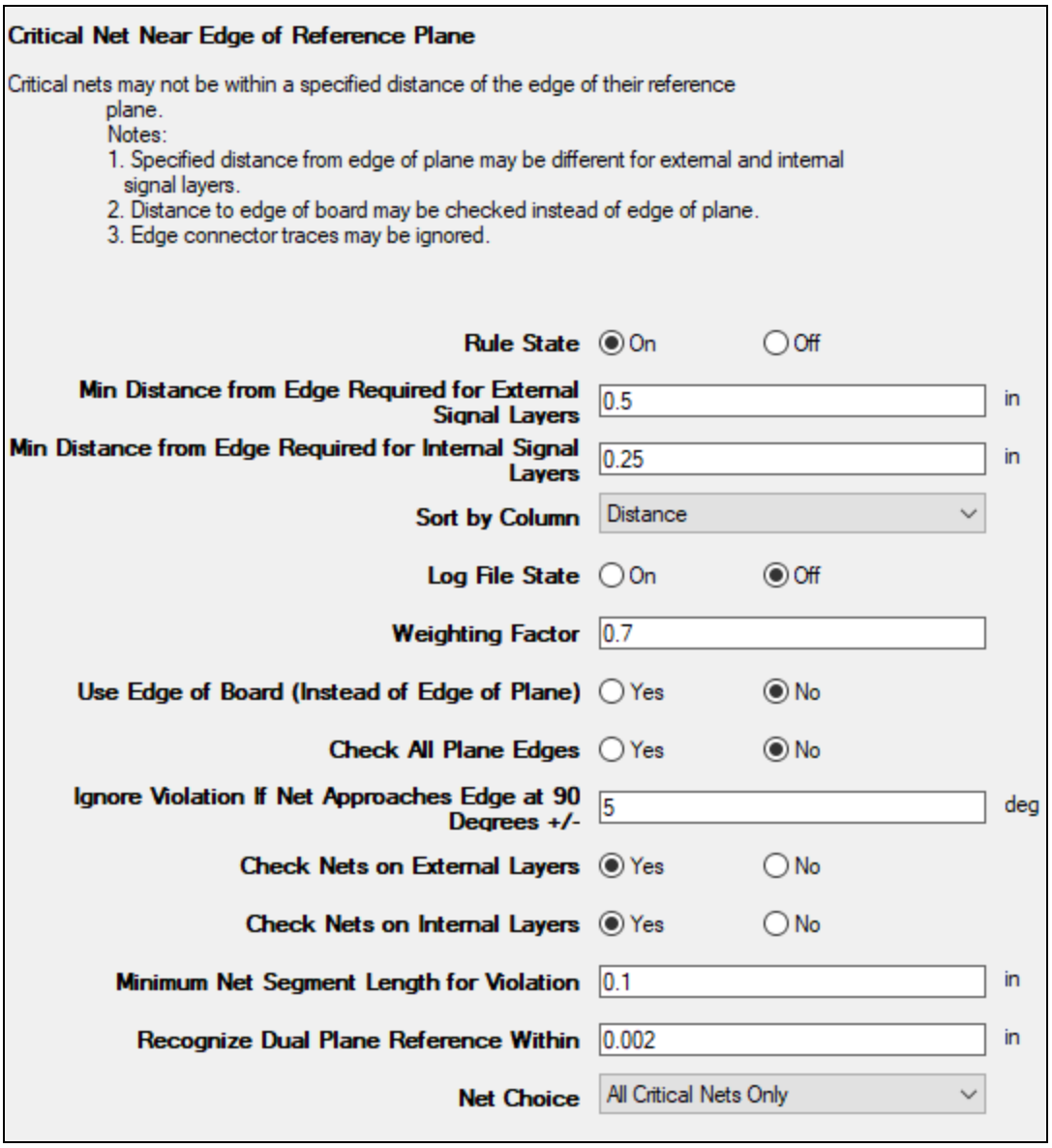

This rule states that critical nets must not be within a specified distance of the edge of their reference plane.

From here, you can set the following:

- **Rule State** – toggles Net Near Edge of Reference rules on or off.
- **Min Distance from Edge Required for External Signal Layers** – specifies the minimum distance that must exist between the edge of the reference plane and a critical signal net when the net is on an external layer.

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- **Min Distance from Edge Required for Internal Signal Layers** – specifies the minimum distance that must exist between the edge of the reference plane and a critical signal net when the net is on an internal layer.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Use Edge of Board (Instead of Edge of Plane)** – allows you to check distance from critical nets to the edge of the board instead of the edge of the reference plane. This can be useful if the board is only partially complete and all reference planes are not yet completed.
- **Check All Plane Edges** – checks the distance from nets to any edge of their reference plane, rather than limiting the check to reference plane edges near the edge of the board
- **Ignore Violation If Net Approaches Edge at 90 Degrees +/-** – EMI Scanner ignores edge connectors that approach the edge of the reference plane or board at a 90 degree angle. This option specifies a tolerance that allows the approach to be slightly off a perfect 90 degrees.
- **Check Nets on External Layers** – specifies whether nets on external layers should be checked.
- **Check Nets on Internal Layers** – specifies whether nets on internal layers should be checked.
- **Minimum Net Segment Length for Violation** – specifies the minimum net segment length before EMI Scanner will report a violation if the net is within the specified distance from the edge of the reference plane or board.
- **Recognize Dual Plane Reference Within** – instructs EMI Scanner to consider both planes as a reference when checking for traces too close to the edge of the reference planes when the distance difference to each plane is less than the specified distance. This allows recognition of both planes as references for strip line traces when the trace is offset from the exact center by a small amount (normally for manufacturing reasons).
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

3. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

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Note:

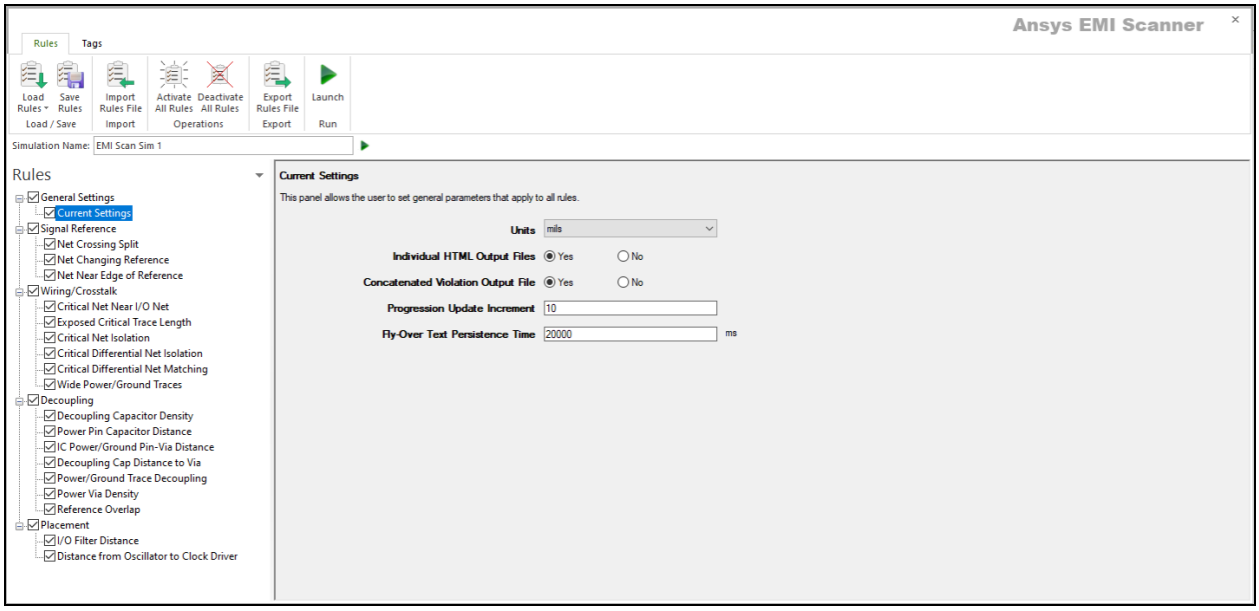
- You can display a description of a rule parameter at any time by hovering the cursor over it.
- Units of measure are set in General Settings.

Applying Wiring/Crosstalk Rules

To change EMI Scanner Wiring/Crosstalk rules:

1. Launch EMI Scanner.

   The **EMI Scanner** window appears, on the **Rules** tab.



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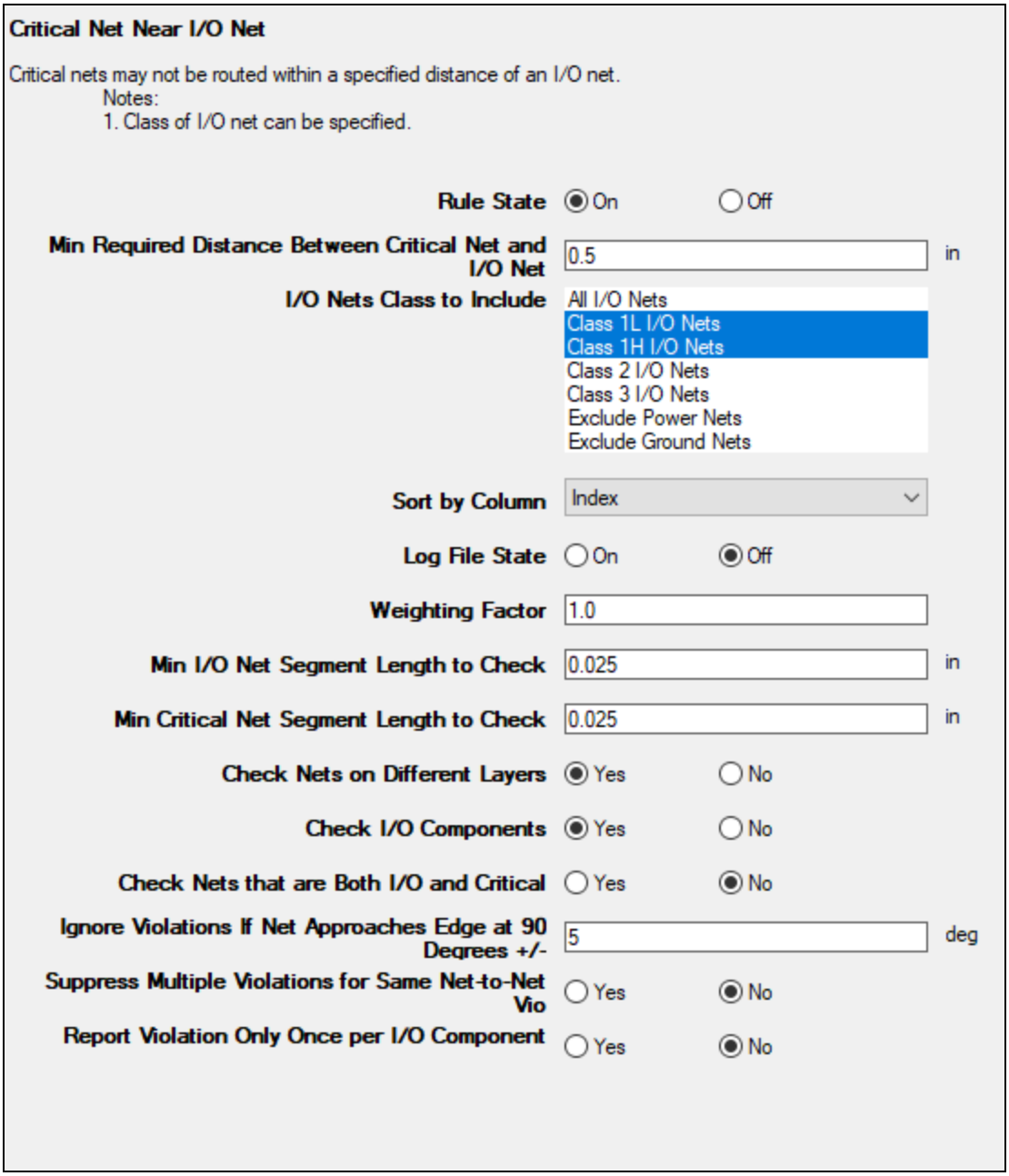
2. From the Rules pane, select one of the six subcategories under **Wiring/Crosstalk**:
   - **Critical Net Near I/O Net** – displays **Critical Net Near I/O Net** rule configuration.



This rule states that critical nets may not be routed within a specified distance from an I/O net.

From here, you can set the following:

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- **Rule State** – toggles Critical Net Near I/O Net rules on or off.
- **Min Required Distance Between Critical Net and I/O Net** – specifies the minimum distance between all critical nets and all I/O nets.
- **I/O Nets Class to Include** – specifies the type(s) of I/O Nets to include. Select one, or Ctrl+click to select multiple types. See Technical Note.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Min I/O Net Segment Length to Check** – specifies the smallest I/O net segment length to check for violations. EMI Scanner ignores All I/O net segments smaller than this length.
- **Min Critical Net Segment Length to Check** – specifies the smallest critical net segment length to check for violations. EMI Scanner ignores all critical net segments smaller than this length.
- **Check Nets on Different Layers** – determines whether to check the distance between I/O nets and critical nets when these nets are on different layers and between the same pair of planes.
- **Check I/O Components** – determines whether any I/O component that is within the specified distance from a critical net will cause a violation.
- **Check Nets that are Both I/O and Critical** – determines whether nets labeled as both critical and I/O should be checked for distance from other I/O nets.
- **Ignore Violations If Net Approaches Edge at 90 Degrees +/-** – EMI scanner ignores edge connectors that approach the edge of the reference plane or board at a 90 degree angle. This option specifies a tolerance that allows the approach to be slightly off a perfect 90 degrees.
- **Suppress Multiple Violations for Same Net-to-Net Ratio** – determines whether to suppress multiple violation reporting when multiple segments on a critical net infringe on the same I/O net.
- **Report Violation Only Once per I/O Component** – reduces run time by checking only for violations between critical nets and I/O components when no other violation has been found for an I/O component.

- **Exposed Critical Trace Length** – displays **Length of Exposed Critical Traces** rule configuration.

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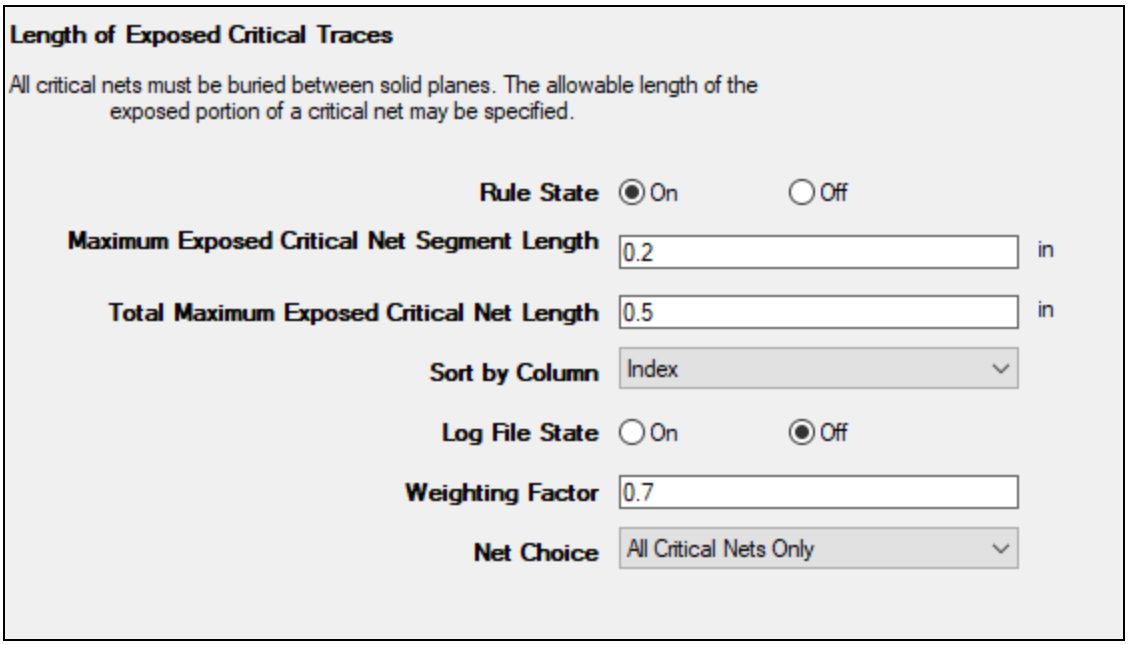

This rule states that all critical nets must be buried between solid planes.

From here, you can set the following:

- **Rule State** – toggles Exposed Critical Trace Length rules on or off.
- **Maximum Exposed Critical Net Segment Length** – specifies the maximum critical net segment length allowed on external (exposed) layers.
- **Total Maximum Exposed Critical Net Length** – specifies the total maximum critical net length allowed on external (exposed) layers (e.g., multiple segments on a critical net may be exposed, but short enough not to cause a violation individually).
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Critical Net Isolation** – displays **Critical Net Isolation (Single-Ended Nets)** rule configuration.

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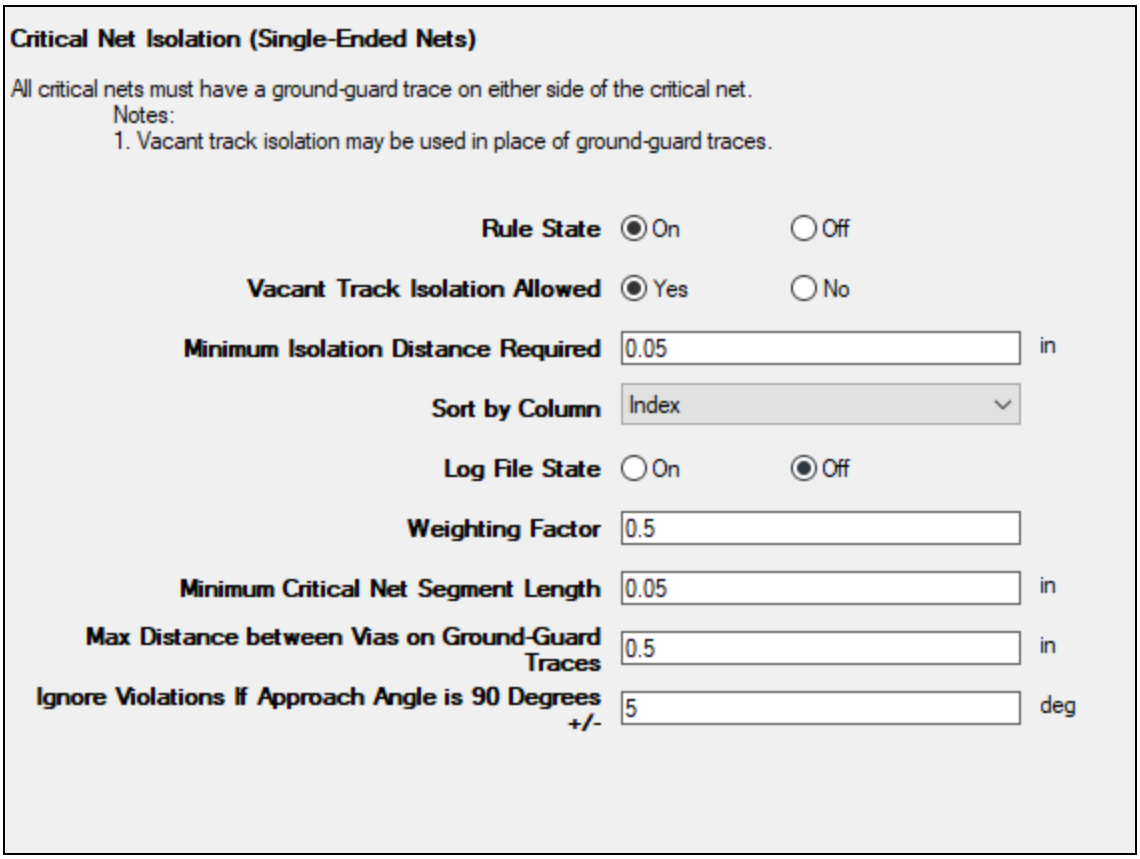

This rule states that all critical nets must have empty tracks or a "ground-guard" trace on either side of the critical net.

From here, you can set the following:

- **Rule State** – toggles Critical Net Isolation rules on or off.
- **Vacant Track Isolation Allowed** – specifies whether vacant tracks (empty space) may be used in place of ground-guard traces.
- **Minimum Isolation Distance Required** – selects the minimum edge-to-edge distance required between critical nets and all other nets before EMI Scanner reports a violation. Used in coordination with **Vacant Track Isolation Allowed**.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

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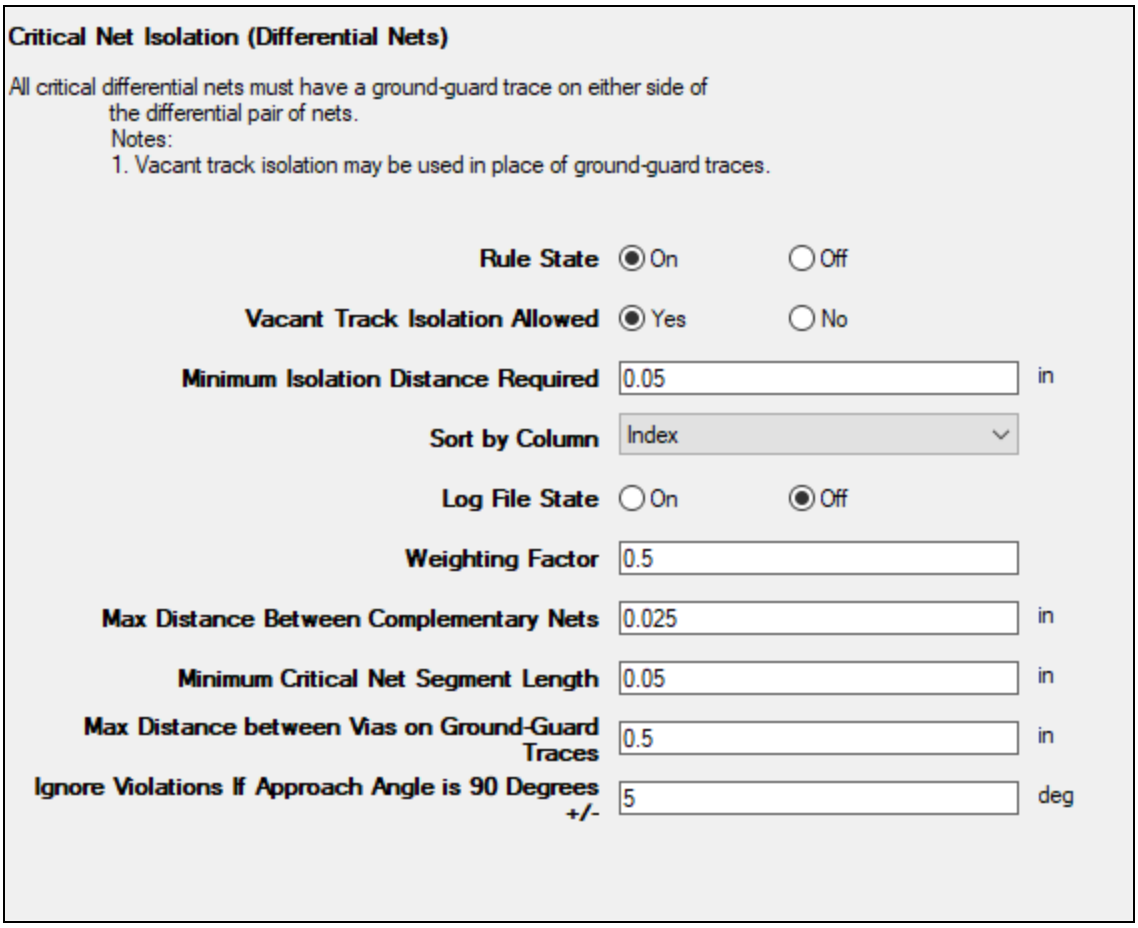
- **Minimum Critical Net Segment Length** – specifies the minimum critical net segment length before EMI Scanner will report a violation. Segments shorter than this length are ignored.
- **Max Distance Between Vias on Ground-Guard Traces** – specifies the maximum distance between vias on ground-guard traces.
- **Ignore Violations If Approach Angle is 90 Degrees +/-** – EMI scanner ignores edge connectors that approach the edge of the reference plane or board at a 90 degree angle. This option specifies a tolerance that allows the approach to be slightly off a perfect 90 degrees.

- **Critical Differential Net Isolation** – displays **Critical Net Isolation (Differential Nets)** rule configuration.



This rule states that all differential critical nets must have empty tracks or a "ground-guard" trace on either side of the differential pair.

From here, you can set the following:

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- **Rule State** – toggles Critical Differential Net Isolation rules on or off.
- **Vacant Track Isolation Allowed** – determines whether vacant tracks (empty space) may be used in place of ground-guard traces.
- **Minimum Isolation Distance Required** – when **Vacant Track Isolation Allowed** is selected, this setting determines the minimum edge-to-edge distance required between critical nets and all other nets before EMI Scanner reports a violation.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Max Distance Between Complementary Nets** – sets the maximum spacing between a pair of critical nets (creating a critical differential pair).
- **Minimum Critical Net Segment Length** – allows you to ignore short critical net segments by specifying the minimum critical net segment length before EMI Scanner will report a violation.
- **Max Distance between Vias on Ground-Guard Traces** – specifies the maximum distance between vias on ground-guard traces.
- **Ignore Violations If Approach Angle is 90 Degrees +/-** – EMI scanner ignores edge connectors that approach the edge of the reference plane or board at a 90 degree angle. This option specifies a tolerance that allows the approach to be slightly off a perfect 90 degrees.

- **Critical Differential Net Matching** – displays **Critical Differential Net Length Matching and Spacing** rule configuration.

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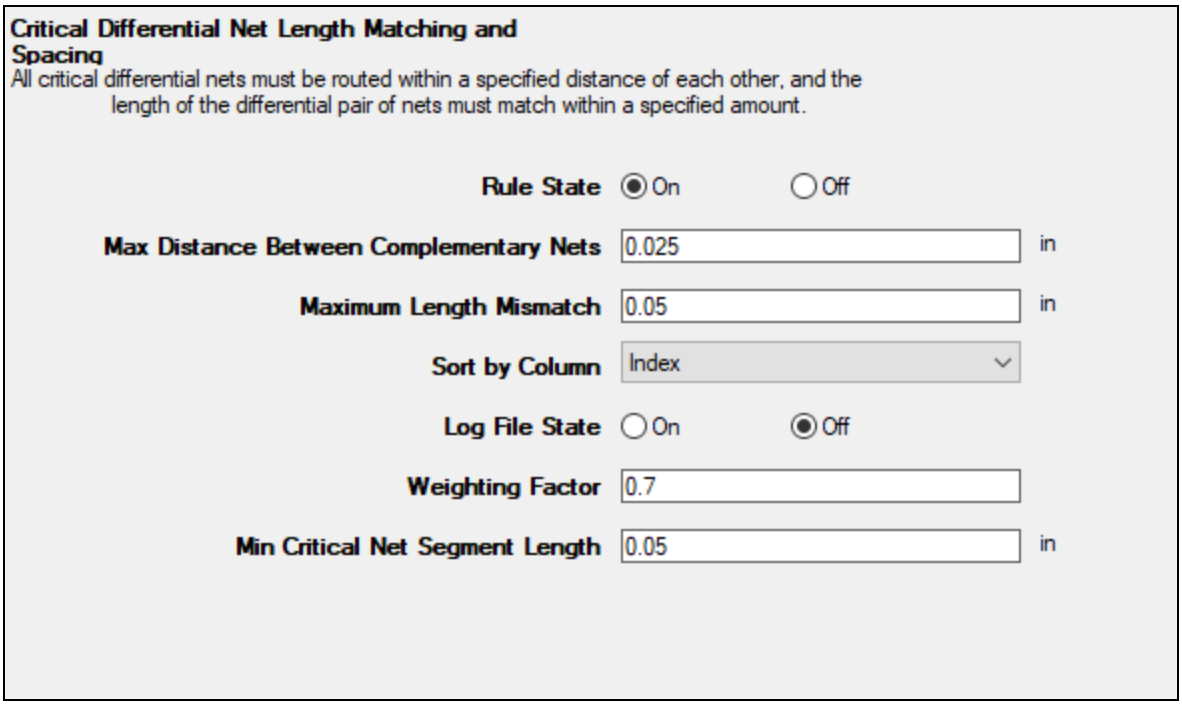

This rule states that all critical nets must be routed within a specified distance of each other, and that the length of the differential pair must match within a specified amount.

From here, you can set the following:

- **Rule State** – toggles Critical Differential Net Matching rules on or off.
- **Max Distance Between Complementary Nets** – sets the maximum spacing between a pair of critical nets (creating a critical differential pair).
- **Maximum Length Mismatch** – specifies the maximum difference in length between a critical differential pair of nets.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Min Critical Net Segment Length** – allows you to ignore short critical net segments by specifying the minimum critical net segment length before EMI Scanner will report a violation.

- **Wide Power/Ground Traces** – displays **Wide Power/Ground Traces** rule configuration.

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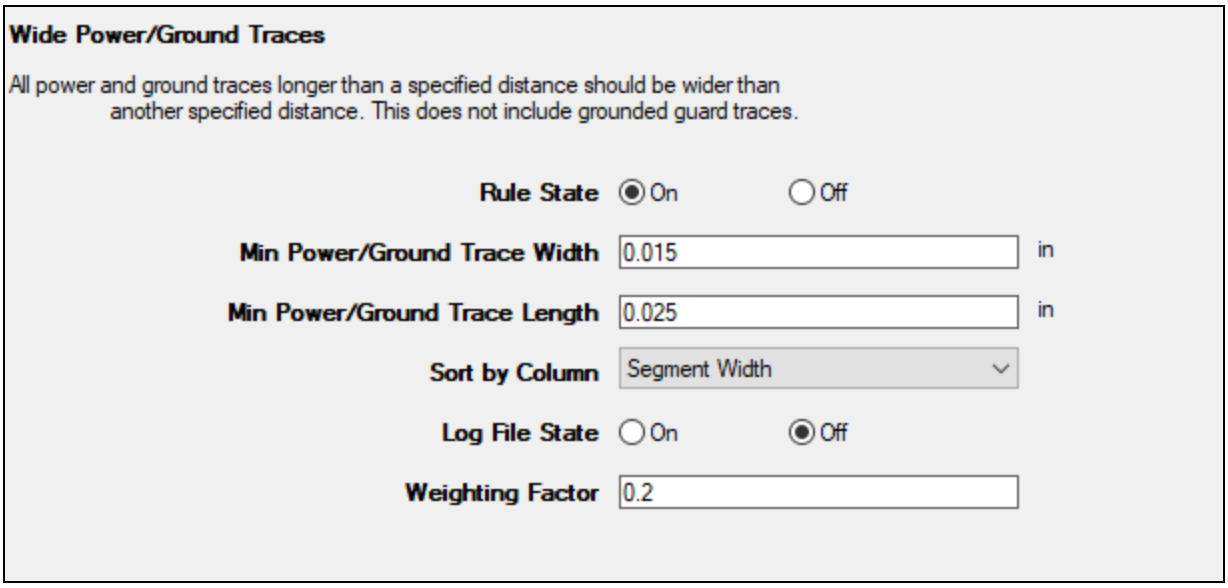

This rule states that all power and ground traces longer than a specified distance must be wider than a specified amount.

From here, you can set the following:

- **Rule State** – toggles Wide Power/Ground Traces rules on or off.
- **Min Power/Ground Trace Width** – sets a minimum width limit for all power/ground traces (except grounded guard traces).
- **Min Power/Ground Trace Length** – specifies the smallest trace length to check for violations. EMI Scanner ignores traces smaller than this length.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

3. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

Note:

- You can display a description of a rule parameter at any time by hovering the cursor over it.
- Units of measure are set in General Settings.

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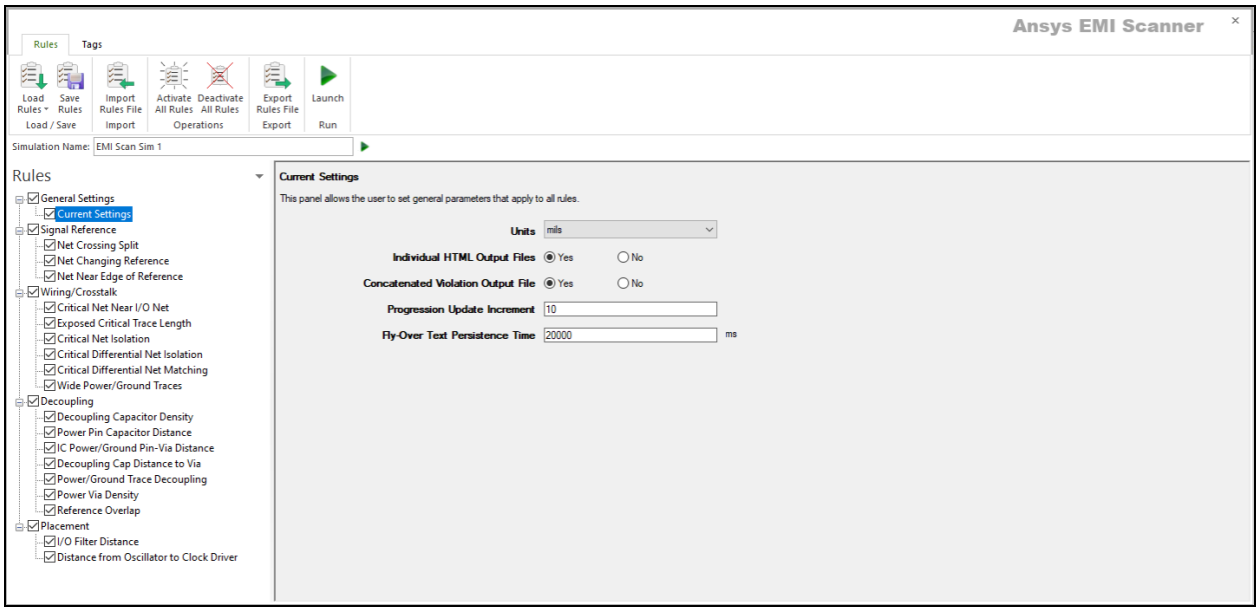
Applying Decoupling Rules

To change EMI Scanner Decoupling rules:

1. Launch EMI Scanner.

   The **EMI Scanner** window appears, on the **Rules** tab.



2. From the Rules pane, select one of the seven subcategories under **Decoupling**:
   - **Decoupling Capacitor Density** – displays **Decoupling Capacitor Density** rule configuration.

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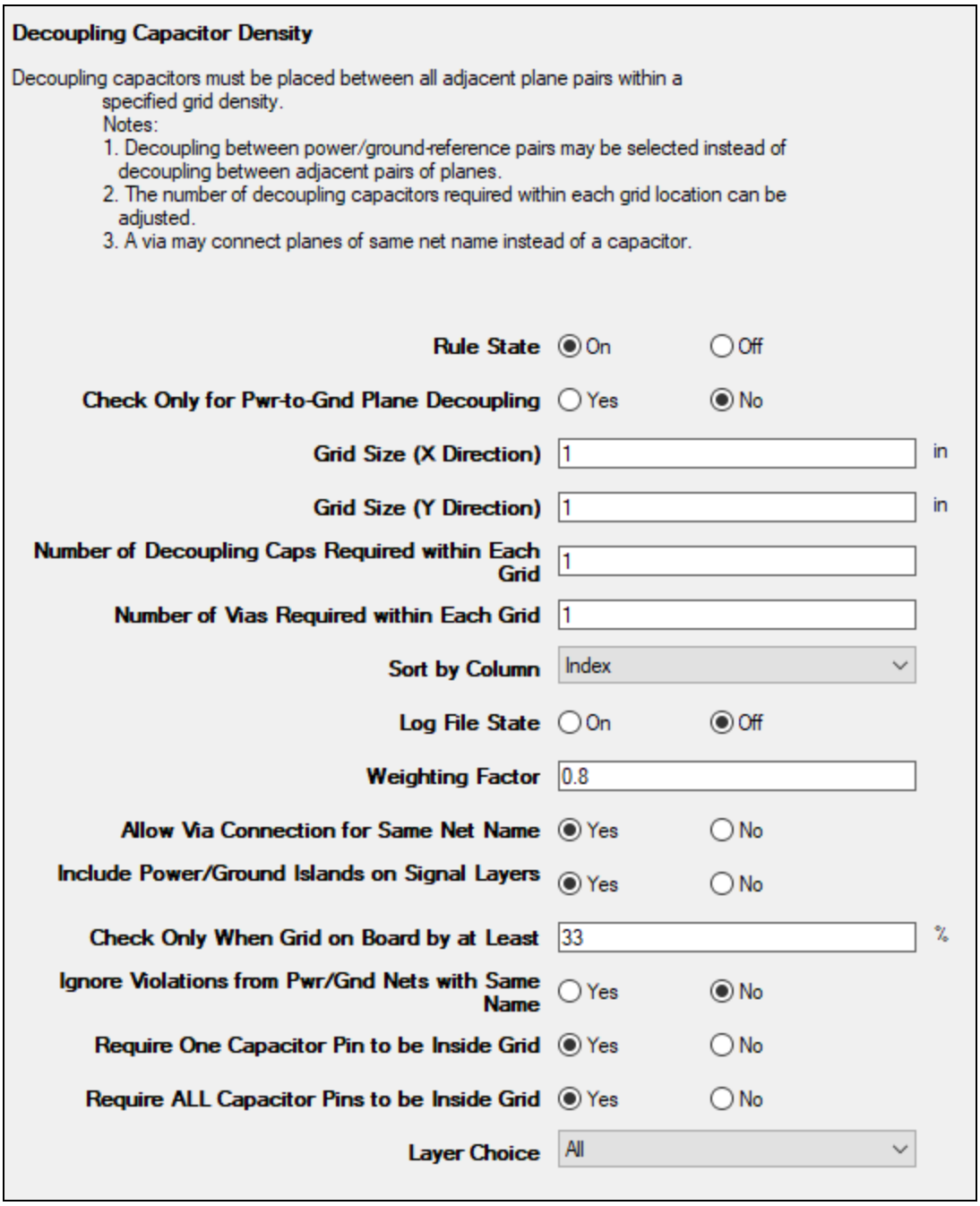

This rule states that decoupling capacitors must be placed between all adjacent plane pairs within a specified grid density.

From here, you can set the following:

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- **Rule State** – toggles Decoupling Capacitor Density rules on or off.
- **Check Only for Pwr-to-Gnd Plane Decoupling** – sets whether to ignore plane-to-plane decoupling and check only for decoupling capacitors between power and ground planes.
- **Grid Size (X Direction)** – specifies the size of the grid used to check for decoupling capacitors. Used in conjunction with **Grid Size (Y Direction)**.
- **Grid Size (Y Direction)** – specifies the size of the grid used to check for decoupling capacitors. Used in conjunction with **Grid Size (X Direction)**.
- **Number of Decoupling Caps Required within Each Grid** – specifies the number of decoupling capacitors connecting between planes that are required within each grid location.
- **Number of Vias Required within Each Grid** – specifies the number of vias connecting between planes that are required within each grid location. You must select **Allow Via Connection for Same Net Name** to use this option.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Allow Via Connection for Same Net Name** – determines whether EMI Scanner allows a via in place of a decoupling capacitor when the two planes are the same net name.
- **Include Power/Ground Islands on Signal Layers** – specifies whether to check for decoupling on power/ground islands.
- **Check Only When Grid on Board by at Least** – specifies the percentage of a grid that must be on the board in order for it to be checked.
- **Ignore Violations from Pwr/Gnd Nets with Same Name** – determines that only one plane of a given name is checked for violations (e.g., if two planes are "gnd" and a violation occurs between gnd and another layer, only one violation is reported).
- **Require One Capacitor Pin to be Inside Grid** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **Require ALL Capacitor Pins to be Inside Grid** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **Layer Choice** – specifies the layers to include in this rule analysis.

- **Power Pin Capacitor Distance** – displays **Decoupling Capacitor Distance from IC Power Pin** rule configuration.

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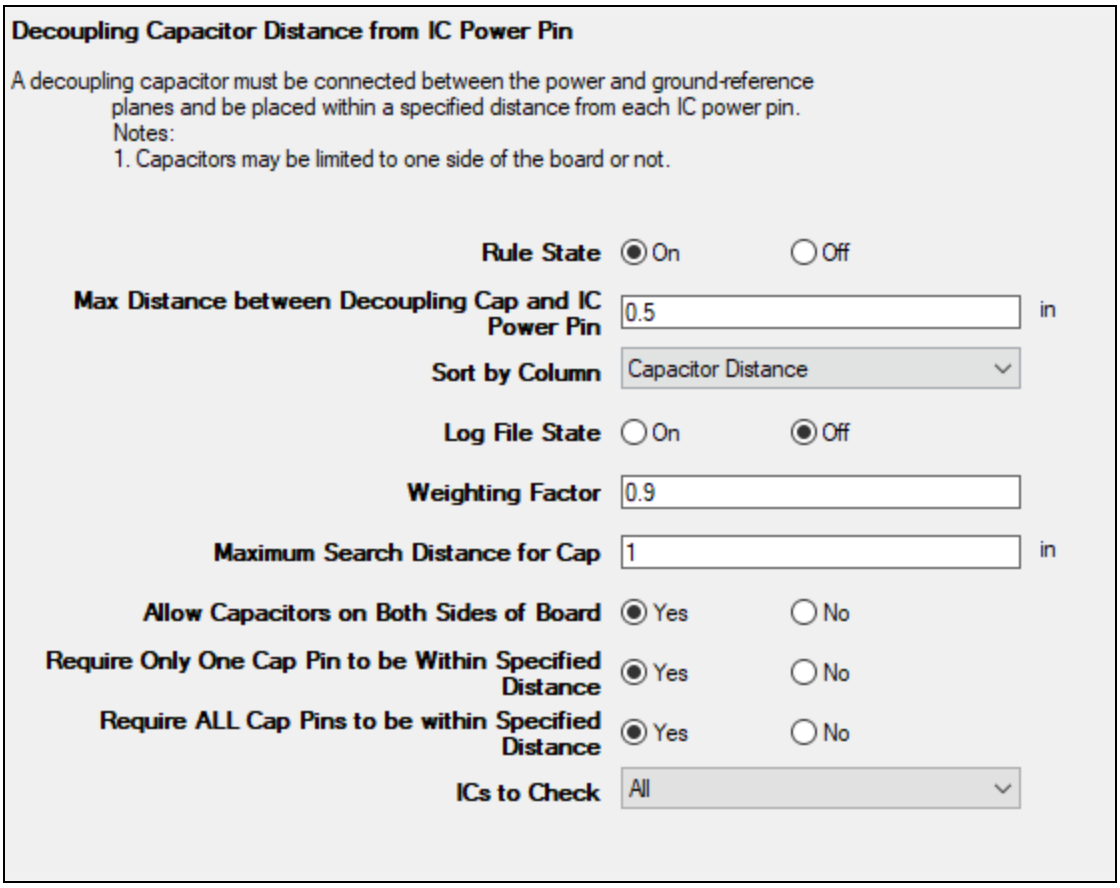

This rule states that a decoupling capacitor must be connected between the power and ground-reference planes and be placed within a specified distance of each IC power pin.

From here, you can set the following:

- **Rule State** – toggles Power Pin Capacitor Distance rules on or off.
- **Max Distance between Decoupling Cap and IC Power Pin** – specifies the maximum distance between an IC power pin and its decoupling capacitor.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Maximum Search Distance for Cap** – specifies a maximum search distance for a capacitor. A larger search box increases the chances of EMI Scanner finding capacitors, but can slow processing time.

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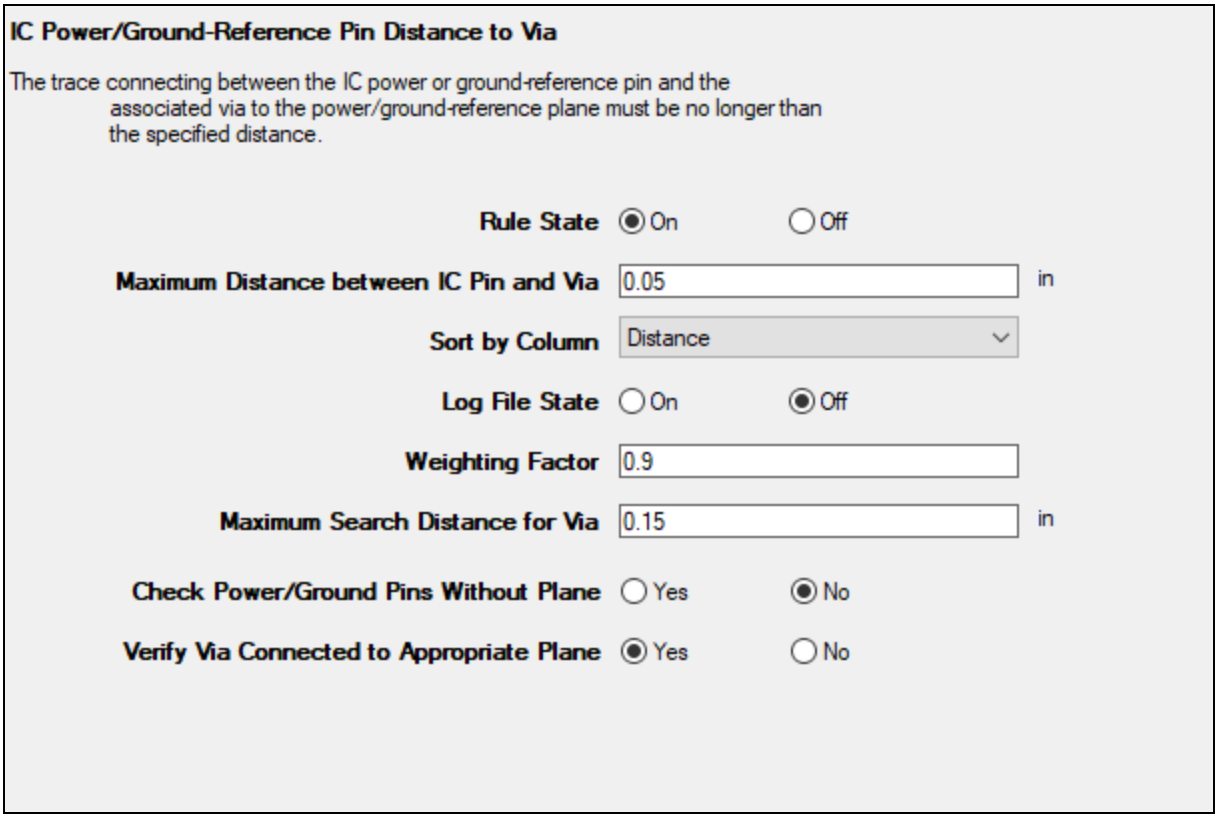
- **Allow Capacitors on Both Sides of Board** – specifies whether to include capacitors on both sides of the board.
- **Require Only One Cap Pin to be Within Specified Distance** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **Require ALL Cap Pins to be within Specified Distance** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **ICs to Check** – selects the types of components to include in this rule analysis.

- **IC Power/Ground Pin-Via Distance** – displays **IC Power/Ground-Reference Pin Distance to Via** rule configuration.



This rule states that the trace connecting the IC power/ground reference pin to its associated via to the power/ground-reference plane must be no longer than a specified distance.

From here, you can set the following:

- **Rule State** – toggles IC Power/Ground Pin-Via Distance rules on or off.

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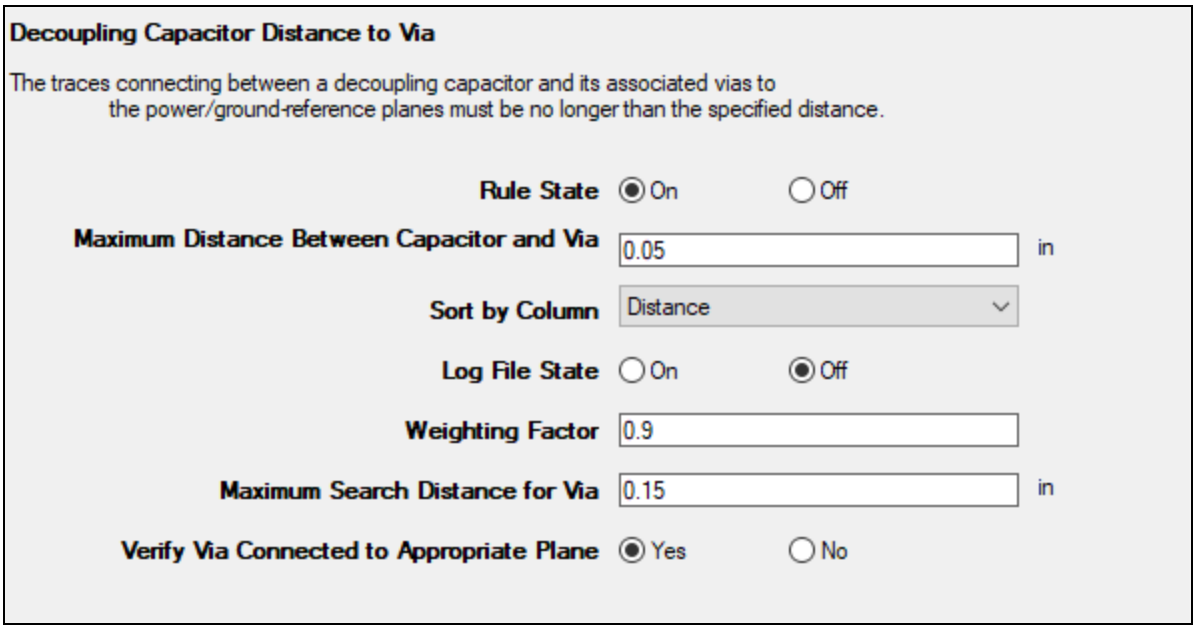
- **Maximum Distance between IC Pin and Via** – specifies the maximum distance between the center of the IC power or ground-reference pin and the center of the via to the power or ground-reference plane.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Maximum Search Distance for Via** – specifies a maximum search distance for a via when a violation is found. This allows you to spot vias that are barely outside the original requirement and therefore not serious violations.
- **Check Power/Ground Pins Without Plane** – checks the distance between the IC power/ground pin and its via when the power/ground plane has not been completed yet.
- **Verify Via Connected to Appropriate Plane** – selecting 'no' speeds up EMI Scanner by not verifying that the via connects to an appropriate plane (shape).

- **Decoupling Cap Distance to Via** – displays **Decoupling Capacitor Distance to Via** rule configuration.



This rule states that the trace connecting a decoupling capacitor to its associated via to the power/ground-reference plane must be no longer than the specified distance.

From here, you can set the following:

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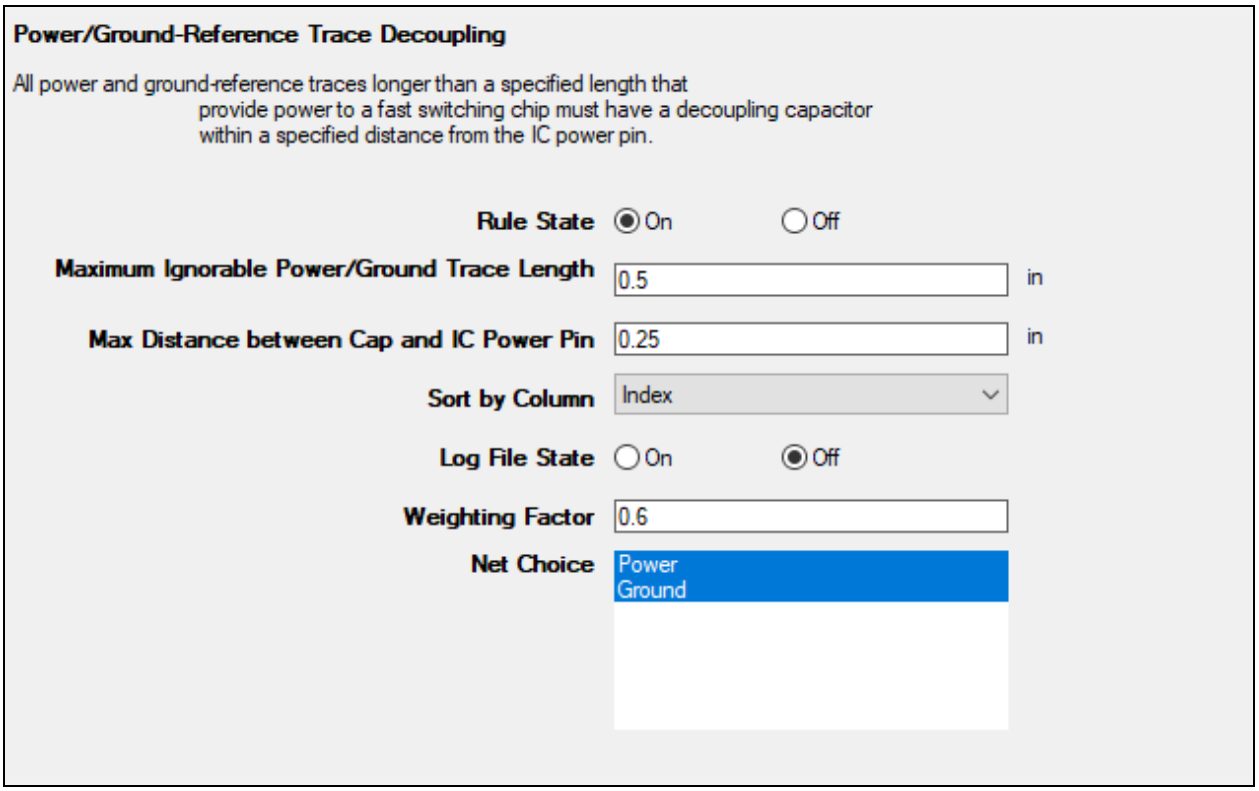
- **Rule State** – toggles Decoupling Cap Distance to Via rules on or off.
- **Maximum Distance Between Capacitor and Via** – specifies the maximum distance between the capacitor pin and the center of the via to the power or ground-reference plane.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Maximum Search Distance for Via** – specifies a maximum search distance for a via when a violation is found. This allows you to spot vias that are barely outside the original requirement and therefore not serious violations.
- **Verify Via Connected to Appropriate Plane** – selecting 'no' speeds up EMI Scanner by not verifying that the via connects to an appropriate plane (shape).

- **Power/Ground Trace Decoupling** – displays **Power/Ground-Reference Trace Decoupling** rule configuration.



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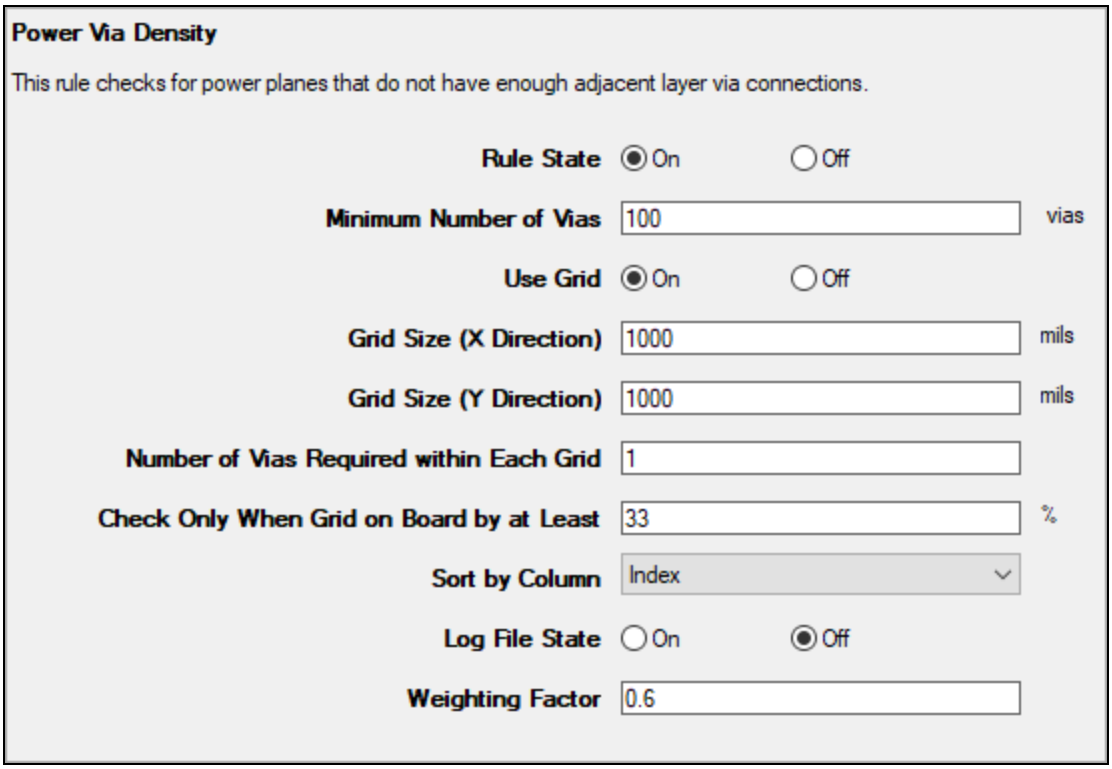
This rule states that all power and ground-reference traces longer than a specified length must have a decoupling capacitor within a specified distance of the IC power pin.

From here, you can set the following:

- **Rule State** – toggles Power/Ground Trace Decoupling rules on or off.
- **Maximum Ignorable Power/Ground Trace Length** – specifies the maximum power/ground trace length that may be ignored. All traces longer than this length must meet this rule's requirement.
- **Max Distance between Cap and IC Power Pin** – specifies the maximum distance between the capacitor pin and the power or ground-reference pin.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Power/Via Density** – displays **Power Via Density** rule configuration.



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This rule checks for power planes that do not have enough adjacent layer via connections.

From here, you can set the following:

- **Rule State** – toggles Power Via Density rules on or off.
- **Minimum Number of Vias** – sets the minimum number of vias required to connect adjacent power planes.
- **Use Grid** – toggles the use of a grid on or off.
- **Grid Size (X Direction/Y Direction)** – when Use Grid is enabled, these fields specify the size of the grid.
- **Number of Vias Required within Each Grid** – when Use Grid is enabled, specifies the number of vias required within each grid.
- **Check Only When Grid on Board by at Least** – specifies the percentage of the grid that must be on the board for analysis to occur.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

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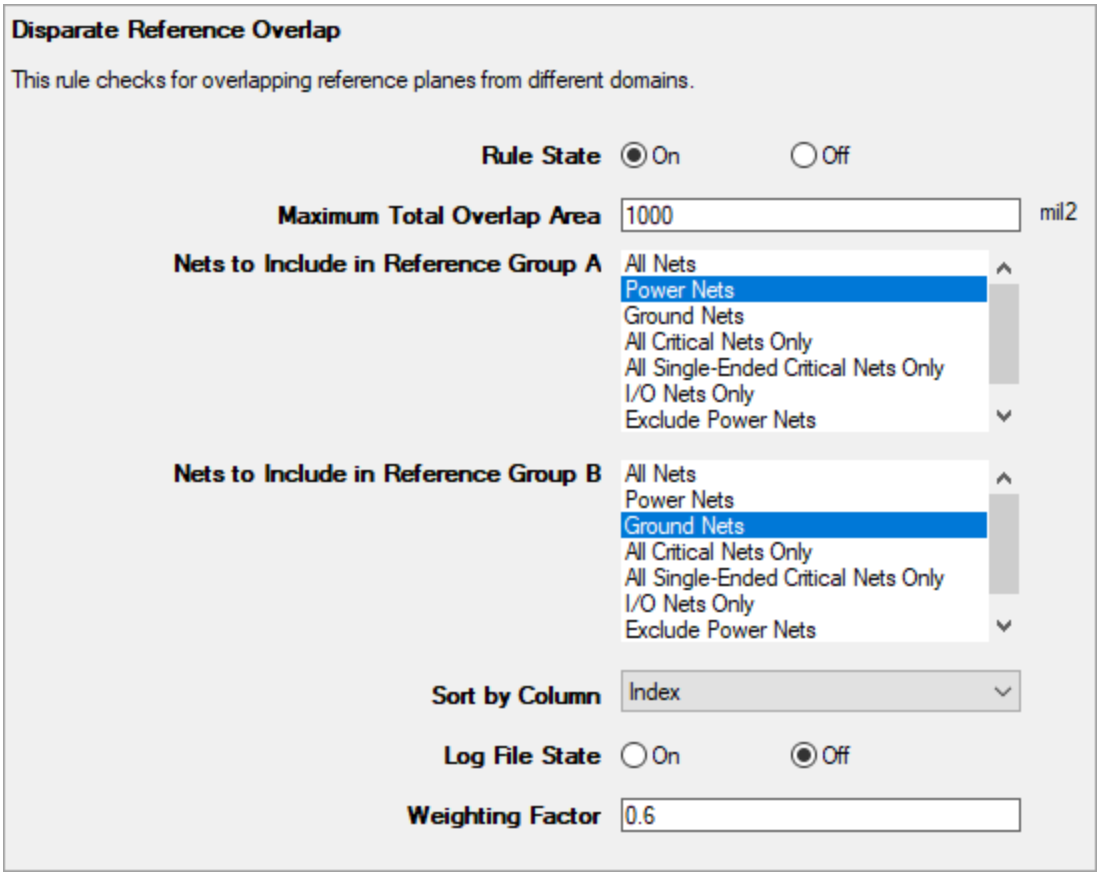
- **Reference Overlap** – displays **Disparate Reference Overlap** rule configuration.



The Disparate Reference Overlap rule checks for overlapping reference planes from different domains.

From here, you can set the following:

- **Rule State** – toggles Disparate Reference Overlap on or off.
- **Maximum Total Overlap Area** – specifies the maximum overlap area that is acceptable. Overlap over this maximum will report a violation.
- **Nets to Include in Reference Group A** – selects a net type.
- **Nets to Include in Reference Group B** – selects a net type.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

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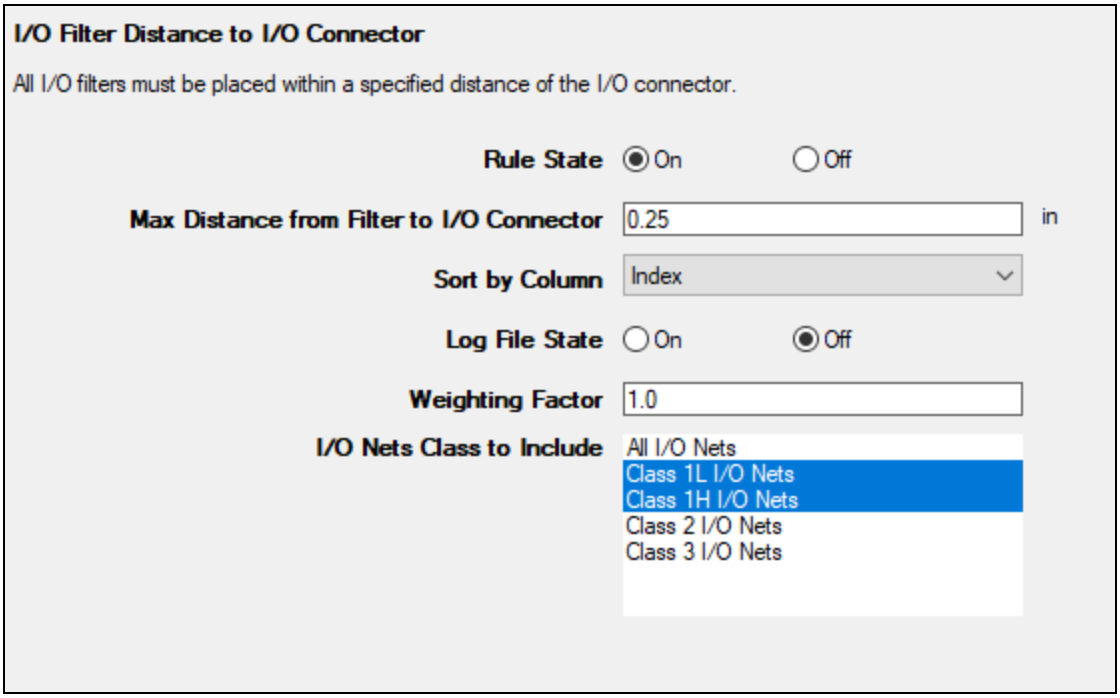
3. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

> **Note:**
>
> - You can display a description of a rule parameter at any time by hovering the cursor over it.
> - Units of measure are set in General Settings.

Applying Placement Rules

To change EMI Scanner Placement rules:

1. From the Rules pane, select one of the two subcategories under **Placement**:
   - **I/O Filter Distance** – displays the **I/O Filter Distance to I/O Connector** rule configuration.



   This rule states that all I/O filters must be placed within a specified distance of the I/O connector.

   From here, you can set the following:

   - **Rule State** – toggles I/O Filter Distance rules on or off.
   - **Max Distance from Filter to I/O Connector** – specifies the maximum distance a filter may be placed from the I/O connector.

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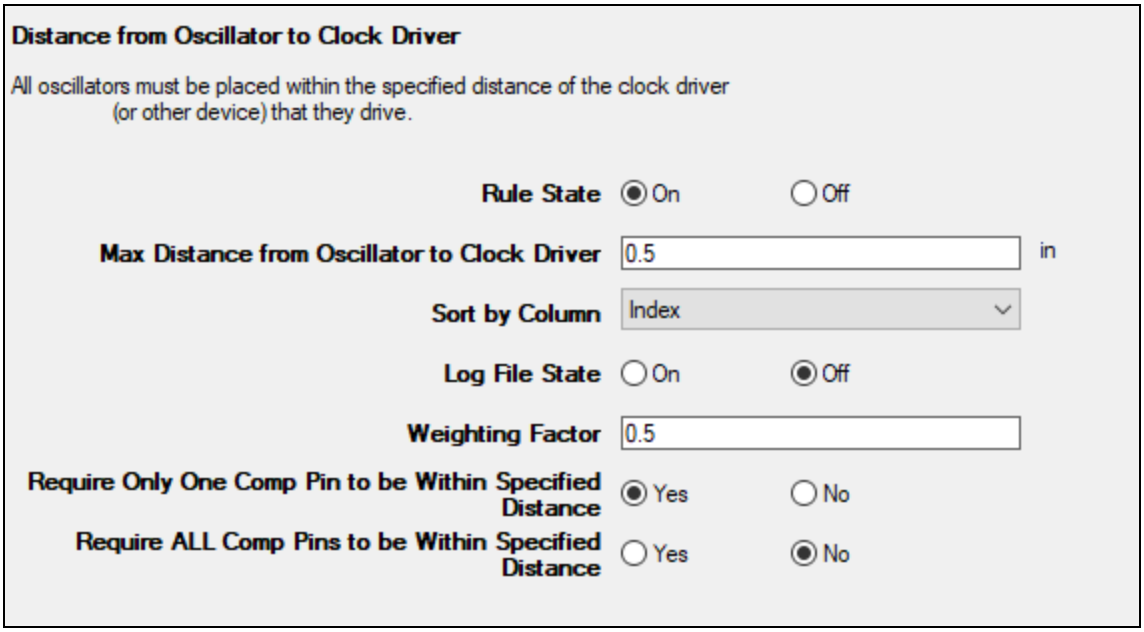
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **I/O Nets to Include** – specifies the type(s) of I/O Nets to include. Select one, or Ctrl+click to select multiple types. See Technical Note.

- **Distance from Oscillator to Clock Driver** – displays the **Distance from Oscillator to Clock Driver** rule configuration.



This rule states that all oscillators must be placed within a specified distance from the clock driver or other device that they drive.

From here, you can set the following:

- **Rule State** – toggles Distance from Oscillator to Clock Driver rules on or off.
- **Max Distance from Oscillator to Clock Driver** – specifies the distance within which all oscillators must be placed of the clock driver (or other device) that they drive.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of

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badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

- **Require Only One Comp Pin to be Within Specified Distance** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **Require ALL Comp Pins to be Within Specified Distance** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.

2. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

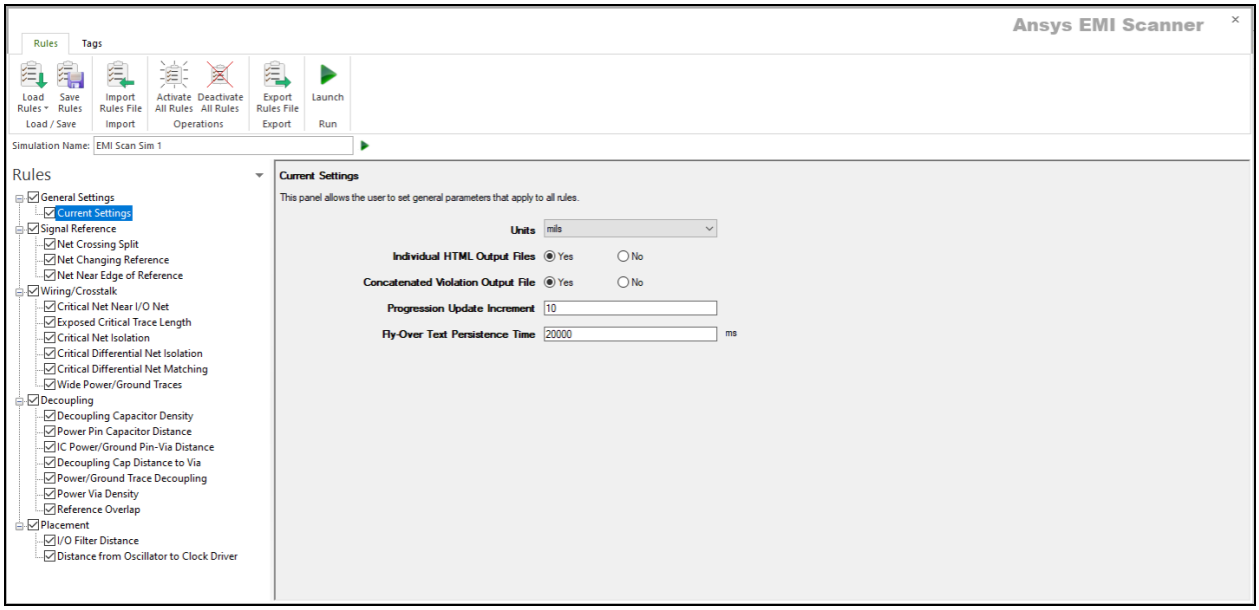
> **Note:**
>
> - You can display a description of a rule parameter at any time by hovering the cursor over it.
> - Units of measure are set in General Settings.

Applying Net Integrity Rules

To change EMI Scanner Net Integrity rules:

1. Launch EMI Scanner.

   The **EMI Scanner** window appears, on the **Rules** tab.



2. Click **Load Rules** and select a profile containing Signal Integrity rules (e.g., Default SI Rules Profile).

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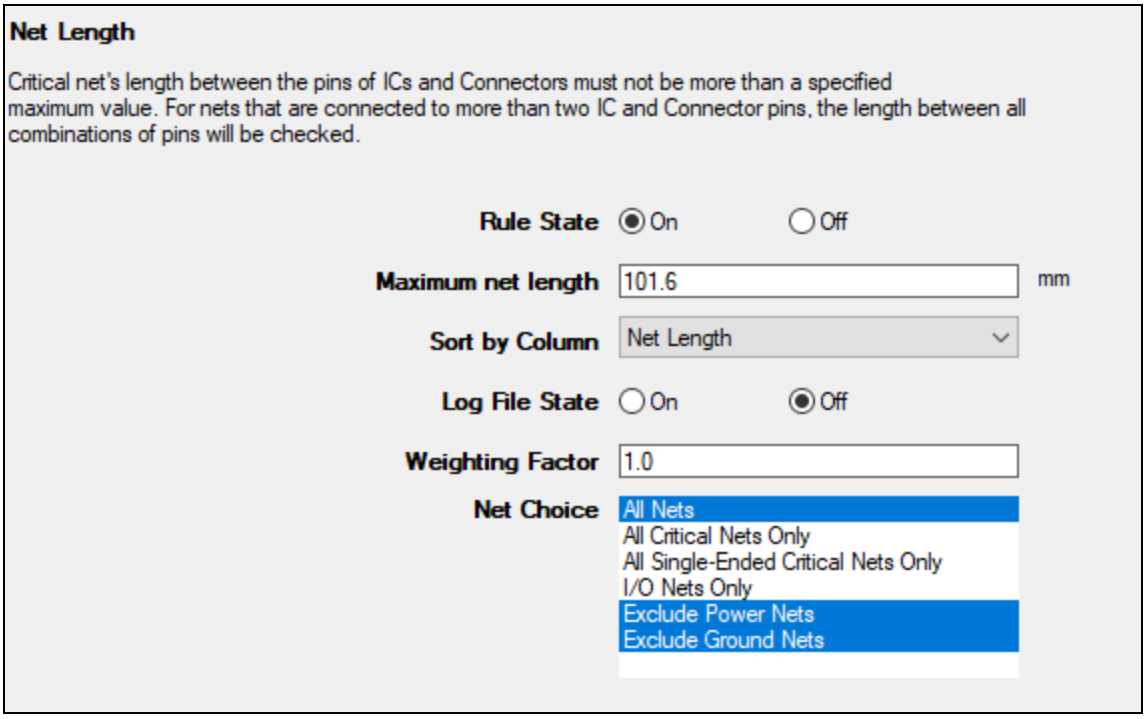
3. From the Rules pane, select one of the eight subcategories under **Net Integrity**:
   - **Net Length** – displays the **Net Length** rule configuration.



This rule states that a critical net's length between pins of ICs and Connectors must not be more than a specified value.

From here, you can set the following:

- **Rule State** – toggles Net Length rules on or off.
- **Maximum Net Length** – specifies the maximum net length.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

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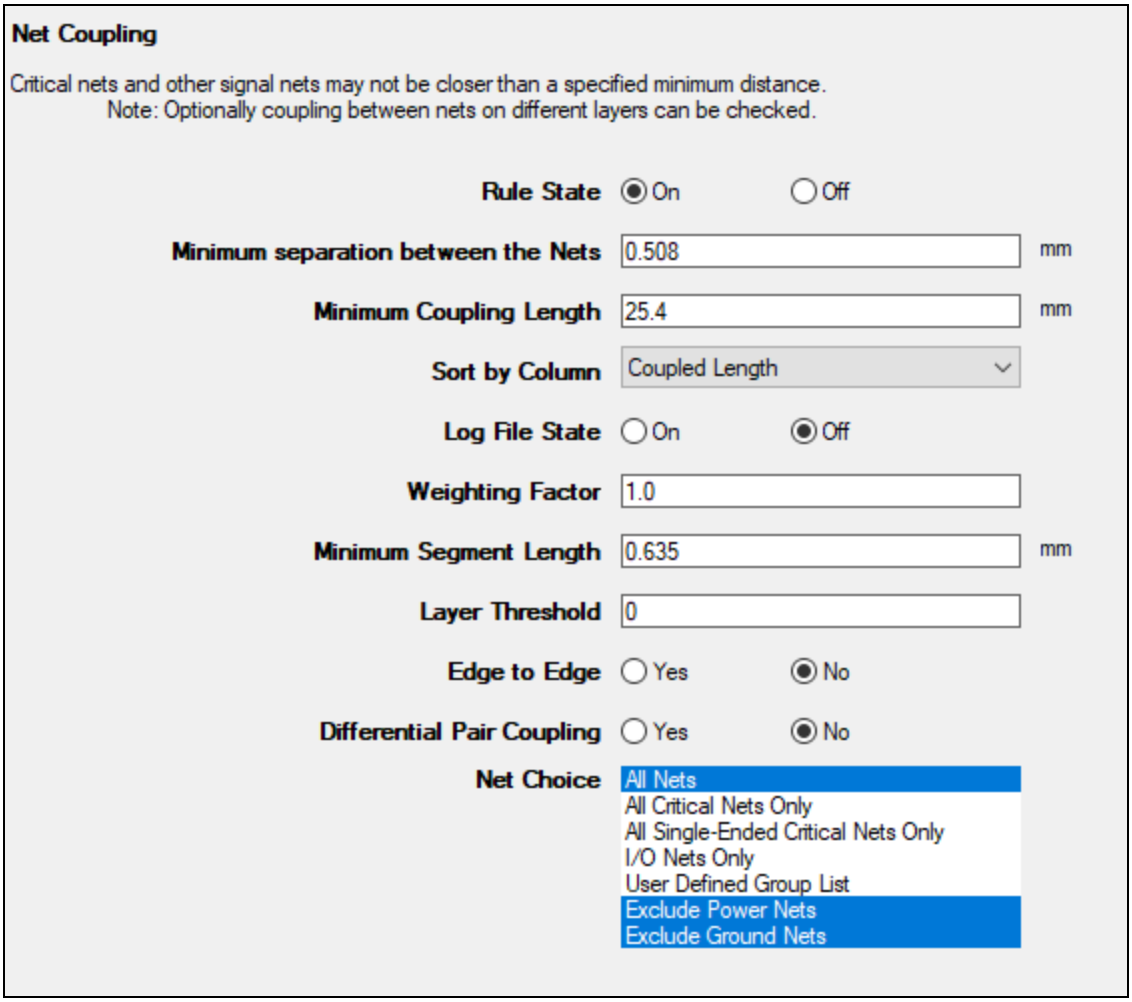
- **Net to Net Coupling** – displays the **Net Coupling** rule configuration.



This rule states that critical nets and other signal nets may not be closer than a specified minimum distance.

From here, you can set the following:

- **Rule State** – toggles Net Coupling rules on or off.
- **Minimum Separation Between the Nets** – controls how close the nets can be before they are considered coupled.
- **Maximum Coupling Length** – specifies how much coupling must exist before a violation is reported.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).

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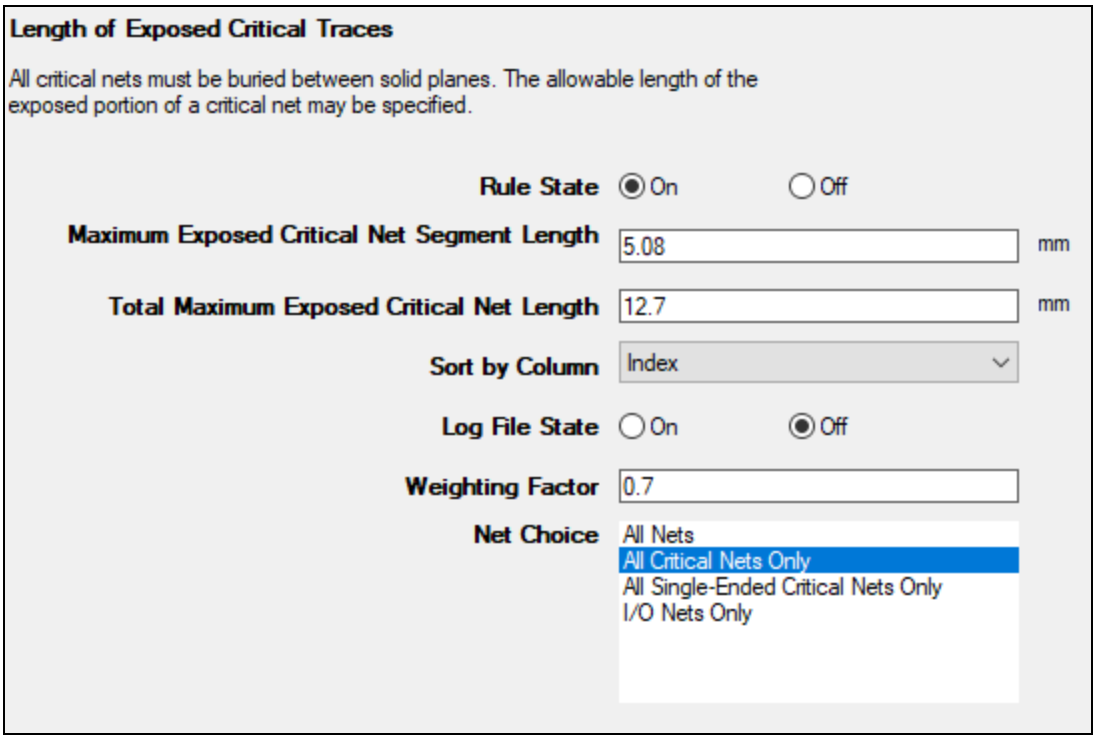
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Minimum Segment Length** – specifies the smallest net segment length to check for coupling. Any segments smaller than this length will be ignored.
- **Layer Threshold** – sets the number of layers above and below to check for coupling (e.g., 0 = only the selected layer, 1 = the selected layer plus one layer above and one layer below).
- **Edge to Edge** – by default, the minimum distance between nets is based on center-to-center measurement. Selecting this option changes the measurement to edge-to-edge.
- **Differential Pair Coupling** – determines whether to allow or ignore coupling between the nets that make up a differential pair.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Exposed Critical Trace Length** – displays the **Length of Exposed Critical Traces** rule configuration.



This rule states that all critical nets must be buried between solid planes.

From here, you can set the following:

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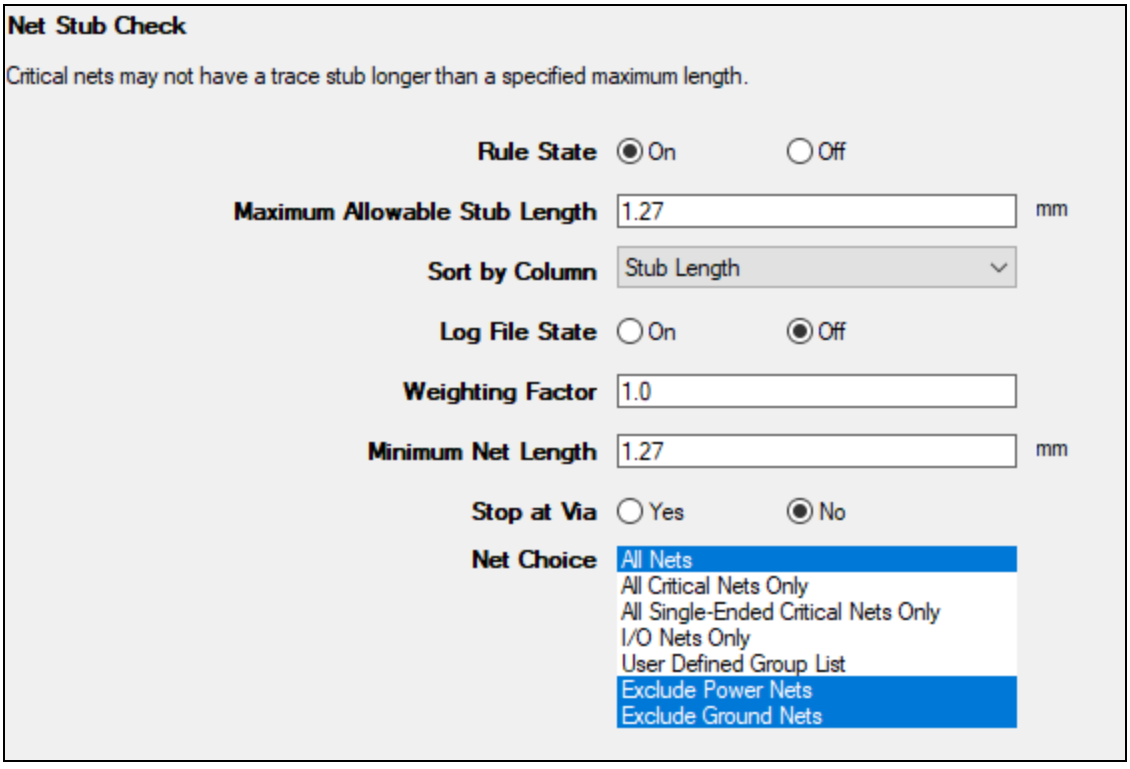
- **Rule State** – toggles Net Length rules on or off.
- **Maximum Exposed Critical Net Segment Length** – specifies the maximum critical net segment length allowed on external (exposed) layers.
- **Total Maximum Exposed Critical Net Length** – specifies the total maximum critical net length allowed on external (exposed) layers (e.g., multiple segments on a critical net may be exposed, but short enough to not cause a violation individually).
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Net Stub** – displays the **Net Stub Check** rule configuration.



This rule states that critical nets may not have a trace stub longer than the specified maximum length.

From here, you can set the following:

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- **Rule State** – toggles Net Stub Check rules on or off.
- **Maximum Allowable Stub Length** – specifies the maximum stub length. Stubs longer than this are violations.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Minimum Net Length** – sets the minimum length at which nets are included. Nets must be longer than this length to be considered.
- **Stop at Via** – determines whether vias count as a stub termination condition. By defauly, the termination of a stub is a pin or a fork in the net, whichever is found first. Setting this parameter to 'yes' adds vias (to pins and forks) as a stub termination condition.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Net Crossing Split** – displays the **Critical Net Crossing Split Reference Plane** rule configuration.

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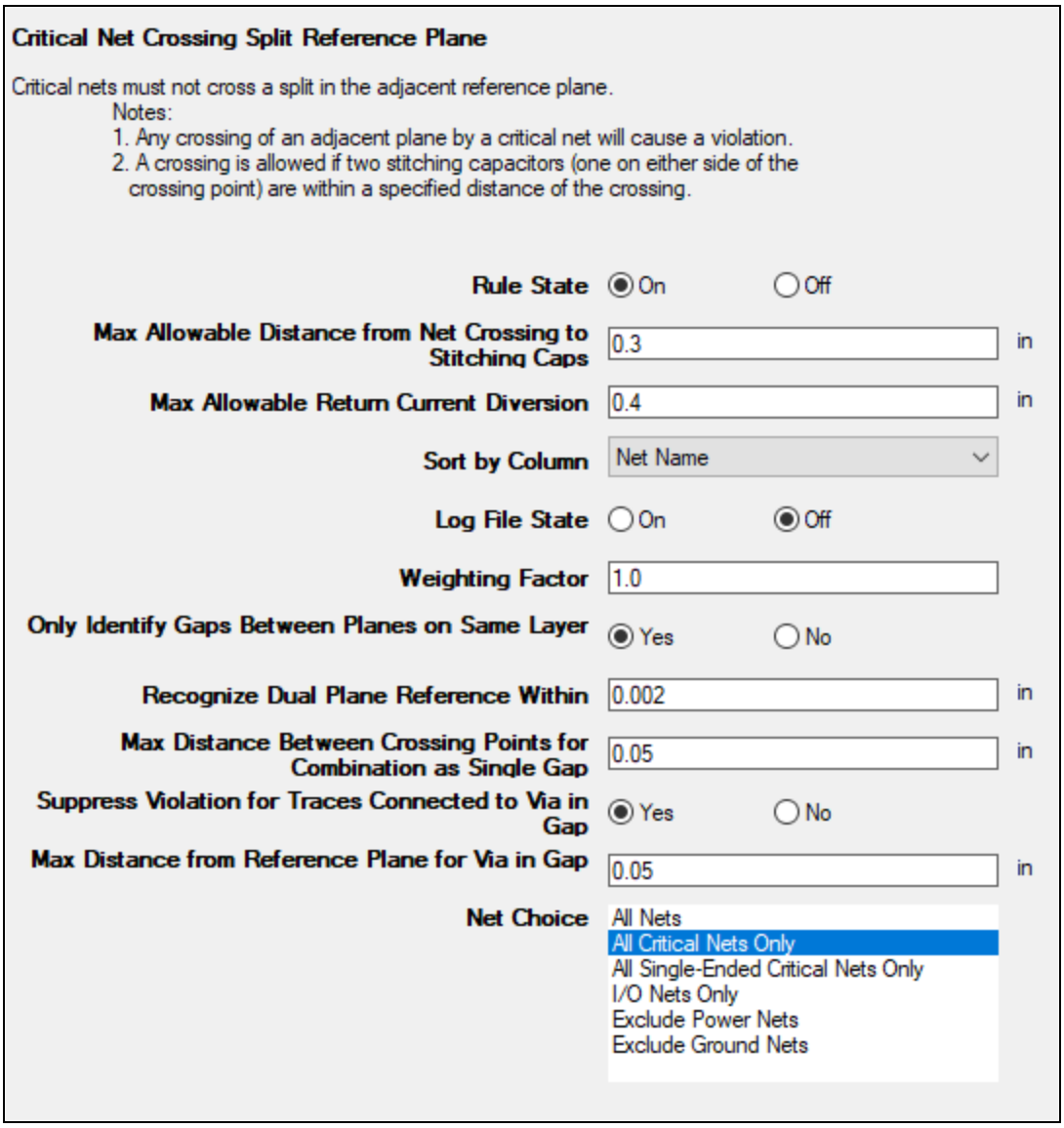

This rule states that critical nets must not cross a split in the adjacent reference plane.

From here, you can set the following:

- **Rule State** – toggles Net Crossing Split rules on or off.
- **Max Allowable Distance from Net Crossing to Stitching Caps** – sets the distance from the point where the net crosses a split in its reference plane at which two stitching capacitors must be found.
- **Max Allowable Return Current Diversion** – determines whether a signal's return current can divert itself around the gap in the reference plane. The total distance of the diversion must be less than this value.

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- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Only Identify Gaps Between Planes on Same Layer** – chooses whether or not gaps are only between planes on the same layer. When the rule tries to pair up nearby plane boundary crossing points and identify gaps, this parameter will enable or disable a check for layer commonality.
- **Recognize Dual Plane Reference Within** – specifies a distance and instructs EMI Scanner to consider both planes as a reference when checking for gap crossing when the distance difference to each plane is less than the specified distance. This allows recognition of both planes as references for strip line traces when the trace is offset from the exact center by a small amount (normally for manufacturing reasons).
- **Max Distance Between Crossing Points for Combination as a Single Gap** – specifies the distance under which nearby crossing points are combined into a single violation. Setting too large a value can cause the algorithm to pair up unrelated crossing points, and setting too small a value can prevent crossing points from being paired up, resulting in more violations. It is recommended to set the value slightly larger than the typical plane separation within a layer, based on the board design technology being used.
- **Suppress Violation for Traces Connected to Via in Gap** – instructs EMI Scanner whether to ignore trace crossing split/gap when connected to a via within that gap.
- **Max Distance from Reference Plane for Via in Gap** – specifies the maximum distance from edge of the reference plane to the via. Violations will not be suppressed (from above) for vias within gap if the trace extends greater than the specified distance.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Net Near Edge of Reference** – displays the **Critical Net Near Edge of Reference Plane** rule configuration.

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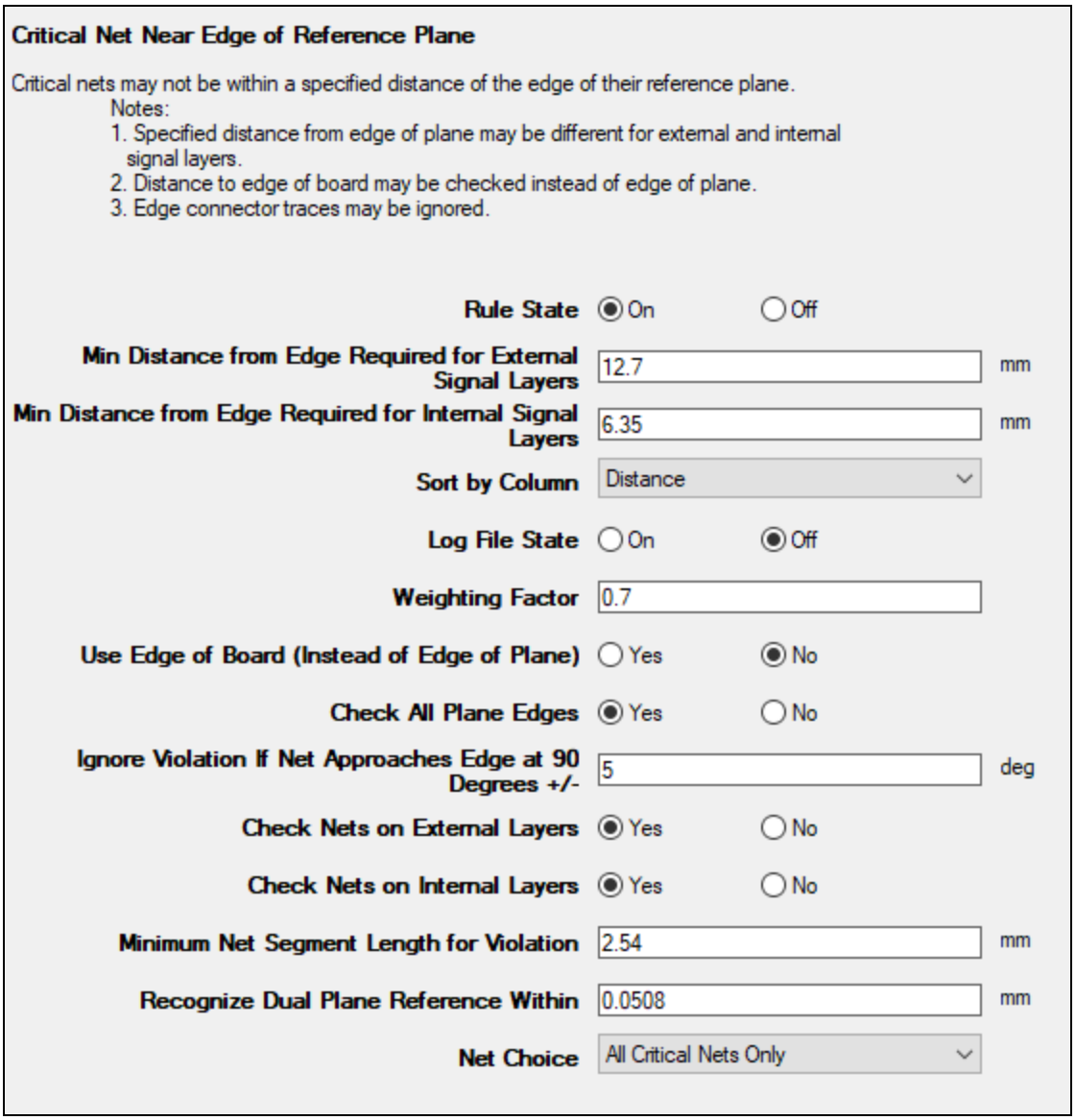

This rule states that critical nets may not be within a specified distance of the edge of their reference plane.

From here, you can set the following:

- **Rule State** – toggles Net Near Edge of Reference rules on or off.
- **Min Distance from Edge Required for External Signal Layers** – specifies the minimum distance that must exist between the edge of the reference plane and a critical signal net when the net is on an external layer.

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- **Min Distance from Edge Required for Internal Signal Layers** – specifies the minimum distance that must exist between the edge of the reference plane and a critical signal net when the net is on an internal layer.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Use Edge of Board (Instead of Edge of Plane)** – allows EMI Scanner to check distance from critical nets to the edge of the board instead of the edge of the reference plane. This can be useful if the board is only partially complete and all reference planes are not yet completed.
- **Check All Plane Edges** – checks the distance from nets to any edge of their reference plane, rather than limiting the check to reference plane edges near the edge of the board.
- **Ignore Violation If Net Approaches Edge at 90 Degrees +/-** – EMI scanner ignores edge connectors that approach the edge of the reference plane or board at a 90 degree angle. This option specifies a tolerance that allows the approach to be slightly off a perfect 90 degrees.
- **Check Nets on External Layers** – specifies whether nets on external layers should be checked.
- **Check Nets on Internal Layers** – specifies whether nets on internal layers should be checked.
- **Minimum Net Segment Length for Violation** – specifies the minimum net segment length before EMI Scanner will report a violation if the net is within the specified distance from the edge of the reference plane (or board).
- **Recognize Dual Plane Reference Within** – specifies a distance and instructs EMI Scanner to consider both planes as a reference when checking for traces too close to the edge of reference planes when the distance difference to each plane is less than the specified distance. This allows recognition of both planes as references for strip line traces when the trace is offset from the exact center by a small amount (normally for manufacturing reasons).
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Between Ref Plane Routing** – displays the **Net Routing Between Two Reference Planes** rule configuration.

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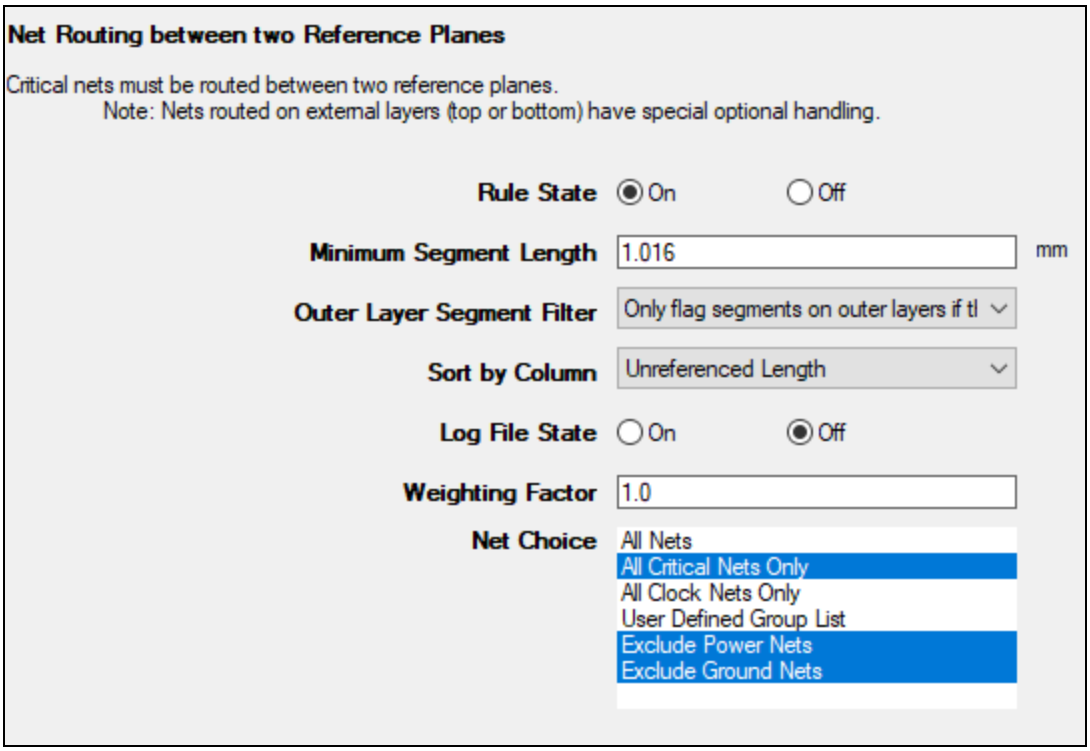

This rule states that critical nets must be routed between two reference planes.

From here, you can set the following:

- **Rule State** – toggles Net Routing Between Two Reference Planes rules on or off.
- **Minimum Segment Length** – specifies the minimum net segment length before EMI Scanner will report a violation.
- **Outer Layer Segment Filter** – specifies how segments on outer layers are to be treated.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Diff Running Skew** – displays the **Critical Differential Net Running Skew** rule configuration.

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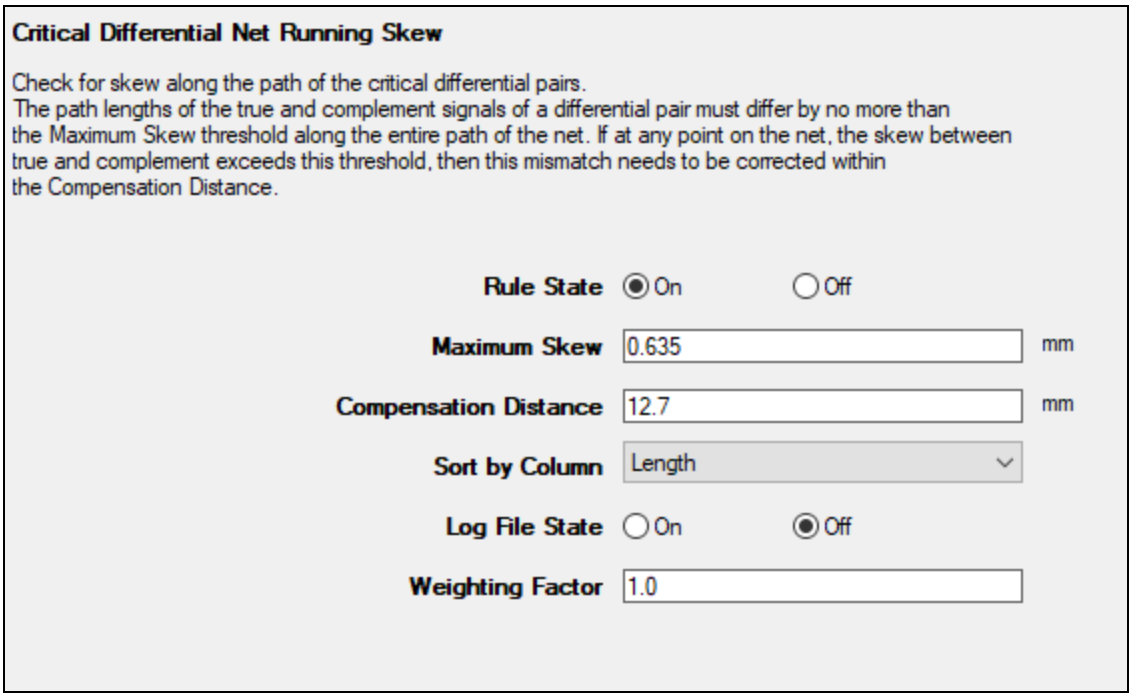

This rule checks for skew along the path of critical differential pairs.

From here, you can set the following:

- **Rule State** – toggles Diff Running Skew rules on or off.
- **Maximum Skew** – sets the maximum allowable skew.
- **Compensation Distance** – skew that exceeds the maximum allowable skew must be corrected within this distance.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

4. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

Note:

- You can display a description of a rule parameter at any time by hovering the cursor over it.
- Units of measure are set in General Settings.

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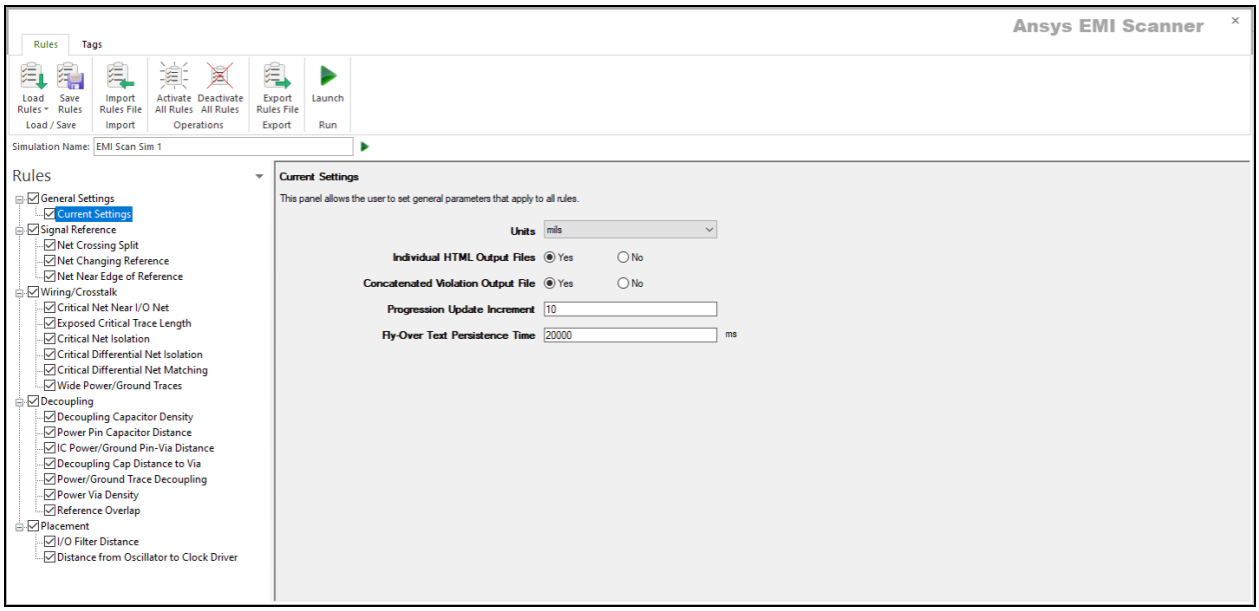
Applying Via Integrity Rules

To change EMI Scanner Via Integrity rules:

1. Launch EMI Scanner.

   The **EMI Scanner** window appears, on the **Rules** tab.



2. Click **Load Rules** and select a profile containing Signal Integrity rules (e.g., Default SI Rules Profile).

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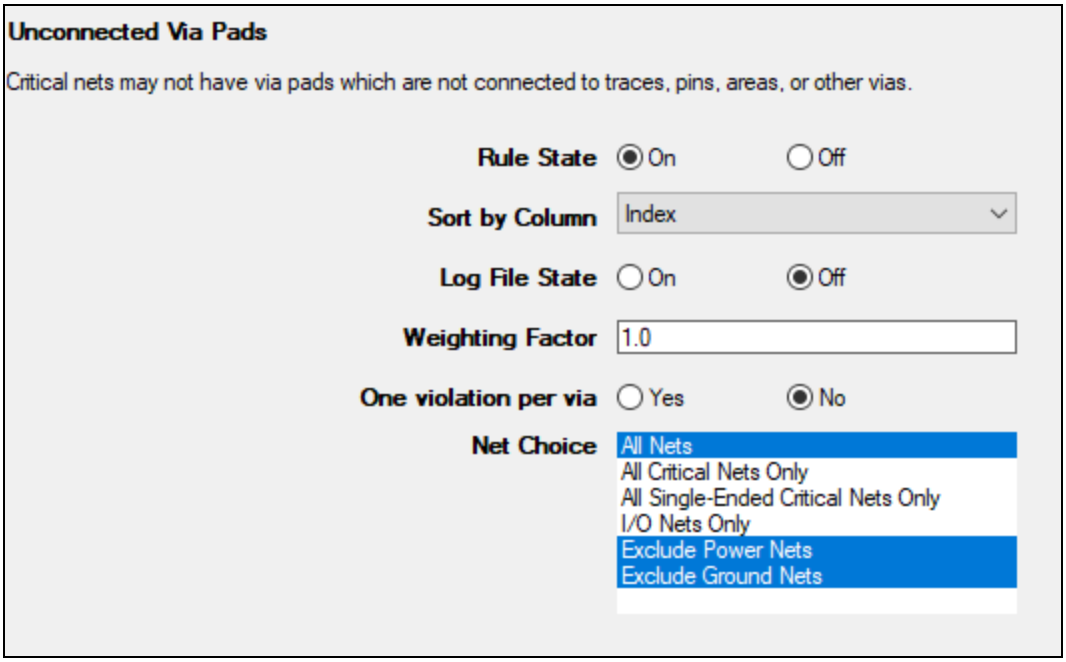
3. From the Rules pane, select one of the four subcategories under **Via Integrity**:
   - **Unconnected Via Pads** – displays the **Unconnected Via Pads** rule configuration.



This rule states that critical nets may not have via pads that are not connected to traces, pins, areas, or other vias.

From here, you can set the following:

- **Rule State** – toggles Unconnected Via Pads rules on or off.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **One Violation Per Via** – when selected, multiple violations on a via will be counted as one violation.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

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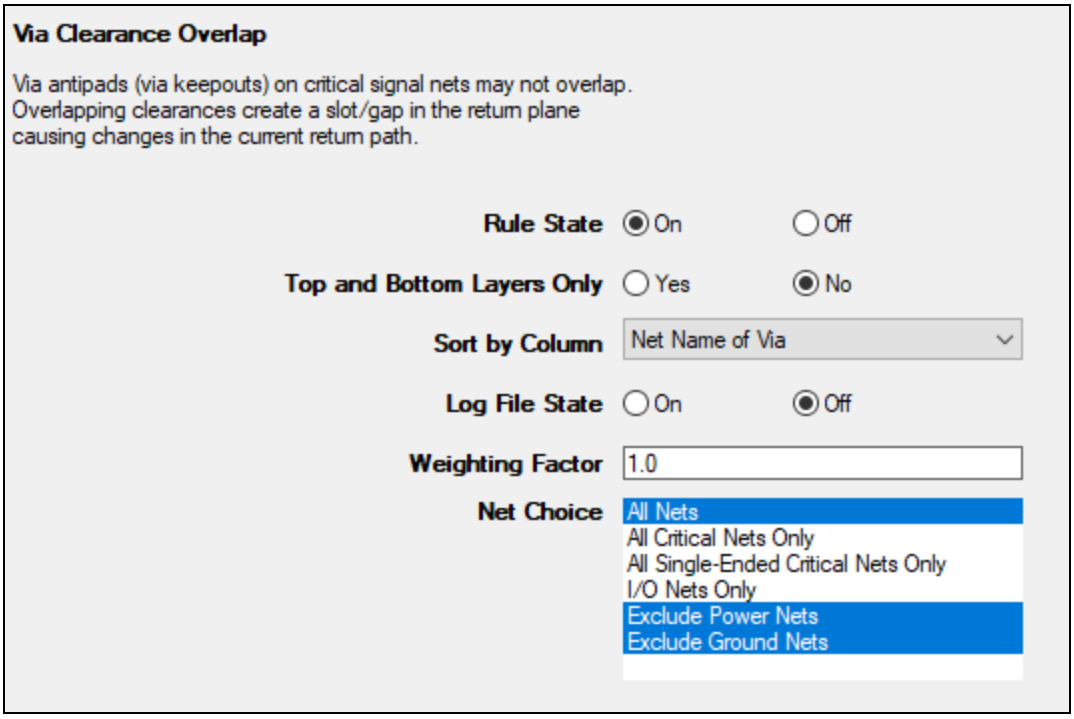
- **Via Clearance Overlap** – displays the **Via Clearance Overlap** rule configuration.



This rule states that via antipads on critical signal nets may not overlap.

From here, you can set the following:

- **Rule State** – toggles Via Clearance Overlap rules on or off.
- **Top and Bottom Layers Only** – limits analysis to the top and bottom layers only.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

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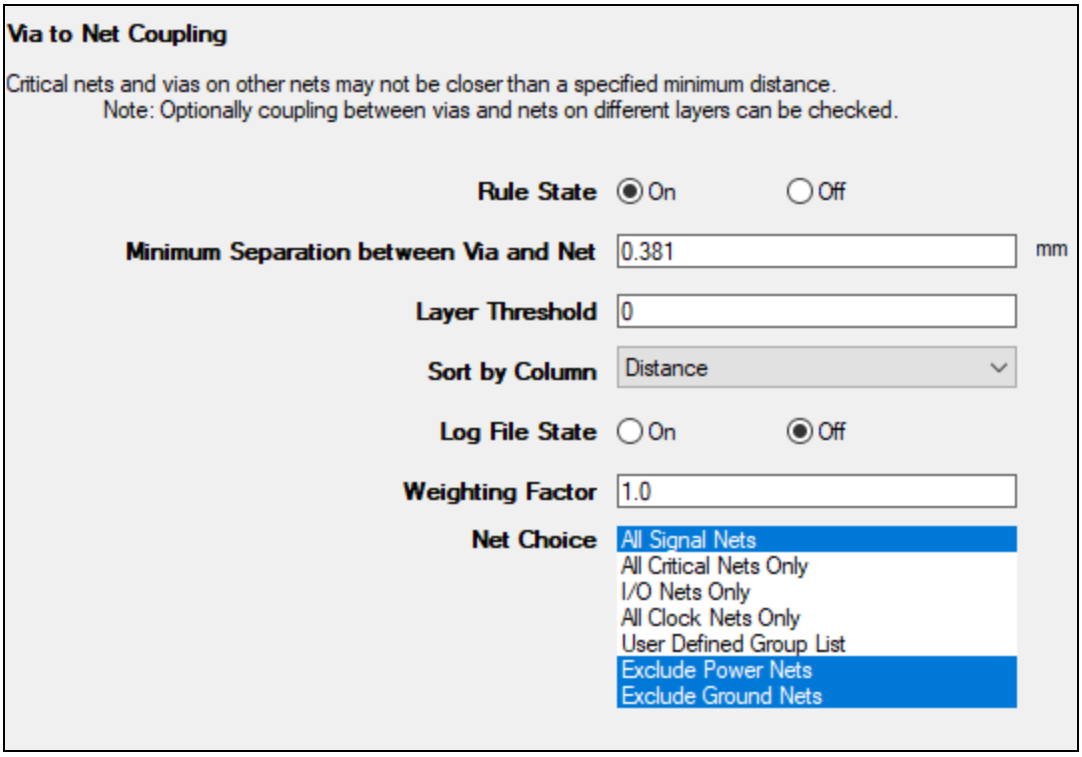
- **Via to Net Coupling** – displays the **Via to Net Coupling** rule configuration.



This rule states that critical nets and vias on other nets may not be closer than a specified minimum distance.

From here, you can set the following:

- **Rule State** – toggles Via to Net Coupling rules on or off.
- **Minimum Separation Between Via and Net** – controls how close the net and the via can be before they are considered coupled.
- **Layer Threshold** – sets the number of layers above and below to check for coupling (e.g., 0 = only the selected layer, 1 = the selected layer plus one layer above and one layer below).
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

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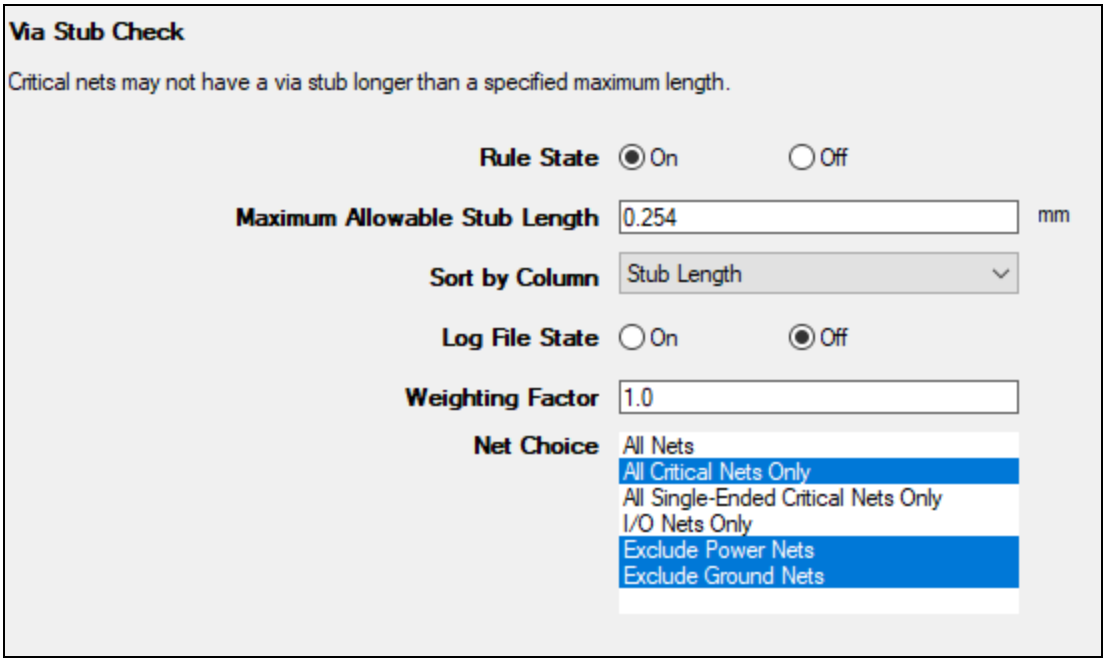
- **Via Stub** – displays the **Via Stub Check** rule configuration.



This rule states that critical nets may not have a via stub longer than a specified maximum length.

From here, you can set the following:

- **Rule State** – toggles Via Stub rules on or off.
- **Maximum Allowable Stub Length** – specifies the maximum stub length. Any stub longer than this setting is a violation.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

4. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

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Note:

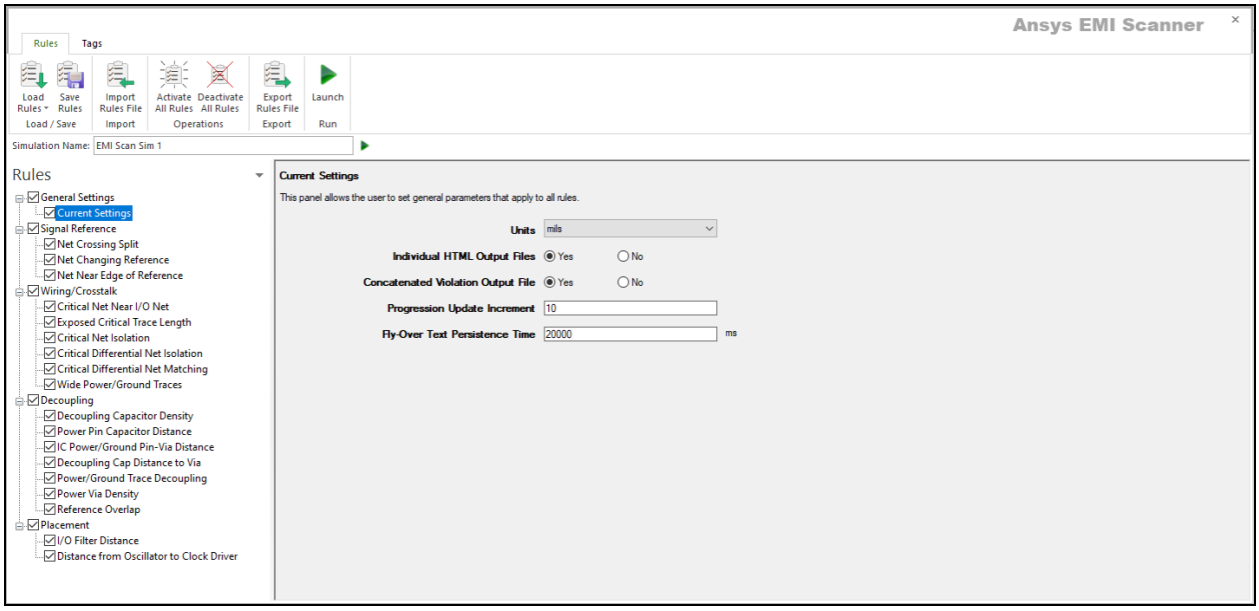
- You can display a description of a rule parameter at any time by hovering the cursor over it.
- Units of measure are set in General Settings.

Applying Power Integrity Rules

To change EMI Scanner Power Integrity rules:

1. Launch EMI Scanner.

   The **EMI Scanner** window appears, on the **Rules** tab.



2. Click **Load Rules** and select a profile containing Signal Integrity rules (e.g., Default SI Rules Profile).
3. From the Rules pane, select one of the seven subcategories under **Power Integrity**:
   - **Wide Power/Ground Traces** – displays the **Wide Power/Ground Traces** rule configuration.

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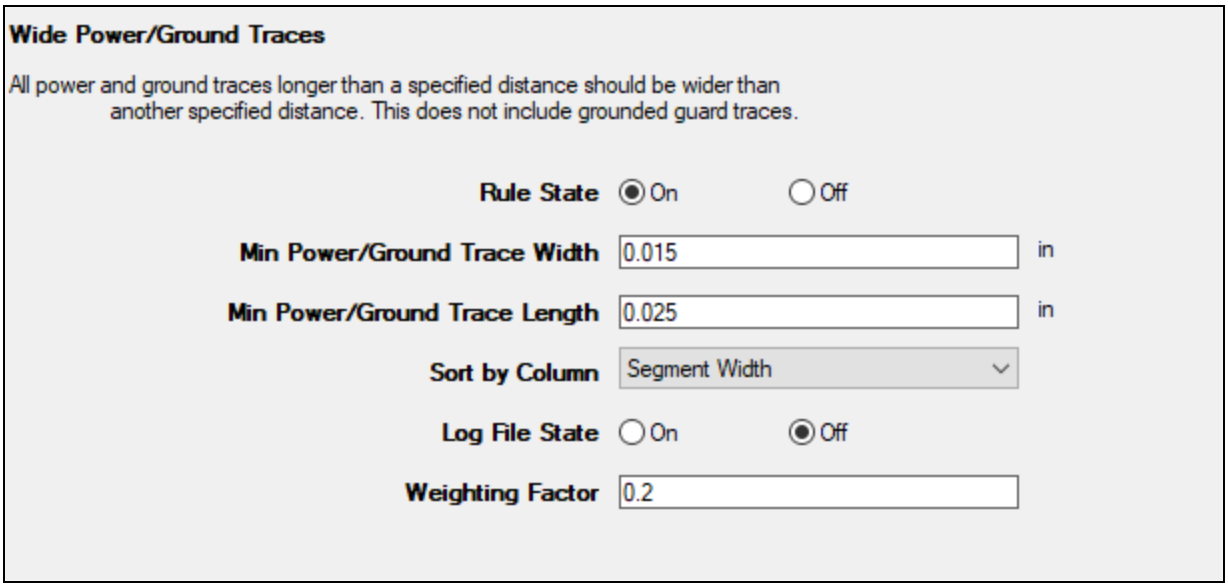

This rule states that all power and ground traces longer than a specified distance should be wider than another specified distance.

From here, you can set the following:

- **Rule State** – toggles Wide Power/Ground Traces rules on or off.
- **Min Power/Ground Trace Width** – sets the minimum width limit for all power/ground traces (except grounded guard traces).
- **Min Power/Ground Trace Length** – sets the minimum length limit for all power/ground traces (except grounded guard traces).
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

- **Decoupling Capacitor Density** – displays the **Decoupling Capacitor Density** rule configuration.

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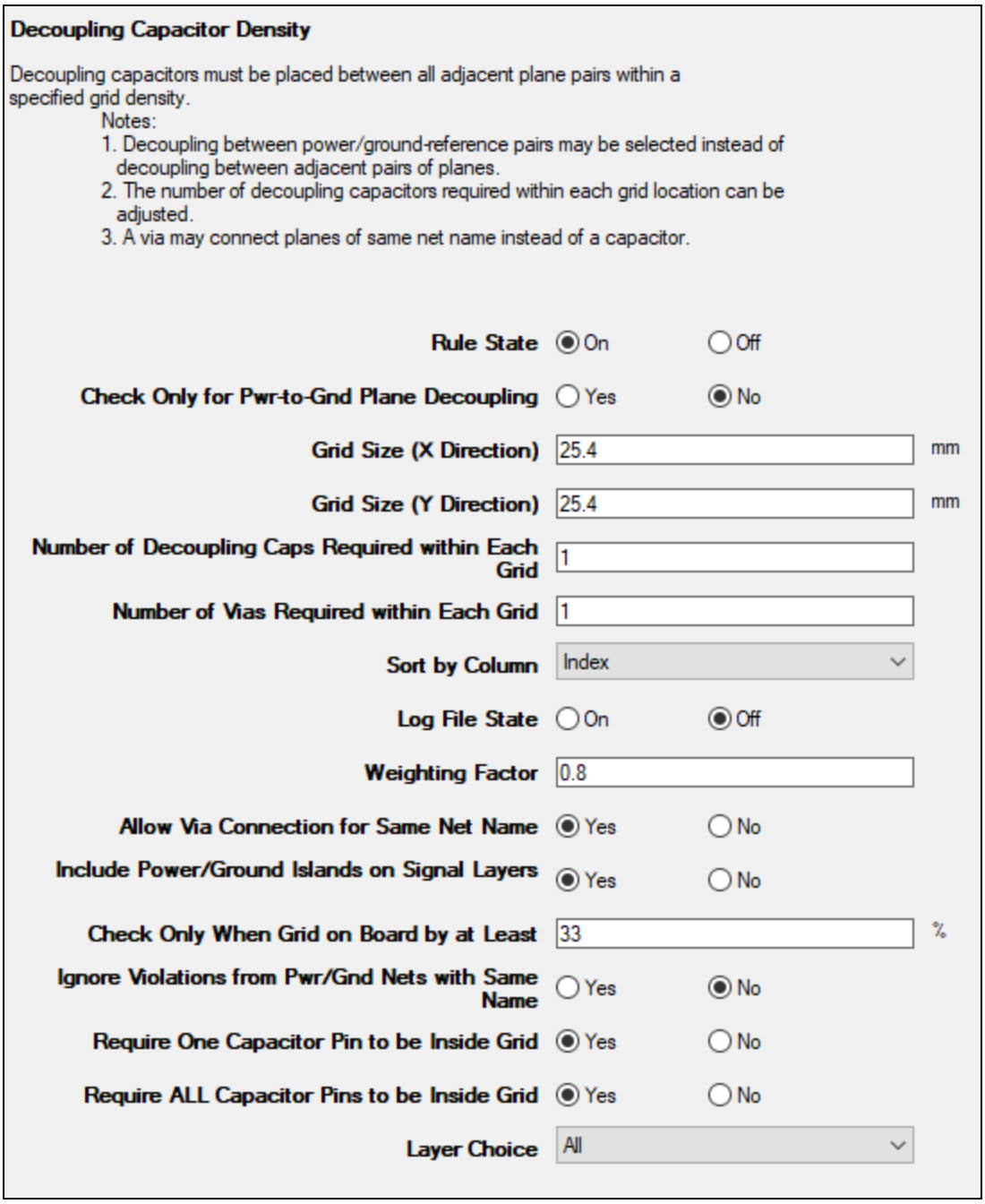

This rule states that decoupling capacitors must be placed between all adjacent plane pairs within a specified grid density.

From here, you can set the following:

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- **Rule State** – toggles Decoupling Capacitor Density rules on or off.
- **Check Only for Pwr-to-Gnd Plane Decoupling** – sets whether to ignore plane-to-plane decoupling and check only for decoupling capacitors between power and ground planes.
- **Grid Size (X Direction)** – specifies the size of the grid used to check for decoupling capacitors. Used in conjunction with **Grid Size (Y Direction)**.
- **Grid Size (Y Direction)** – specifies the size of the grid used to check for decoupling capacitors. Used in conjunction with **Grid Size (X Direction)**.
- **Number of Decoupling Caps Required within Each Grid** – specifies the number of decoupling capacitors connecting between planes that are required within each grid location.
- **Number of Vias Required within Each Grid** – specifies the number of vias connecting between planes that are required within each grid location. You must select **Allow Via Connection for Same Net Name** to use this option.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Allow Via Connection for Same Net Name** – determines whether EMI Scanner allows a via in place of a decoupling capacitor when the two planes are the same net name.
- **Include Power/Ground Islands on Signal Layers** – specifies whether to check for decoupling on power/ground islands.
- **Check Only When Grid on Board by at Least** – specifies the percentage of a grid that must be on the board in order for it to be checked.
- **Ignore Violations from Pwr/Gnd Nets with Same Name** – determines that only one plane of a given name is checked for violations (e.g., if two planes are "gnd" and a violation occurs between gnd and another layer, only one violation is reported).
- **Require One Capacitor Pin to be Inside Grid** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **Require ALL Capacitor Pins to be Inside Grid** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **Layer Choice** – specifies the layers to include in this rule analysis.

- **Power Pin Capacitor Distance** – displays the **Decoupling Capacitor Distance from IC Power Pin** rule configuration.

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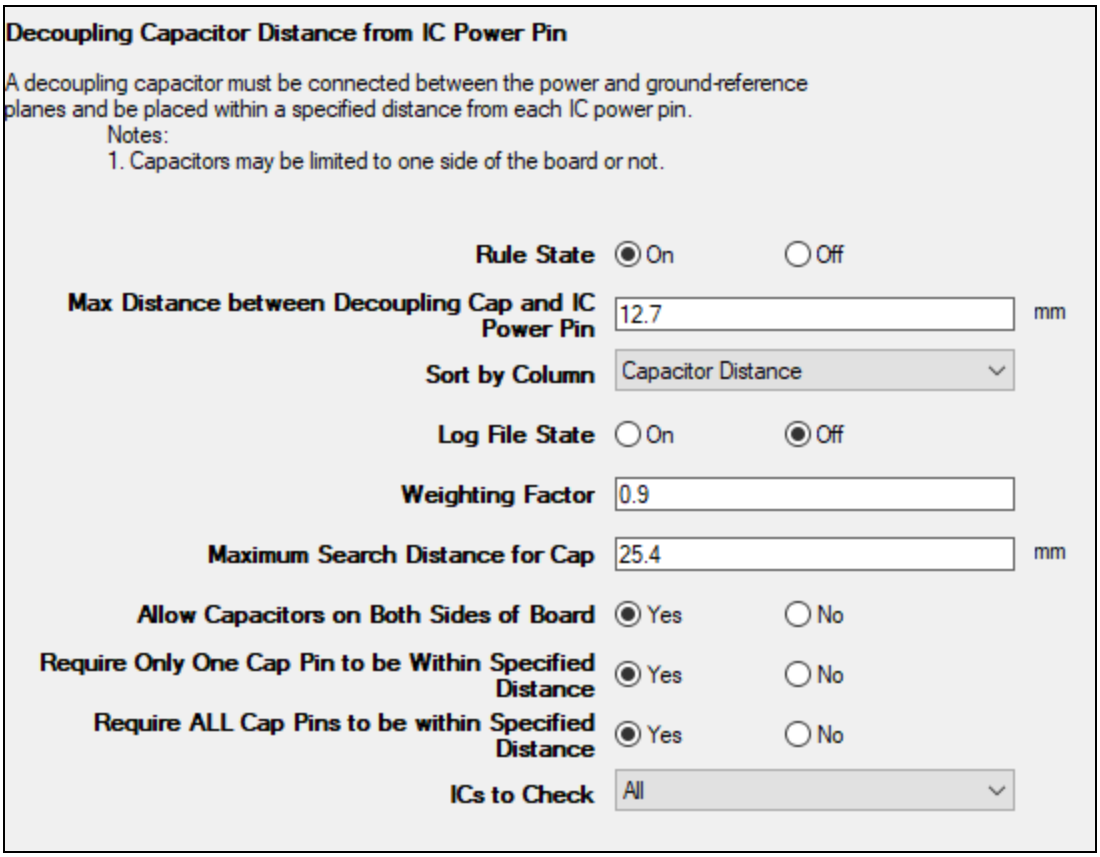

This rule states that a decoupling capacitor must be connected between the power and ground-reference planes and be placed within a specified distance of each IC power pin.

From here, you can set the following:

- **Rule State** – toggles Power Pin Capacitor Distance rules on or off.
- **Max Distance Between Decoupling Cap and IC Power Pin** – specifies the maximum distance between an IC power pin and its decoupling capacitor.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Maximum Search Distance for Cap** – specifies the maximum search distance for a capacitor. A larger search box increases the chances of EMI Scanner finding capacitors, but can slow processing time.

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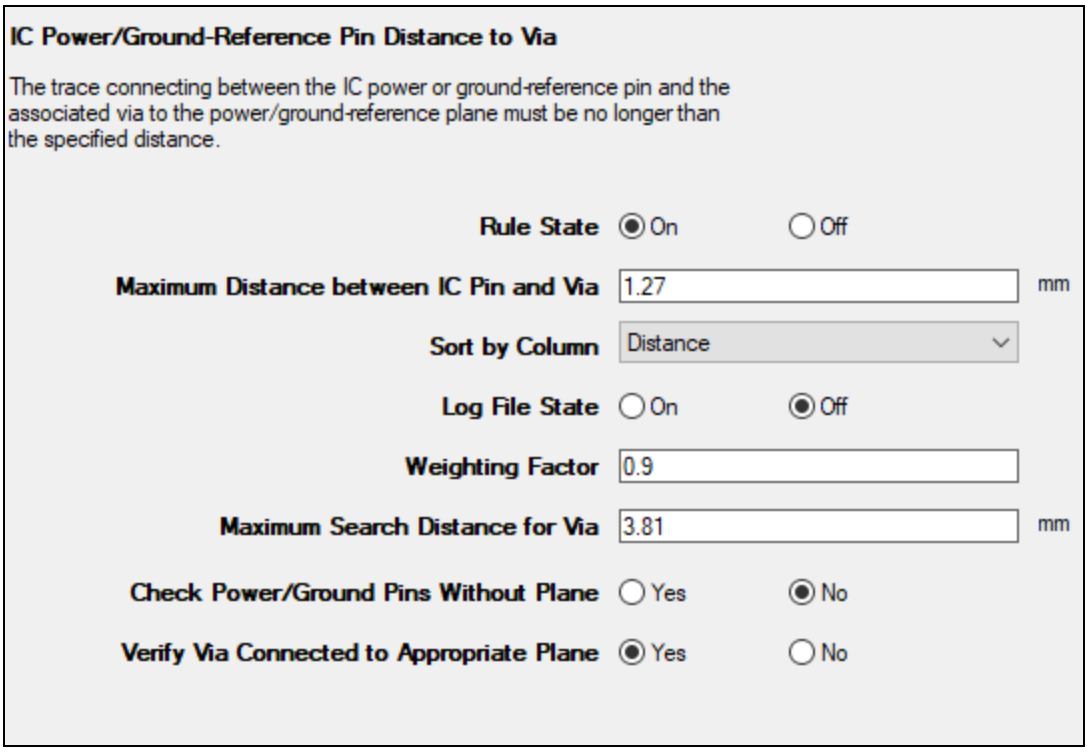
- **Allow Capacitors on Both Sides of Board** – allows EMI Scanner to include capacitors on both sides of the board to satisfy this rule.
- **Require Only One Cap Pin to be within Specified Distance** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **Require ALL Cap Pins to be within Specified Distance** – changes how EMI Scanner determines whether a component is inside or outside the grid. See Technical Note.
- **ICs to Check** – specifies the types of components to include in this rule analysis.

- **IC Power/Ground Pin-Via Distance** – displays the **IC Power/Ground-Reference Pin Distance to Via** rule configuration.



This rule states that the trace connecting the IC power or ground-reference pin and the associated via to the ground/reference plane must be no longer than a specified distance..

From here, you can set the following:

- **Rule State** – toggles IC Power/Ground Pin-Via Distance rules on or off.
- **Maximum Distance Between IC Pin and Via** – specifies the maximum distance between the IC power or ground-reference pin and the via to the power or ground-reference plane.

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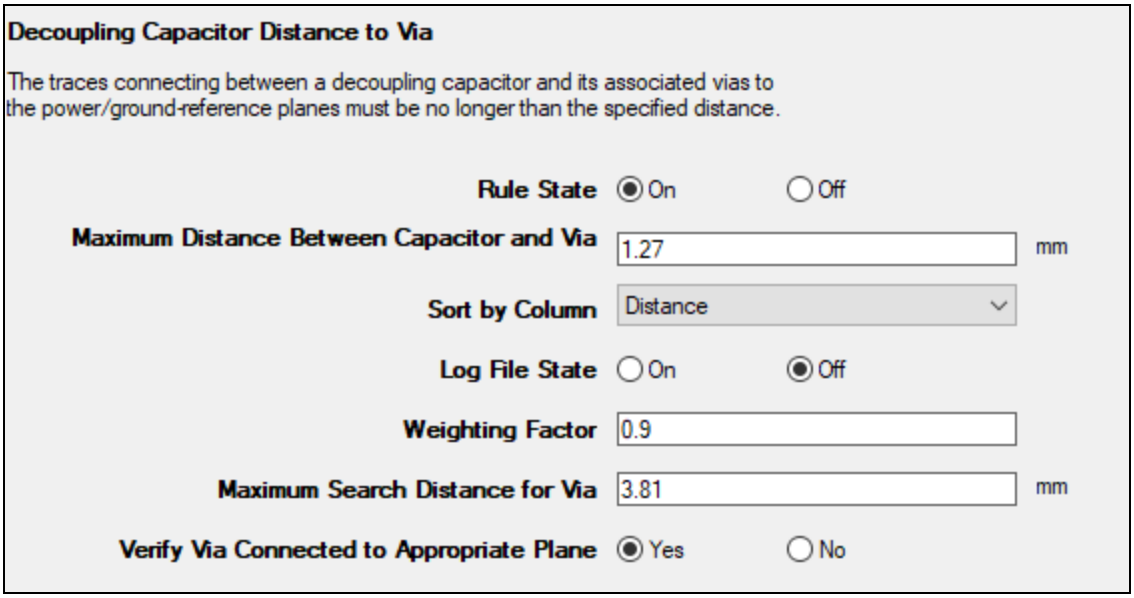
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Maximum Search Distance for Via** – specifies the maximum search distance for a via when a violation is found. This allows users to quickly determine if the via is barely outside the original requirement and therefore not a serious violation.
- **Check Power/Ground Pins Without Plane** – specifies whether to check the distance between the IC power/ground pin and its via when the power/ground plane has not been completed yet.
- **Verify Via Connected to Appropriate Plane** – specifies whether or not EMI Scanner verifies that the via connects to an appropriate plane (shape). Selecting 'no' speeds up processing.

- **Decoupling Cap Distance to Via** – displays the **Decoupling Capacitor Distance to Via** rule configuration.



This rule states that the traces connecting a decoupling capacitor and its associated vias to the power/ground-reference planes must be no longer than a specified distance.

From here, you can set the following:

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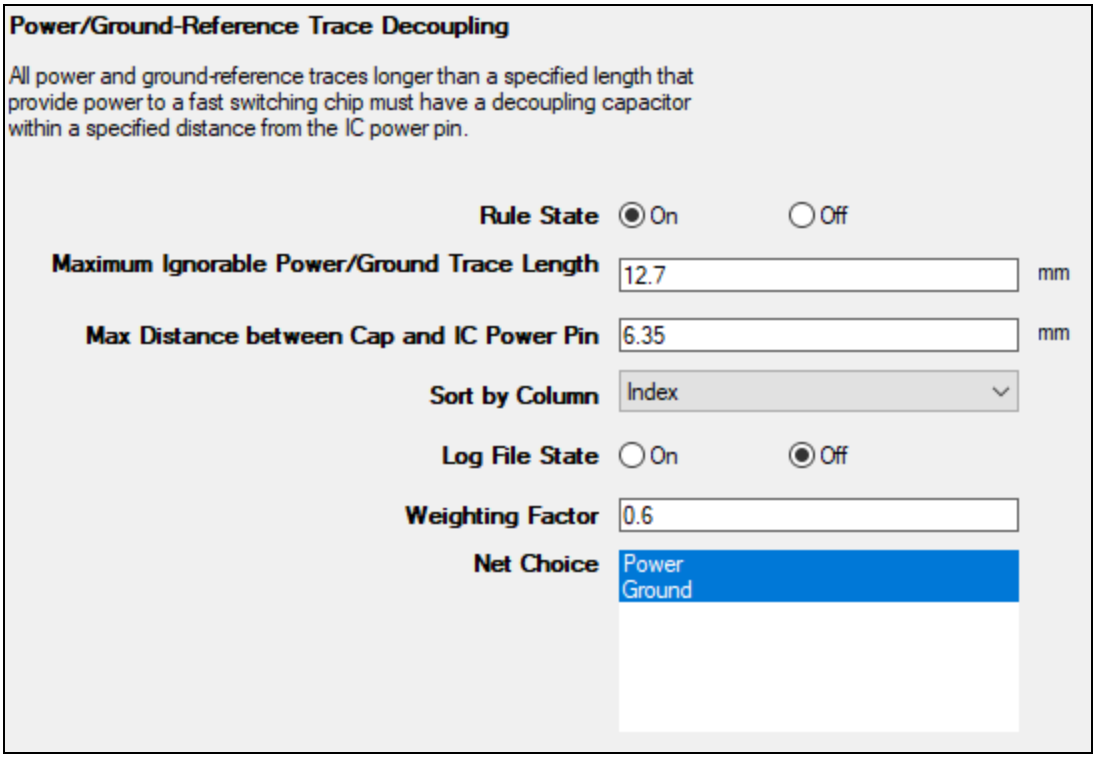
- **Rule State** – toggles Decoupling Capacitor Distance to Via rules on or off.
- **Maximum Distance Between Capacitor and Via** – specifies the maximum distance between the capacitor pin and the via to the power or ground-reference plane.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Maximum Search Distance for Via** – specifies the maximum search distance for a via when a violation is found. This allows users to quickly determine if the via is barely outside the original requirement and therefore not a serious violation.
- **Verify Via Connected to Appropriate Plane** – specifies whether or not EMI Scanner verifies that the via connects to an appropriate plane (shape). Selecting 'no' speeds up processing.

- **Power/Ground Trace Decoupling** – displays the **Power/Ground-Reference Trace Decoupling** rule configuration.



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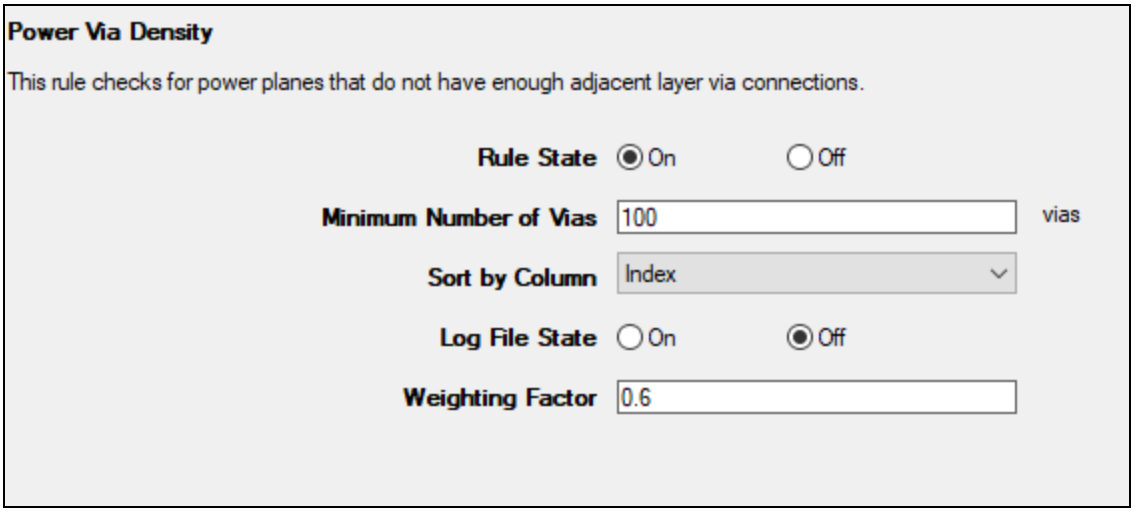
This rule states that all power and ground-reference traces longer than a specified length that provide power to a fast switching chip must have a decoupling capacitor within a specified distance from the IC power pin.

From here, you can set the following:

- **Rule State** – toggles Power/Ground-Reference Trace Decoupling rules on or off.
- **Maximum Ignorable Power/Ground Trace Length** – specifies the maximum allowable power/ground trace length that may be ignored. All traces longer than this length must meet this rule's requirement.
- **Max Distance Between Cap and IC Power Pin** – specifies the maximum distance between the capacitor pin and the power or ground-reference pin.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.
- **Net Choice** – specifies the nets to include in this rule analysis. Select one, or Ctrl+click to select multiple nets.

- **Power Via Density** – displays the **Power Via Density** rule configuration.



This rule checks for power planes that do not have enough adjacent layer via connections.

From here, you can set the following:

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- **Rule State** – toggles Power Via Density rules on or off.
- **Minimum Number of Vias** – sets the minimum number of vias required to connect adjacent power planes.
- **Sort by Column** – specifies the column by which results are sorted.
- **Log File State** – determines whether EMI Scanner creates a log file with additional details (intended for use in debugging).
- **Weighting Factor** – specifies the weighting factor (0<factor<=1) that is applied to violations of this rule when assigning a rank. A violation's rank is its own "degree of badness" multiplied by the weighting factor. See Exporting EMI Scanner Results and Analyzing EMI Scanner Results Using iQ-Harmony.

4. Rules are automatically saved for the current EMI scan. To save them for a future scan, click **Save Rules**.

Note:

- You can display a description of a rule parameter at any time by hovering the cursor over it.
- Units of measure are set in General Settings.

Using Tags in EMI Scanner

The EMI Scanner **Tags** tab contains tag assignment panes as well as a ribbon with the following buttons:

- **Save Tags** – saves tags to the **Tags** pane.
- **Import Tags File** – allows you to import tags from a *.tgs file.
- **Auto Tag Settings** – allows you to change default tagging behavior.
- **Rescan Design & Auto Tag** – applies new tagging behavior.
- **Clear All Tag Assignments** – unassigns all nets and components from tags.
- **Switch User Defined Tags Library** – allows you to browse to a different tagset.
- **New Tag** – creates a new tag.
- **Rename Tag** – renames a user-created tag.
- **Copy Tag** – copies a tag's properties into a new tag.
- **Delete Tag** – removes a tag from the **Tags** pane.
- **Record/Stop Macro** – starts or stops macro recording.
- **Run Macro** – runs a previously recorded macro.
- **Undo** – used to undo the previous action (only for manual assignments).
- **Redo** – used to restore an undone action (only for manual assignments).
- **Export Tags File** – allows you to export tags in a *.tgs file for later use.
- **Launch** – begins the EMI scan.

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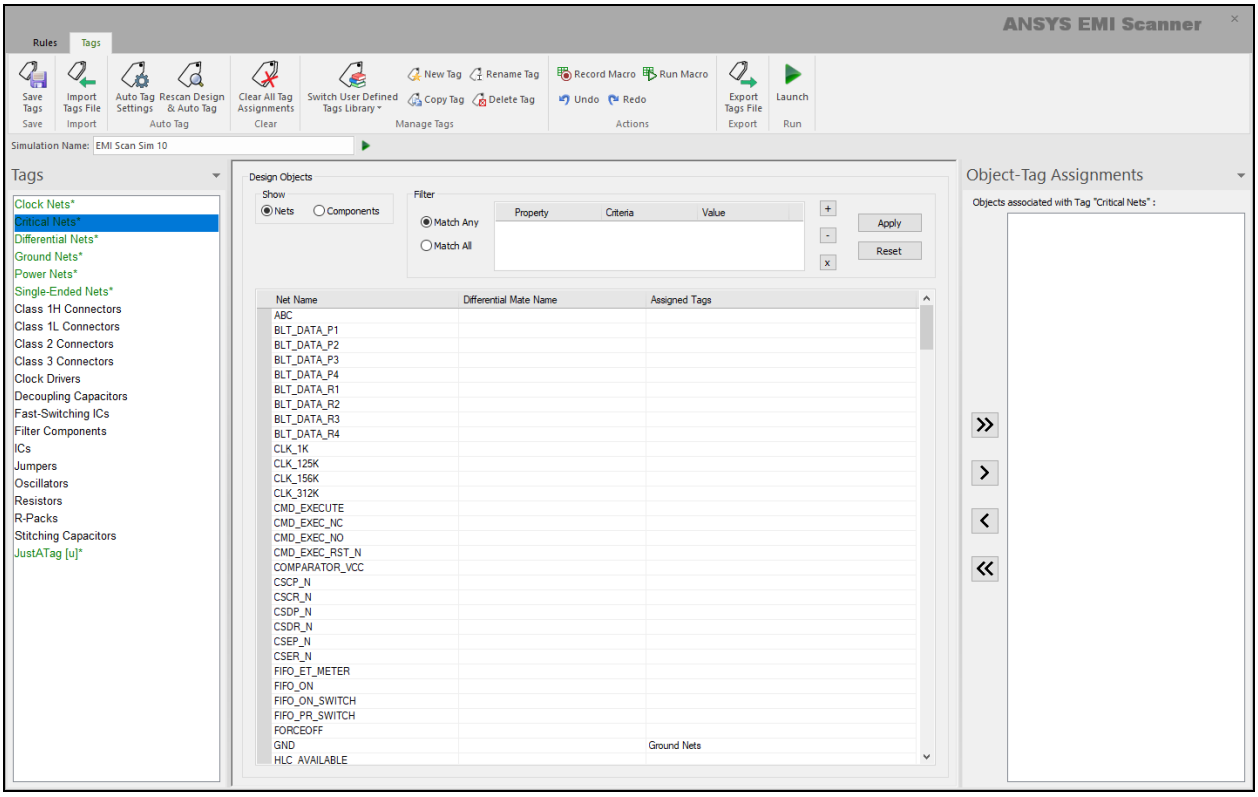

From the Tags pane (located on the left), Net tags appear in green, while Component tags appear in black. User-created tags are denoted by **[u]**.

Tags can be assigned automatically or manually.

You can also add custom tags or create a tagging macro.

Assigning Tags Automatically

Upon loading, some tags are automatically assigned nets or components. By default, Auto Tag makes the following selections:

- **Critical Nets** – non power-ground nets that have a port.
- **Differential Nets** – those set up in the Differential Nets workspace.
- **Power/Ground Nets** – those set up in the Power/Ground workspace. Otherwise, distinguished by net name.
- **Decoupling Capacitors** – capacitors with names starting from C or EMC, with a value less than 10uF.
- **Stitching Capacitors** – capacitors connecting two power planes or two ground planes.

To change Auto Tag settings:

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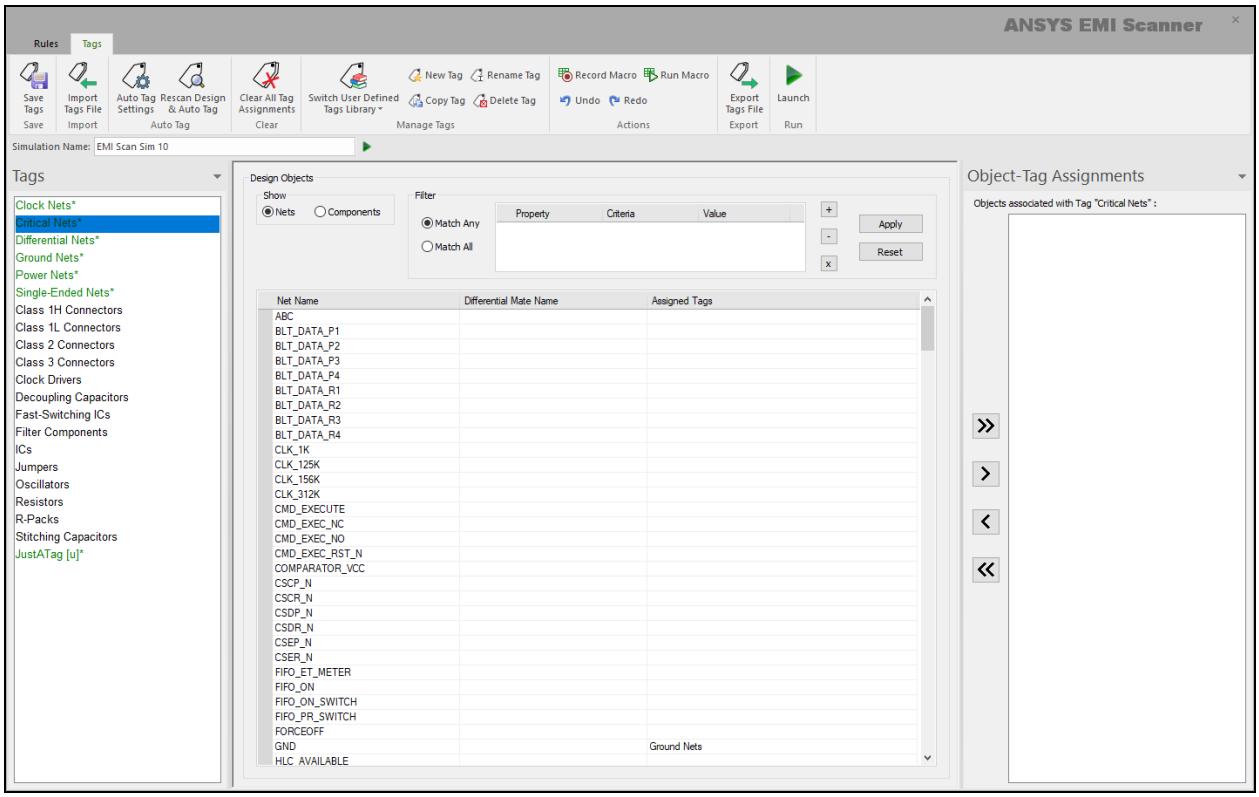
1. Launch EMI Scanner.
2. Click **Tags**.

   The **EMI Scanner** displays the **Tags** tab.



   Net tags appear in green, while Component tags appear in black.
3. From the **Auto Tag** area, click **Auto Tag Settings**.

   The **Auto Tag Settings** window appears.

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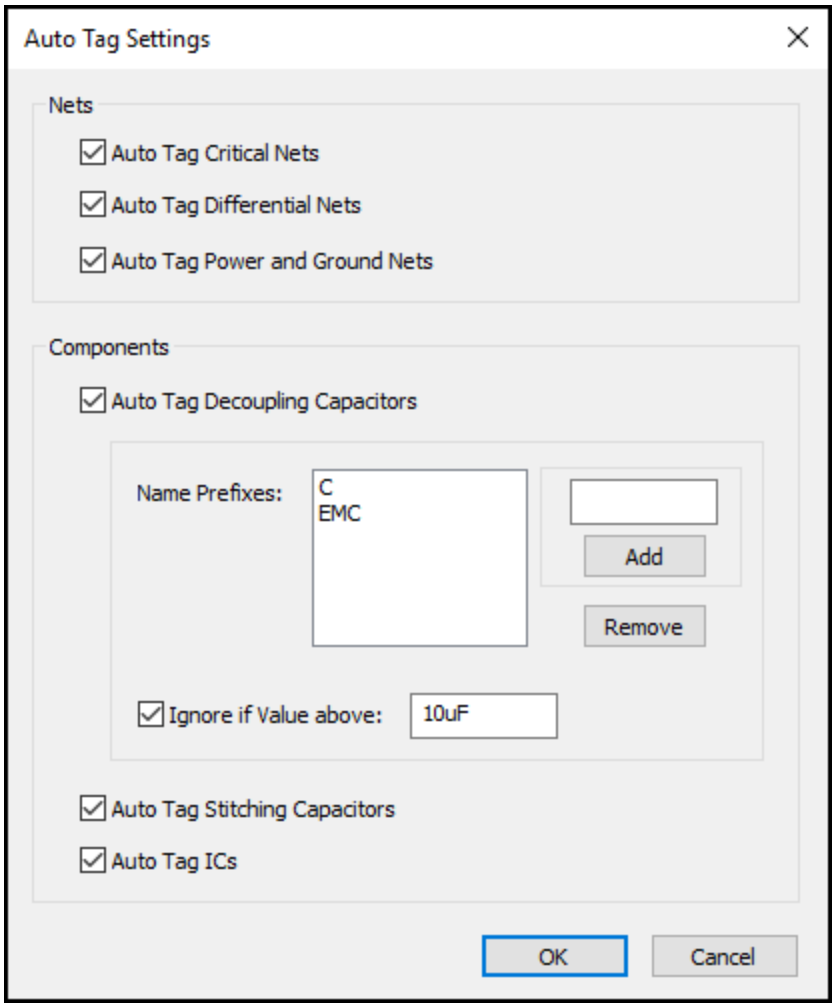

4. From the **Nets** area, determine the types of nets you would like automatically tagged.
5. From the **Components** area, use the check boxes to determine whether to automatically tag Decoupling Capacitors, Stitching Capacitors, or ICs.

   If you select **Auto Tag Decoupling Capacitors**, you can choose to **Add** or **Remove** name prefixes using the list and text field. You can also select **Ignore if Value above** to ignore capacitors above the value you specify.
6. Click **OK** to apply settings and return to the **EMI Scanner** window.
7. Click **Rescan Design & Auto Tag**.

   The design is scanned and tagged according to your settings.

   The **EMI Scanner** window displays the new tags in the **Object-Tag Assignments** pane for each tag.

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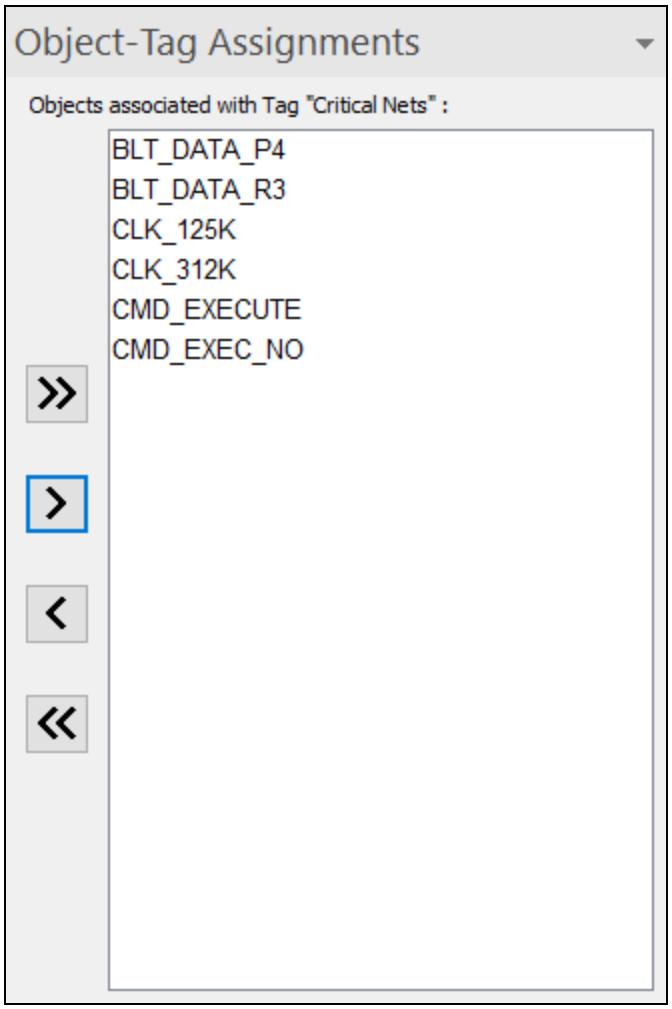

Assigning Tags Manually

To assign tags manually:

1. Launch EMI Scanner.
2. Click **Tags**.

   The **EMI Scanner** displays the **Tags** tab.

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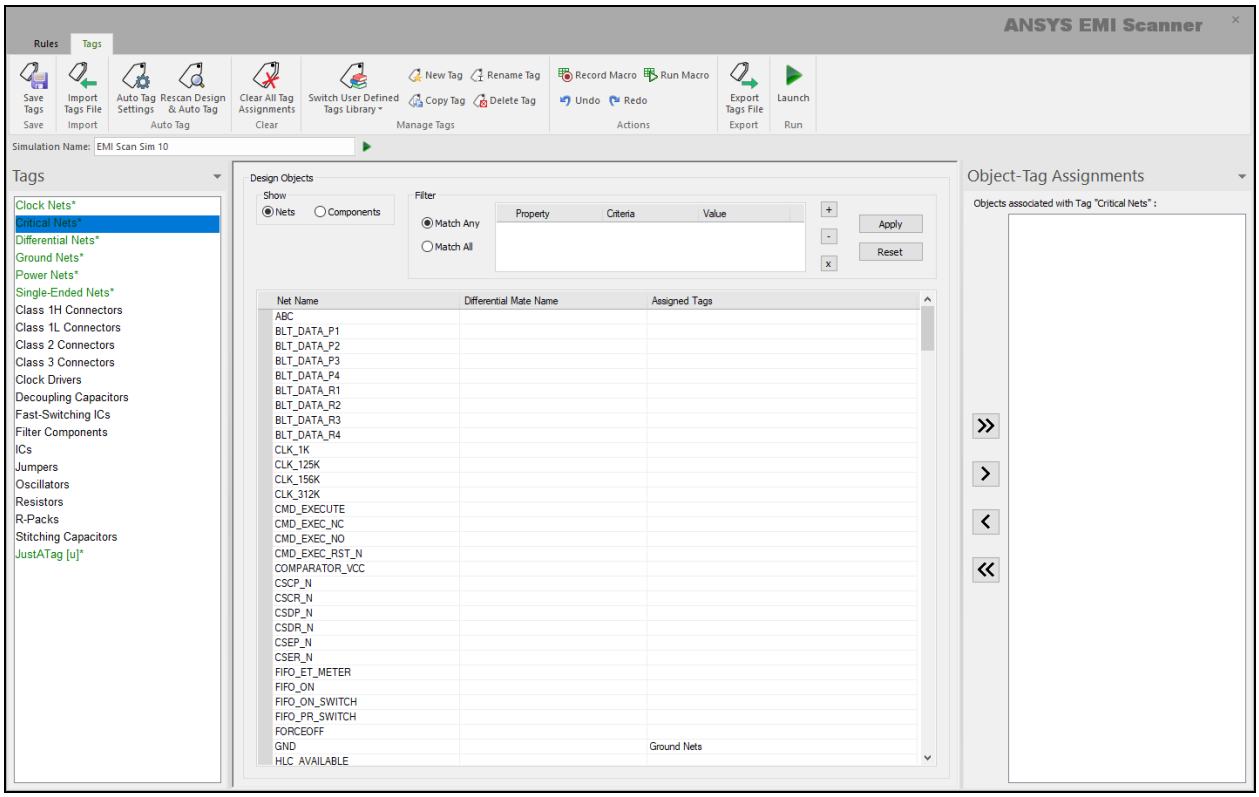
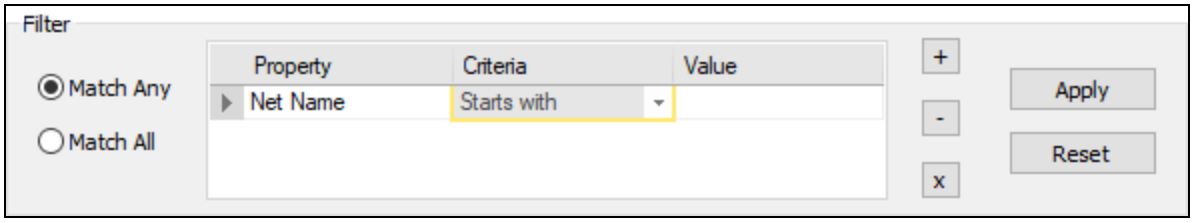


Net tags appear in green, while Component tags appear in black.

3. From the **Tags** pane, select a tag (e.g., Clock Nets, Decoupling Capacitors, Resistors) to which you would like to assign nets or components. You can also add custom tags.
4. The center pane updates to display a list of eligible nets or components. If appropriate, you can apply filters to view only the nets or components you're looking for:



a. Select either **Match Any** (nets or components matching any one criterion will display) or **Match All** (only nets or components meeting all criteria will display).
b. Add or remove rows from the filter list using the Add (**+**) and Remove (**-**) buttons. You can also clear all criteria by clicking (**X**).

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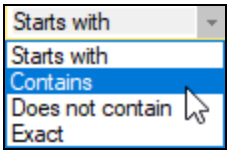
c. Use the **Criteria** drop-down menu to select the filter type.



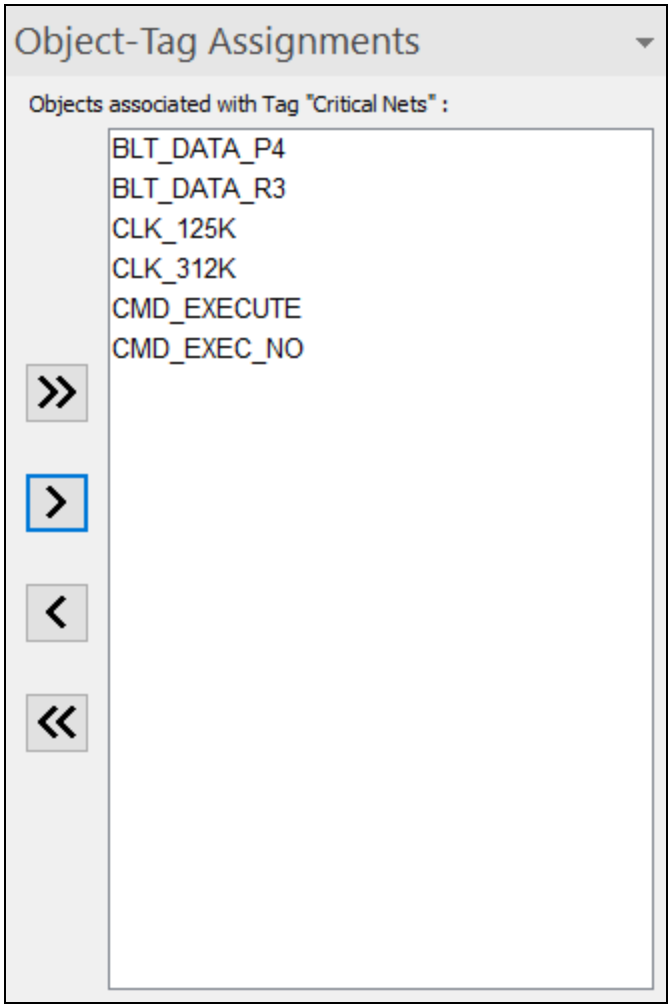
d. Enter filter values in the **Value** field.

e. Click **Apply** to apply the filters and update the net/component list.

f. Click **Reset** to remove the filter and display the default nets or components.

5. Select nets or components in the list, and use the right arrow button (**>**) to assign them. Use the double arrow (**>>**) to assign all listed nets or components to that tag.

   Assigned nets or components appear in the **Object-Tag Assignments** pane.



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You can unassign nets or components individually by selecting them and using the left arrow (**<**), or unassign all nets or components using the double arrow (**<<**).

6. If appropriate, click **Export Tags File** to save your tags as a *.tgs file. You can later click **Import Tags File** to use these settings again.

Working with Custom Tags

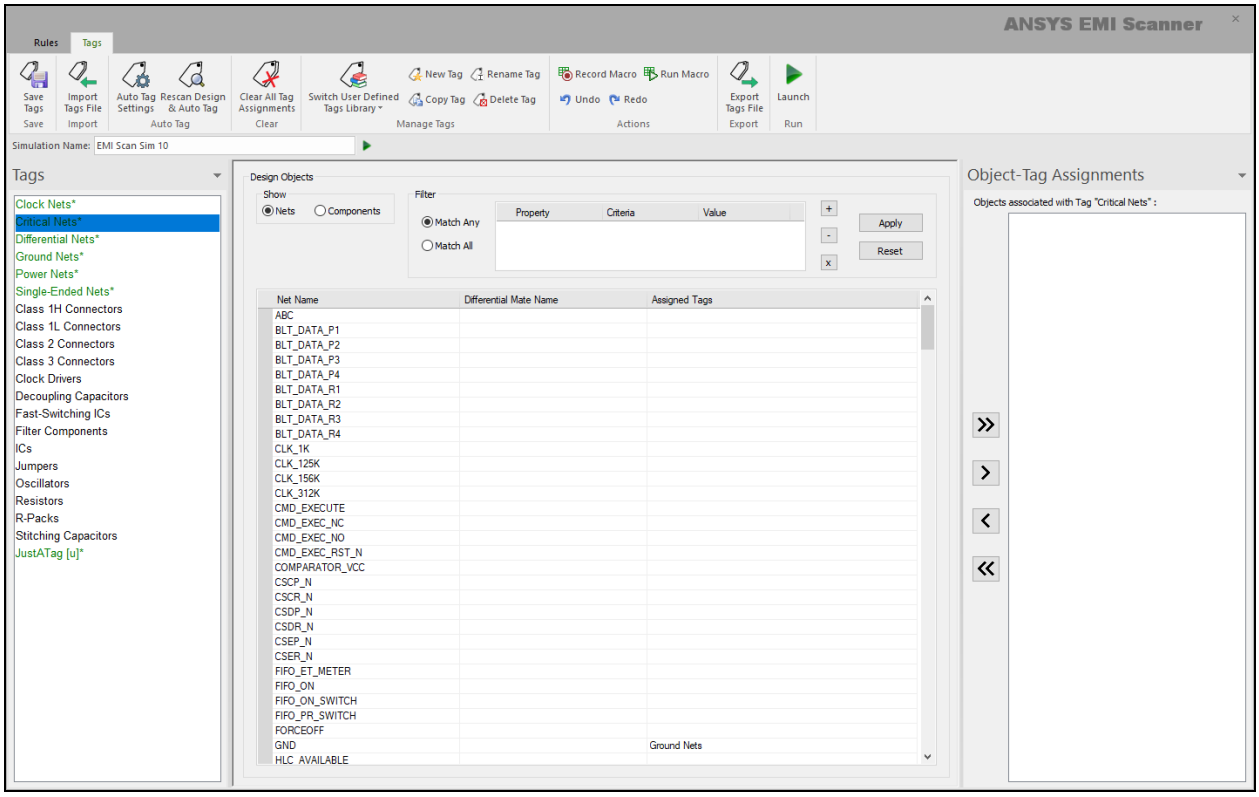
In addition to the default tags, EMI Scanner allows you to create and assign custom tags. User-created tags are denoted by **[u]** in the Tags pane, and can be assigned manually.

Adding Custom Tags

To add tags:

1. Launch EMI Scanner.
2. Click **Tags**.

   The **EMI Scanner** displays the **Tags** tab.



Tags are listed in the Tags pane on the left. Net tags appear in green, while Component tags appear in black.

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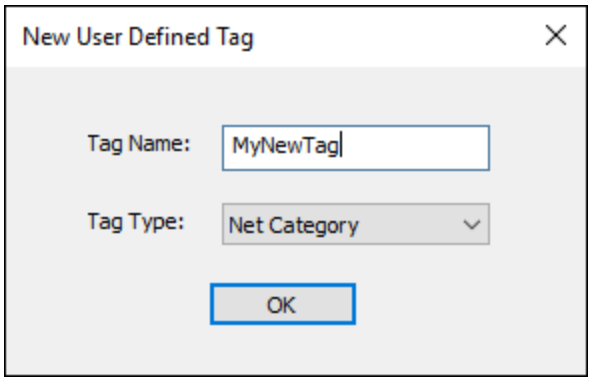
3. From the **Manage Tags** area of the ribbon, click **New Tag**.

   The **New User Defined Tag** window appears.



4. Enter a **Tag Name** and select the **Tag Type**. You can create a tag either in the **Net Category** or **Component Category**.
5. Click **OK** to return to the **EMI Scanner** window.

   The new tag appears at the bottom of the **Tags** pane, with a **[u]** indicating that it is a user-created tag.

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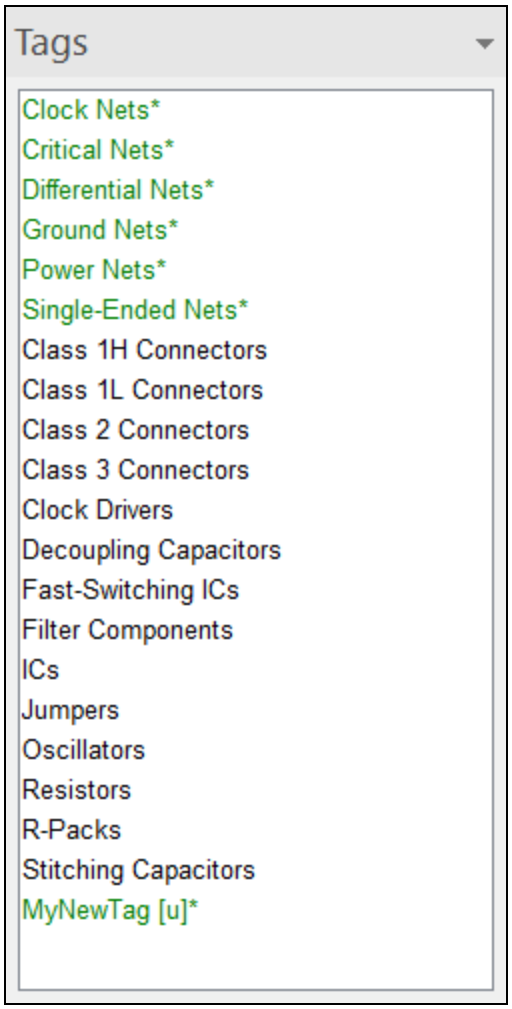

6. To save your tags, click **Save Tags**.

   Your tags will appear in the **Tags** pane the next time you launch EMI Scanner.

You can also create a custom tag from an existing tag. To do so:

1. Select a tag from the **Tags** pane.
2. From the **Manage Tags** area, click **Copy Tag**.

   The **Copy User Defined Tag** window appears, with the **Tag Type** already selected.
3. Name the new tag and click **OK**.

   The new tag appears in the **Tags** pane.

Renaming a Custom Tag

To rename a custom tag:

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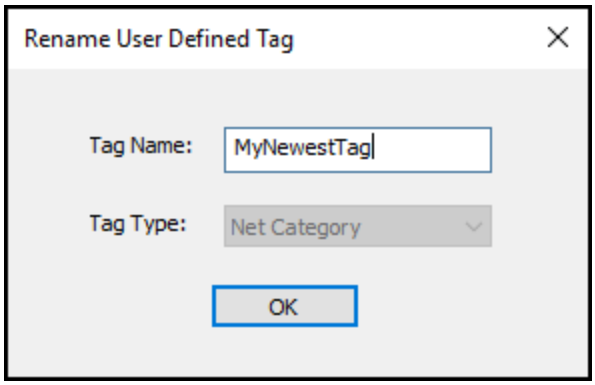
1. Select the tag from the **Tags** pane.
2. From the **Manage Tags** area, click **Rename Tag**.

   The **Rename User Defined Tag** window appears.



3. Rename the tag and click **OK**.

> **Note:**
>
> You can only rename custom tags. You cannot rename a default tag.

Deleting a Custom Tag

To delete a custom tag:

1. Select the tag from the **Tags** pane.
2. Use the double left arrow (**<<**) in the **Object-Tag Assignments** pane to remove any assignments.

> **Important:**
>
> You cannot delete a tag until all object assignments are removed from it.

3. From the **Manage Tags** area, click **Delete Tag**.

   The tag disappears from the **Tags** pane.

> **Note:**
>
> You can only delete custom tags. You cannot delete a default tag.

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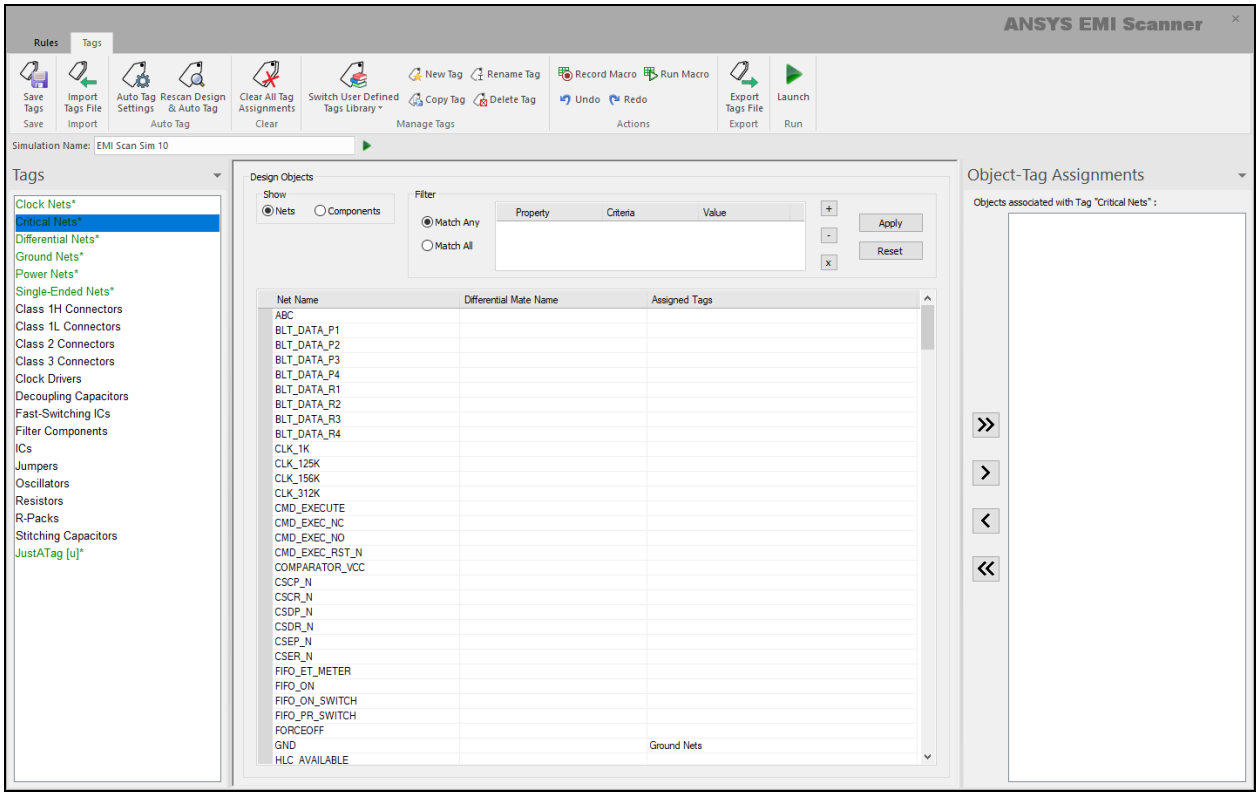
Creating Tagging Macros

You can save your tagging process as a series of steps. Macros are saved as XML-based *.tmx files.

To create a macro:

1. Launch EMI Scanner.
2. Click **Tags**.

   The **EMI Scanner** displays the **Tags** tab.



3. From the **Actions** area of the ribbon, click **Record Macro**.

   The **Record to Macro File** window appears.

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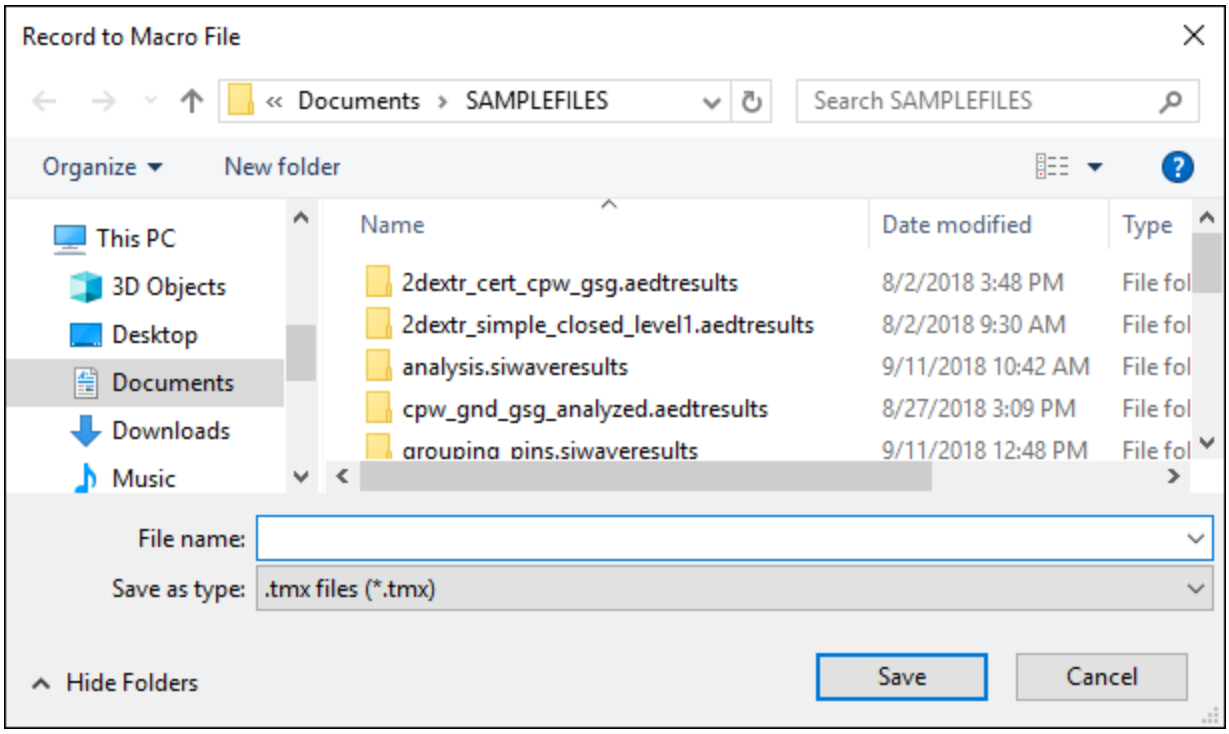
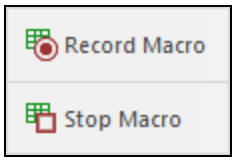


4. Navigate to your appropriate save location, enter a **File name**, and click **Save**.

   The **Record Macro** button becomes a **Stop Macro** button.



5. Perform the actions you wish to save as a macro. You can **Undo** or **Redo** actions using the buttons in the Actions area.
6. When you are finished, click **Stop Macro**.

   The macro *.tmx file is saved at the location you specified earlier.

To run a saved macro, click **Run Macro**.

> **Note:**
>
> You cannot record and run a macro at the same time.

Viewing EMI Scanner Results

To view EMI Scanner results:

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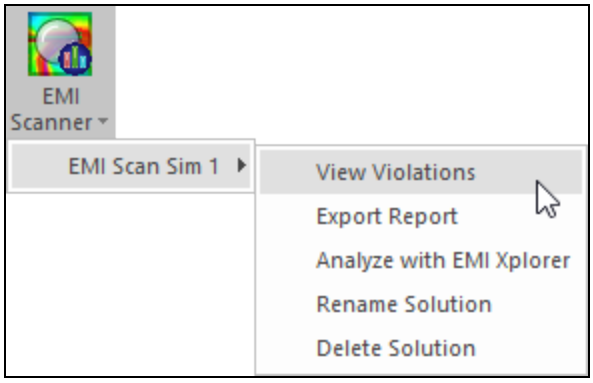
1. Click **Results** > **EMI Scanner** > **[Simulation Name]**.



   Results Menu options include:

   - **View Violations** – opens the violations viewer.
   - **Export Report** – allows you to export an HTML report of EMI rules and violations.
   - **Analyze with EMI Xplorer** – opens the EMI Xplorer.
   - **Rename Solution** – allows you to rename the EMI scan.
   - **Delete Solution** – allows you to delete EMI scan results.

2. Select **View Violations**.

   The **EMI Scan Violations** window appears.

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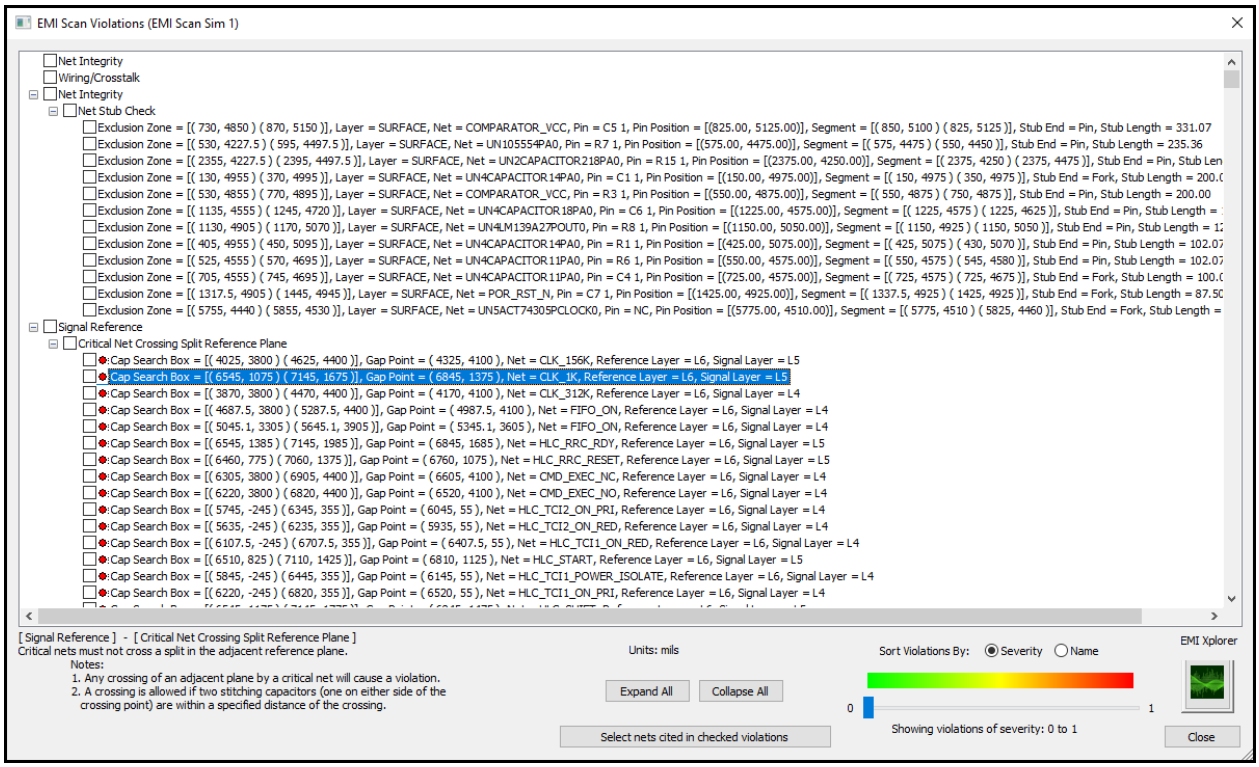
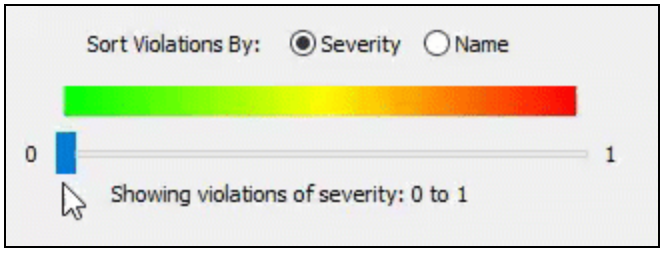


Violations are listed in a tree, by type.

Use the **+** and **-** buttons to expand and collapse items in the tree, or click **Expand All** and **Collapse All**.

Use the controls at the lower-right to sort the violations by **Severity** or by **Name**, or to limit the range of violations displayed.



3. Click a violation to view its location in the Modeling workspace. A red arrow, line, or box indicates the violation.

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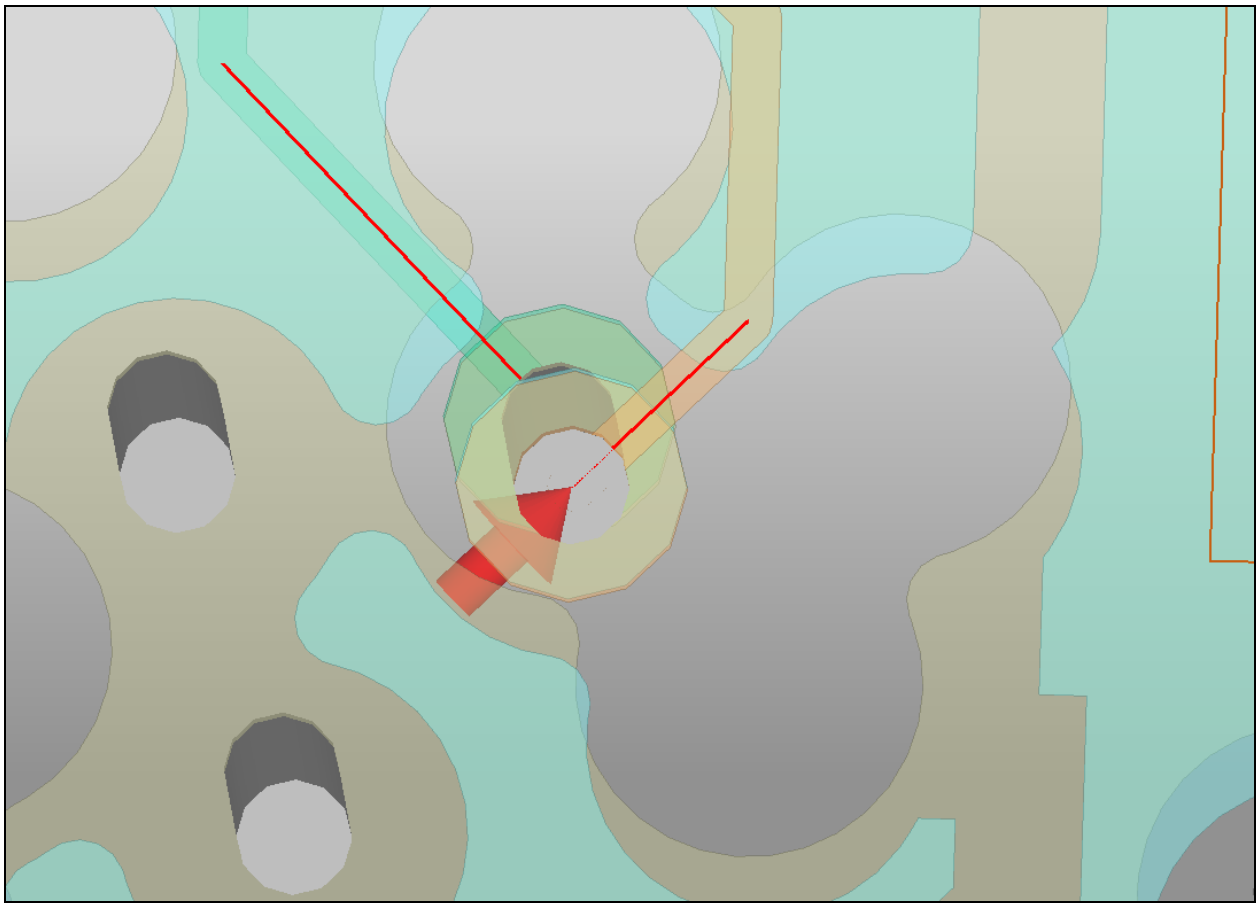

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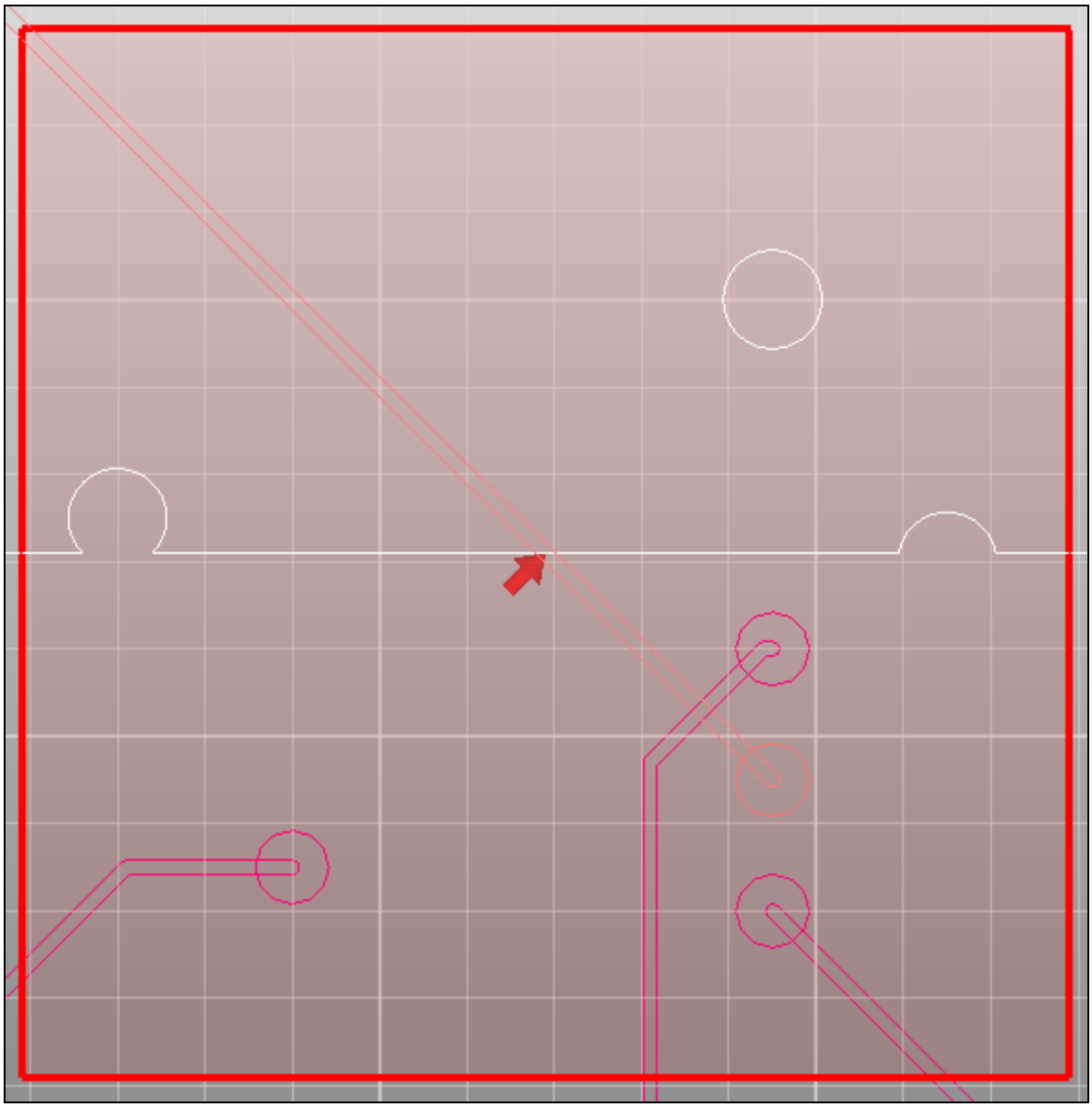

Clicking a violation also populates the **EMI Scan Violations** window with a description of the violation:

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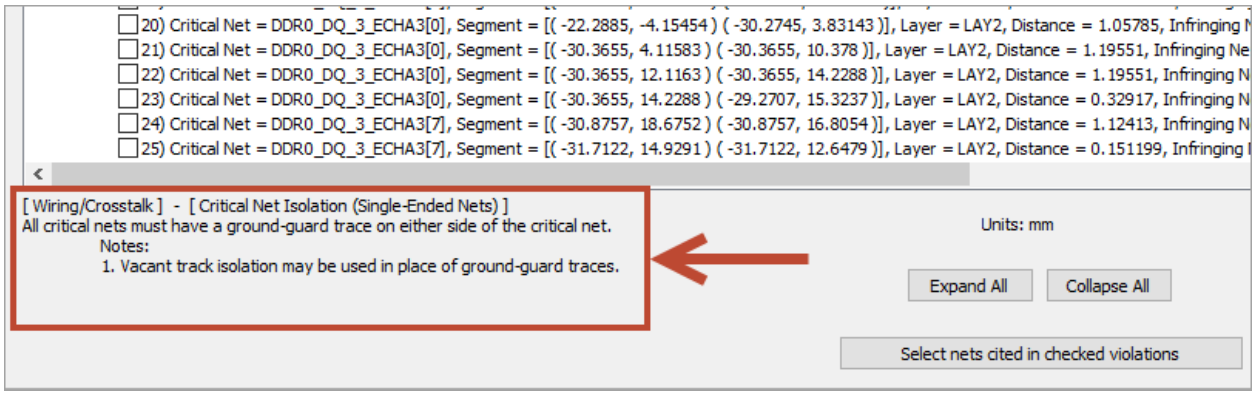


Use the check boxes in the tree to select multiple violations. Click **Select nets cited in checked violations** to select these nets in the Modeling workspace.

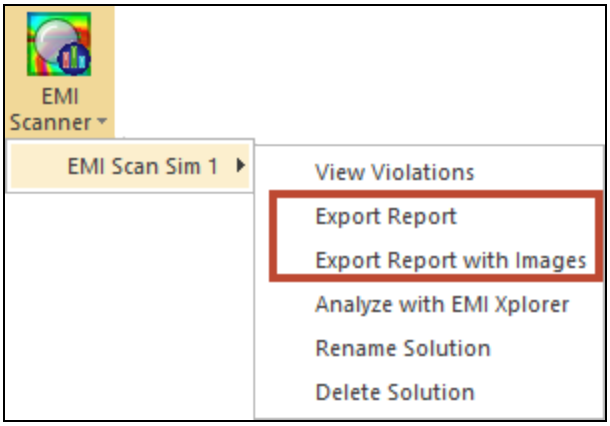
Select a violation and click the EMI Xplorer icon to open EMI Xplorer.

Exporting EMI Scanner Results

EMI Scanner can export an HTML report with or without images.

To export EMI Scanner results, click one of the following:

- **Results** > **EMI Scanner** > **[Simulation Name]** > **Export Report**.
- **Results** > **EMI Scanner** > **[Simulation Name]** > **Export Report with Images**.



An HTML report opens in your default Internet browser.

HTML Report without Images

The HTML report without images displays a list of rules that were analyzed:

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ANSYS EMI Scanner RULES

ANSYS EMI Scanner RULE RESULTS

SIGNAL REFERENCE

Critical Net Crossing Split Reference Plane - Violations: 0	ON
Critical Net Changing Reference Plane - Violations: A - 6, B - 0, C - 0	ON
Critical Net Near Edge of Reference Plane - Violations: 0	ON

WIRING/CROSSTALK

Critical Net Near I/O Net - Violations: 0	ON
Length of Exposed Critical Traces - Violations: 10	ON
Critical Net Isolation (Single-Ended Nets) - Violations: 0	ON
Critical Net Isolation (Differential Nets) - Violations: 0	ON
Critical Differential Net Length Matching and Spacing - Violations: 0	ON
Wide Power/Ground Traces - Violations: 434	ON

DECOUPLING

Decoupling Capacitor Density - Violations: 0	ON
Decoupling Capacitor Distance from IC Power Pin - Violations: 101	ON
IC Power/Ground-Reference Pin Distance to Via - Violations: 178	ON
Decoupling Capacitor Distance to Via - Violations: 146	ON
Power/Ground-Reference Trace Decoupling - Violations: 0	ON
Power Via Density - Violations: 1	ON

PLACEMENT

I/O Filter Distance to I/O Connector - Violations: 0	ON
Distance from Oscillator to Clock Driver - Violations: 0	ON

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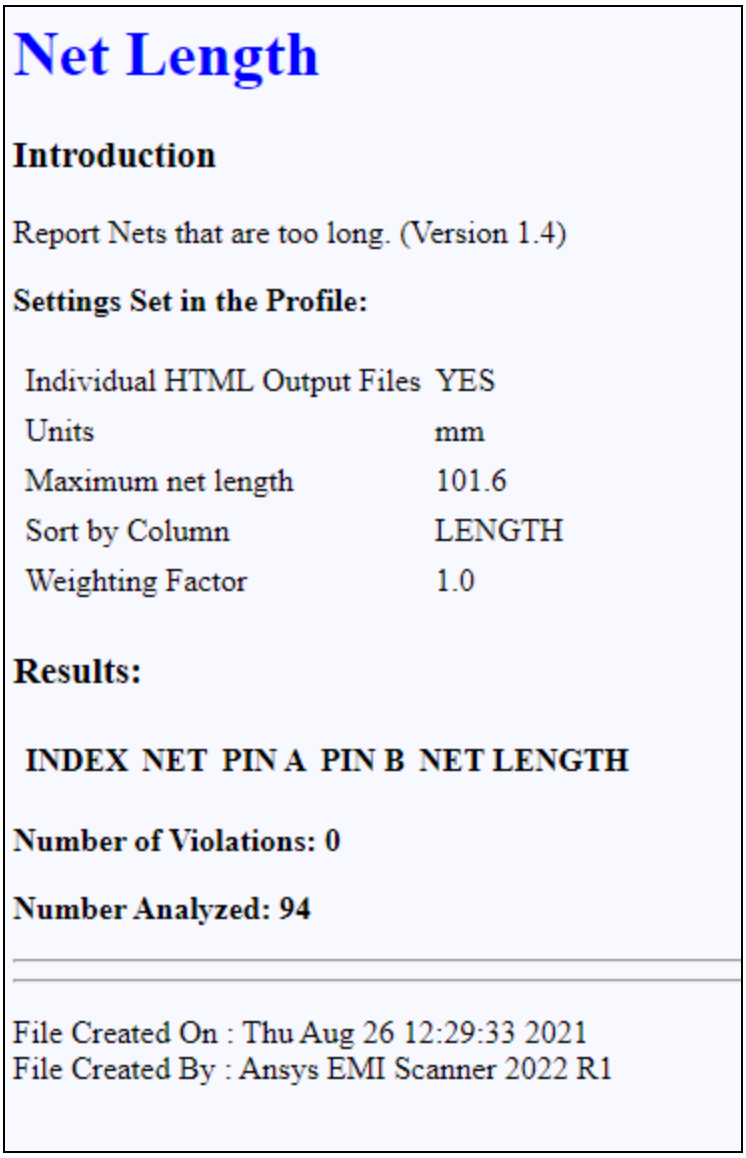
Clicking any rule takes you to another HTML file with a detailed report for that rule:



Net Length

Introduction

Report Nets that are too long. (Version 1.4)

Settings Set in the Profile:

Individual HTML Output Files	YES
Units	mm
Maximum net length	101.6
Sort by Column	LENGTH
Weighting Factor	1.0

Results:

INDEX NET PIN A PIN B NET LENGTH

Number of Violations: 0

Number Analyzed: 94

File Created On : Thu Aug 26 12:29:33 2021
File Created By : Ansys EMI Scanner 2022 R1

HTML Report with Images

The HTML report with images lists violations by rule. Click the **Navigate** arrow adjacent to a rule to view more information, including images of the violations.

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EMI Scan Simulation Report

Generated By: SIwave 2022 R1
Creation Date: Thu Aug 26 12:48:10 2021

Design File: analysis2.siw
Simulation Name: EMI Scan Sim 1

EMI Violations Summary

Rule Type	Rule Name	Number of Violations	Navigate
Net Integrity	Net Length	0	
Net Integrity	Net Coupling	0	
Wiring/Crosstalk	Length of Exposed Critical Traces	0	
Net Integrity	Net Stub Check	0	
Signal Reference	Critical Net Crossing Split Reference Plane	14	
Signal Reference	Critical Net Near Edge of Reference Plane	0	
Net Integrity	Above/Below Reference Plane check for specified Nets	0	
Net Integrity	Critical Differential Net Running Skew	0	
Via Integrity	Unconnected Via Pads	148	
Via Integrity	Via Clearance Overlap	0	
Via Integrity	Via to Net Coupling	19	
Via Integrity	Via Stub Check	0	
Wiring/Crosstalk	Wide Power/Ground Traces	0	
Decoupling	Decoupling Capacitor Density	0	
Decoupling	Decoupling Capacitor Distance from IC Power Pin	0	
Decoupling	IC Power/Ground-Reference Pin Distance to Via	0	
Decoupling	Decoupling Capacitor Distance to Via	0	
Decoupling	Power/Ground-Reference Trace Decoupling	0	
Decoupling	Power Via Density	1	

Note:

You can change whether EMI Scanner produces one large, combined HTML report or several individual HTML files in the EMI Scanner General Settings.

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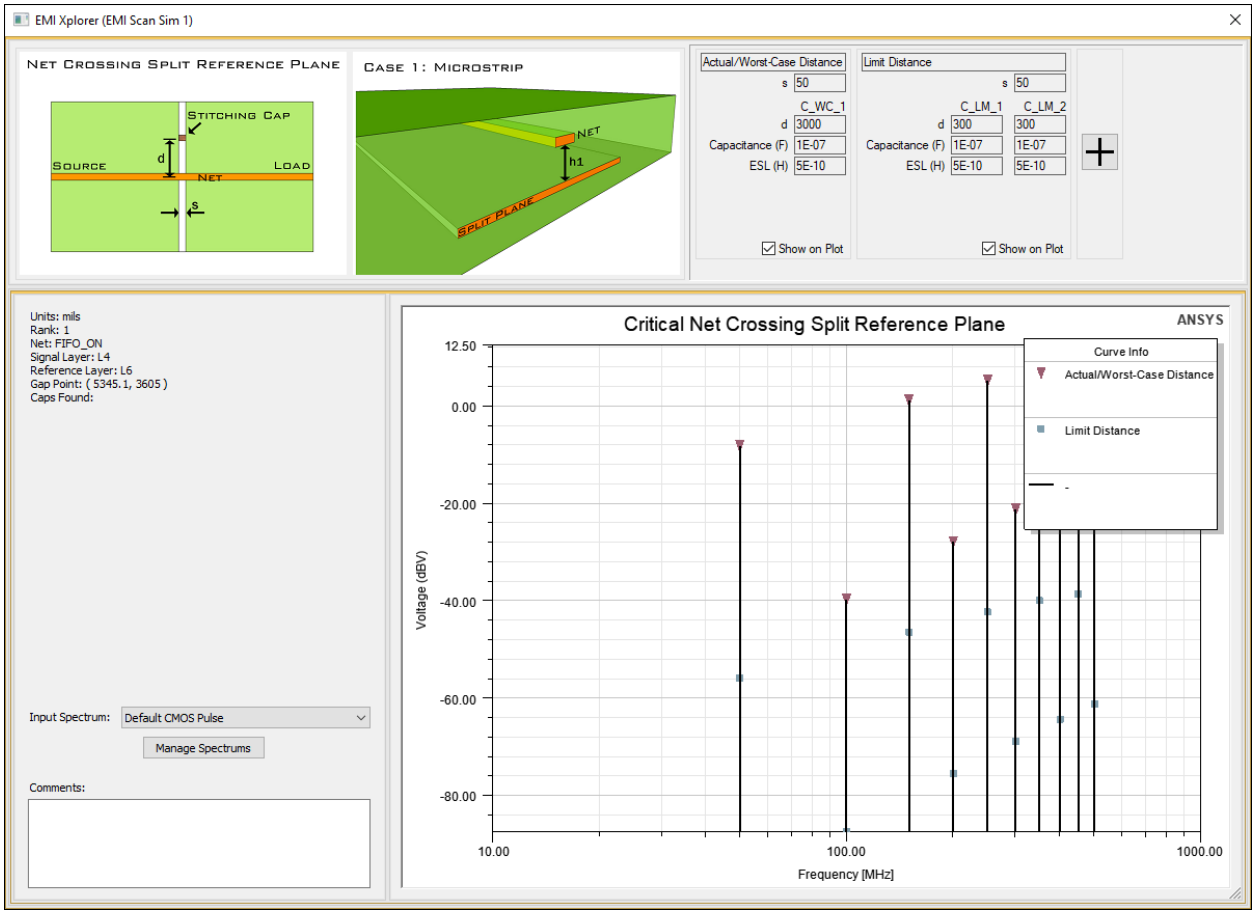
Analyzing EMI Scanner Results Using EMI Xplorer

EMI Xplorer receives violations from the EMI Scanner and, based on signal characteristics, makes predictions on the seriousness of the violations. This offers meaningful comparison between rule limits and violations, and allows you to make "what if" comparisons and determine impacts.

To analyze EMI Scanner results:

1. Run an EMI scan.
2. Click **Results > View Violations**.
3. Select a violation and click the EMI Xplorer icon.

   The **EMI Xplorer** appears.



The window contains four panes:

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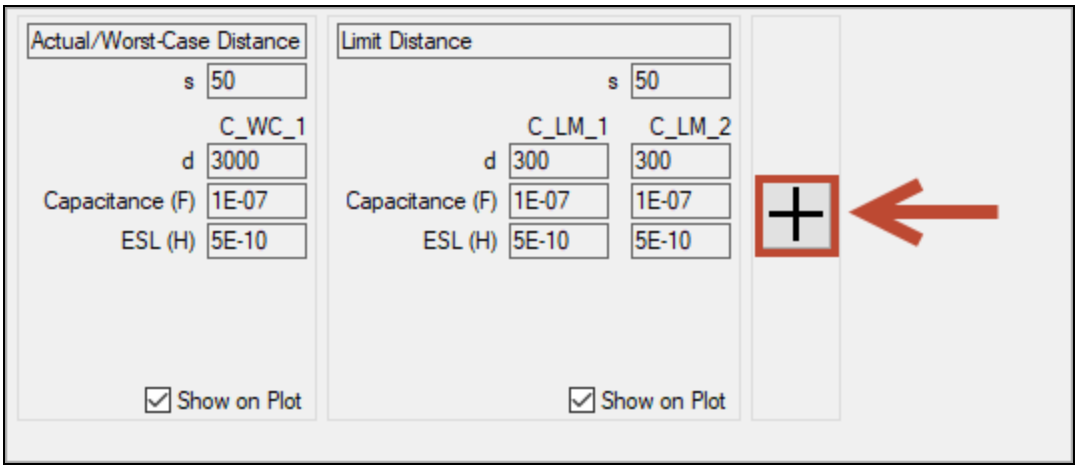
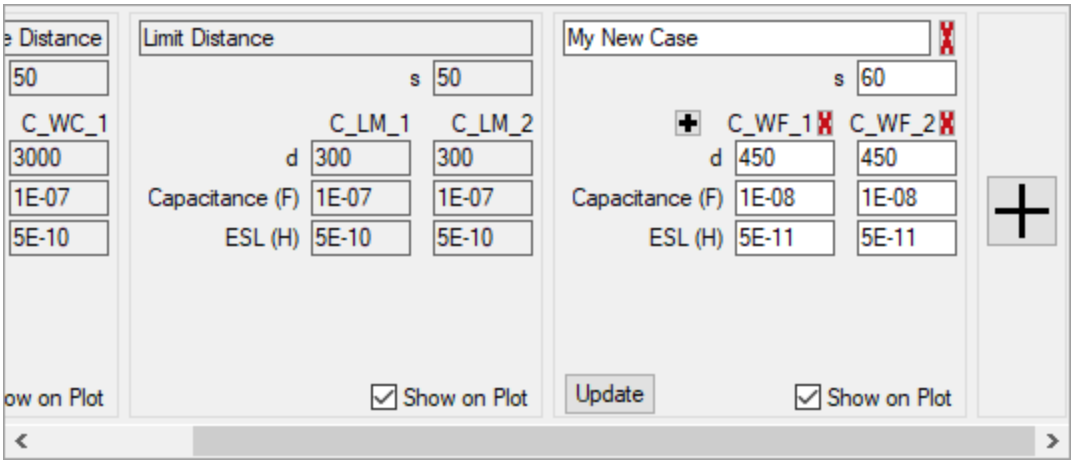
- **Top-Left Pane** – illustrates the violation type.
- **Top-Right Pane** – contains the comparison cases (e.g., worst case) that are displayed on the plot. Comparison cases allow you to see how changes in signal characteristics would affect the violations. Use the **Show on Plot** check boxes to determine which cases are displayed. You can add a case by clicking the plus sign (+) and entering the information for the case.





Some notes about comparison cases:

- **Actual Distance** – displays the results calculated for the design tested.
- **Limit Distance** – displays what the values would be if the distance were set to the threshold value configured for the rule.
- **Worst-Case Distance** – displays what the results would be for a distance that is ten times the limit distance. This is an arbitrarily large number.

Each case contains one or more columns for individual capacitors.

To delete a comparison case, click the red X adjacent to the case name.

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To add or remove a capacitor, click the plus sign (+) or red X next to the capacitor.

- **Bottom-Left Pane** – lists information about the violation's location, and allows you to add comments or configure spectra. You can select any existing **Input Spectrum**, or add a new spectrum by clicking **Manage Spectrums**.
- **Bottom-Right Pane** – displays a plot of the cases. You can change how the plot displays and perform additional plotting actions.

4. Analyze the data as appropriate, then close **EMI Xplorer**.

   You are returned to the violations viewer, and can select a new violation for analysis.

Spectra Configuration

To configure the Spectra library:

1. Run an EMI scan.
2. Click **Results** > **View Violations**.
3. Select a violation and click the EMI Xplorer icon.

   The **EMI Xplorer** appears.

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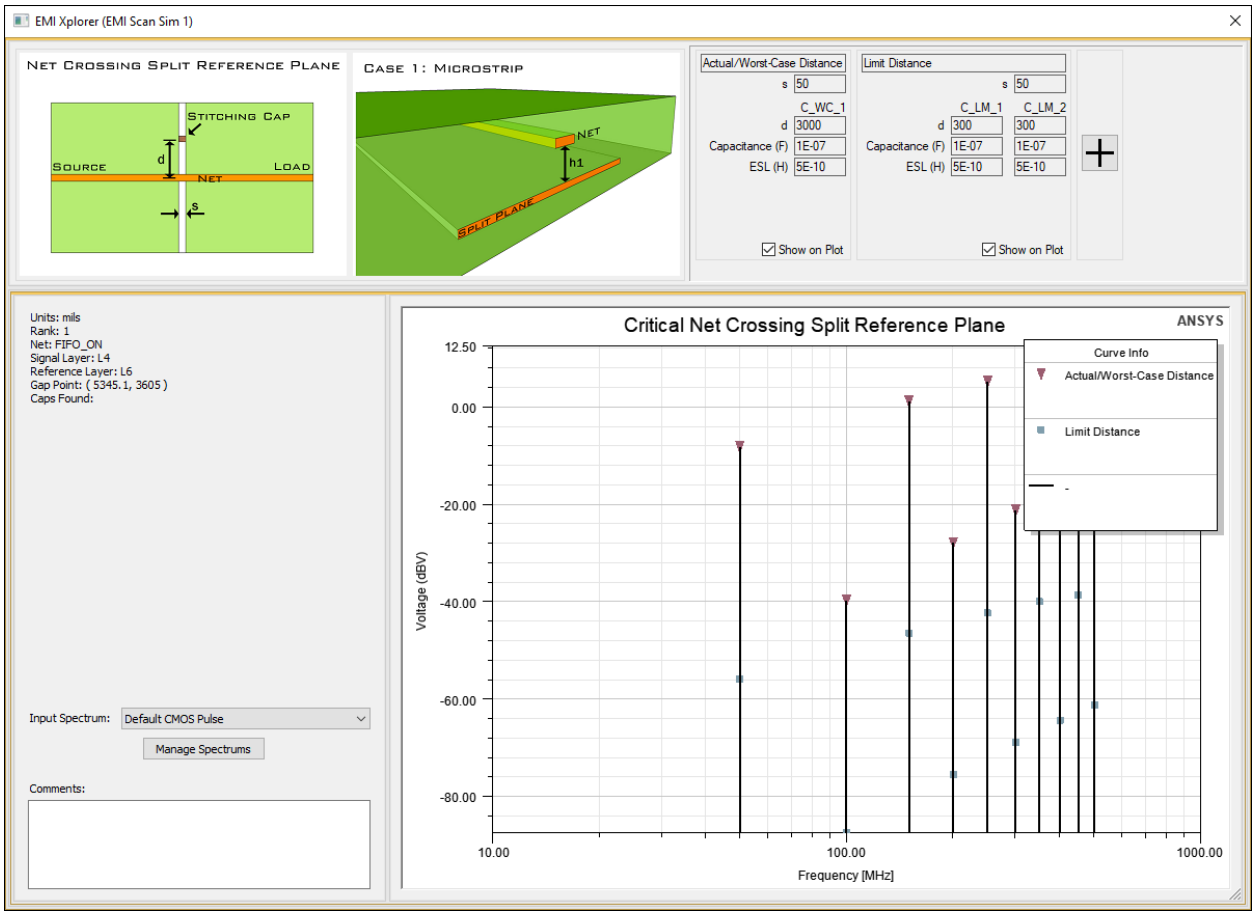
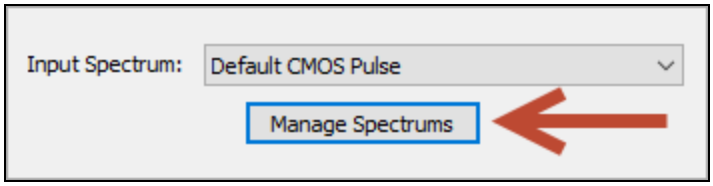


4. From the bottom-left pane, click **Manage Spectrums**.



The **Manage Spectrums** window appears.

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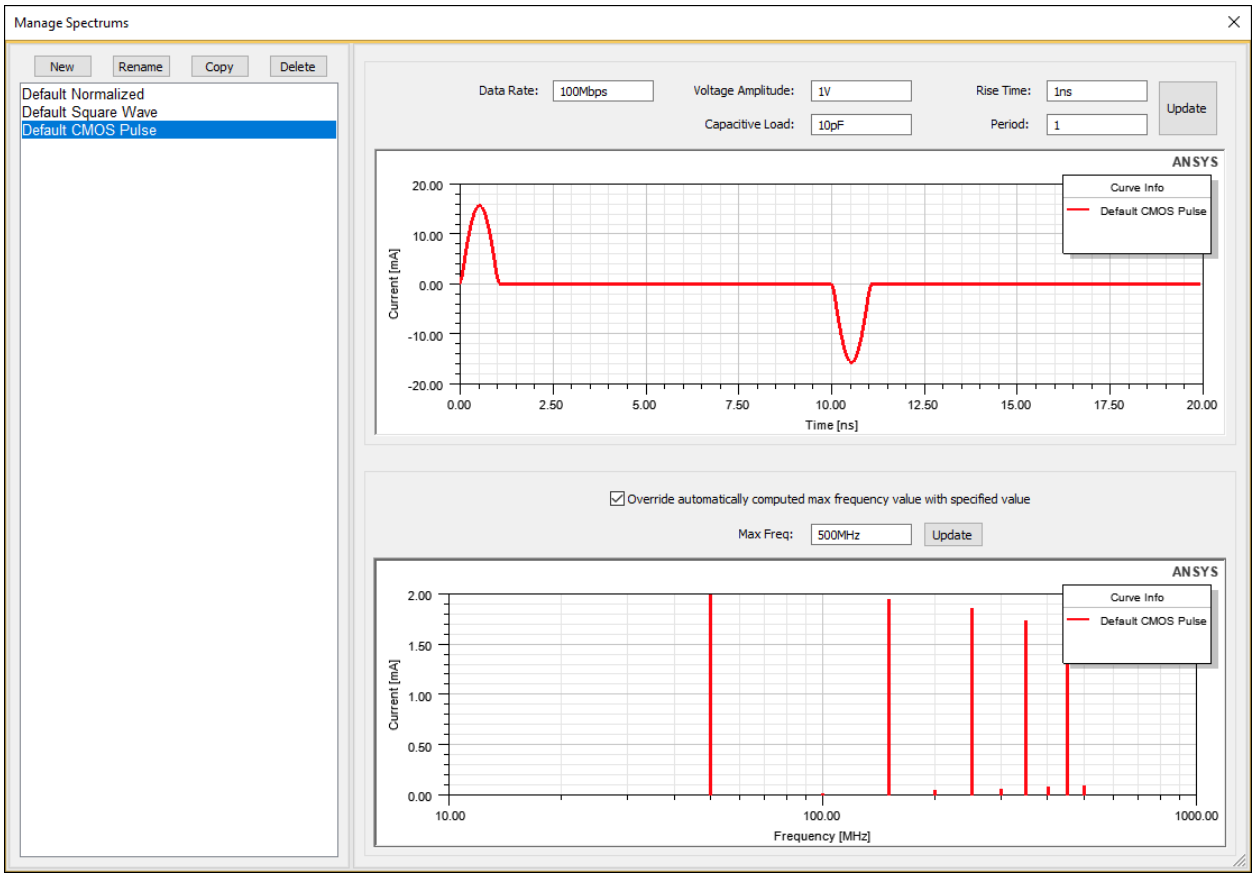

5. To change a spectrum's settings, select the spectrum from the left pane and change its settings in the right pane. Then click **Update**.

   The plots update to reflect the new settings.

> **Note:**
>
> Configurable settings vary based on the type of spectrum.

From the Spectra Configuration window, you can also perform the following actions:

- **New** – create a new spectrum.
- **Rename** – change a spectrum name.
- **Delete** – remove a spectrum.
- **Copy** – create a copy of an existing spectrum with a new name.

Creating a New Spectrum

To create a new spectrum from the **Manage Spectrums** window:

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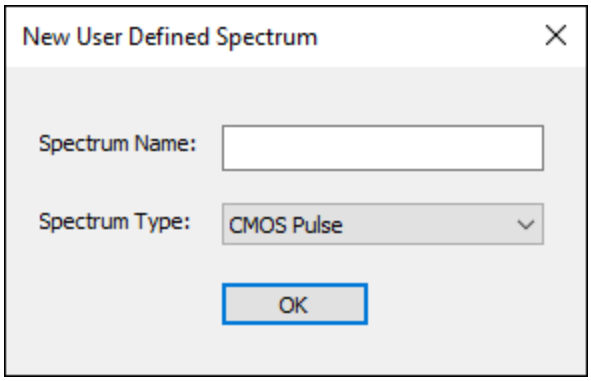
1. Click **New**.

   The **New User Defined Spectrum** window appears.



2. Enter a **Spectrum Name** and use the **Spectrum Type** drop-down menu to select **Normalized Current**, **Square Wave**, or **CMOS Pulse**.

   The new spectrum appears in the left pane, and its settings and plots appear to the right.
3. Edit the settings and click **Update** to refresh the plots.

   Note:

   Configurable settings vary based on the type of spectrum you selected previously.
4. Close the **Manage Spectrums** window.

   You can now select the new spectrum from EMI Xplorer.

Network Data Explorer

The Network Data Explorer provides visualization, analysis, and manipulation tools for network data.

To access Network Data Explorer:

1. Click **Tools**.
2. From the **S-Parameter Tools** area, click **Network Data Explorer**.

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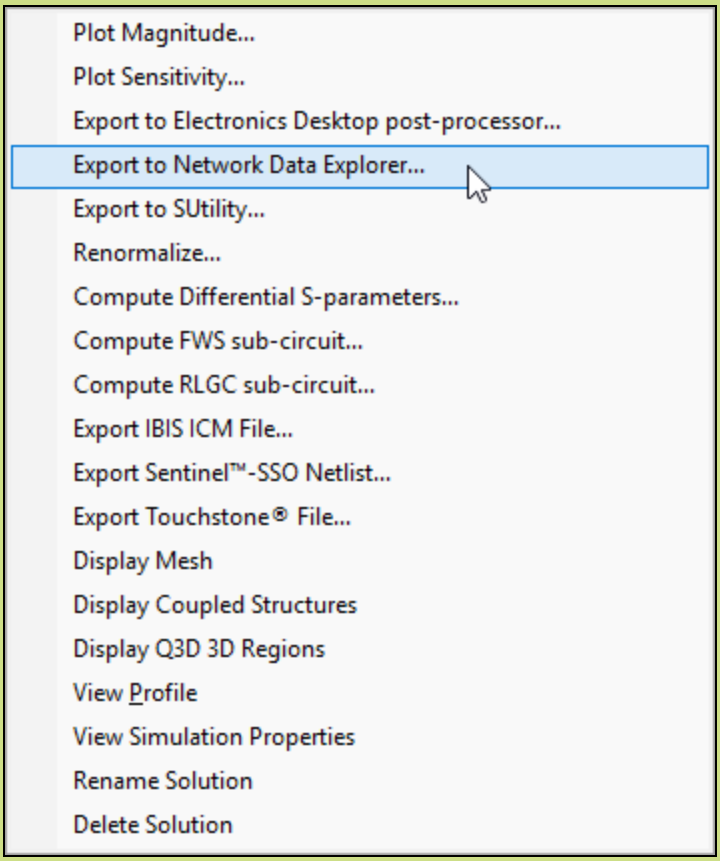
Note:

If you have already performed an SYZ sweep, you can also access the Network Data Explorer from the **Results** window.

To do so, right-click the SYZ results and select **Export to Network Data Explorer**.



The **Network Data Explorer** window appears.

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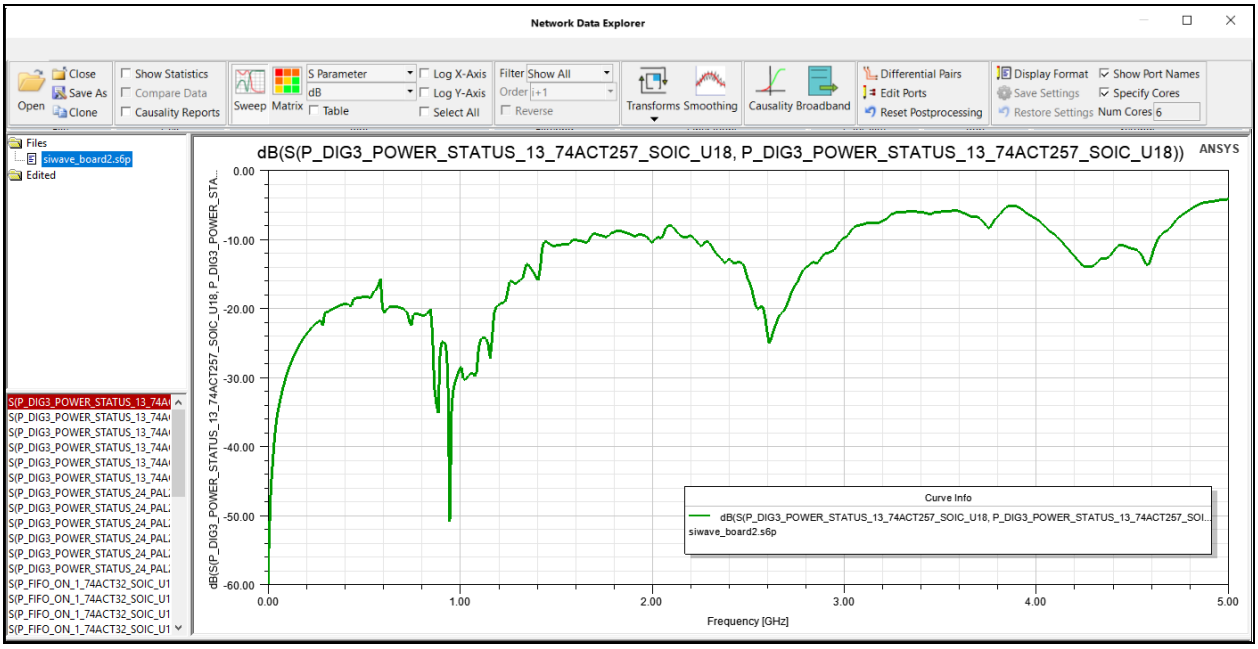

Network Data Explorer topics include:

- Network Data Explorer Overview
- Loading Data into Network Data Explorer
- Exporting Data from Network Data Explorer
- Edit Menu Commands
- Data Display Pane Shortcut Menus
- Exploring Network Data and Modifying the Display

Network Data Explorer Overview

The Network Data Explorer window is divided into the following panes:

1. **Network Data Explorer Ribbon** – allows you to perform Network Data Explorer's functions.
2. **Data Selection Pane** – allows you to select a network data file.
3. **Cell and Frequency Selection Pane** – allows you to narrow your selection.
4. **Data View Pane** – displays data in table or plot format.

The panes are shown in the following figure. Additional information about each pane follows.

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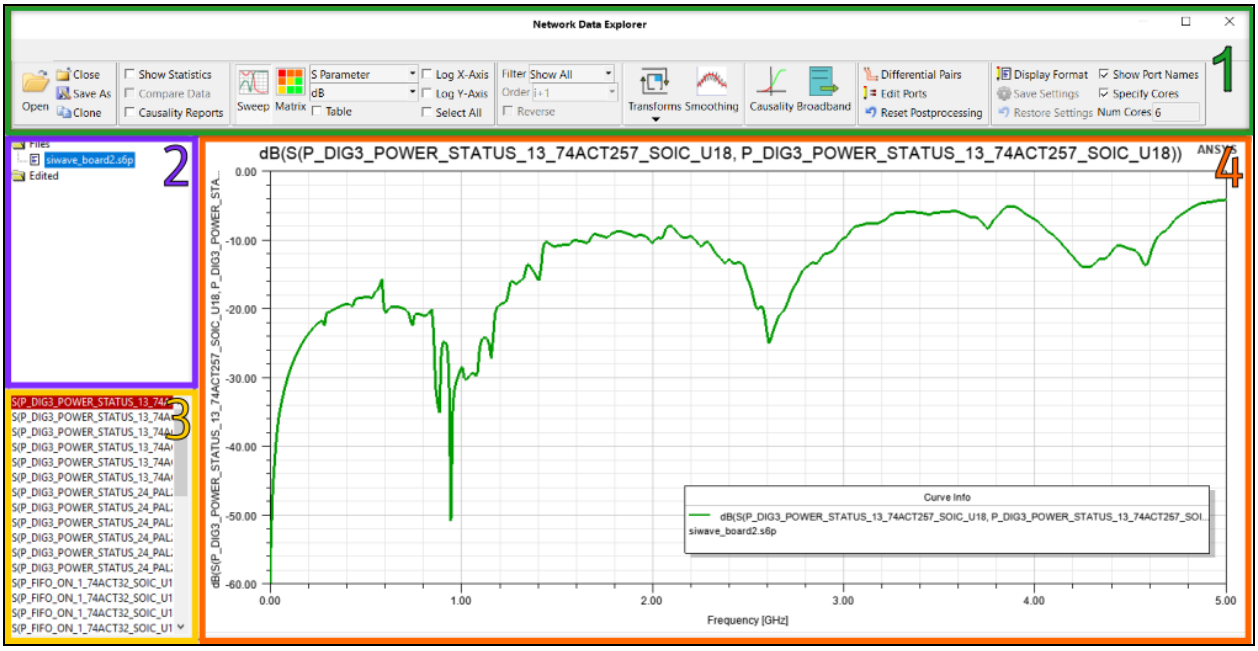

Network Data Explorer Ribbon

From the ribbon, you can control:

- **Plotting** – determine how the data is displayed. Click the **Sweep** or **Matrix** icon to select a plot type.
- **Quantity** – select the type of quantity to display (parameter values, matrix statistics, or causality plots).
- **Parameter Type** – choose parameters for display (S, Y, or Z parameters, Port Impedance, or Gamma).
- **Format** – decide the display function to apply to the data (e.g., magnitude, phase, dB, real, or imaginary).
- **Export** – export either SYZ data (*.s1p, *.ts, *.nmf, *.tab, *.m, *.cit) or Broadband data (*.sp).
- **Causality Checking** – check causality.
- **Cores** – enable or disable multithreading.
- **Post-Processing** – choose between terminal data and differential pairs, if your design includes differential pairs.

See: Network Data Explorer Ribbon.

Data Selection Pane

This pane allows you to view and compare various data sets. Original data sets appear under **Files**. Click one of these to see the dataset as it was when it was opened. Altered data sets (data

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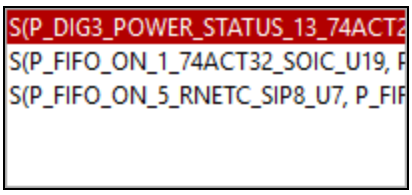
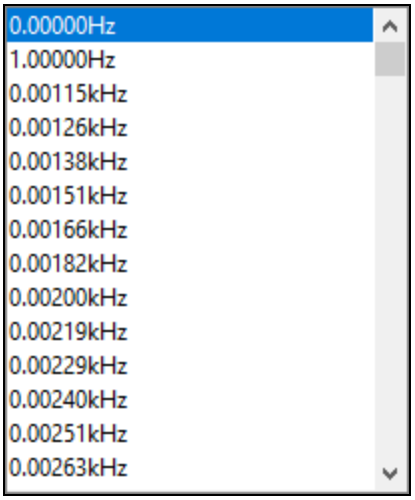
sets that have been smoothed, transformed, or changed in some way) are listed under **Edited**.

Cell and Frequency Selection Pane

This pane allows you to choose to choose which cells or frequencies to display.





To select all frequencies or cell entries, use the **Select All** check box on the ribbon.

This pane can also list available variations. Selecting a variation activates it and affects table, plot, and statistics displays. When displayed by frequency, the entire matrix is presented in the Data View pane for each selected frequency. When displayed by matrix cell, the data for the individually chosen cells is shown across all frequencies. Use the **Select All** check box to select all variations.

> **Warning:**
>
> Given the volume of data in many network data sets, choosing **Select All** may take a considerable time to generate, especially in Plot view.

Data View Pane

The Data View Pane displays either table or plot data, depending on your selections.

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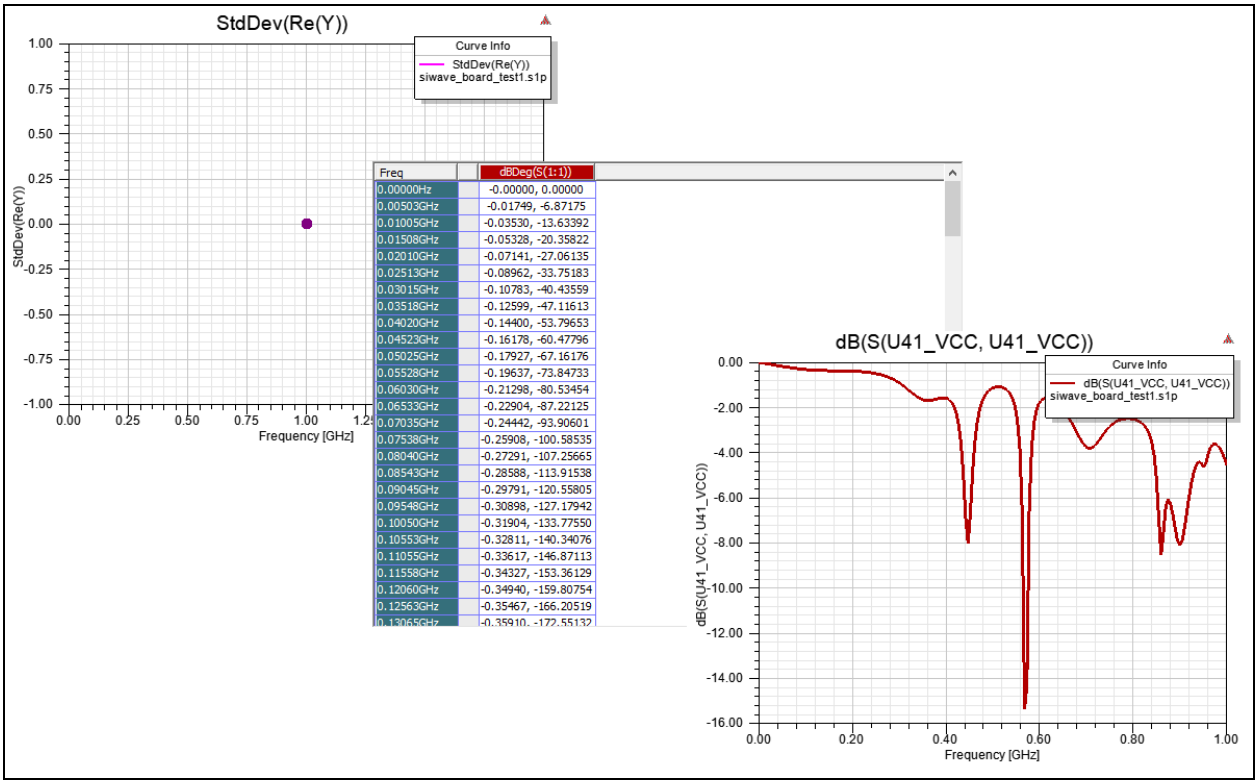

Loading Data into Network Data Explorer

If you have run an SYZ sweep and launched Network Data Explorer from the Results window, solution data is automatically loaded and ready for viewing.

Otherwise, you must load a data file into Network Data Explorer.

You can import the following file types:

- Touchstone Format (*.s*p)
- Touchstone 2 Format (*.ts, *.sp)
- Citifile (*.cit)
- Neutral Format (*.nmf)
- State Space File (*.sss)

> **Note:**
>
> When a State Space File (*.sss) is loaded, Network Data Explorer regenerates s-parameter data based on the file.
>
> You can compare the regenerated s-parameters to the original data.

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To import a file into Network Data Explorer:

1. From the ribbon, click **Open**. An **Open** window appears.
2. Navigate to and select a file.
3. Click **Open**. The file appears in the Data Selection Pane, under **Files**.

The file browser allows you to open multiple files at a time. However, the displayed data always corresponds to the data set indicated in the Network Data Selection pane. Click the file you want in that pane to switch between data sets. Use the **Shift** and **Ctrl** keys to select and display data sets from multiple files simultaneously.

Exporting Data from Network Data Explorer

Network Data Explorer allows you to export data to a variety of different file formats.

In this section, you will learn about:

Exporting SYZ Data

Exporting a Macro Model

Exporting SYZ Data

To export SYZ data from within Network Data Explorer, click **Save As** on the ribbon. The **Save File As** window appears.

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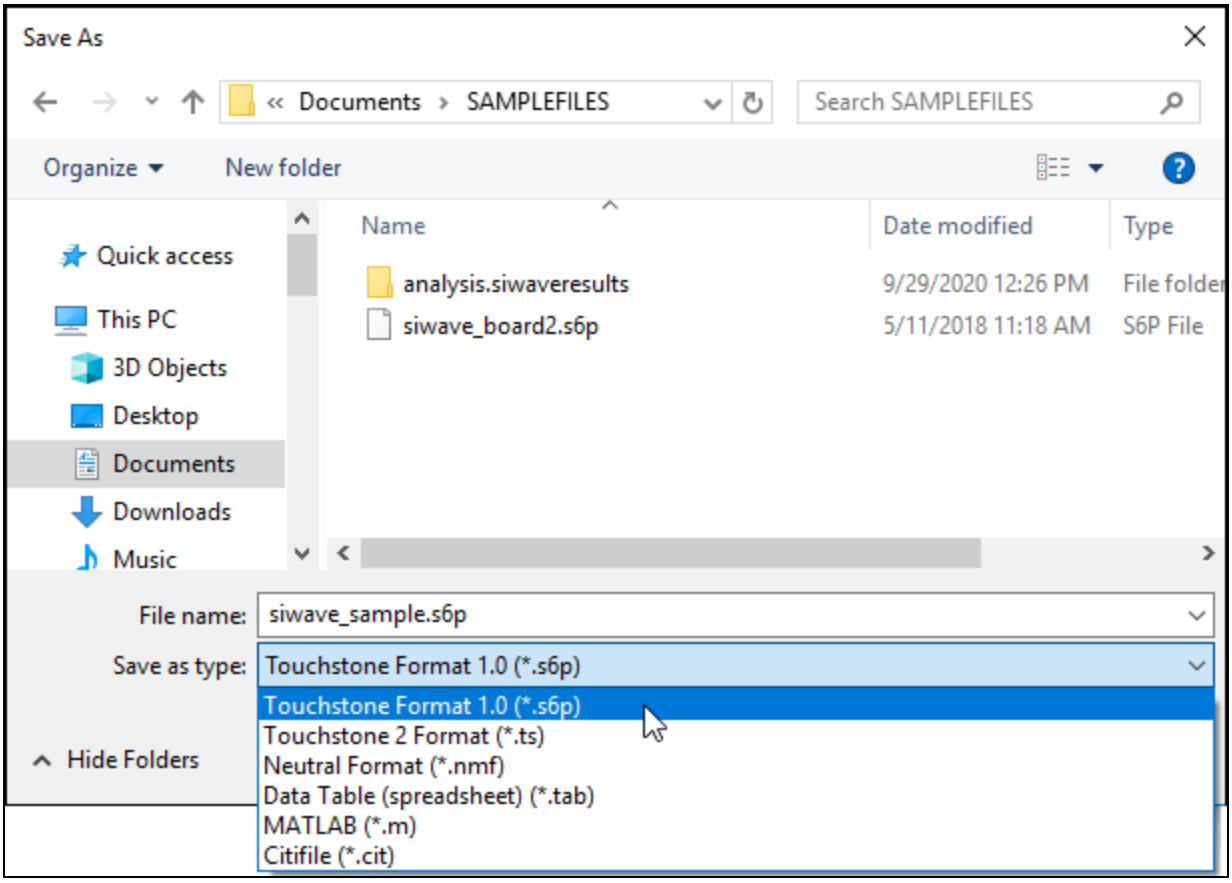

You can export data in any of six file types:

- Touchstone Format 1.0 (*.s*p)
- Touchstone 2 Format (*.ts)
- Neutral Format (*.nmf)
- Data Table Spreadsheet (*.tab)
- MATLAB (*.m)
- Citifile (*.cit)

Select a file type and name for export. A **Specify Export Options** window appears.

Depending on the type of export file, different options appear. However, all file types allow you to:

- Select from **S Matrix**, **Y Matrix**, and **Z Matrix** data.
- Select the **Display Format**.

Exporting Macro Model

Network Data Explorer lets you export macro model data.

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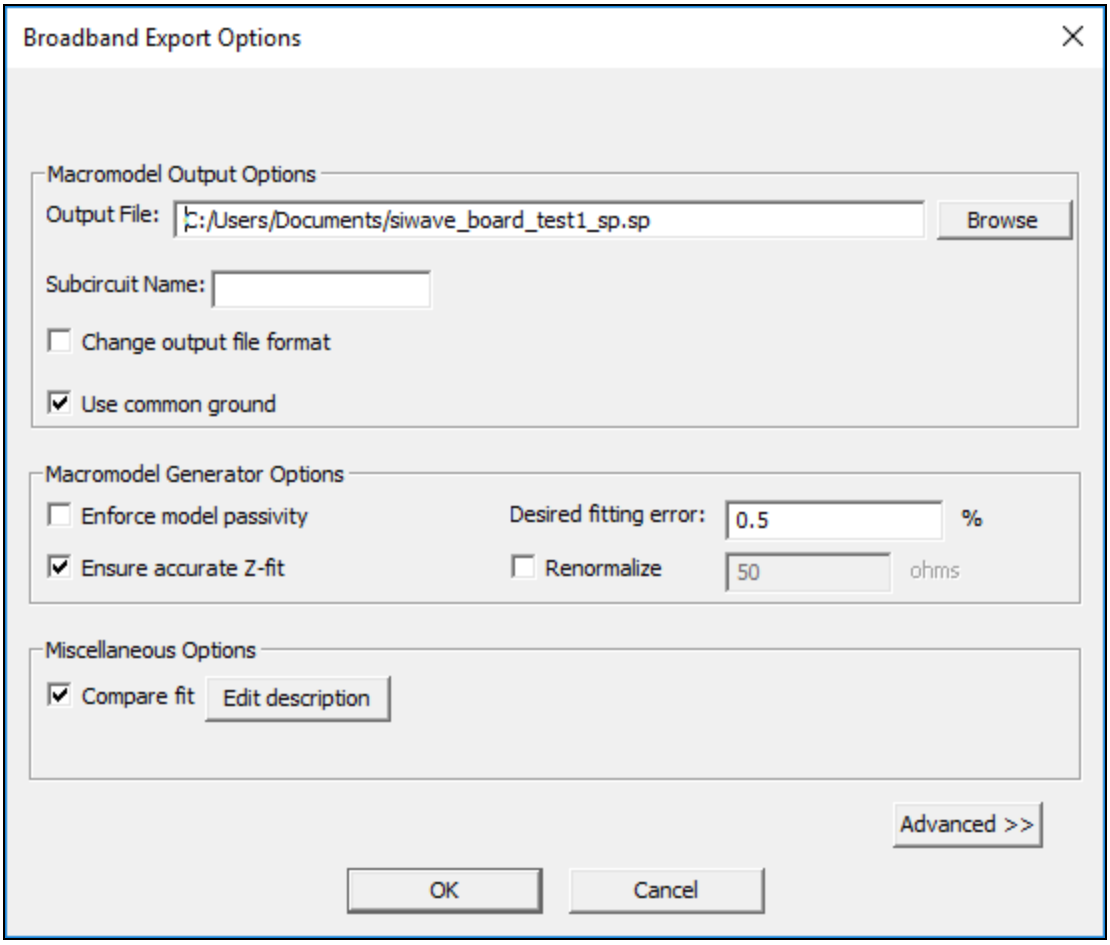
From the Network Data Explorer ribbon, click **Broadband**.

The **Broadband Export Options** window appears.



Click **Advanced >>** to view all options.

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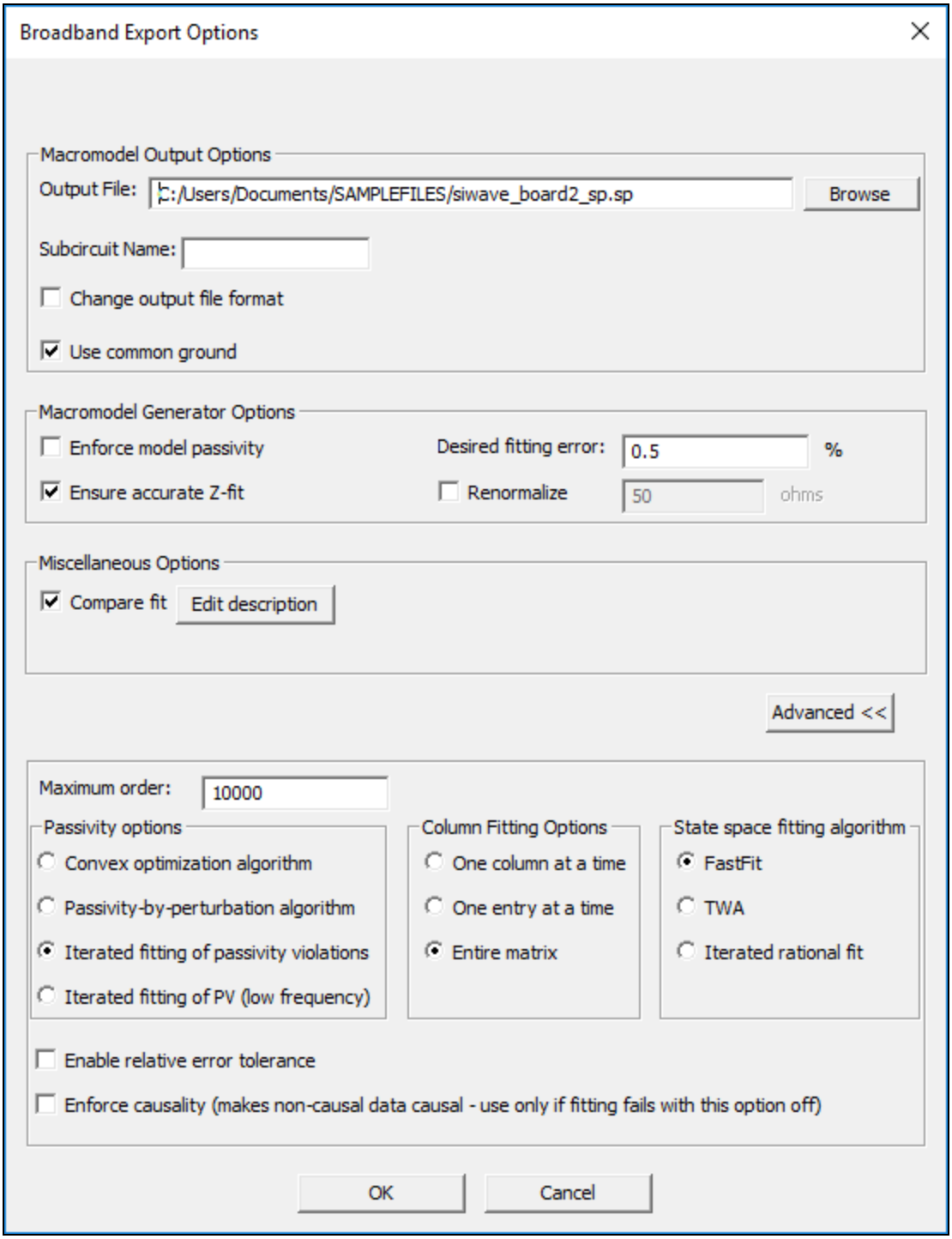

Macromodel Output Options include:

- **Output File** – allows you to choose the name and location of the file.
- **Subcircuit Name** – use this field to name the subcircuit.

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- **Change Output File Format** – check this box to open a submenu allowing you to select a new output format.
- **Use Common Ground** – check this box to use common ground. When this option is on, ports are referenced to ideal ground (node 0). When this option is off, extra ports are generated to provide the reference levels. Common grounding is best when the pins are physically near to each other and ideal ground is suitable. For distant connections and circuits with non-ideal reference levels such as differential pairs, common grounding is not used.

Macromodel Generator Options include:

- **Enforce Model Passivity** – check this box to enforce passivity.
- **Ensure Accurate Z-fit** – check this box when state-space fitting of Y-parameters or Z-parameters does not produce an accurate fit.
- **appropriate Fitting Error** – allows you to select the value at which rational fitting fails (if the fitting error exceeds this value).
- **Renormalize** – check this box to renormalize using the specified impedance item. 50 ohms is the default setting, but you can type a different value.

Note:

- R and L values may be sensitive to S-parameter values. This presents an issue if the actual impedance value is much greater than or much less than the reference impedance of the S-parameters.
- Since resistances of power cables are typically in the milliohms range at DC, using a reference impedance of 50 ohms is 5000 times higher. This causes any fitting errors in the state space model to be multiplied by 5000 when the R and L values are computed.
- For high-power applications, a reference impedance of 1 ohm is generally a better choice than 50 ohms.

Miscellaneous Options include:

- **Compare Fit** – when this box is checked, the original and derived solution will be available for comparison. You can click **Edit Description** to open the **Derived Solution Description**

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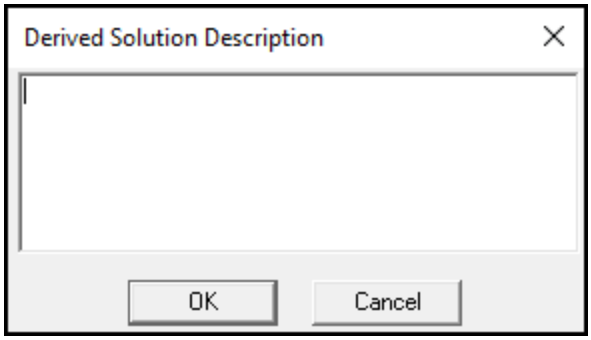
window and add a text description to better identify the export.



Advanced Options include:

- **Maximum Order** – allows you to specify the number of poles. See Note below.
- **Passivity Options** – If you enabled **Enforce Model Passivity**, this area allows you to select the passivity enforcement method.
  - Convex optimization algorithm – guarantees a passive state-space realization, but is very slow and memory-intensive.
  - Passivity-by-perturbation algorithm – designed for systems with a large number of ports.
  - Iterated fitting of passivity violations (IFPV) (default) – less accurate than other algorithms but quickly estimates a fit with low memory usage.
  - Iterated fitting of PV (low frequency) – similar to IFPV while improving the fit to "Z" at DC and low frequencies.
- **Column Fitting Options** – this area allows you to choose how poles are matched to columns:
  - **One Column at a Time** – the set of poles will be shared across all entries of a single column.
  - **One Entry at a Time** – each entry will be fitted using a separate set of poles.
  - **Entire Matrix** – the set of poles will be shared across all entries of the matrix being fitted.

    Note:

    Typically, using the same set for all entries is adequate, and yields the most compact models. However, if all the entries of the matrix have completely unrelated transfer functions, it may be better to fit them using separate pole sets.

    The options **One column at a time** and **One entry at a time** do not work when either **Ensure accurate Z-fit** or FastFit is used.
- **State Space Fitting Algorithm** – allows you to select FastFit, TWA, Iterated rational fitting. See Note below.

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- **Enable Relative Error Tolerance** – allows you to enable relative error tolerance, which works best with TWA fitting.
- **Enforce Causality** – allows you to make non-causal data causal. Use this option only if fitting fails without it.

Note:

Broadband models are built from a rational-function approximation to the data. The fidelity of this approximation can be controlled by setting the Maximum order (number of poles).

Note:

By default, Network Data Explorer uses a proprietary fitting method, FastFit, for calculating the state-space matrices from the network data. The FastFit algorithm for state-space fitting is an alternative to the Tsuk-White algorithm (TWA) and Iterative Rational Fitting (IRF). FastFit is generally as accurate as TWA, but is significantly faster than both TWA and IRF. It also aims to fit the lower frequencies with higher fidelity. FastFit is the default method for state-space fitting.

The Tsuk-White Algorithm (TWA) is an alternative Ansys-proprietary method for fitting a state space model to extracted s-parameter data. It uses techniques based on Singular Value Decomposition (SVD) to quickly determine required number of poles for fitting a model.

The iterated rational fitting approach takes a matrix of S-parameter data and, for each matrix entry, tries a succession of different pole-zero approximations (increasing the number of poles used at each iteration) until it can find an acceptable fit to the data. For broad frequency sweeps and large numbers of excitations this process can be time consuming because of all the iterations and is not guaranteed to produce a good fit to the data. It is retained as a fall-back if the TWA fails.

Note that the **Enable Relative Error Tolerance** option works best with the TWA fitting algorithm, is not recommended for use with iterated rational fitting, and is disabled when either FastFit or **Ensure accurate Z-fit** is used.

Click **OK** to begin export.

Comparing Original S-Parameters with Exported S-Parameters

If **Compare Fit** was selected during export, the **Data Selection Pane** updates to list both the original and exported solution, and the **Compare** check box is checked.

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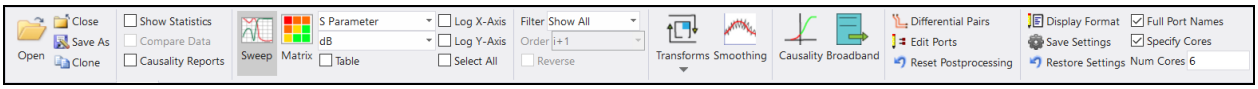
Network Data Explorer Ribbon Actions

The Network Data Explorer ribbon provides access to many of Network Data Explorer's functions.



In this section, you will learn about:

Setting Display Format

Displaying Full Port Names

Saving or Restoring Default Settings

Smoothing All Frequencies

Cell Filtering

Editing Port Properties

Defining Differential Pairs and Displaying Mixed Mode Parameters

Network Data Explorer – Setting Display Format

The **Display Format** window affords additional control over the display of values in Network Data Explorer.

To access this window from the ribbon, click **Display Format** ( ).

The **Display Format** window appears.

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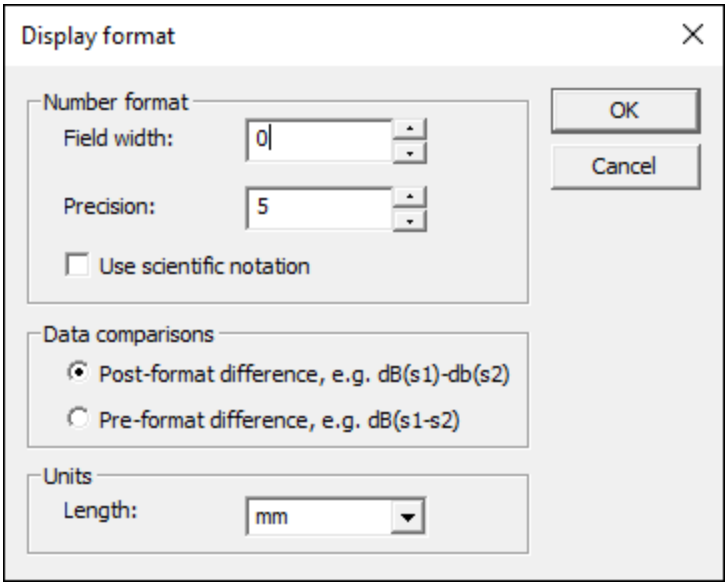

The **Number Format** options allow you to specify **Field Width** (the minimum number of characters used to display a number) and **Precision** (the number of decimals to display). You can also check the **Use scientific notation** check box, if appropriate.

The Data Comparisons options allow you to choose Post-format difference or Pre-format difference.

- **Post-format difference** – when comparing datasets, subtract values after applying the formatting function (dB, magnitude, etc.); the values displayed will be the difference between the magnitude, dB, and so on.
- **Pre-format difference** – when comparing datasets, subtract values before applying the formatting function (dB, magnitude, etc.); the values displayed will be the magnitude, dB, etc., of the complex difference.

The **Units** option allows you to specify the **Length** unit (the unit used to display and interpret length values). The default is mm.

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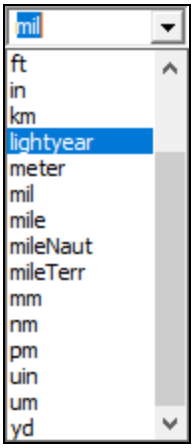
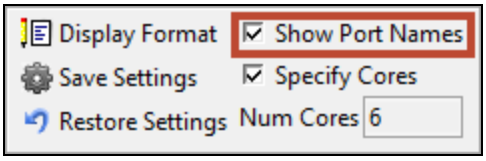


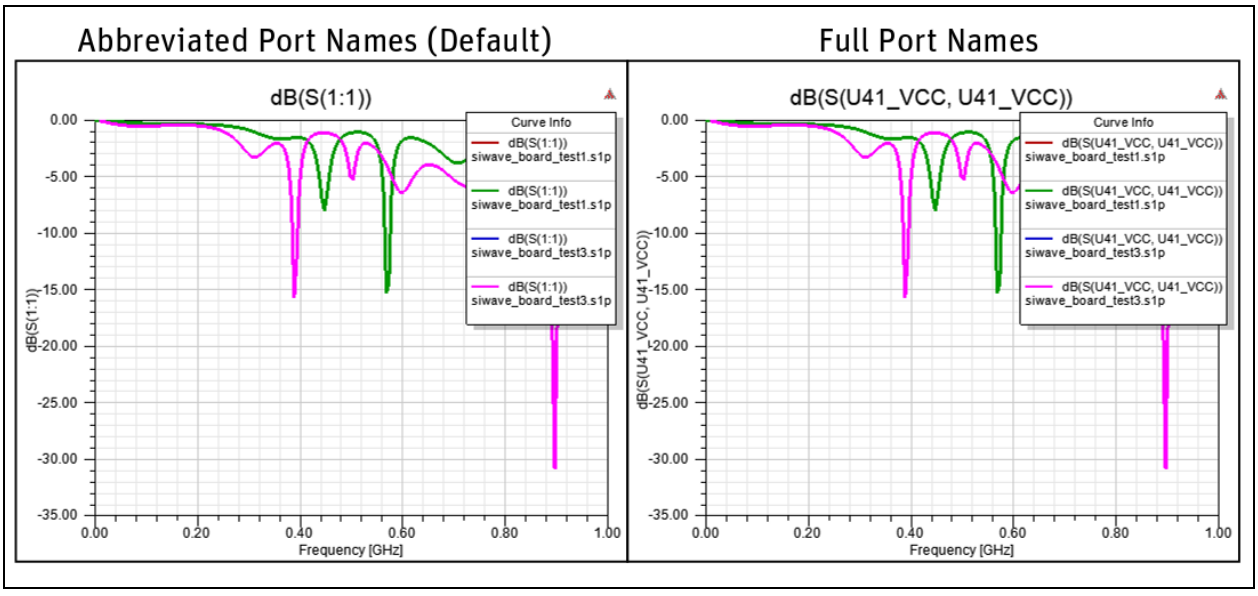
Network Data Explorer – Displaying Full Port Names

By default, port names in Network Data Explorer are displayed in an abbreviated form: P1, P2, etc. This applies to both the Data Selection pane and the Data View pane.

To change this so that full port names are displayed, select **Show Port Names** on the ribbon:



The following figure shows the difference in display for a plot.



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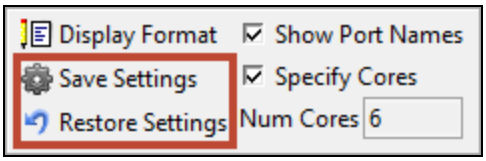
> **Note:**
>
> Tool-tips always display the full port name.

Network Data Explorer – Saving or Restoring Default Settings

To save field settings as the default, click **Save Settings**. The next time Network Data Explorer is opened, the chosen settings will be selected by default.

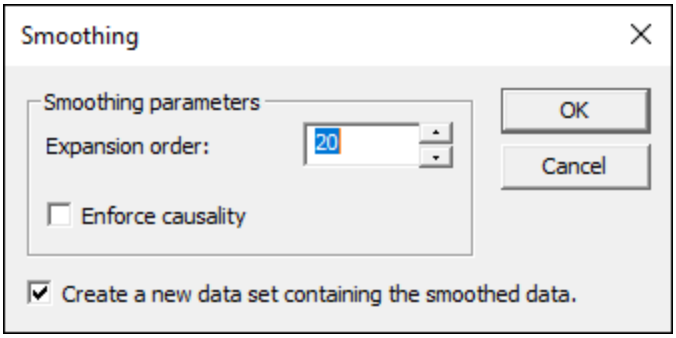
To restore the original defaults, click **Restore Settings**. The next time Network Data Explorer is opened, the original settings will be selected by default.



Network Data Explorer – Smoothing

To access data smoothing options from the ribbon, click **Smoothing**:

The **Smoothing** window appears.



2. The **Smoothing Parameters** area allows you to choose the **Expansion Order**. This can be any discrete value between 1 and 150.
3. If appropriate, check the **Enforce Causality** check box.

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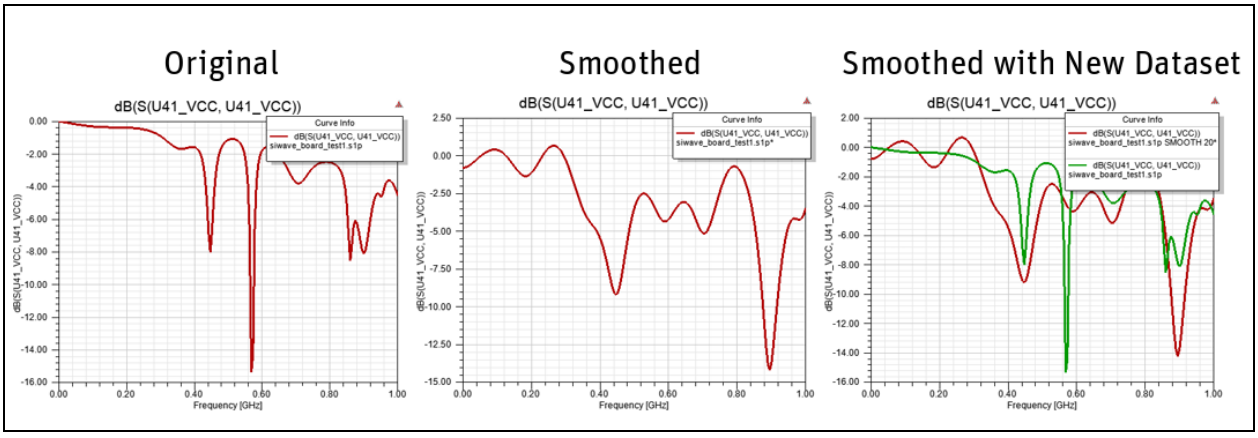
4. If appropriate, check the **Create a new dataset containing the smoothed data** check box. If selected, the smoothed data appears alongside the original data.
5. Click **OK**.

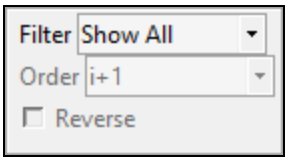
The Data View Pane updates. The following image shows a plotted result with **Create a new dataset containing the smoothed data** unchecked and checked.



Network Data Explorer – Cell Filtering

The cells available in the data selection pane may be restricted using cell filtering.

Cell filtering controls appear on the Network Data Explorer ribbon:



Cell filtering is modeless, and filters are immediately applied to the cell list. Filtering remains in effect when the window has been closed.

For an n-port model with a total of 2n pins in the standard arrangement, the choices are:

- **Show All** – displays all available cells. There are n-squared choices.
- **Return Loss** – shows S(i, i). There are n choices.
- **Insertion Loss** – shows S(i, i+1). There are n choices.
- **Lower Triangle** – shows S(i, j) for all j < i. There are n(n-1)/2 choices.

Three pin arrangements are recognized:

- **S(i, i+1)** and its **Reverse order**, S(i, i-1)
- **S(i, i+n)** and its **Reverse order**, S(i, i-n)

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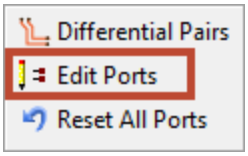
- **S(i, 2*n-i+1)** and its **Reverse order**, S(i, 2*n-i-1)

Reverse order is activated by selecting **Reverse**.

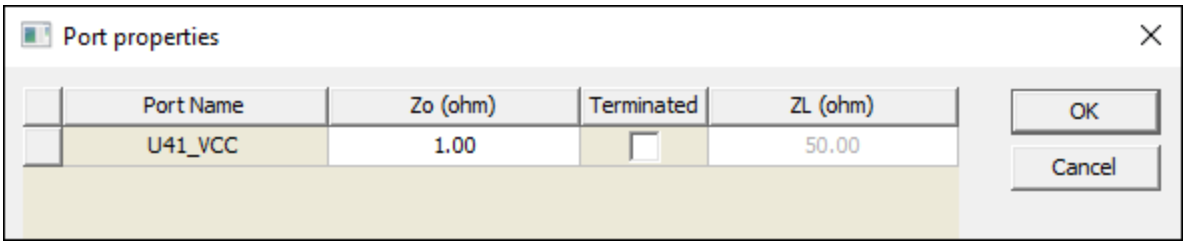
Network Data Explorer – Changing Port Properties and Reducing Matrix Size

The normalization impedance, termination, port order, gamma values, and de-embedding distance may all be edited from the Port Properties window.

To access these options from the ribbon, click Edit Ports:



The **Port Properties** window appears.



Ports appear in a table. Click a column heading to sort by that column. Click within a cell to edit the port property:

- **Zo (ohm)** and **ZL (ohm)** – specify Impedance values. Accepted syntaxes are:
  - real (e.g., 50)
  - real + imag i (e.g., 50+5i)
  - imag i (e.g., 5i).
- **Terminated** – use the check box to terminate a port. Terminated ports are eliminated from the matrix, reducing the matrix size. Existing datasets with mismatching port numbers will no longer be available for data comparisons.
- **De-Embedding** – this column appears only if gamma values are available. Default units can be changed from the Set Display Format window.

To reorder ports, click and drag a row to a new location.

To save changes, click **OK**.

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Resetting All Port Properties

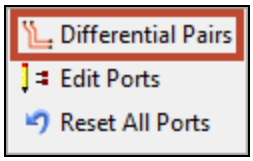
The **Reset All Ports** button clears reference impedances and terminations, but does not disable all differential pairs.

Network Data Explorer – Displaying Mixed-Mode Parameters using Differential Pairs

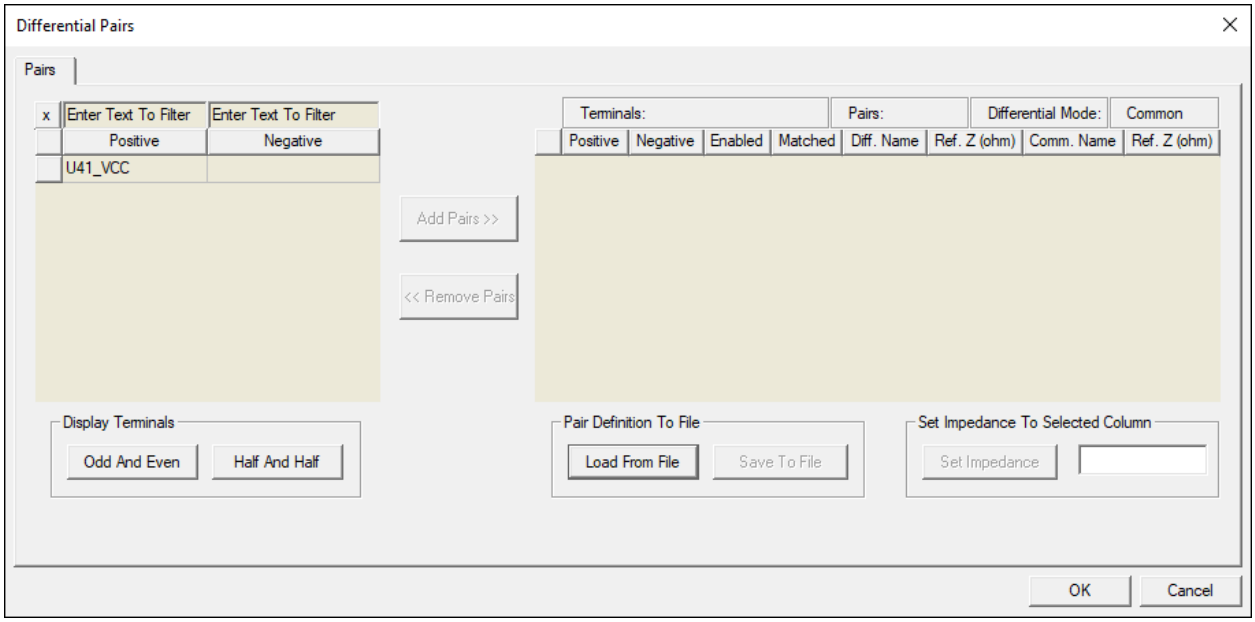
Network Data Explorer displays mixed-mode parameters when differential pairs are both defined and activated.

To define differential pairs:

1. Select existing ports.
2. Open Network Data Explorer.
3. On the ribbon, click **Differential Pairs**.



The **Differential Pairs** window appears.



4. Select a pair from the list on the left and click **Add Pairs**.
5. Click **OK**.

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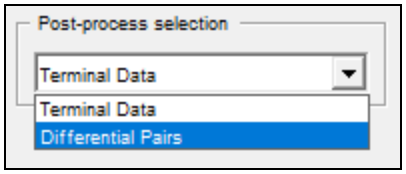
6. Select **Differential Pairs** from the **Post-process selection** field to view mixed-mode parameters.



Note:

The Network Data Explorer **Reset All Ports** button deactivates all pairs, but it does not clear differential pair settings. Since **Reset All Ports** also clears reference impedances and terminations, it should not be used when users want to disable all differential pairs. To disable all differential pairs, click the **Active** column header in the **Differential Pairs** window to deselect all pairs.

Data View Pane Shortcut Menus

The Data View pane presents different right-click menu options, depending on the context. Some of these options are also available on the ribbon.

Network Data Explorer commands unique to the shortcut menus are:

- Multiple Frequency Statistics
- Highlight Min/Max
- Select Transpose
- Color Legend Attributes
- Matrix Entries Plot Menu

Multiple Frequency Statistics

The **Multiple Frequency Statistics** menu option determines the statistical composite to display when multiple frequencies have been selected for the matrix display. The statistical data is always the first matrix displayed, followed by matrices for each individual frequency. The **Multiple Frequency Statistics** option also indicates the data used in the colored matrix plot when multiple frequencies have been selected.

This menu option appears when the **Frequencies** radio button is selected, regardless of whether you are in Table or Plot view.

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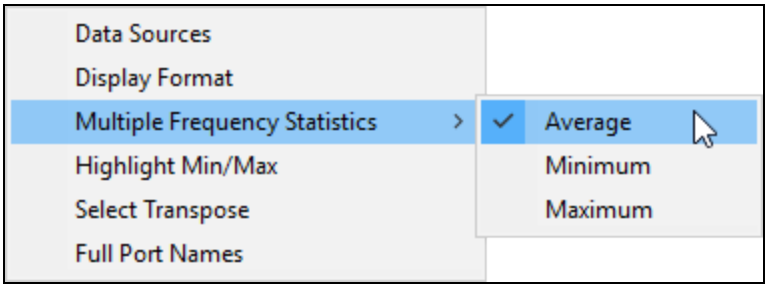


The menu options are:

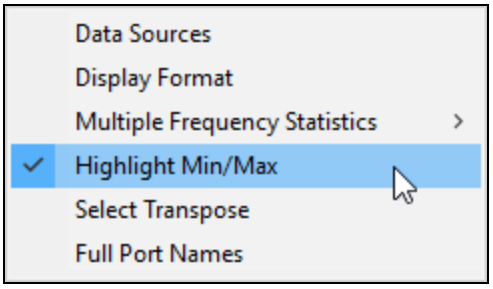
- **Average** – displays the average of the matrix values across selected frequencies.
- **Minimum** – displays the minimum matrix values across selected frequencies.
- **Maximum** – displays the maximum matrix values across selected frequencies.

The selected information also appears in a tool-tip when you hover the cursor over a cell.

Highlight Min/Max

The **Highlight Min/Max** menu option determines whether the minimum and maximum matrix entries should be highlighted in the matrix table and color plot view.

This menu option appears when the **Frequencies** radio button is selected, regardless of whether you are in Table or Plot view.



Select Transpose

The **Select Transpose** menu option determines whether transpose cells are highlighted along with selected cells.

This shortcut menu option appears in the **Matrix** plot, regardless of whether you are in Table or Plot view.

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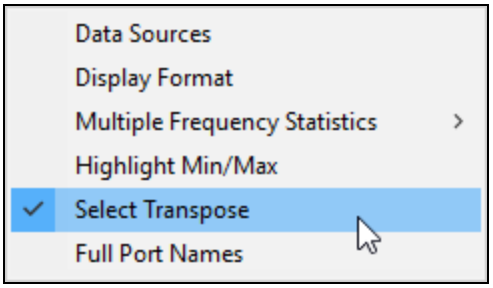
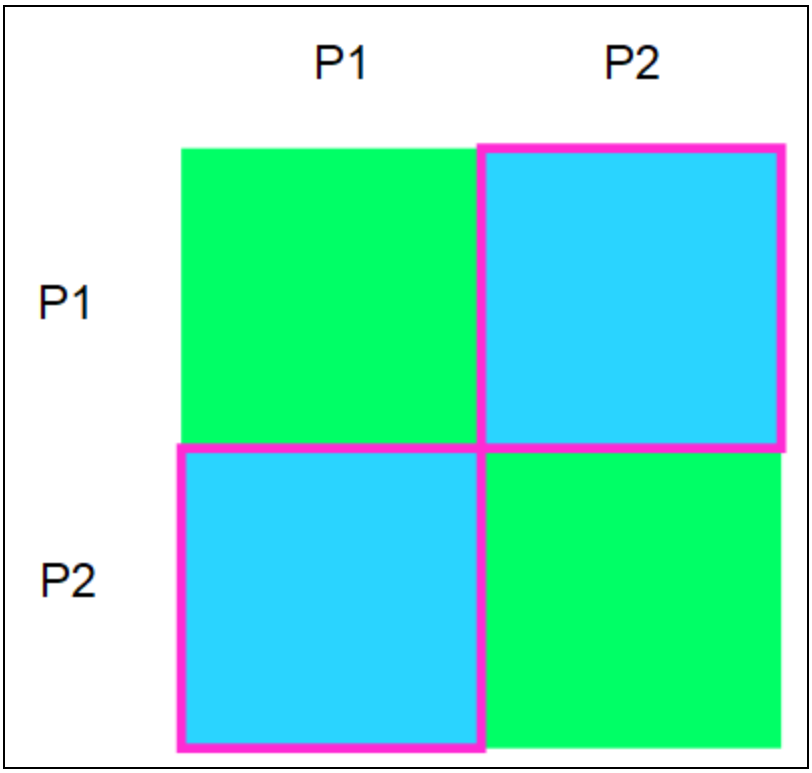


Transpose cells are highlighted in Table or Plot view, as shown below.

0.01000GHz	P1	-57.10340, -81.97841	-57.72581, 85.70836	-0.00213, -0.18916
	P2	-57.72582, 85.70825	-57.09556, -81.98749	-66.27113, 99.16916
	P3	-0.00213, -0.18916	-66.27110, 99.16941	-57.10246, -81.95892
	P4	-66.27112, 99.16942	-0.00213, -0.18929	-57.72556, 85.71465



Color Legend Attributes

The **Color Legend Attributes** menu option allows you to change the granularity of the color scheme and the value range for plots.

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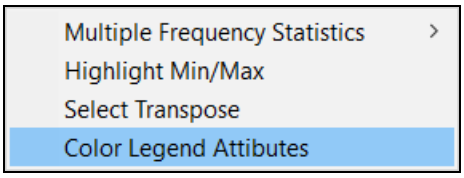
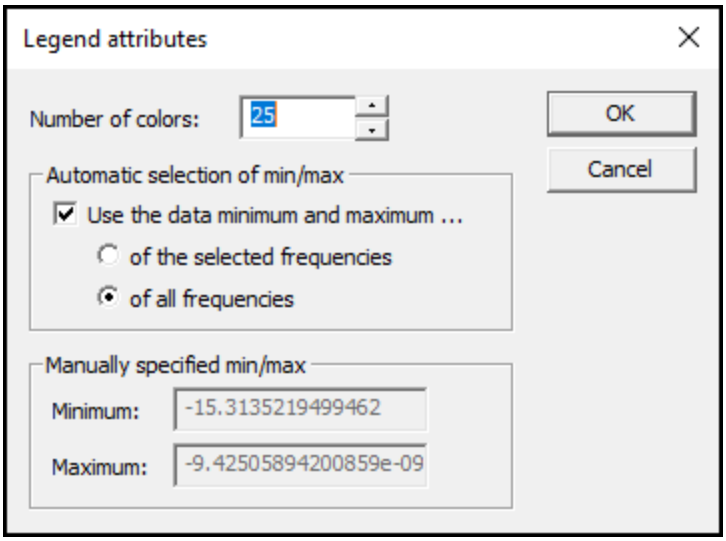
This menu option appears when the **Frequencies** radio button is selected and you are viewing the data in **Plot** mode.



Alternatively, double-click the matrix color plot to open the **Legend Attributes** window.



Options include:

- **Number of colors** – allows you to select number of color entries in the legend (i.e., the number of divisions between the start/end of the data range). This can be set to any discrete number between 1 and 50.
- **Automatic selection of min/max** – check the **Use the data minimum and maximum** check box to automatically select the data range using the minimum and maximum values from either selected frequencies or all frequencies in the dataset.
- **Manually specified min/max** – when the when the range is not automatically determined, these fields permit users to manually enter hard values (e.g., for S parameter data magnitude data, you could enter a minimum of 0 and a maximum of 1).

Using a standard range across all frequencies permits you to quantitatively compare plots, and ndExplorer retains legend settings for each data-type and display-format pair.

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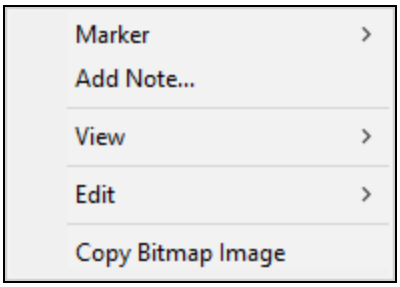
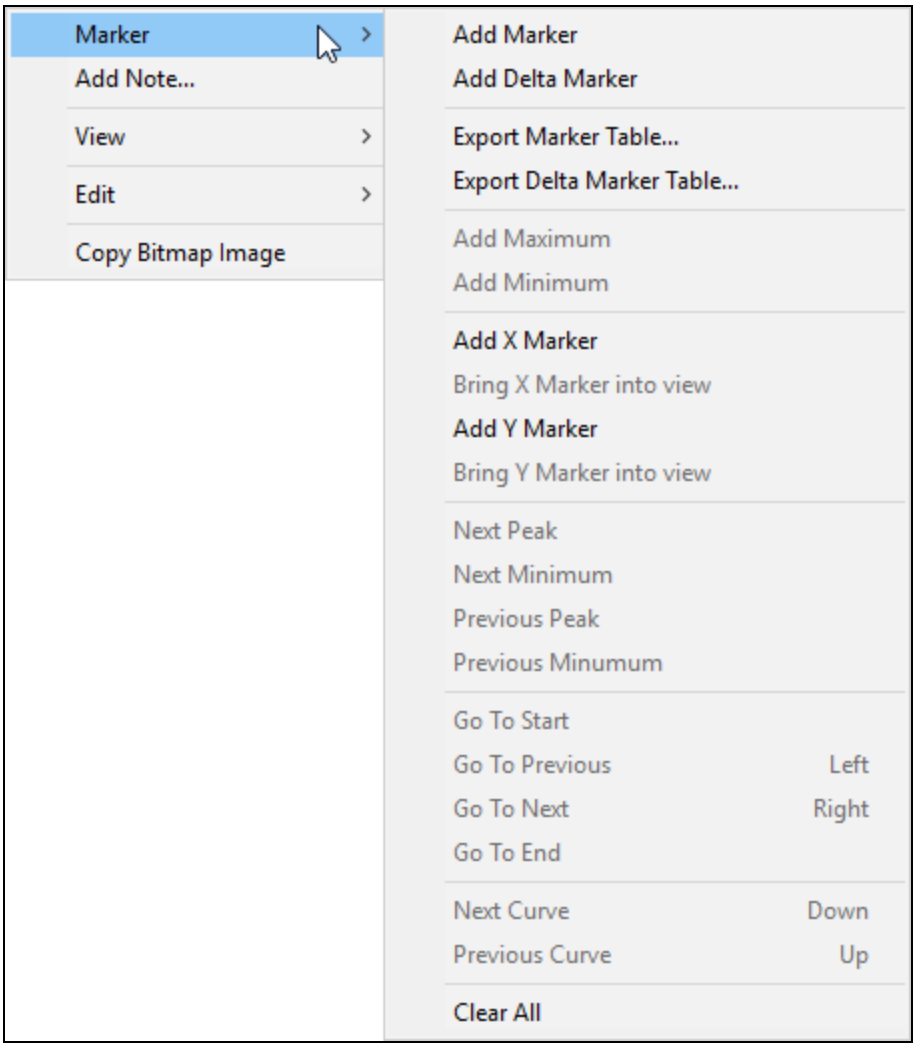
Matrix Entries Plot Menu

When the **Matrix entries** radio button is selected and you are viewing the data in **Plot** mode, several new shortcut menu options appear.



The **Marker** sub-menu provides commands for adding markers to plots.



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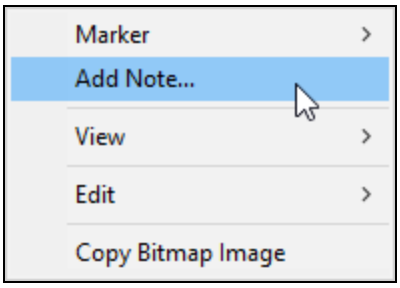
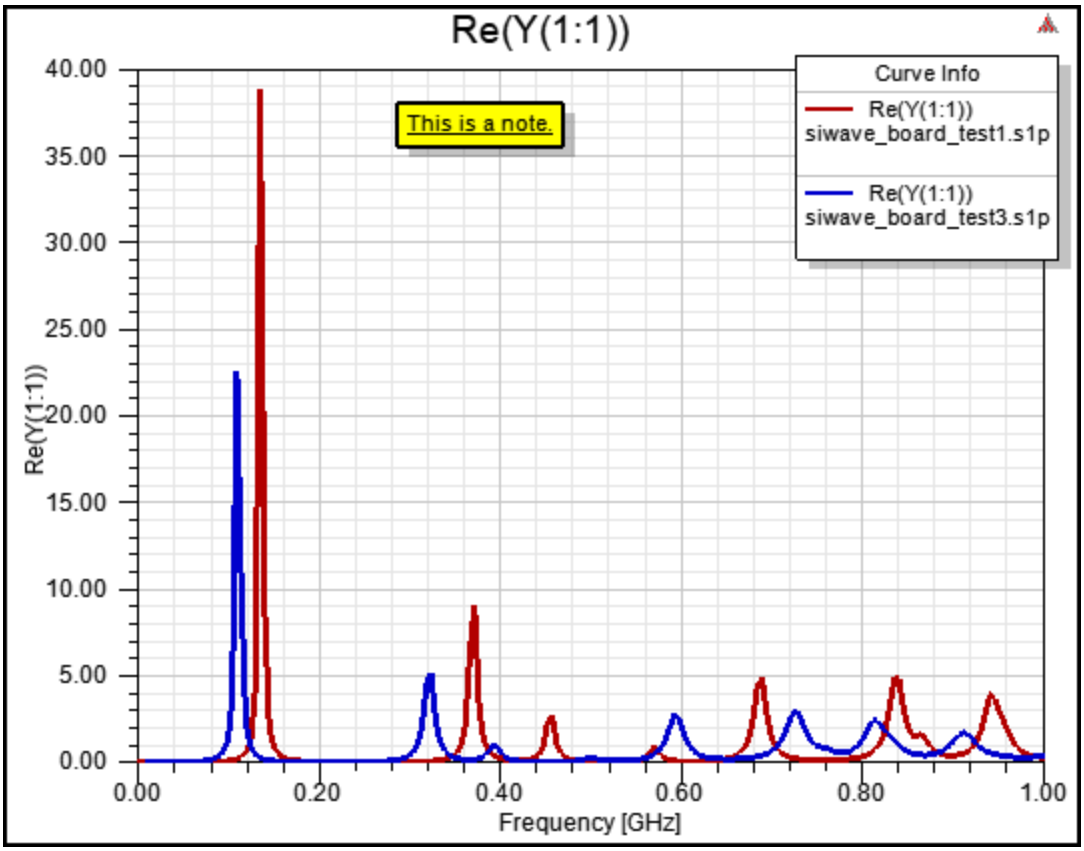
The **Add Note** menu option allows you to add a note to the plot.



The note appears at the location you right-clicked. You can click and drag the note to a new location, or double-click the note to change its color and font.



The **View** sub-menu provides commands for viewing, panning, zooming, and fitting elements to your plot.

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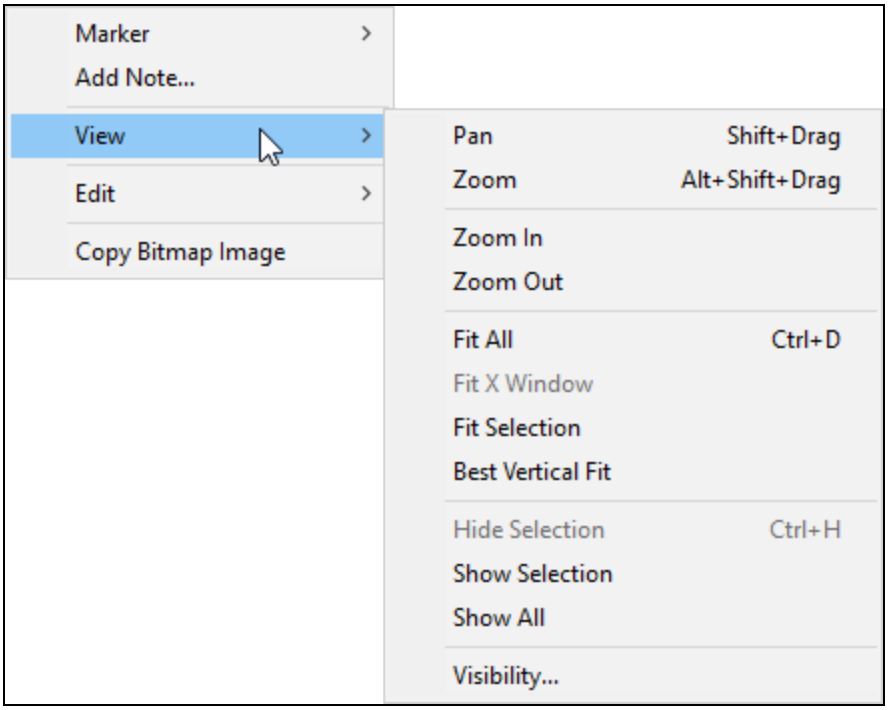
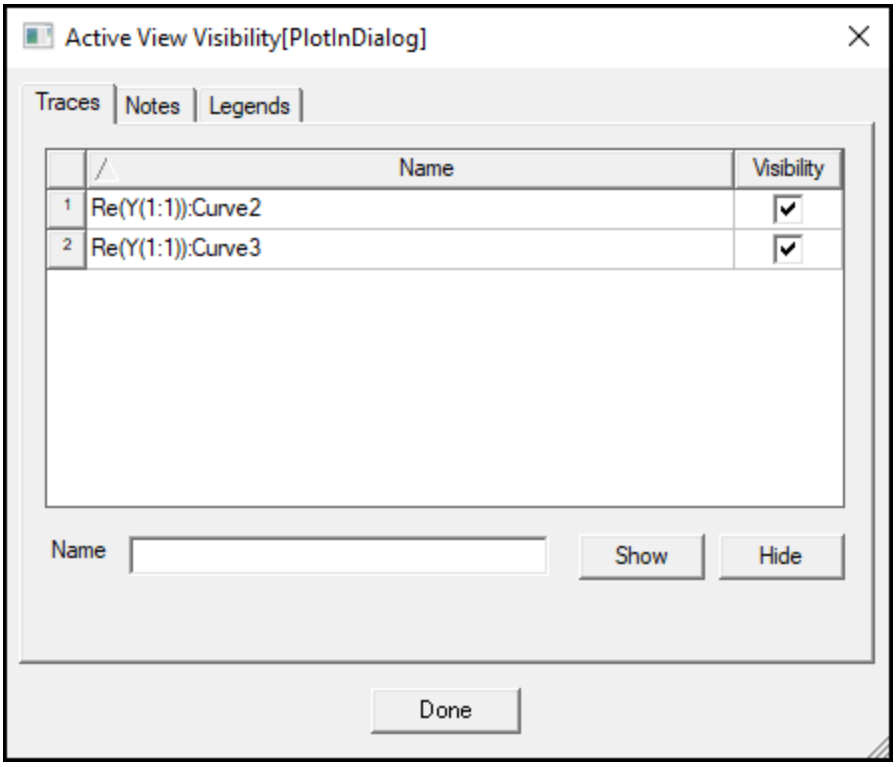


Click **Visibility** to open the **Active View Visibility** window, where you can select the visibility of traces, notes and legends.



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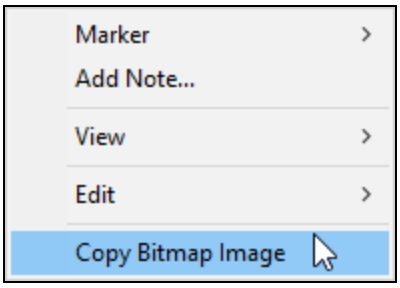
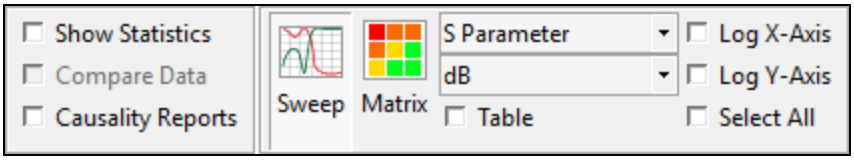
The **Copy Bitmap Image** menu option copies the plot to your clipboard. You can then paste it into a graphics editor.



Exploring Network Data and Modifying the Display

Network Data Explorer allows you to view data and modify various aspects of the display, including color plots, color coding, viewing across frequencies, and displaying individual statistics.

Plot options are selected from the ribbon:



Consult the following topics on Network Data Explorer capabilities:

- Viewing the S, Y, or Z Matrix for a Frequency
- Viewing a Color-coded Matrix Plot
- Displaying a Cell Graph Across All Frequencies
- Displaying Matrix Statistics by Frequency
- Displaying Individual Statistics for All Frequencies
- Creating a Statistics Plot
- Comparing Network Data
- Causality Checking and Plots

Viewing a Matrix Table

To view the S, Y or Z matrix:

1. Use the parameter drop-down menu to select **S Parameter**, **Y Parameter**, or **Z Parameter**.
2. Click **Matrix**.
3. Enable the **Table** check box.

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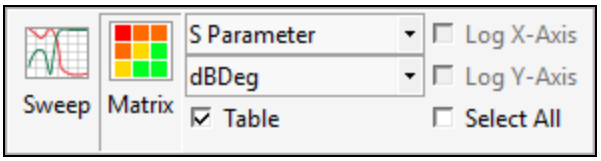
The settings in the ribbon will look like this:



The S, Y, or Z matrix displays.

Freq		P_DIG3_POWER_...	P_DIG3_POWER_...	P_FIFO_ON_1_74...	P_FIFO_ON_5_29...	P_FIFO_ON_5_RN...	P_FIFO_ON_18_7...
0.00000Hz	P_DIG3_PC	-59.89503, 0.00000	-0.00880, 0.00000	-129.00527, 0.00000	-161.37095, 0.00000	-145.24749, 180.00000	-130.21536, 180.00000
	P_DIG3_PC	-0.00880, 0.00000	-59.89503, 0.00000	-129.00527, 180.00000	-161.37095, 180.00000	-145.24749, 0.00000	-130.21536, 0.00000
	P_FIFO_ON	-129.00527, 0.00000	-129.00527, 180.00000	-6.03564, 180.00000	-6.02469, 0.00000	-6.02304, 0.00000	-6.02911, 0.00000
	P_FIFO_ON	-161.37095, 0.00000	-161.37095, 180.00000	-6.02469, 0.00000	-6.03858, 180.00000	-6.00807, 0.00000	-6.04705, 0.00000
	P_FIFO_ON	-145.24749, 180.00000	-145.24749, 0.00000	-6.02304, 0.00000	-6.00807, 0.00000	-6.03530, 180.00000	-6.04542, 0.00000
	P_FIFO_ON	-130.21536, 180.00000	-130.21536, 0.00000	-6.02911, 0.00000	-6.04705, 0.00000	-6.04542, 0.00000	-6.08050, 180.00000

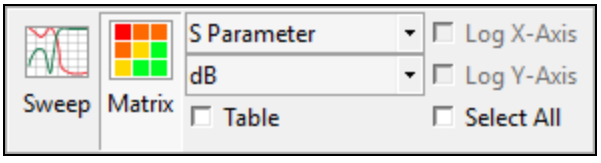
- Maximum values are highlighted in red stripes. If Select Transpose is enabled, transposes are highlighted in red stripes as well.
- Minimum values are highlighted in blue stripes.
- Selected cells appear in solid blue. If Select Transpose is enabled, the transpose is highlighted in blue as well.
- Double-clicking a cell switches to a matrix cell view, in which values for all frequencies for that cell are displayed. The double-clicked frequency is highlighted with solid red shading.
- Complex values are compared using their modulus. When multiple frequencies or variations are selected, the data display depends on the Multiple Frequency Statistics setting.

Viewing a Color-coded Matrix Plot

To view a color-coded matrix plot:

1. Use the parameter drop-down menu to select **S Parameter**, **Y Parameter**, or **Z Parameter**.
2. Click **Matrix**.
3. Ensure the **Table** check box is deselected.

The settings in the ribbon will look like this:



The color-coded matrix plot displays.

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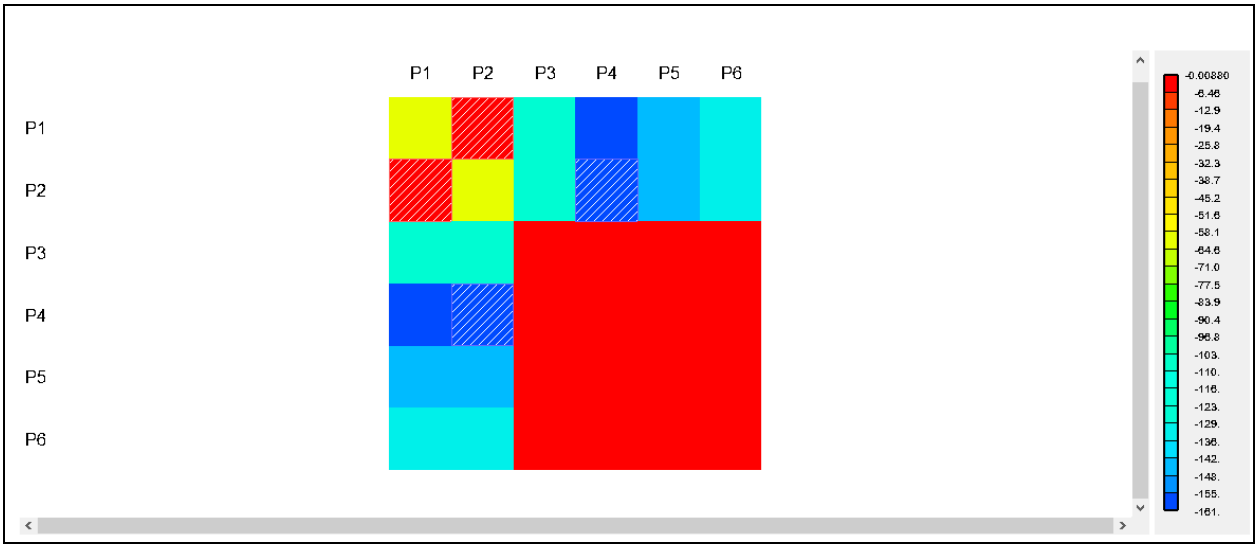


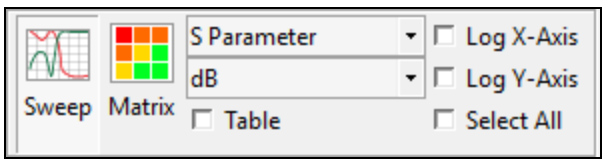
- Matrix values display in a color-coded grid. If the selected **Format** is a complex value, only the real component is used to determine the display color. When multiple frequencies or variations are selected, the data display depends on the Multiple Frequency Statistics setting.
- Maximum values are highlighted in red.
- Minimum values are highlighted in dark blue.
- Hover the cursor over any cell to view information about it.
- Click any cell to select it. Selected cells appear with a pink outline. If Select Transpose is enabled, the transpose is selected in pink as well.
- Double-click any cell to view a matrix cell plot in which all frequency values for that matrix cell are displayed as a graph.

Displaying a Cell Graph Across All Frequencies

Network Data Explorer can plot a cell across all frequencies.

1. From the ribbon, use the **Parameter** type drop-down menu to select **S parameter**, **Y parameter**, or **Z parameter**.
2. Click **Sweep**.

   The settings in the ribbon will look like this:



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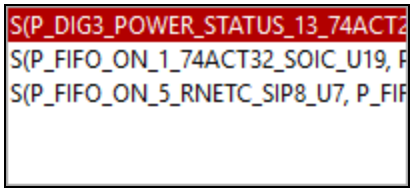
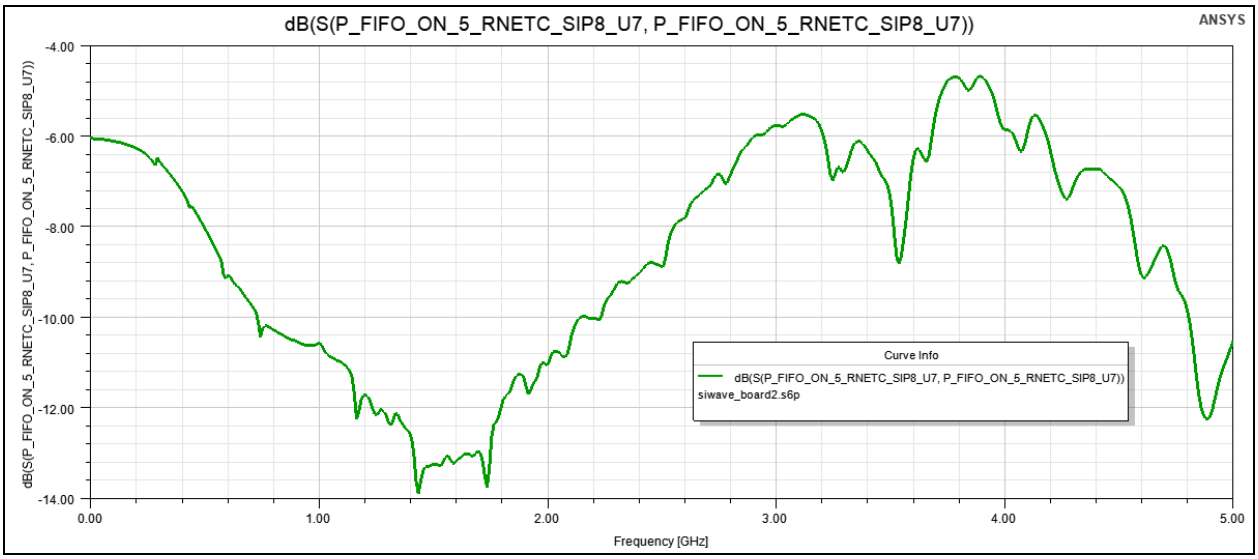
3. From the Cell and Frequency Selection pane, select frequencies to display.



   Alternately, enable the **Select All** check box on the ribbon to select all frequencies.

4. To add a log scale to the X-axis, click **Log X-Axis** on the **NDE** ribbon.
5. To add a log scale to the Y-axis, click **Log Y-Axis** on the **NDE** ribbon.

The graph displays. Right-click the graph to view additional commands.

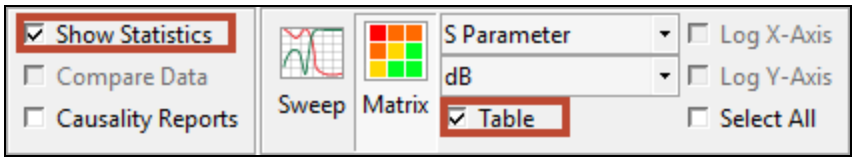


Displaying Matrix Statistics by Frequency

Network Data Explorer can display various statistical measurements.

1. From the ribbon, click **Matrix**.
2. Enable the **Table** and **Show Statistics** check boxes.

   The selections in the ribbon should look similar to this:



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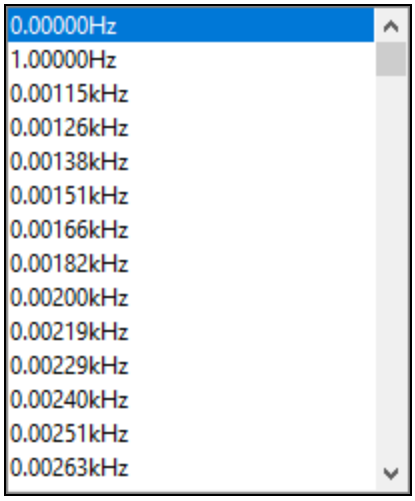
3. From the Cell and Frequency Selection pane, select frequencies to display.



The statistics display:

Freq		Average	Minim...	Maxim...	StdDev	NTI	Passivity
50.00000MHz		-28.20530	-56.41050	-0.00010	28.20520	2	1.00000
100.00000MHz		-25.19490	-50.38960	-0.00020	25.19470	2	1.00000
150.00000MHz		-23.43390	-46.86750	-0.00030	23.43360	2	1.00000
200.00000MHz		-22.18450	-44.36850	-0.00050	22.18400	2	1.00000
250.00000MHz		-21.21535	-42.43000	-0.00070	21.21465	2	0.99999
300.00000MHz		-20.42350	-40.84620	-0.00080	20.42270	2	1.00000
350.00000MHz		-19.75405	-39.50700	-0.00110	19.75295	2	0.99999
400.00000MHz		-19.17415	-38.34700	-0.00130	19.17285	2	1.00000
450.00000MHz		-18.66265	-37.32380	-0.00150	18.66115	2	1.00001

Click a column header to sort data by that column.

Hover the cursor over a cell to view information about it.

Only real (not complex) data formats are offered for statistical analysis. **Passivity** is only available for S-parameter data (comparisons inactive). **NTI** refers to the number of trivial items; for S-parameters, this includes all zeros and ones; for all other data (and data comparisons), only zeros are counted as trivial. The minimum value for each column is highlighted in blue; the maximum is highlighted in red.

Displaying Individual Statistics for All Frequencies

To view individual statistics across all frequencies:

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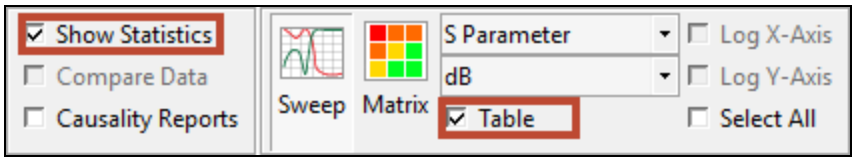
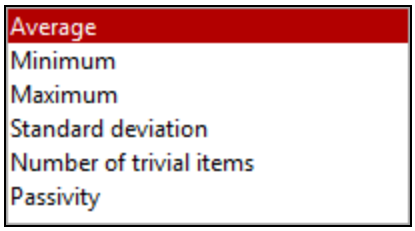
1. From the ribbon, click **Sweep**.
2. Ensure that **Table** and **Show Statistics** are selected.

   The selections in the ribbon should look similar to this:



3. From the Cell and Frequency Selection pane, select statistics to display.



Selected statistics are displayed for all frequencies.

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Freq		Average	Minimum	Maximum	StdDev	NTI	Passivity
0.00000Hz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
1.00000Hz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00115kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00126kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00138kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00151kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00166kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00182kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00200kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00219kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00229kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00240kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00251kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00263kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00275kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00288kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00302kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00316kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00331kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00347kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00363kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00380kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00398kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00417kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00437kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00457kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00479kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00501kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00525kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00550kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00575kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000
0.00603kHz		-68.88080	-161.37095	-0.00880	66.64507	16	1.00000

Passivity is only available for S-parameters (comparisons inactive).

For S-parameters, the **Number of Trivial Items (NTI)** includes all values of 0 and 1. For other data and data comparisons, only values of 0 are counted as trivial.

Creating a Statistics Plot

Network Data Explorer can display a graph of selected statistical measures across all frequencies.

1. From the ribbon, click **Sweep**.
2. Ensure that **Show Statistics** is enabled.

The selections on the ribbon should look similar to this:

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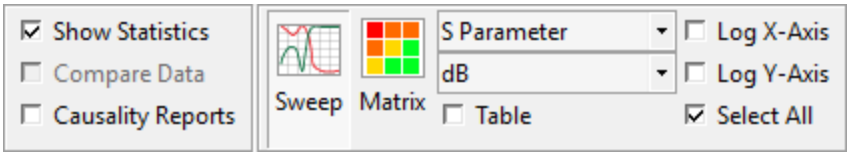
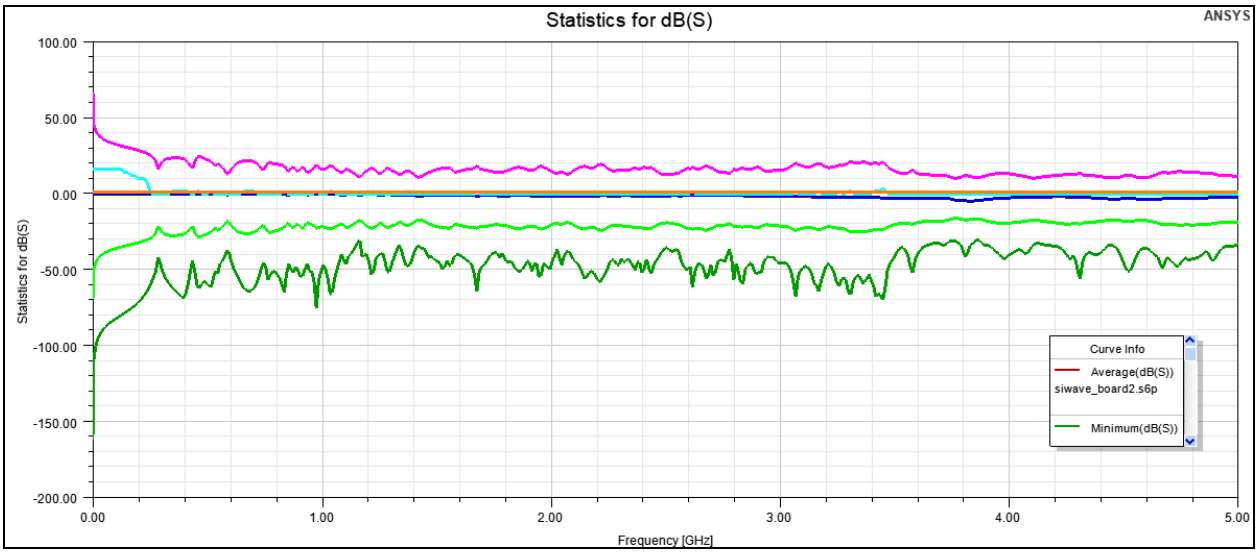


The selected statistics are plotted.



Hover the cursor over a statistic to view more information about it.

Passivity is only available for S-parameters (comparisons inactive).

For S-parameters, the **Number of Trivial Items (NTI)** includes all values of 0 and 1. For other data and data comparisons, only values of 0 are counted as trivial.

Comparing Network Data

Network Data Explorer can compare variations for two network data sets that are the same size.

1. From the ribbon, click **Sweep**.
2. From the Network Data Selection pane, select exactly two data sets.
3. From the ribbon, click **Compare Data**.
4. From the Cell and Frequency Selection pane, select which cells you want to compare . For each value along the X-axis, the Y-axis values are subtracted, one from the other, to create the comparison plot. The second selected data is subtracted from the first selected data.
5. If appropriate, enable the **Show Statistics** check box to show values applied to all cells and all frequencies.

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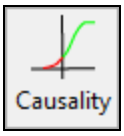
Note:

- It is not possible to compare a dataset against itself unless the dataset has been loaded twice.
- Traces for a given cell or statistical measure are displayed for all data sets; you can use tool tips to distinguish between them.
- If a single cell or statistical measure is displayed, different colors are used for each data trace. If multiple cells or statistical measures are selected, a single color is used for all data traces for each cell or statistical measure.
- In a data comparison, traces are shown for all selected data sets. This is true for both cell and statistical traces.
- If dB format is shown, you can either subtract values before or after applying the dB function. See: Display Format.

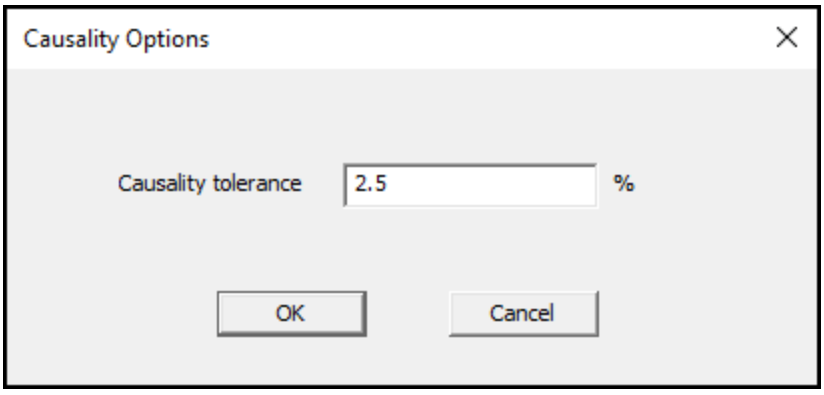
Causality Checking

Network Data Explorer can perform a causality check on S-parameter data from any source (solution or file), and provide plots of the results in various formats.

When S-parameter data is loaded into Network Data Explorer, the **Causality** button is enabled. Click to start the causality check:



The **Causality Options** window appears. Enter a tolerance and click **OK**.



Depending on the size of the S-parameter data, the causality check may take several minutes to complete.

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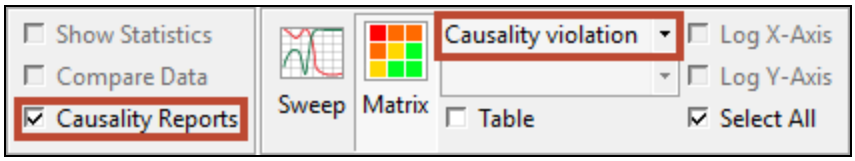
Reconstruction Error Tolerance – Causality of a frequency response is determined by calculating the generalized Hilbert transform of the data at all frequencies. A causal frequency response is equal to its generalized Hilbert transform. The reconstruction error is the difference between the tabulated data and its transform at a given frequency. The message shows the maximum reconstruction error tolerance for a causal frequency response. The default tolerance of 0.01 is equal to the state-space fitting tolerance.

Maximum Causality Error – The maximum causality error for all port pairs and all frequencies, along with the matrix indices (port numbers) where the maximum noncausality occurs. A noncausal response is one where all matrix entries can be conclusively analyzed, and at least one entry exceeds the causality tolerance. The maximum reconstruction appears first, followed by port numbers in brackets, e.g. [port number, port number]. When all results are conclusive but no matrix reconstruction error exceeds the tolerance, the maximum causality error is reported as zero, and no matrix entry is listed.

Causality Plots

To see the plotted results of the causality check:

1. From the ribbon, enable **Causality Reports**.
2. Click **Matrix**, or use the drop-down menu to select **Causality violation**.



A rectangular plot displays, with dimension N x N and color-coding to indicate the causality status of each port pairing.

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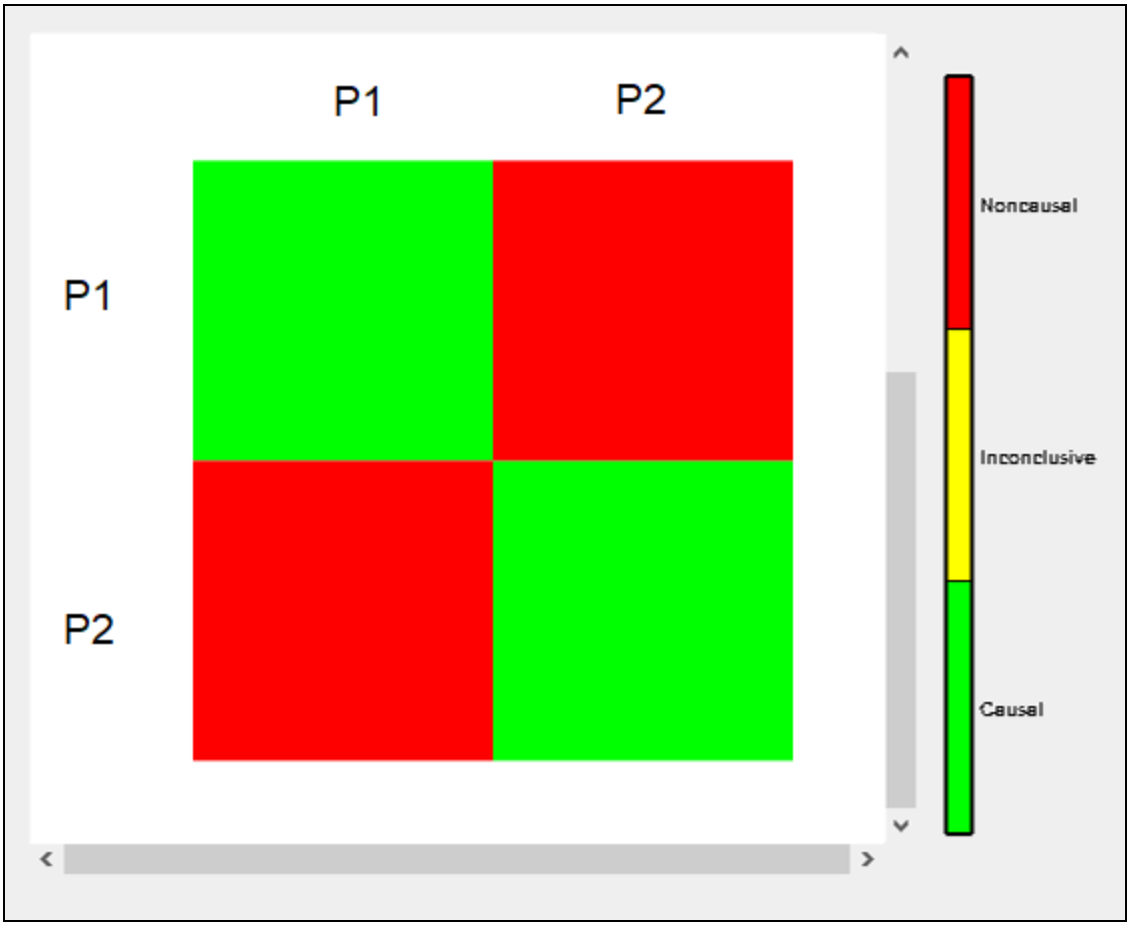

In this plot, the cells go from (Port 1, Port 1) at the upper-left area to (Port N, Port N) at the lower-right corner. The result shows the causality over all frequencies in the data. In this example, the matrix is symmetric, so that both S12 and S21 are noncausal, while S11 and S22 are causal.

To see the details for each frequency, select the **Table** radio button in the Data View Pane.

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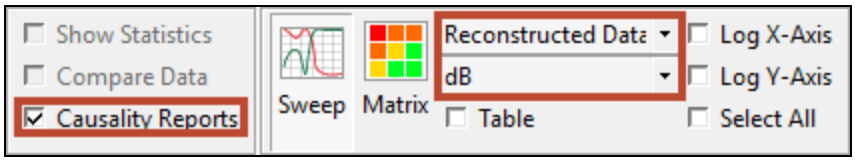
Freq		U41_VCC	U41_VCC
0.00000Hz	U41_VCC	0.00003, 0.00000	0.00018, 0.00000
0.00503GHz	U41_VCC	0.00076, 0.00000	0.00041, 0.00000
0.01005GHz	U41_VCC	0.00048, 0.00000	0.00043, 0.00000
0.01508GHz	U41_VCC	0.00044, 0.00000	0.00035, 0.00000
0.02010GHz	U41_VCC	0.00037, 0.00000	0.00035, 0.00000
0.02513GHz	U41_VCC	0.00032, 0.00000	0.00032, 0.00000
0.03015GHz	U41_VCC	0.00027, 0.00000	0.00030, 0.00000
0.03518GHz	U41_VCC	0.00023, 0.00000	0.00027, 0.00000
0.04020GHz	U41_VCC	0.00019, 0.00000	0.00024, 0.00000
0.04523GHz	U41_VCC	0.00015, 0.00000	0.00020, 0.00000
0.05025GHz	U41_VCC	0.00012, 0.00000	0.00017, 0.00000
0.05528GHz	U41_VCC	0.00008, 0.00000	0.00013, 0.00000
0.06030GHz	U41_VCC	0.00006, 0.00000	0.00009, 0.00000
0.06533GHz	U41_VCC	0.00002, 0.00000	0.00005, 0.00000
0.07035GHz	U41_VCC	0.00000, 0.00000	0.00001, 0.00000
0.07538GHz	U41_VCC	0.00003, 0.00000	0.00003, 0.00000
0.08040GHz	U41_VCC	0.00005, 0.00000	0.00007, 0.00000
0.08543GHz	U41_VCC	0.00007, 0.00000	0.00011, 0.00000
0.09045GHz	U41_VCC	0.00008, 0.00000	0.00015, 0.00000
0.09548GHz	U41_VCC	0.00010, 0.00000	0.00018, 0.00000
0.10050GHz	U41_VCC	0.00011, 0.00000	0.00022, 0.00000
0.10553GHz	U41_VCC	0.00012, 0.00000	0.00025, 0.00000
0.11055GHz	U41_VCC	0.00013, 0.00000	0.00028, 0.00000
0.11558GHz	U41_VCC	0.00014, 0.00000	0.00031, 0.00000
0.12060GHz	U41_VCC	0.00015, 0.00000	0.00034, 0.00000
0.12563GHz	U41_VCC	0.00015, 0.00000	0.00036, 0.00000
0.13065GHz	U41_VCC	0.00015, 0.00000	0.00037, 0.00000

To plot the reconstructed frequency response generated by the causality checker:

1. From the ribbon, enable **Causality Reports**.
2. Click **Sweep**, or use the drop-down menu to select **Reconstructed Data**.
3. Use the **Format** drop-down menu to select an appropriate format. dB is selected by default.



The plot appears, showing the reconstruction error at each frequency divided by the tolerance.

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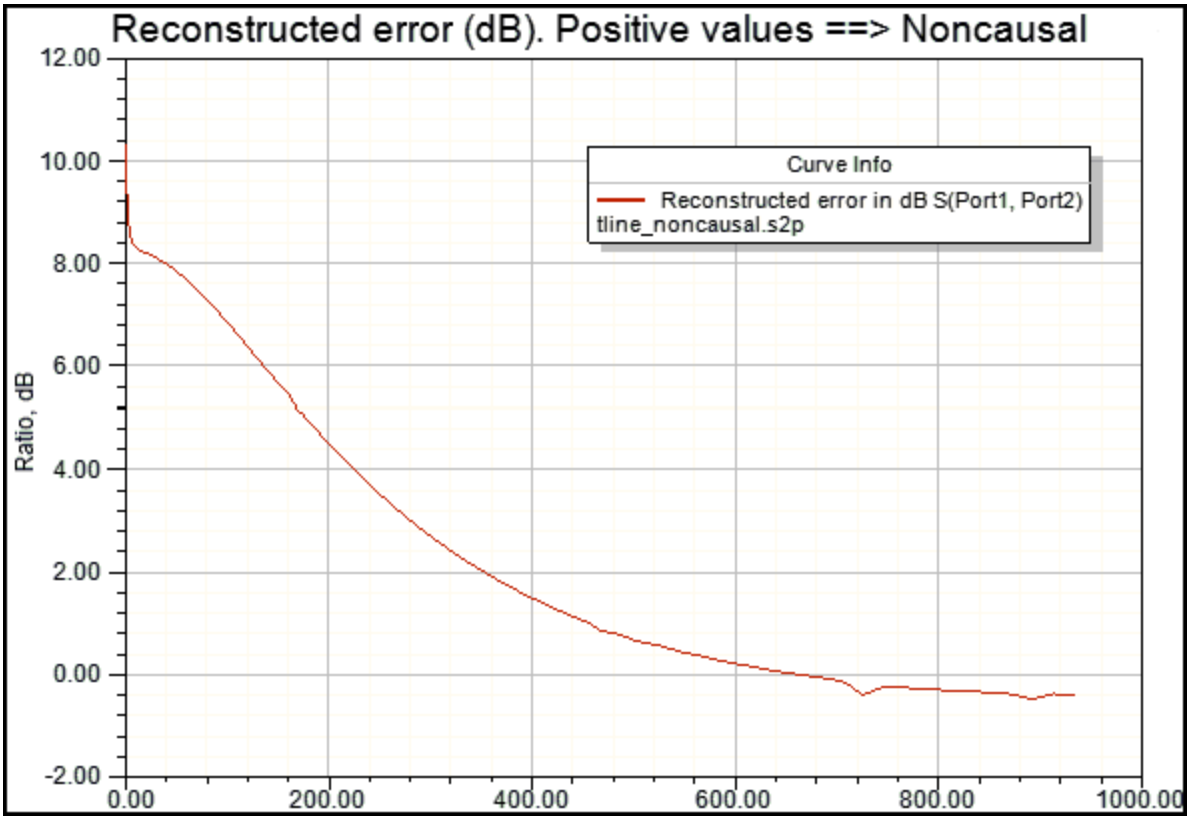

The reconstruction error ratio for parameter S12 is positive for frequencies less than about 680MHz, indicating a broad range of noncausal behavior.

To compare the real part of the reconstructed data to the real part of the actual data, set the **Format** to **Real**.

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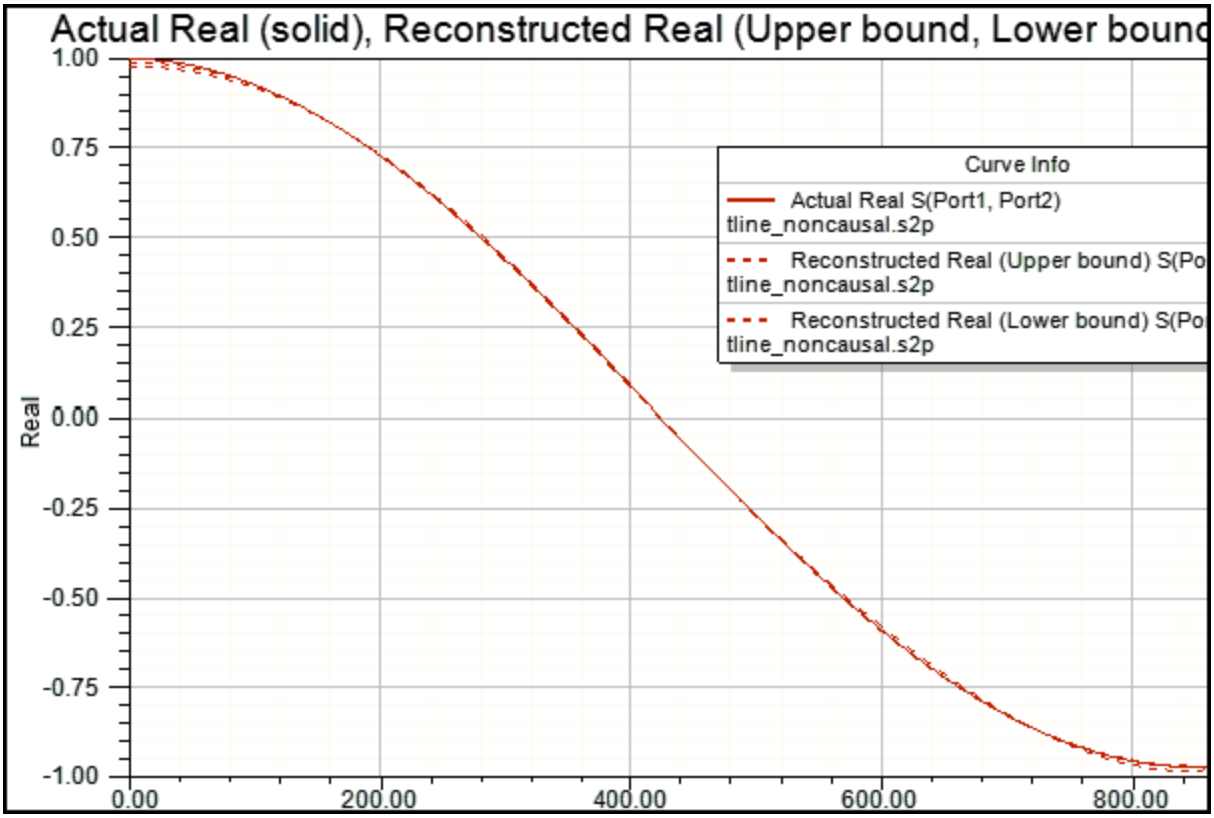

For a causal frequency response, the actual data (solid line) will be within the upper and lower bounds of the reconstruction (dotted lines) at all frequencies.

To compare the imaginary part of the reconstructed data to the imaginary part of the actual data, set the **Format** to **Imaginary**.

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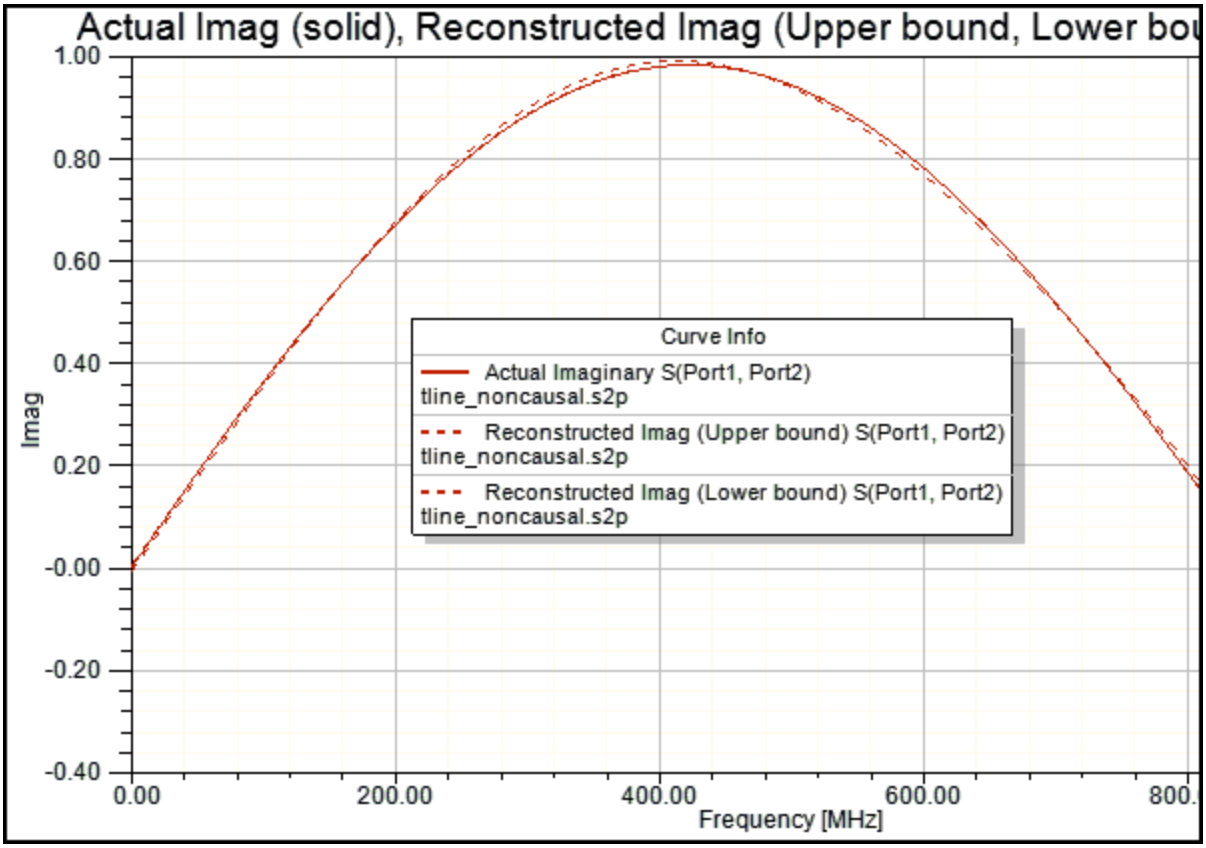

For a causal frequency response, the actual data (solid line) will be within the upper and lower bounds of the reconstruction (dotted lines) at all frequencies.

To view the frequency-dependent discretization error, set the **Format** to **Discretization**.

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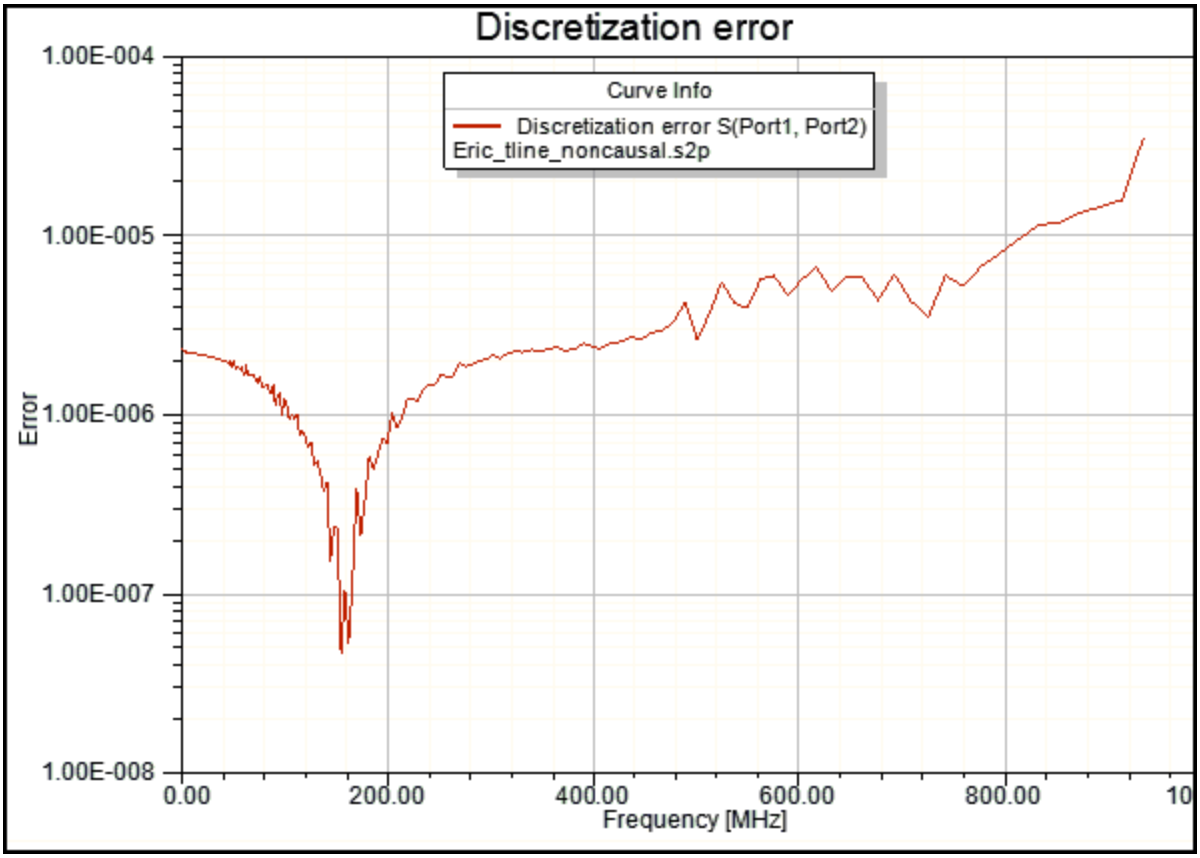

The discretization error is the error that is due to the fact that the data are available only at discrete frequencies rather than for a continuous spectrum. A discretization error near or greater than the causality tolerance renders the causality check inconclusive. Data at more frequencies could reduce the discretization error and render the analysis conclusive. This set of data exhibits low discretization errors (<<0.01) at all frequencies, and the causality check is conclusive (conclusively noncausal in this example).

Multithreading

By default, multithreading (execution on multiple cores) is enabled for Causality Checking and Macro Model export. Multithreading saves significant time in the Causality Check calculation, and improves the time for other state-space fitting operations.

The **Num Cores** field on the Network Data Explorer ribbon defaults to half the number of cores detected on your computer.

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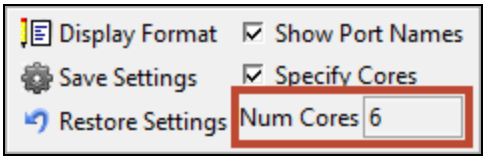

For best performance, disable hyper-threading on your computer. When hyper-threading is enabled, the number of cores includes the physical cores and an equal number of logical cores. With hyper-threading disabled, the display shows only half the number of physical cores.

To disable multithreading, deselect the **Specify Cores** check box.

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9 - Running Simulations

The SIwave platform includes multiple solvers. Each solver offers a different combination of uses along three dimensions: the scale of features that can be conveniently solved, the applicability of the solution to signal integrity or power integrity issues, and the degree of integration into SIwave.

Solver Scale

Solvers fall into three classes when you consider the scale of geometric features that can be solved conveniently.

- **Small-scale solvers** can solve selected traces, signals, nets and ICs.
- **Medium-scale solvers** can handle packages and packages with ICs.
- **Large-scale solvers** can analyze PCBs, with or without Packages and ICs.

Solver Applicability

A solver can yield results for signal integrity or power integrity studies (including thermal).

Degree of Integration into SIwave

Solvers can be accessible from within SIwave as tools, as solvers on demand, or as cosimulators using dynamic links. Some are external cosimulators, which use the import and export functions.

- **S-Parameter Tools** are accessed from the **Tools** menu (See: Network Data Explorer and SUtility).
- **Solvers on Demand** and **Cosimulators using dynamic links** are accessible from the **Simulation** menu.
- **Import and Export** operations are accessed from the **File** menu, from simulation setup menus, and from simulation results menus.

Summary Table for SIwave Solvers

Table 1 summarizes the scale, integration, and applicability of the SIwave solvers, with links.

Solver	Description
SIwave SYZ	The SIwave SYZ extractor is a high-speed hybrid solver for medium and large-scale analysis of PCBs and packages. SIwave SYZ calculates frequency-dependent S-parameters for signal integrity and EMI investigations, as well as board-level power supply impedance modeling. The SIwave SYZ solver is accessed via the **Simulation** menu.
SIwave Resonant Modes	On-demand Resonant mode analysis solves for frequency-dependent voltage swings between layers of a PCB or multi-layer package. The SIwave Resonant Mode solver is accessed via the **Simulation** menu.

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Solver	Description
SIwave DC_IR	DC_IR analysis solves for the voltage drop across the power plane of the PCB. The DC solution can provide you with important information pertaining to power delivery. The SIwave DC_IR solver is accessed via the **Simulation** menu.
SIwave EM MTTF	The EM MTTF simulation provides an estimate of Mean Time to Failure (MTTF) of metallization due to electron flow, based on Black's Equation.
SIwave Frequency Sweep	Frequency sweep analysis allows you to evaluate the effects on the voltage and current distribution of applied AC voltage and current sources on your PCB across a specified frequency range. The SIwave Frequency Sweep solver is accessed via the **Simulation** menu.
SIwave Near Fields	The SIwave Near Field solver analyzes the radiated fields associated with a PCB. The near-field region exists at less than a wavelength from an energy source. Near fields can play a role in EMI. The SIwave Near Field solver is accessed via the **Simulation** menu.
SIwave Far Fields	The SIwave Near Field solver analyzes the radiated fields associated with a PCB. The far-field radiation occurs at more than a wavelength from an energy source. Far-fields can play a role in EMI. The SIwave Far Field solver is accessed via the **Simulation** menu.
SIwave Induced Voltage	SIwave Induced Voltage solver computes the induced voltage generated on the board by a plane wave incident at a particular angle and having a specific polarization.
PSI SYZ	PSI extracts the SYZ-parameters with high-speed Finite Element Meshing (FEM) using prism elements. PSI SYZ is optimized for power integrity and signal integrity analyses of packages. The PSI SYZ solver is accessed via the **Simulation** menu.
PSI AC Currents	The PSI AC Current solver evaluates the effects on the voltage and current distribution of applied AC voltage and current sources on a package across a specified frequency range. The PSI AC Current solver is accessed via the **Simulation** menu.
HFSS 3D Layout SYZ	The HFSS 3D Layout SYZ solver handles signal integrity analyses of layer-based ECAD designs with 3D precision. HFSS 3D Layout analyses typically focus on individual traces or nets within a package or PCB. The HFSS 3D Layout SYZ solver is accessed via the **Simulation** menu.
PI Advisor	The SIwave PI Advisor performs a loop inductance and sensitivity analysis on the capacitors already mounted on the PCB. The analysis produces several solutions or schemes, each of which seeks to optimize the trade-off between cost and performance. PI Advisor is accessed from the **Simulation** menu.
SIwizard	You can initiate a cosimulation with Ansys Electronics Desktop Circuit/Schematic from SIwave. By default, the SIwizard uses the Ansys Electronics Desktop-SIwave dynamic link. Selected nets are given ports and buffer models and set up as S-parameter dynamic link N-ports in Ansys Electronics Desktop. SIwizard is accessed from the **Simulation** menu.

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Solver	Description
TDRwizard	You can initiate a cosimulation with Ansys Electronics Desktop Circuit/Schematic from SIwave. By default, the TDRwizard uses a Nexxim netlist that points to a S-parameter touchstone file generated from SIwave. You can also use a schematic approach that has a Ansys Electronics Desktop-SIwave dynamic link. The TDRwizard automates the creation of pin groups for power/ground pins and of ports on both signal and power nets.
PDN Channel Builder	PDN Channel Builder extracts a power delivery network (PDN) model in either SIwave or PSI. It generates a power channel model of a combined die and package. The model includes the Power and Ground nets in the die and the voltage regulator module (VRM). PDN Channel Builder is accessed from the **Simulation** menu.
IC Die Network	If your design contains a set of pins representing connection points for an IC die, you can create an IC Die Network. Such a network consists of resistive and/or capacitive elements that model the on-chip power distribution (e.g., VDD and GND net) interconnect parasitics. **Create IC Die Network** is accessed from the **Tools** menu.
Signal Net Analyzer	The Signal Net Analyzer gives you the ability to get a quick idea of characteristic impedance and also to rapidly generate transient voltage waveforms of pin-to-pin signal propagation by co-simulating with HSPICE or Nexxim. Traces comprising propagation path are modeled as frequency dependent W-element transmission lines and source/sink pins can have IBIS driver/receiver models. Signal Net Analyzer is accessed from the **Tools** menu.
Capacitor/Inductor Library Browser	The Capacitor/Inductor Library Browser allows you to define VRM parameters and impedance requirements for a PCB, then automatically select and mount capacitors that meet the impedance requirements. You can plot the impedance of vendor or imported capacitor components versus frequency. The Capacitor/Inductor Library Browser is accessed from the **Tools** menu.
Q3D SYZ	The Q3D SYZ solver provides 3D accuracy for package-level SI analyses. The interface to Q3D is via 3D export.
HFSS for MCAD SYZ	The HFSS for MCAD SYZ solver produces high accuracy for critical traces. The interface to HFSS for MCAD is via 3D export.
RedHawk, Totem	The Apache tools are optimized power analyses of packages and ICs. The interface to these tools is via CPM import, and SSO export.
Icepak	Ansys Icepak performs thermal analysis of PCB-level designs. The interface to Icepak is via file import and export from the DC_IR solver.
CPA	A CPA model comprises DC resistance and low frequency inductance and capacitance effects. High resolution resistance and inductance color maps generated after running a CPA simulation help in package probing. A comprehensive HTML reporting feature summarizes the layout geometry, setup and simulation results. The CPA model can be seamlessly imported into Ansys RedHawk for Chip + Package cosimulation.

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Simulation Options and Setup

Before starting simulation, some preliminary steps are typically required (e.g., you may need to identify power and ground nets and define ports or voltage probes). See Simulation Setup for details.

SIwave, PSI, HFSS 3D Layout, and Q3D Extractor have options that you can set as part of the Simulation menu.

SIwave Simulations

You can define SIwave simulation options and compute the following simulations in SIwave:

- Resonant Modes
- Frequency Sweep
- Near Field Simulation
- Far Field Simulation
- DC IR-Drop Simulation
- EM MTTF Simulation
- Induced Voltage
- Crosstalk Scan, Frequency Domain
- Crosstalk Scan, Time Domain
- Icepak Simulation
- S-, Y-, Z- parameter Sweep

After you have computed the S-,Y-, Z- parameters, you can compute:

- Differential S-parameter Sweep
- RLGC Subcircuits
- Full-wave Subcircuit

PDN Channel Builder and PI Advisor simulations can use either the SIwave solver or the PSI solver:

- PDN Channel Builder Simulation
- PI Advisor Simulation

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Note:

SIwave simulations will automatically detect the CPU type (i.e., AMD or Intel) and determine whether to use AMD Math Library (i.e., AMDL) or Intel Math Kernel Library (i.e., Intel MKL) algorithms. Each library contains a collection of optimized mathematical routines for scientific computing, including functions for linear algebra, Fast Fourier Transforms (i.e., FFTs), and vector math, designed for a particular processor type.

SIwave Simulation Options

SIwave options can be set globally for all SIwave simulation types. These global parameters include geometry options, solver settings, and mesh refinement settings. A few options are specific to one or more simulation types.

To define SIwave simulation options:

1. Click **Simulation**.
2. From the SIwave area, click **Options** to open the **SIwave Options** window.

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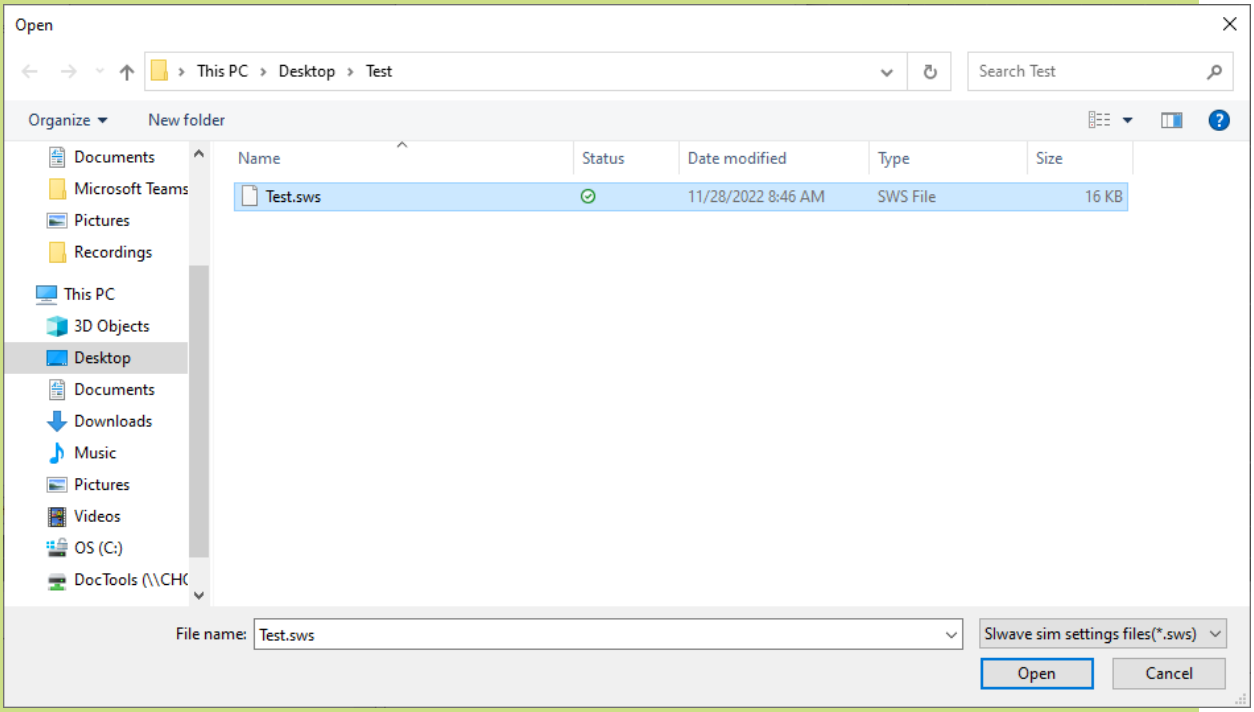
Note:

To import a configuration file, click **Import Settings** at the bottom-left side of the window, which opens an explorer window. Then use the explorer window to navigate to an appropriate directory and select the **SIwave sim settings file** (e.g., **Test.sws**). Finally, click **Open** to close the explorer window and apply the saved settings to the current simulation.



3. The **SIwave Options** window opens at the **SI/PI** tab . Use the radio buttons to select either **SI simulation** or **PI simulation**, and move the corresponding slider if you want to increase speed or accuracy.

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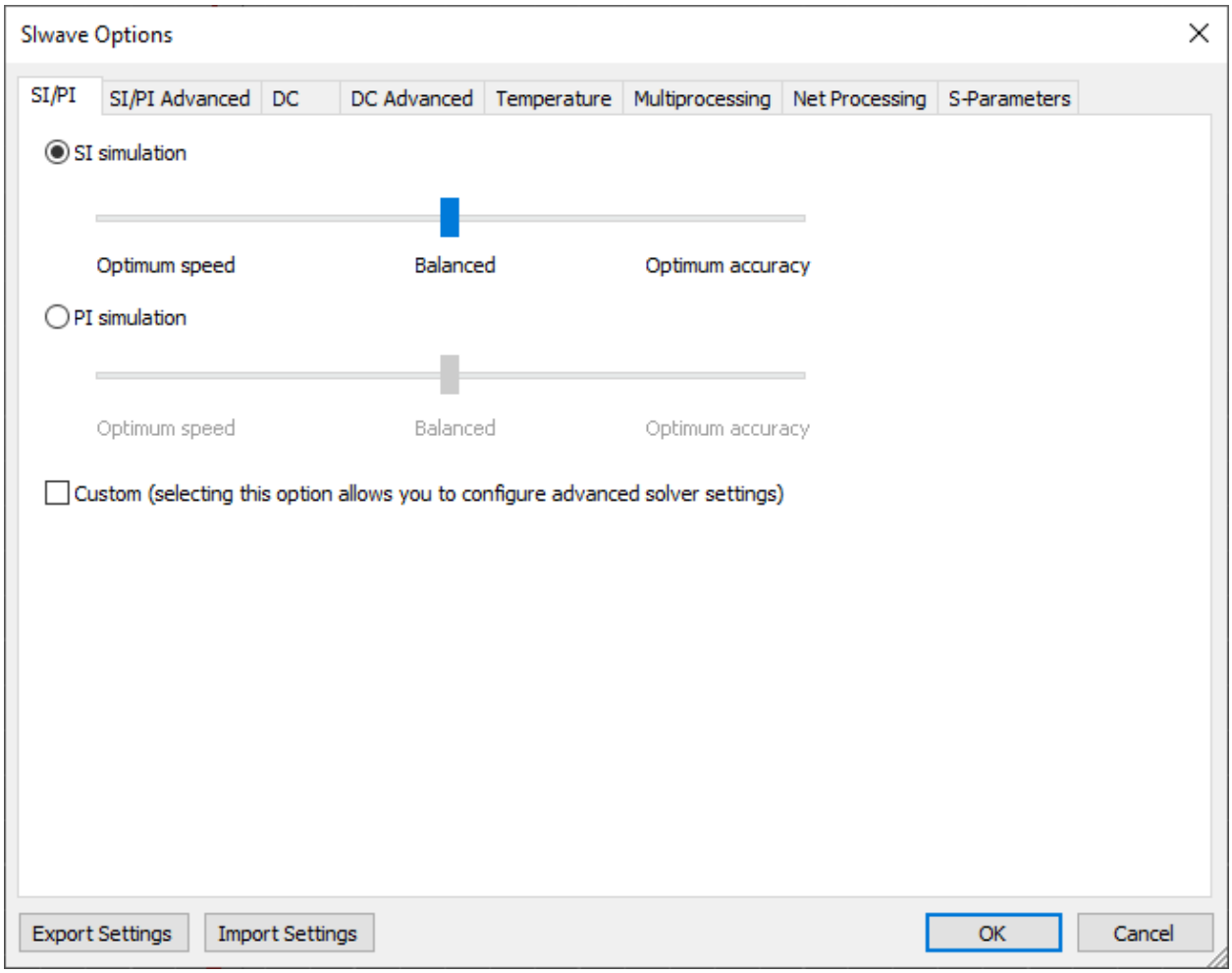

For SI simulations:

- **Optimum speed** means only trace coupling will be selected.
- **Balanced** means trace, coplane, split-plane and Cavity field coupling will also be selected.
- **Optimum accuracy** means trace return current distribution will also be selected.

For PI simulations:

- **Optimum speed** means no coupling options will be selected.
- **Balanced** means Cavity field coupling will be selected.
- **Optimum accuracy** means trace, coplane, and split-plane coupling will also be selected.

4. If appropriate, check the **Custom** check box to configure the advanced solver settings in the **SI/PI Advanced** tab. Some options are always available, while others can be selected only if **Custom** has been selected.
5. Specify the SI/PI advanced options in the **SI/PI Advanced** tab.

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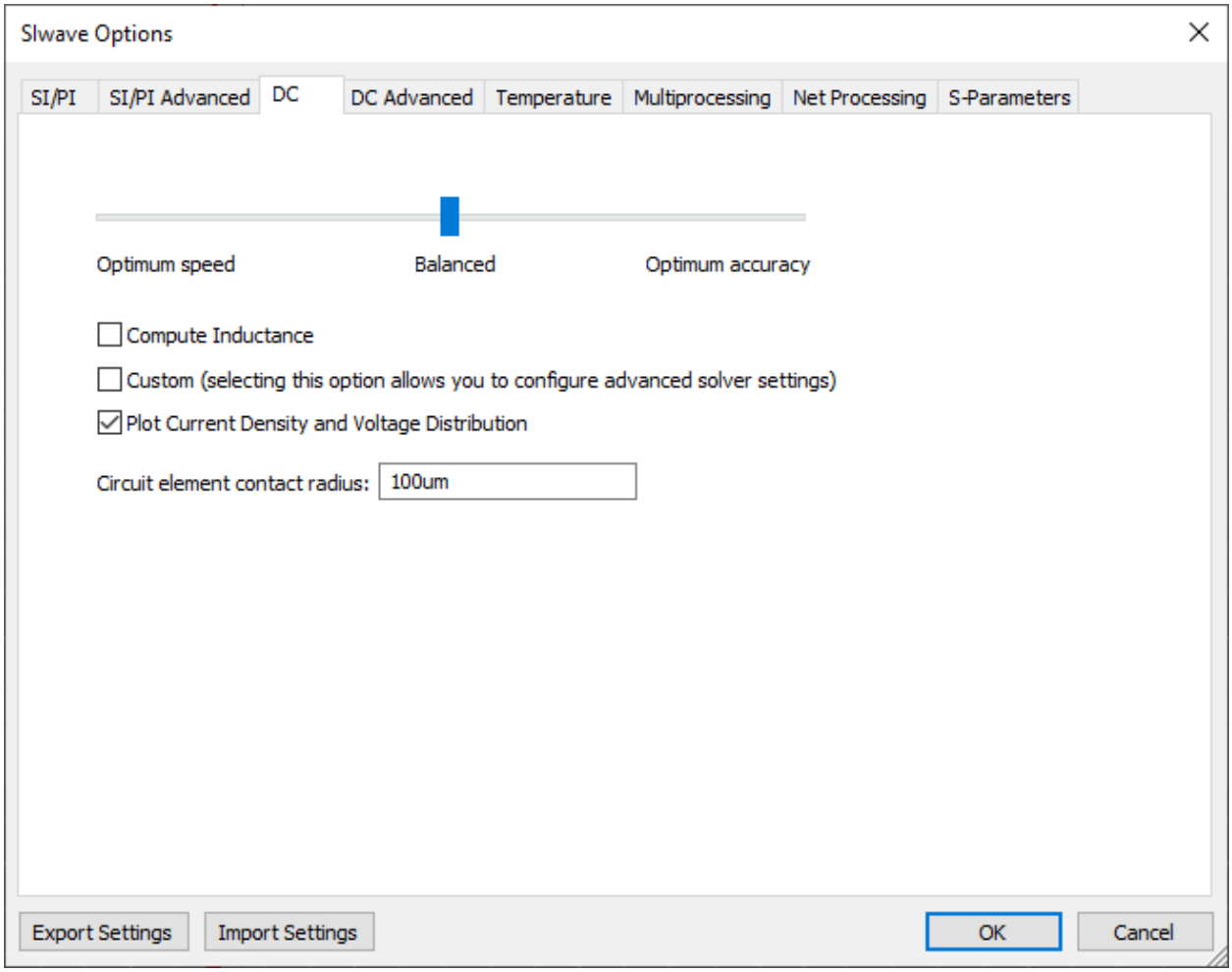
6. Select the **DC** tab.



7. On the **DC** tab:
   a. Move the slider to increase either speed or accuracy.
      - **Optimum speed** – all options in the **DC Advanced** tab are turned off.
      - **Balanced** – the Mesh Bondwires and Mesh Vias options are selected, along with adaptive Mesh Refinement.
      - **Optimum accuracy** – the mesh will be refined on bondwire and vias, and more aggressive refinement parameters will be specified.
   b. Optionally, check **Compute Inductance** to compute the DC inductance. The inductance is computed by integrating the vector potential at DC using an efficient, multi-level fast multipole method with two-level parallelization. In some cases, this may require significant computational time and memory.
   c. Optionally, check **Custom** to configure the advanced solver settings.
   d. Check **Plot Current Density and Voltage Distribution** to display the current density and voltage distribution plots after running the solution. Clear this check box to save disk

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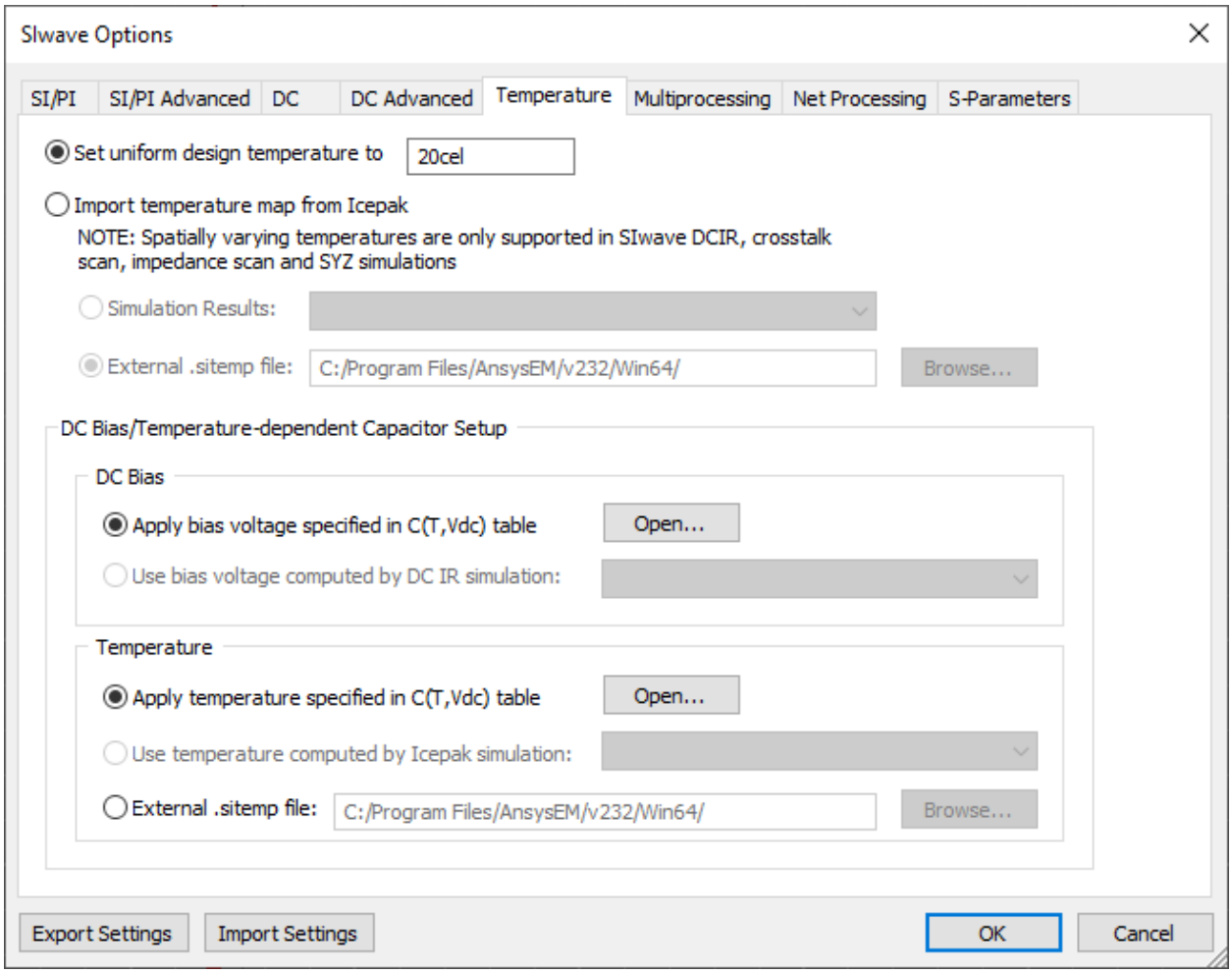
space if you don't need to post-process voltage and current plots (e.g., if you only want to export a SPICE netlist after a DC simulation, it might not be helpful to save any field data to disk).

e. Enter a value in the **Circuit element contact radius** box. Equal potential is enforced within the contact radius, and no mesh refinement is done inside the contact region.

8. Specify the DC advanced options in the **DC Advanced** tab. All options are available only if you have selected the **Custom** check box in the **DC** tab.
9. Select the **Temperature** tab.



From the **DC Bias/Temperature-dependent Capacitor Setup** area, you can apply bias voltage and temperature by selecting either a derating table (in *.csv format) or a previously run simulation.

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> **Note:**
>
> These DC voltage bias and temperature values will only impact simulation results if Murata SPICE (dynamic capacitor models) have been mapped to capacitors in the design that are connected to nets included in the simulation. This mapping can be verified by clicking **Open...** to view the table and ensuring that at least one capacitor part has a checkmark.

If appropriate, specify the **Uniform Design Temperature**, in cels. The temperature specified here is used to bias any dynamic capacitor models and modify metal conductivity during SIwave high-frequency (AC, SYZ, etc.) simulations.

> **Note:**
>
> For temperatures to have an impact on metal conductivity, thermal modifiers must be defined (through the Material Manager) for metals present in the design stackup. See: Assigning Thermal and Spatial Modifiers.

10. Set **Temperature** settings:
    a. Select either **Set uniform design temperature** or **Import temperature map from Icepak**.

       If you choose to set a uniform design temperature, enter its value in Celsius. Temperatures below absolute zero (–273.15C) cannot be simulated.

       If you choose to import a temperature map, you can do using either an Icepak simulation's results, or an external *.sitemp file.

       > **Note:**
       >
       > SIwave prevents users from selecting separate profiles for geometry and capacitors. If a spatially varying profile is selected, this exact profile must be also be applied to dynamic capacitor models. However, selection of uniform design temperature allows one to independently select a spatially varying temperature profile for capacitors.

    b. From the **DC Bias** area, select one of the options:
       - **Apply bias voltage specified in C(T,Vdc) table** – allows you to specify DC bias on a part-by-part basis.
       - **Use bias voltage computed by DC IR simulation** – use the results of a previously computed DC IR simulation.

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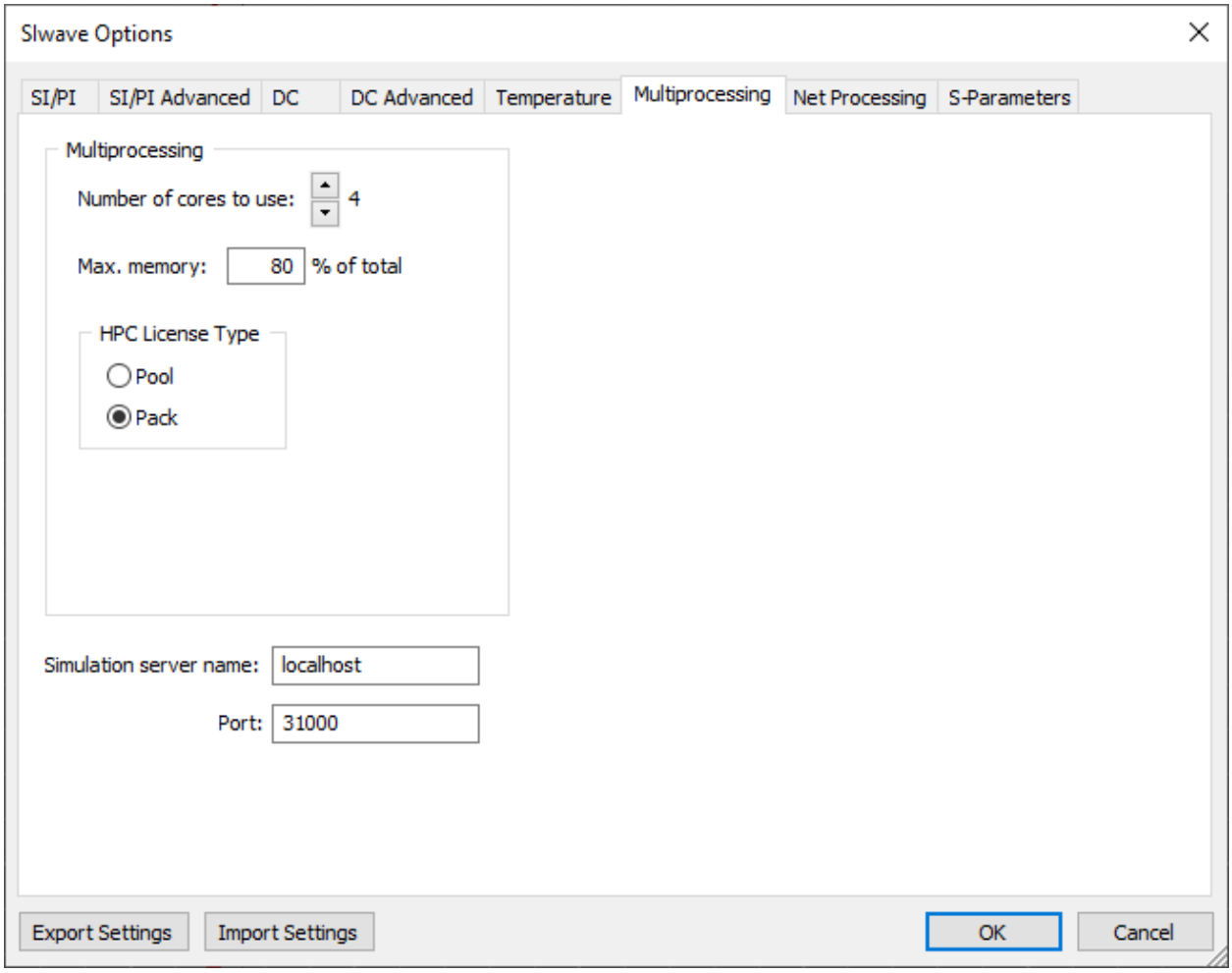
c. From the **Temperature** area, select one of the options:
   - **Apply temperature specified in C(T,Vdc) table** – allows you to specify temperature on a part-by-part basis.
   - **Use temperature computed by Icepak Simulation** – use the results of a previously computed Icepak simulation.
   - **External .sitemp file** – select an external *.sitemp file.

11. If you have more than one CPU, use the **Multiprocessing** tab to configure the system.



12. Set **Multiprocessing** settings:
    a. Set the **Number of cores to use** when computing the solution. This feature is available only if you have purchased the multiprocessing or HPC license option for SIwave.
    b. Select **Use HPC licensing** to enable shared memory multiprocessing.

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c. Select either **Use Ansys HPC licenses** or **Use legacy Electronics HPC licenses**.

> **Note:**
>
> The option to choose a license type (either Ansys HPC or Electronics HPC) is not available when SIwave is running in Pro/Premium/Enterprise licensing mode.

d. For the **HPC License Type**, select **Pool** to use HPC licenses for distribution, or **Pack** to use HPC Pack licenses.
e. **Max. Memory** allows you to set the memory used as a percentage of total RAM. This option is only available if **Use HPC licensing** is selected.
f. From the **Simulation server name** field, specify the name or IP address of the simulation server.
g. Enter the **Port** number. See Remote Solve for details on setting up for remote solves.

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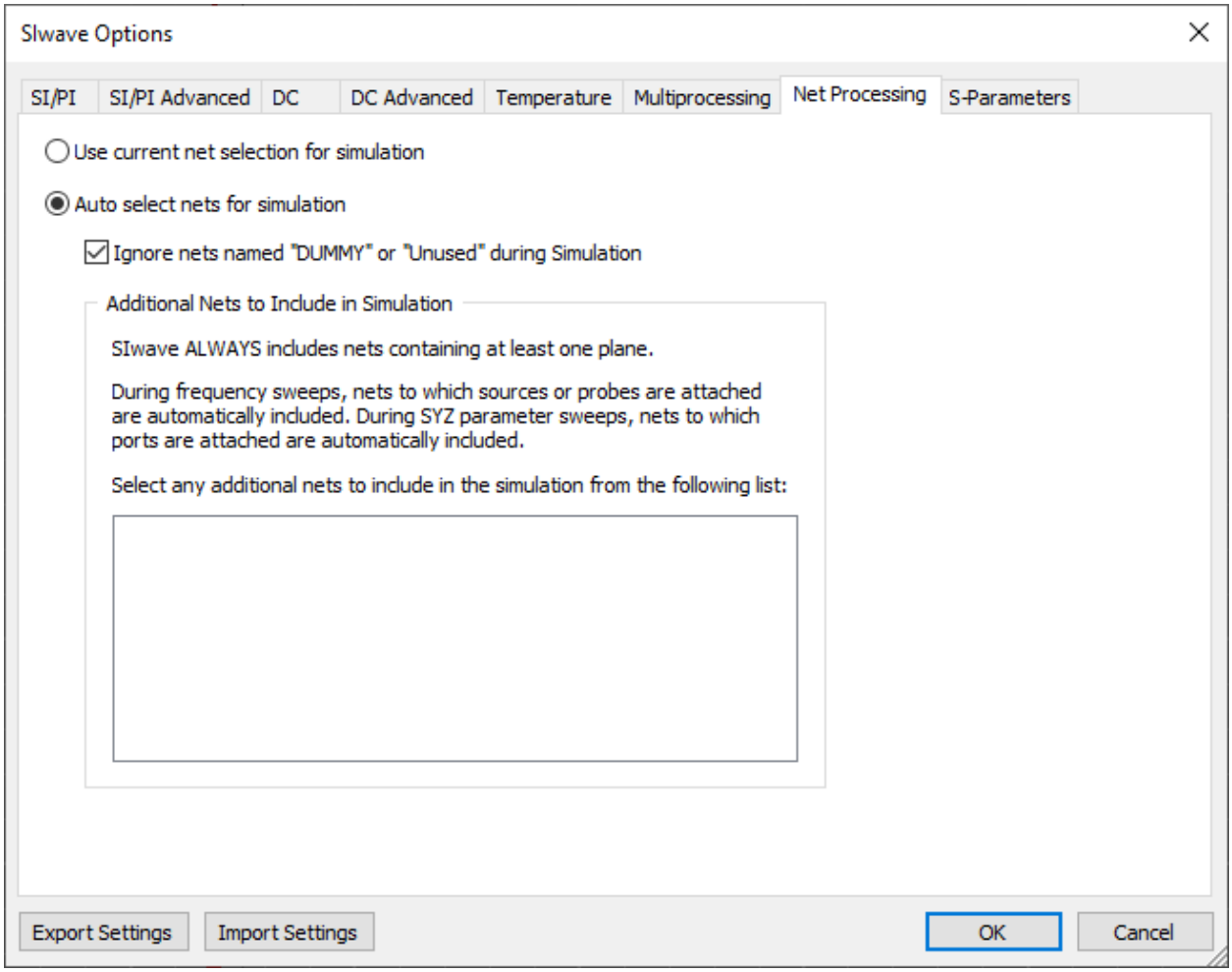
13. Use the **Net Processing** tab to configure net processing.



14. From the **Net Processing** tab, select **use current net selection for simulation** if you want to run a simulation including only the nets that are selected in the **Nets** workspace. Otherwise, leave the default setting of **Auto select nets for simulation**. If you want to include dummy/unused nets in the simulations, clear the **Ignore nets named "DUMMY" or "Unused" during Simulation** check box. By default, these nets are ignored.

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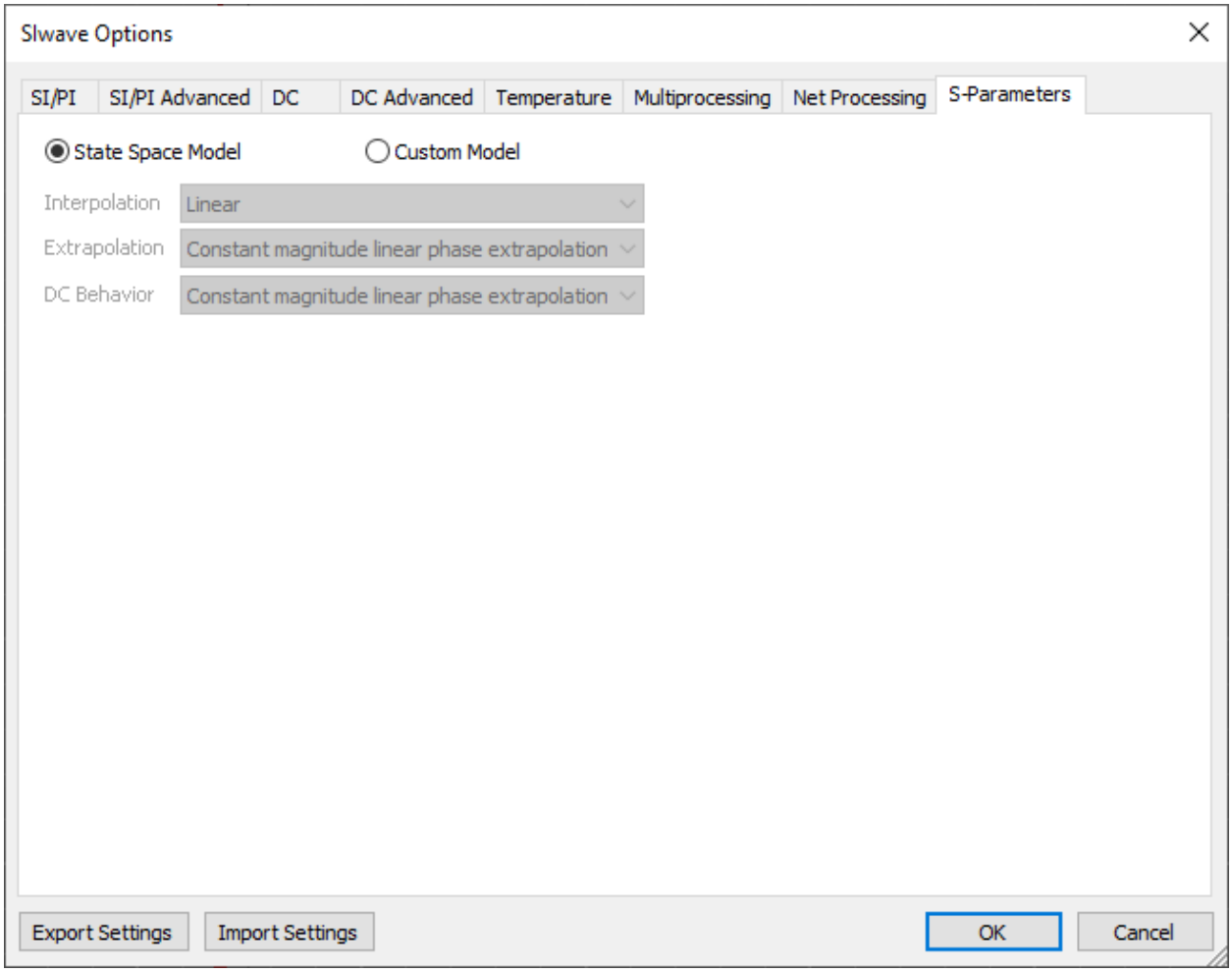
15. Select the **S-Parameters** tab.



16. Select **State Space Model** or **Custom Model**. If **Custom Model** is selected, set the following options:
    - **Interpolation** – select an interpolation method for data points in the frequency range of the Touchstone data. Choose from the following:
        - Point – uses known samples at selected data points to evaluate directly. All requested data points **must** exist.
        - Linear – provides a piecewise linear interpolation from the available data point sample's magnitudes and phases
        - Step – provides a piecewise constant interpolation from the available data point sample's magnitudes and phases. Angle is interpreted in radians and unwrapped before interpolation.
    - **Extrapolation** – select the extrapolation method for data points outside the frequency range of the Touchstone data. Choose from the following:

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- Zero padding – adds zeroes for the magnitude and phase of data points outside of the known frequency range
- Same as last point – adds further data points outside the highest known data point with the same magnitude and phase values
- Linear extrapolation from last 2 points – generates data sample values outside of the known data set based on linear extrapolation of the magnitude and phase of the last two known data points.
- Constant magnitude linear phase extrapolation – estimates the value of unknown data points outside of the known data set by assuming values will remain constant

- **DC Behavior** – select the behavior of the N-Port at DC (zero frequency). Choose from the following:
  - Zero padding – assumes the DC value is real and sets the value to zero
  - Same as last point – assumes the DC value is real and equal to the magnitude of the lowest available data point value
  - Linear extrapolation from last 2 points – assumes the DC value is real and based on the first two available lowest frequency data points
  - Constant magnitude linear phase extrapolation – assumes the DC value is real and equal to the magnitude of the lowest frequency data point, at constant, and the sign determined from the angle of the linear phase extrapolation from the lowest available data point value rounded the nearest multiple of pi
  - Series Capacitor – extrapolates to DC assuming the low frequency behavior matches a capacitor in series
  - Leave all signal lines open circuited – treats DC value as an open circuit. The S-parameter matrix is the identity matrix at DC.

> **Note:** Refer to the following page to use a preconfigured Python script to generate an Ansys ECAD database file, which can then be imported into **Electronics Desktop** to create a custom SIwave setup.

17. Once all settings are specified, click **Export Settings** at the bottom-left side of the window to open an explorer window. Then use the explorer window to navigate to an appropriate directory and enter a name in the **File name** field (e.g., **Test**). Finally, click **Save** to close the explorer window and save the configuration file in the selected directory.

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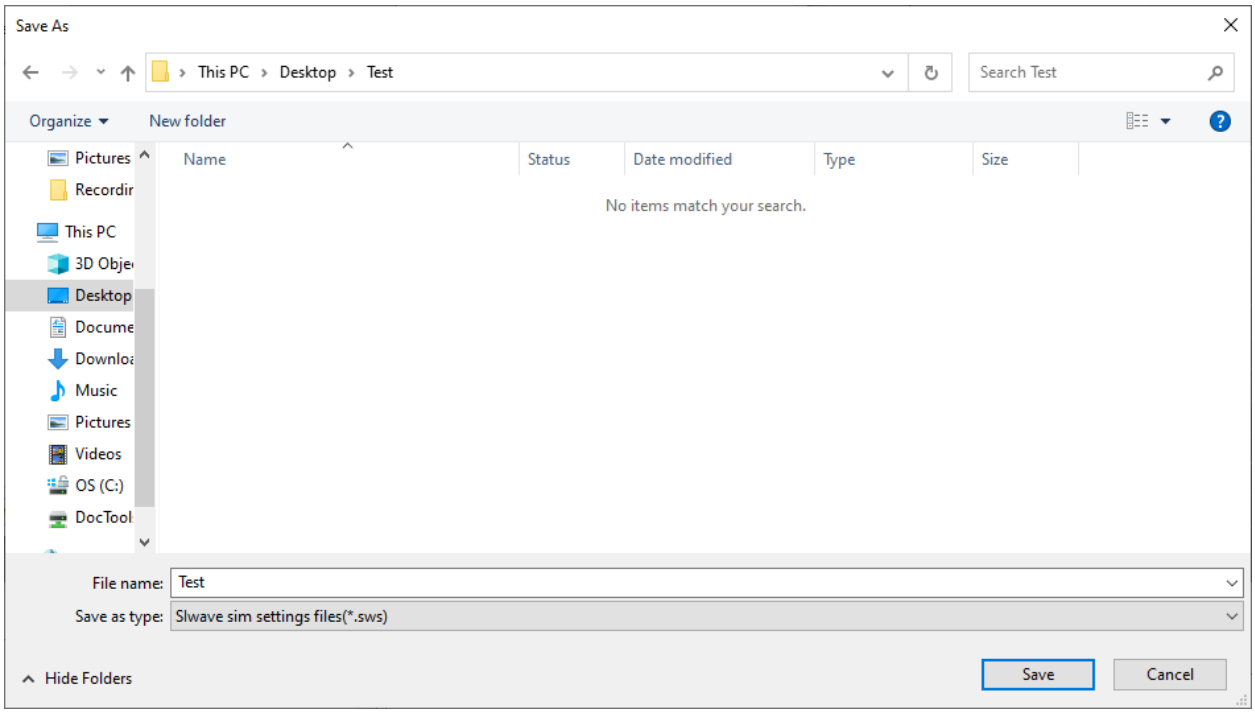

18. Click **OK** to save your settings.

> **Note:** Refer to Using a Python Script to Change an SIwave Solution Setup to generate an Ansys ECAD database file, which can then be imported into **Electronics Desktop** to create a custom SIwave setup.

Selecting SI/PI Advanced Options

To configure advanced SI/PI options for SIwave simulation in SIwave:

1. Click **Simulation**.
2. From the SIwave area, click **Simulation Options**.
3. Select the **SI/PI Advanced** tab.

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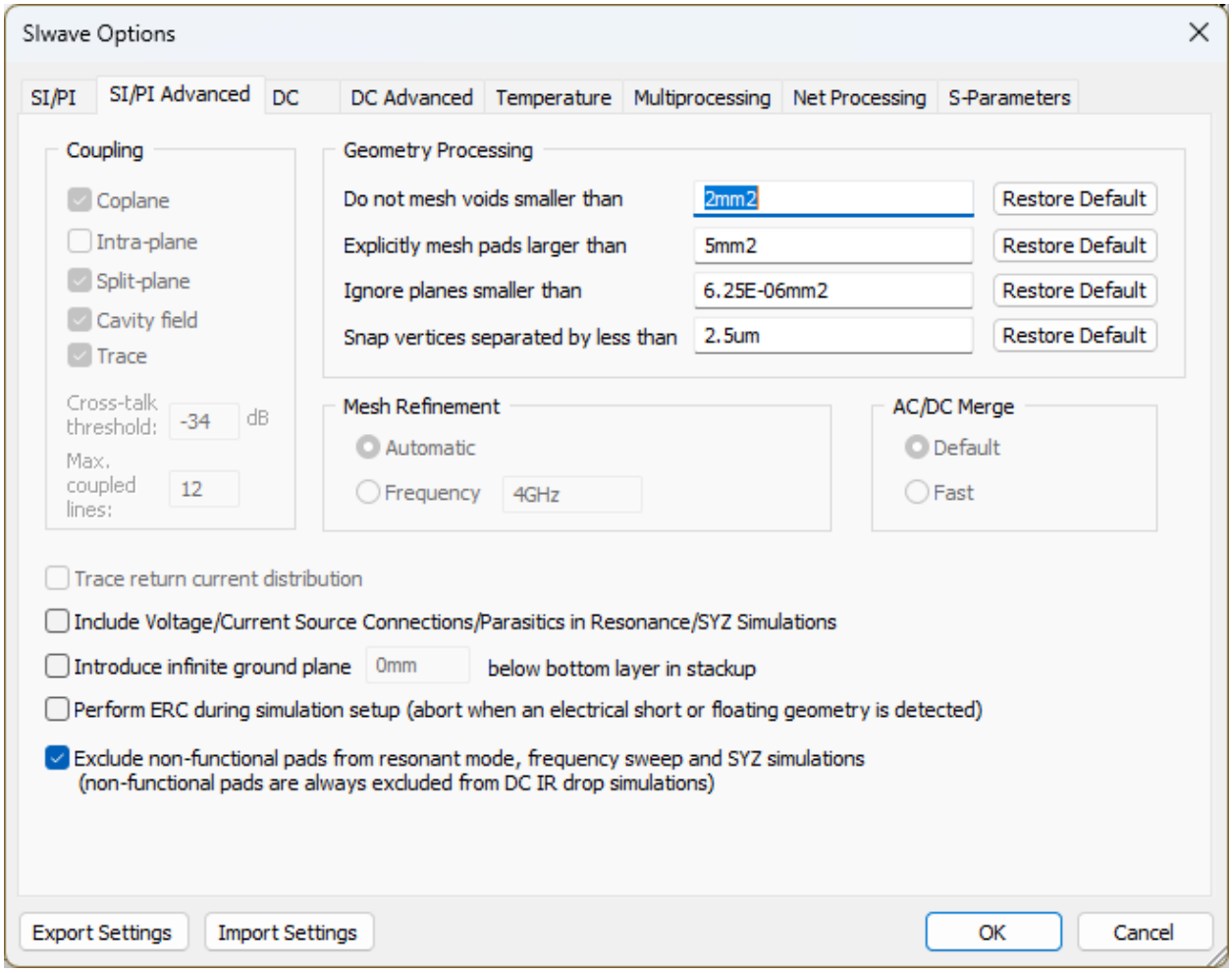

4. From the **Geometry Processing** area, specify plane void meshing values, and control geometry defeaturing and vertex snapping.

> **Note:**
>
> Ansys recommends using the default settings. Refer to Advanced Geometry Processing Options.

5. **Coupling** options are available only if you have selected the **Custom** check box in the **SI/PI** tab:
   - Check **Coplane** to enable coupling between traces and adjacent plane edges. This option provides a model for the crosstalk between signal lines and planes. Plane edges couple to traces when they are parallel. When the solver detects any "trace-like" plane shape, the shape is treated as a trace and the solver checks whether there are nearby coplanes that can couple to it.

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> **Note:**
>
> Traces and coplanar edges which are oblique to each other or do not overlap cannot be considered for coupling.

- Check **Intra-plane** to enforce intra-plane coupling during AC and DC solutions. Intra-plane coupling occurs through metal planes at low frequencies when skin depth becomes greater than the plane thickness. It provides more accurate low frequency solution, but the solver uses more memory and CPU time. Use this option when high accuracy low frequency solution is required (e.g., during log sweep), or when generating FWS models.
- Check **Split-plane** to account for coupling between adjacent parallel plane edges. Primarily, two different cases are being considered: plane edges which form a split and plane edges which form a narrow trace-like plane. The former leads to crosstalk between adjacent planes for which a specific coupling model is applied. For the latter, fringing effects are considered to model accurately the propagation characteristics of trace-like cavities. Further, the coupling between narrow planes is also modeled by enabling this feature.
- Check **Cavity Field** to model the effect of fringe field coupling between stacked cavities.
- Check **Trace** to model coupling between adjacent traces. Coupling is considered for parallel and almost parallel trace segments.

> **Note:**
>
> Coupling features are dependent on each other. Enabling **Split-plane** enables **Coplane** and **Trace**.
>
> Enabling **Coplane** enables **Trace**.

- The **Cross-talk threshold** field is available only if you have selected **SI simulation** and the **Custom** check box on the **SI/PI** tab. Enter a value, in dB. This value specifies the coupling crosstalk threshold, and allows you to control the degree of electromagnetic coupling (trace/coplane/split-plane) included in the simulation. The default value is -34dB. If you decrease it, the simulation will consider more distantly spaced geometry as coupled.

> **Note:**
>
> Simulation time increases when more coupled geometry is included.

- The **Max coupled lines** field is available only if you have selected **SI simulation** and the **Custom** check box on the **SI/PI** tab. **Max coupled lines** is used to limit the size of the coupled multi-conductor transmission line model. Without this limit, the transmission line model could include too many lines satisfying the cross-talk threshold. With this limit, the

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weakest couplings are dropped in order to break the large multi-conductor transmission line model into smaller ones. The default values (12 for optimum speed or balanced simulation, 40 for optimum accuracy) are sufficient in most cases. For special cases, you can specify a value to make sure important couplings are not dropped.

6. The **Trace return current distribution** option is available only if you have selected the **Custom** check box in the **SI/PI** tab. Check this option to accurately model the change of the characteristic impedance of transmission lines caused by a discontinuous ground plane. Instead of injecting the return current of a trace into a single point on the ground plane, the return current for a high impedance trace is spread out.

   The trace return current is not distributed when all traces attached to a node have a characteristic impedance of less than 75 ohms, or if the difference between two connected traces is less than 25 ohms.

7. Check **Include Voltage/Current Source Connections/Parasitics in Resonance/SYZ Simulations** to include the effect of parasitic elements from voltage and current sources.
8. From the **Introduce infinite ground plane** field, specify the elevation of the infinite unconnected ground plane to be placed under the design. The ground plane serves as a voltage reference for traces and planes if they are not defined in the layout.
9. Clear the **Perform ERC during simulation setup** check box to turn off error checking while generating the solver input file. In some designs, the same net may be divided into multiple nets with separate names; these nets are connected at a "star point." To simulate these nets, error checking for DC shorts must be turned off. All overlapping nets are internally united during simulation.
10. Check **Exclude non-functional pads from resonant mode, frequency sweep and SYZ simulations** to remove non-functional pads. All layers in which a via does not make an electrical connection to any other geometry do not contain a pad. By default, non-functional pads are not included in the simulation. Typically non-functional pads are removed when a PCB is manufactured.
11. The **Mesh Refinement** area is available if the **Custom** box is checked on the **SI/PI** tab. This parameter controls how the finite element mesh used in SIwave is generated. You can select from the following options: **Automatic** – automatically picks the suitable mesh refinement frequency. It is dependent on the drawing size, the number of modes, and/or the maximum sweep frequency. This is the recommended option.
    - **Frequency** – allows you to control the mesh size and is based on the effective wavelength of the specified frequency. See Meshing Technical Notes for details.
12. The **AC/DC Merge** area is automatically configured depending on the positions of the SI/PI simulation sliders on the **SI/PI** tab. If **Optimum speed** is selected (from either the SI or PI simulation sliders), **AC/DC Merge** is set to **Fast**. If **Balanced** or **Optimum accuracy** is selected, **AC/DC Merge** is set to **Default**. If the **Custom** box is checked on the **SI/PI** tab, the user can manually select either option:
    - **Default** – Accurately preserves circuit element effects and resonances by converting RLCs to ports, for more accurate results with potentially longer run times. Recommended

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for detailed analysis.

- **Fast** – Corrects the DC-point with minimal extra computation, preserving circuit element effects. Recommended for faster calculations (e.g., when many user-defined resistors or shunt capacitors are involved).

13. Click the **Export Settings** button to save your settings as an SIwave Sim Settings File (*.sws). Click **Import Settings** to browse and select an *.sws file for import.
14. Click **OK** to apply settings.

Selecting DC Advanced Options

To define the DC advanced options for SIwave simulation:

1. Click **Simulation**.
2. From the SIwave area, click **Options**.

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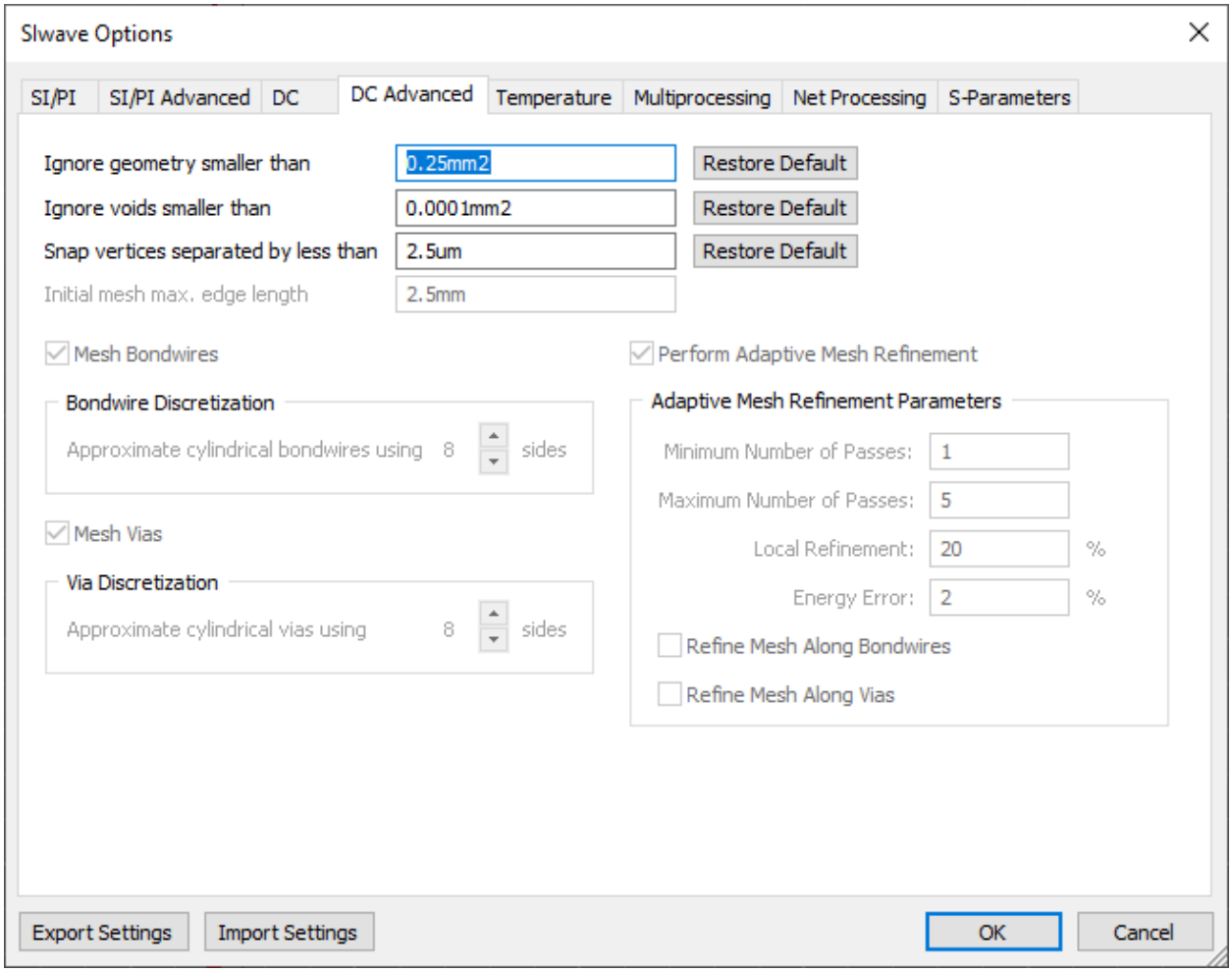
3. Select the **DC Advanced** tab.



> **Important:**
>
> These options are available only if you have selected the **Custom** check box in the **DC** tab.

4. If appropriate, enter a value in the **Ignore geometry smaller than** field. Geometry whose area (after being combined with any overlapping geometry) falls below this specified threshold is ignored during simulation.
5. If appropriate, enter a value in the **Ignore voids smaller than** field. Voids whose area (after being combined with any overlapping geometry) falls below this specified threshold is ignored during simulation.

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> **Note:**
>
> Ansys recommends using the default settings. Refer to Advanced Geometry Processing Options.

6. If appropriate, enter a value in the **Snap vertices separated by less than** field. Entities (e.g., vias) and vertices that are separated by less than the distance specified in this box may be snapped together during solver pre-processing.
7. From the **Initial Mesh Max. Edge Length** field, enter a value in units you specify. This specifies the maximum edge length appropriate in the mesh (before any adaptive refinement occurs).
8. If you do not want to model bondwires as point connections to mesh, check **Mesh Bondwires**. Specify the **Bondwire Discretization** – the number of sides used to approximate cylindrical bondwires. You can specify any value between 6 and 64. The default value is 8.
9. If you do not want to model vias as point connections to mesh, check **Mesh Vias**. Specify the **Via Discretization** – the number of sides used to approximate cylindrical vias. You can specify any value between 6 and 64. The default value is 8.
10. If you want to perform adaptive mesh refinement, check **Perform Adaptive Mesh Refinement** and populate the fields:
    a. Enter the **Minimum Number of Passes**. An adaptive analysis does not stop unless the minimum number of passes you specify has been completed, even if convergence criteria have been met.
    b. Enter the **Maximum Number of Passes**. This value is the maximum number of mesh refinement cycles that you want SIwave to perform. This value is a stopping criterion for the adaptive solution. If the maximum number of passes has been completed, the adaptive analysis stops; otherwise, the adaptive analysis continues unless the convergence criteria are reached.

    > **Note:**
    >
    > The size of the finite element mesh — and the amount of memory required to generate a solution — increases with each adaptive refinement of the mesh. Setting the maximum number of passes too high can result in SIwave requesting more memory than is available or taking excessive time to compute solutions.

    c. Enter the **Local Refinement**. This value determines how many triangles are added at each iteration of the adaptive refinement process. The triangles with the highest error will be refined. The default value is 20%.
    d. Enter the **Energy Error**. The default value is 2%.

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11. If appropriate, check **Refine Mesh Along Bondwires**.
12. If appropriate, check **Refine Mesh Along Vias**.
13. Optionally, use the **Export Settings** button to save your settings as an SIwave Sim Settings File (*.sws). Click **Import Settings** to browse and select an *.sws file for import.
14. Click **OK** to apply settings.

Displaying Surface Plots

SIwave allows you to display surface plots after a computation.

To view plots for a particular solution in SIwave:

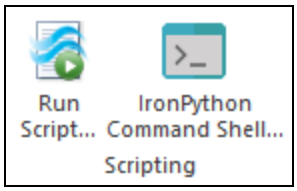
1. Click **View**.
2. From the Show/Hide area, click the **Display Surface Plot** icon ( ). This option is selected by default.
3. From the **Results** window, right-click a simulation and select **Plot Fields**.

Using a Python Script to Configure an SIwave Solution Setup

Complete the steps in either of the following sections to generate an Ansys ECAD database file (i.e., a ***.def** file) via Python script. Then import the newly created custom settings into **Electronics Desktop** to customize an SIwave solution setup.

Running a Python Script

1. From the **Tools** tab, select **Run Script** to open an explorer window.



2. Navigate to an appropriate directory and select the **IronPython Script File** (e.g., **EDB_script_upload.py**).

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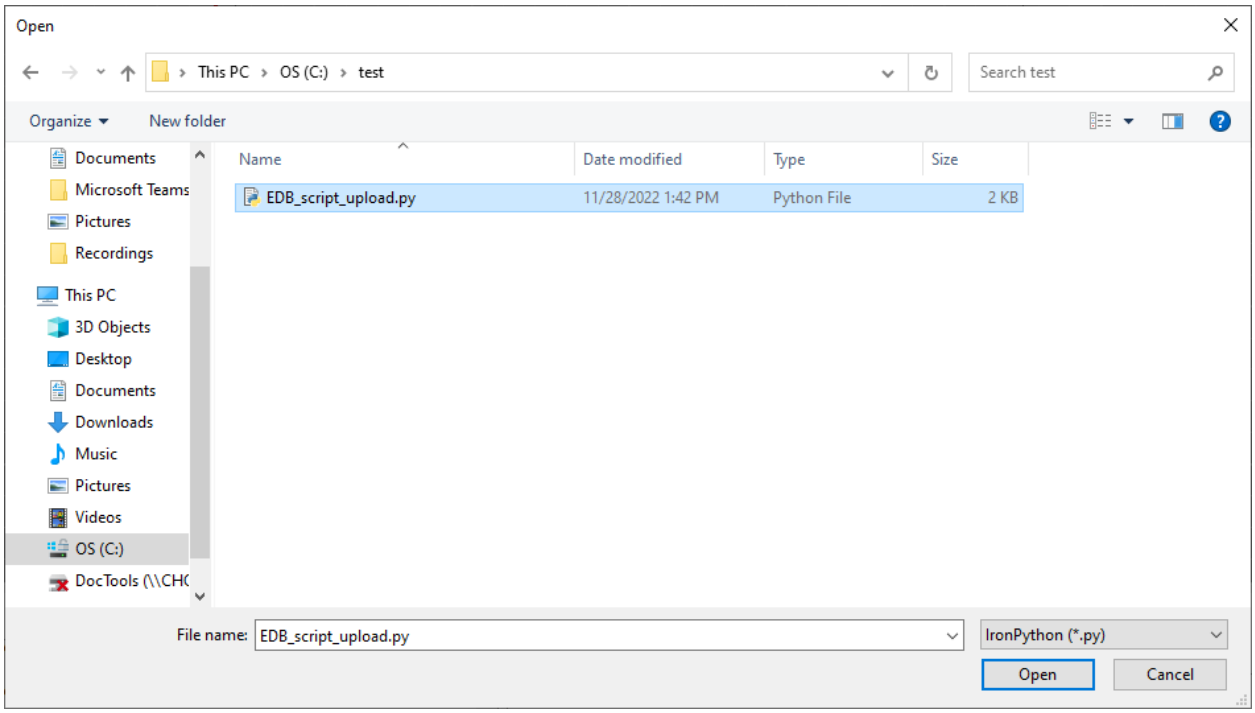

3. Click **Open**. The script generates a new Ansys ECAD database file at the location specified in the script (e.g., `temporaryDirectory = "C:/testDir"`).
4. Open a version of **Ansys Electronics Desktop**.

5. From **File**, select **Import** > **EDB** to open an explorer window.

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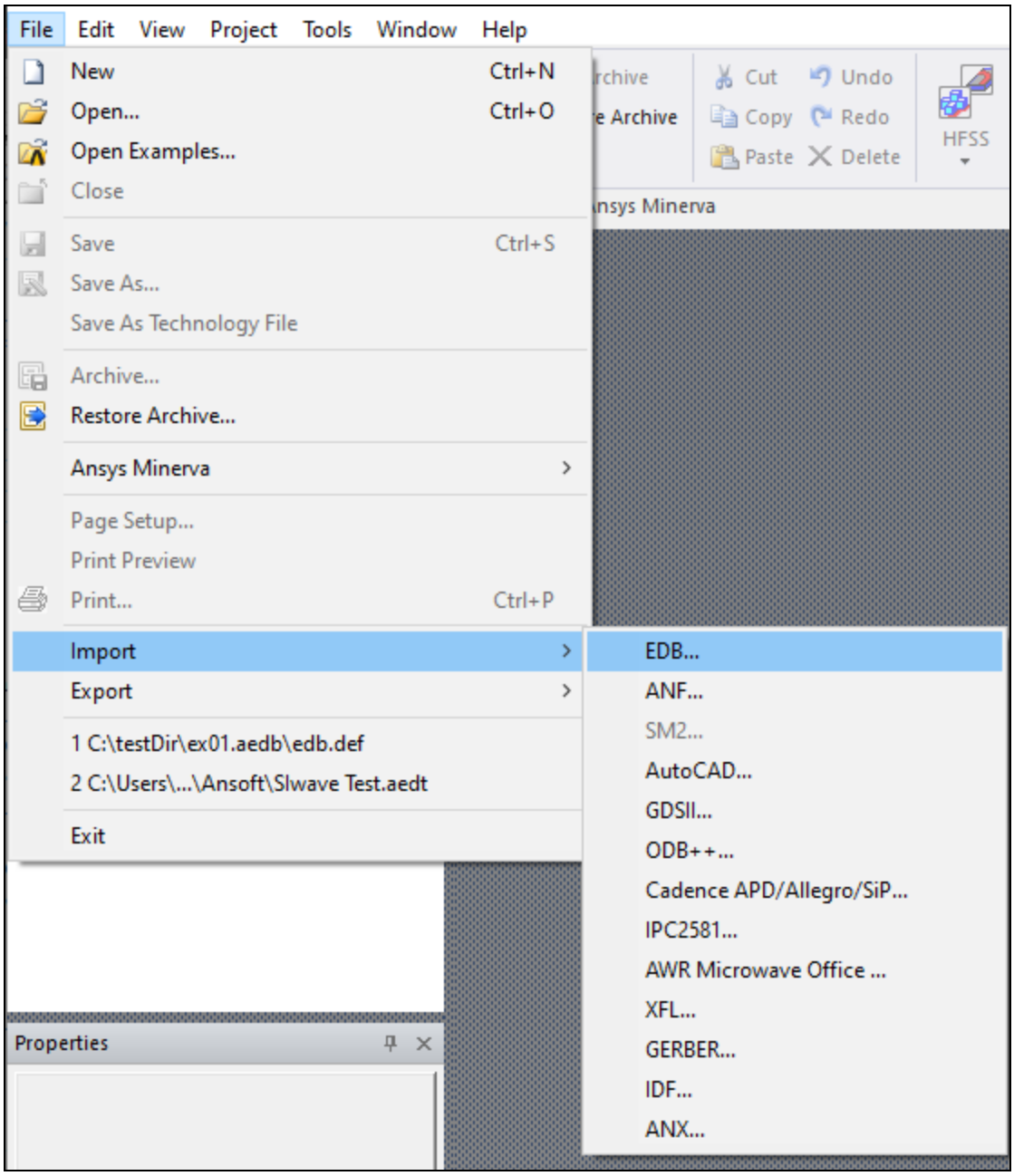

6. Navigate to the directory specified in the script file. Then select the Ansys ECAD database file (i.e., **edb.def**) and click **Open**.

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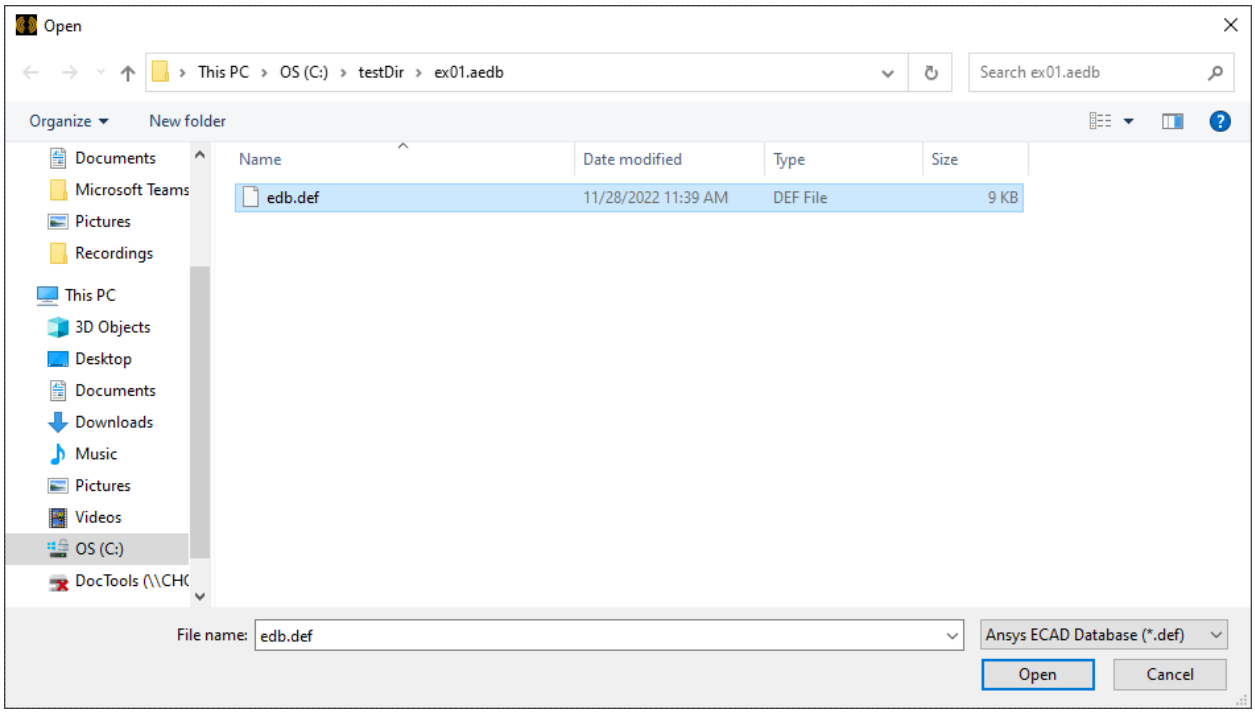
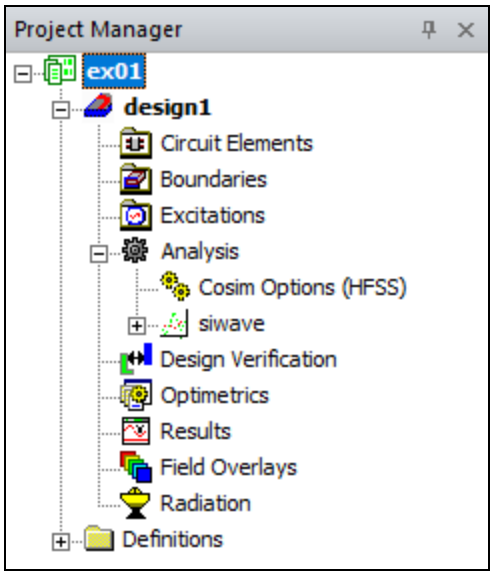


7. The Ansys ECAD database file generates a project configured with the configured settings (e.g., **ex01**), including the SIwave setup (e.g., **siwave**) and custom S-Parameters.



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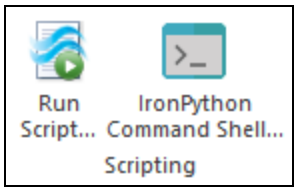
Copying and Pasting Script Commands

1. From the **Tools** tab, select **IronPython Command Shell** to open the **Iron Python Command Window**.



2. Copy and paste (e.g., **Ctrl**+**C**, **Ctrl**+**V**) the script text at the command line. Then press **Enter**.

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IronPython Command Window

```
 - help(obj)  - provides available help on a method or object
 - tutorial() - provides more help on using the console

 try executing "dir(oDesktop)" or dir_sig(oDesktop,"ver")
================================================================

>>> import clr
clr.AddReference('Ansys.Ansoft.CoreDotNet.dll')
clr.AddReference('Ansys.Ansoft.PluginCoreDotNet.dll')
clr.AddReference('Ansys.Ansoft.Edb.dll')
clr.AddReference('Ansys.Ansoft.SimSetupData.dll')
import Ansys.Ansoft.Edb as Edb
import Ansys.Ansoft.SimSetupData as Setup

import os
import tempfile
import shutil
temporaryDirectory = "C:\\testDir"
edbDirectory = os.path.join(temporaryDirectory, 'ex01.aedb')
if os.path.isdir(edbDirectory):
    shutil.rmtree(edbDirectory)
db = Edb.Database.Create(edbDirectory)
cell = Edb.Cell.Cell.Create(db, Edb.Cell.CellType.CircuitCell, 'design1')

siwaveSimSetupInfo = Setup.Data.SimSetupInfo[Setup.Data.SIwave.SIWSimulationSettings]()
siwaveSimSetupInfo.SimulationSettings.DCSettings.DCSliderPos=2
# Use ""Custom Model"
siwaveSimSetupInfo.SimulationSettings.SParamSettings.UseStateSpace = 0
# Interpolation = Point
siwaveSimSetupInfo.SimulationSettings.SParamSettings.Interpolation=Setup.Data.SIwave.SIWSParamSettings
.SParamInterpolation.kPointIn
# Extrapolation = Zero padding
siwaveSimSetupInfo.SimulationSettings.SParamSettings.Extrapolation=Setup.Data.SIwave.SIWSParamSettings
.SParamExtrapolation.kZeroEx
# DC Behavior = Leave all signal lines open circuited
siwaveSimSetupInfo.SimulationSettings.SParamSettings.DCBehavior=Setup.Data.SIwave.SIWSParamSettings.SP
aramDCBehavior.kOpenDC
siwaveSimSetupInfo.Name = "siwave"
sweep = Setup.Data.SweepData('Sweep1')
sweep.IsDiscrete = False
sweep.RelativeSError = 0.001
sweep.Frequencies.Clear()
sweep.SetFrequencies('0GHz', '20GHz', 1001)
sweep.Enabled = True
siwaveSimSetupInfo.SweepDataList.Add(sweep)
siwaveSimulationSetup = Edb.Utility.SIWaveSimulationSetup(siwaveSimSetupInfo)
cell.AddSimulationSetup(siwaveSimulationSetup)

db.Save()
db.Close()
>>>
```

3. The script commands generate a new Ansys ECAD database file at the location specified in the script (e.g., **`temporaryDirectory = "C:/testDir"`**).
4. Open a version of **Ansys Electronics Desktop**.

5. From **File**, select **Import** > **EDB** to open an explorer window.

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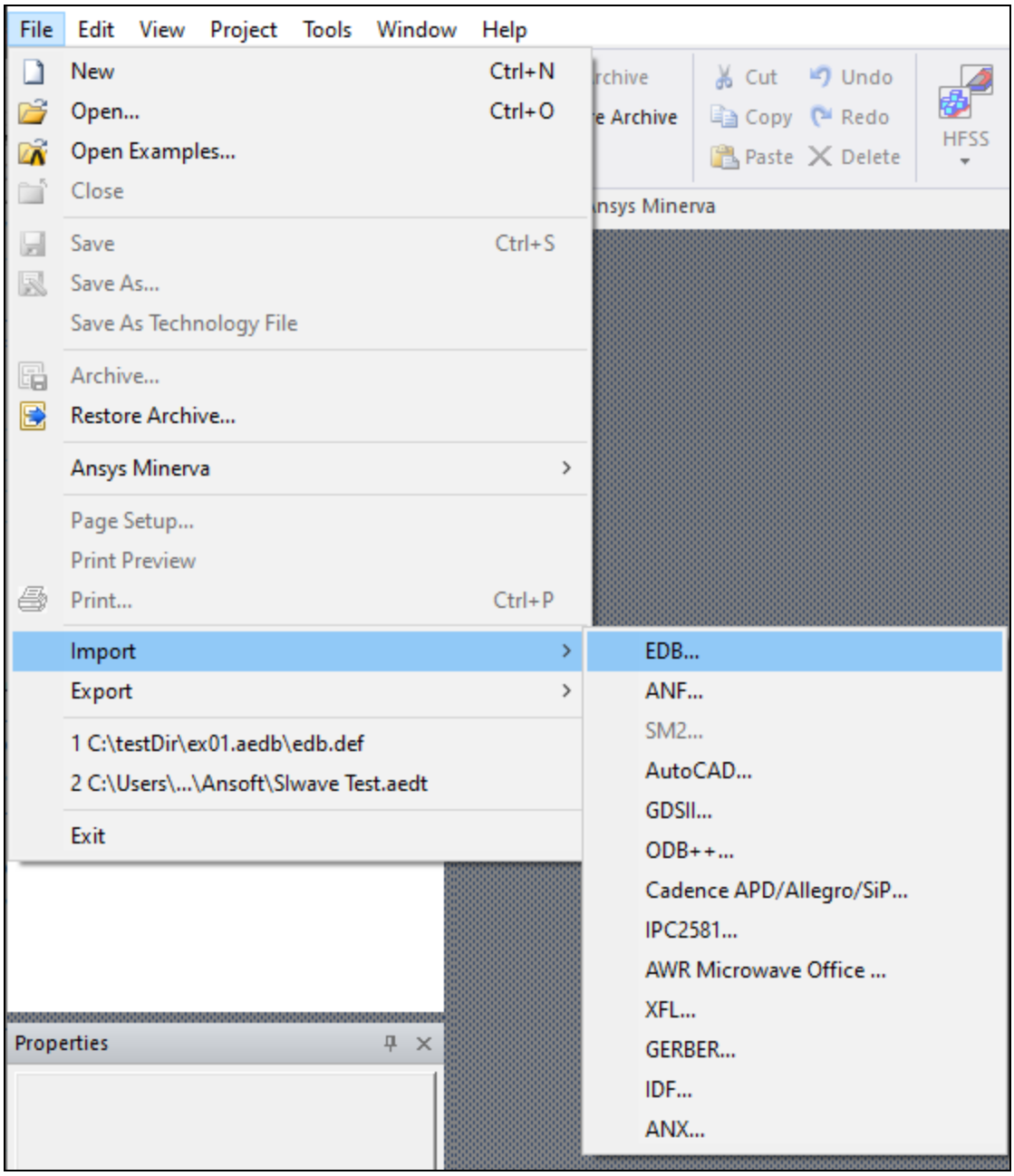

6. Navigate to the directory specified in the script file. Then select the Ansys ECAD database file (i.e., **edb.def**) and click **Open**.

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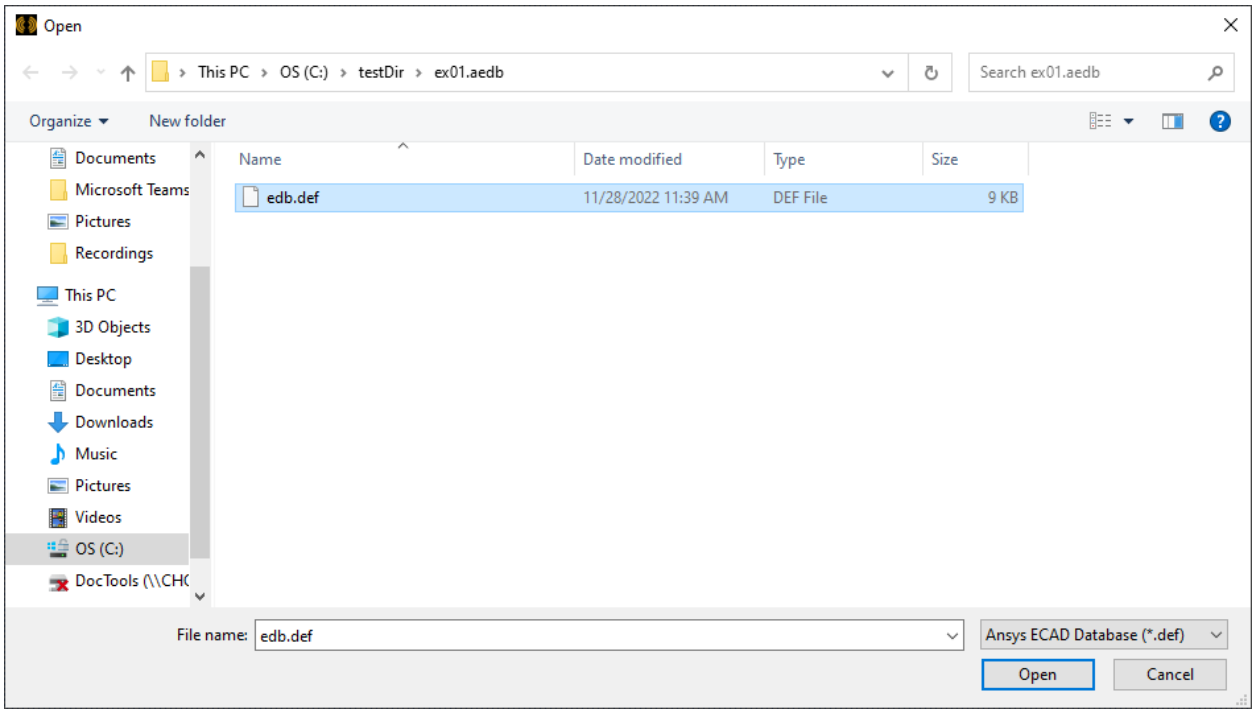
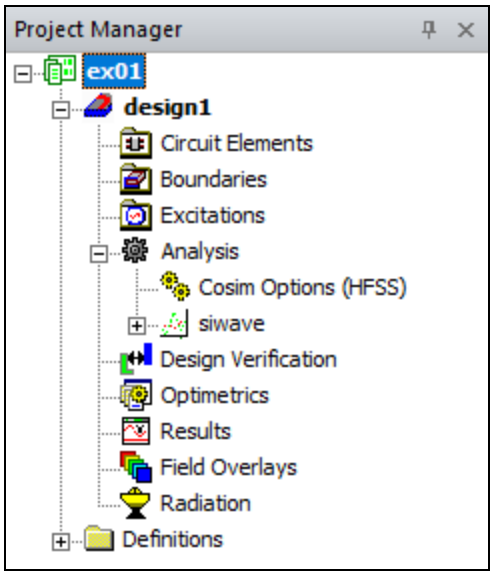


7. The Ansys ECAD database file generates a project configured with the configured settings (e.g., **ex01**), including the SIwave setup (e.g., **siwave**) and custom S-Parameters.



Computing Resonant Modes

PCB or IC packages that contain power/ground plane structures can—at certain frequencies—exhibit resonances in the cavities formed between power and ground planes. Resonant mode

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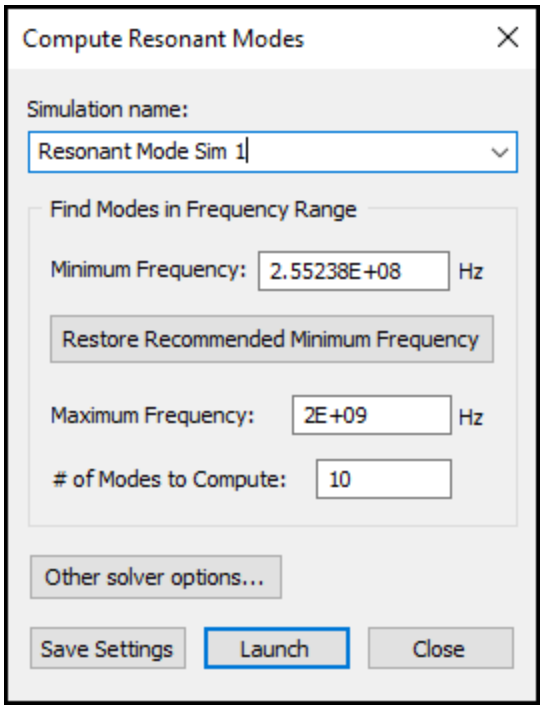
analysis solves for these frequency-dependent voltage swings between layers of a PCB or multi-layer package. The resonant frequencies correspond to peaks in the impedance response of the PCB or package. The best way to view the natural resonances (and to what extent electromagnetic energy sources excite them) is to model the entire structure. See: Resonant Modes.

To compute resonant modes in SIwave:

1. Click **Simulation**.
2. From the SIwave area, click **Compute Resonant Modes**.

   The **Compute Resonant Modes** window appears.



3. From the **Simulation name** field, enter a name for the simulation.
4. From the **Find Modes in Frequency Range** area, enter a value for the **Minimum Frequency**.

   A recommended value is already populated for you. If you change the value and want to return to the recommended value, click **Restore Recommended Minimum Frequency**.

   This is calculated using:

$$\frac{c}{\left(\left(\sqrt{\mathrm{maxPermittivity}}\right)\times 2\times L\right)}$$

   In this formula:

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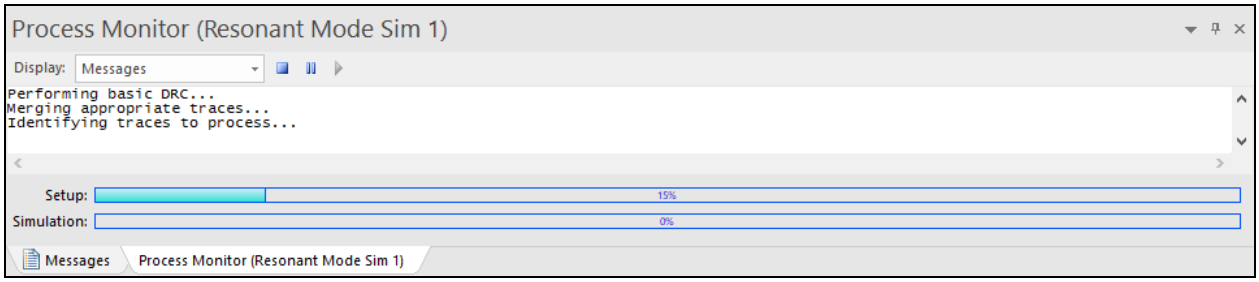
- L is the diagonal distance (in meters) of the geometry bounding box
- c is the speed of light (in m/s)
- maxPermittivity is the maximum relative permittivity of the dielectric layers in the stackup

5. If appropriate, enter a value for the **Maximum Frequency**.
6. Specify the **# of Modes to** compute. The modes indicate the frequencies at which the cavity responds very strongly. This determines the voltage pattern between the top and bottom planes.

> **Note:**
>
> If both the **Maximum Frequency** and the **# of Modes to** compute are given values, the Eigen solver terminates when either of the two conditions is met.

7. To change SIwave simulation options, click **Other solver options**.
8. Click **Save Settings** to keep your settings.
9. Click **Launch** to begin computing resonant nodes.

   The **Messages** window opens a Process Monitor tab that displays the progress.



Viewing Resonant Modes

To view resonant modes analysis results in SIwave:

1. Click **Results**.
2. From the SIwave area, use the **Resonant Mode** drop-down menu to select **[Simulation Name]** > **View Results**.

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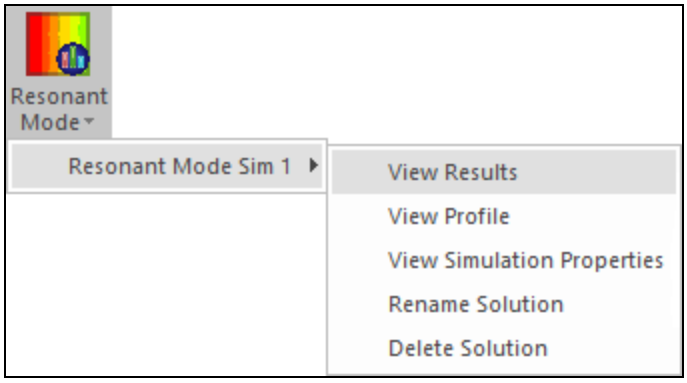
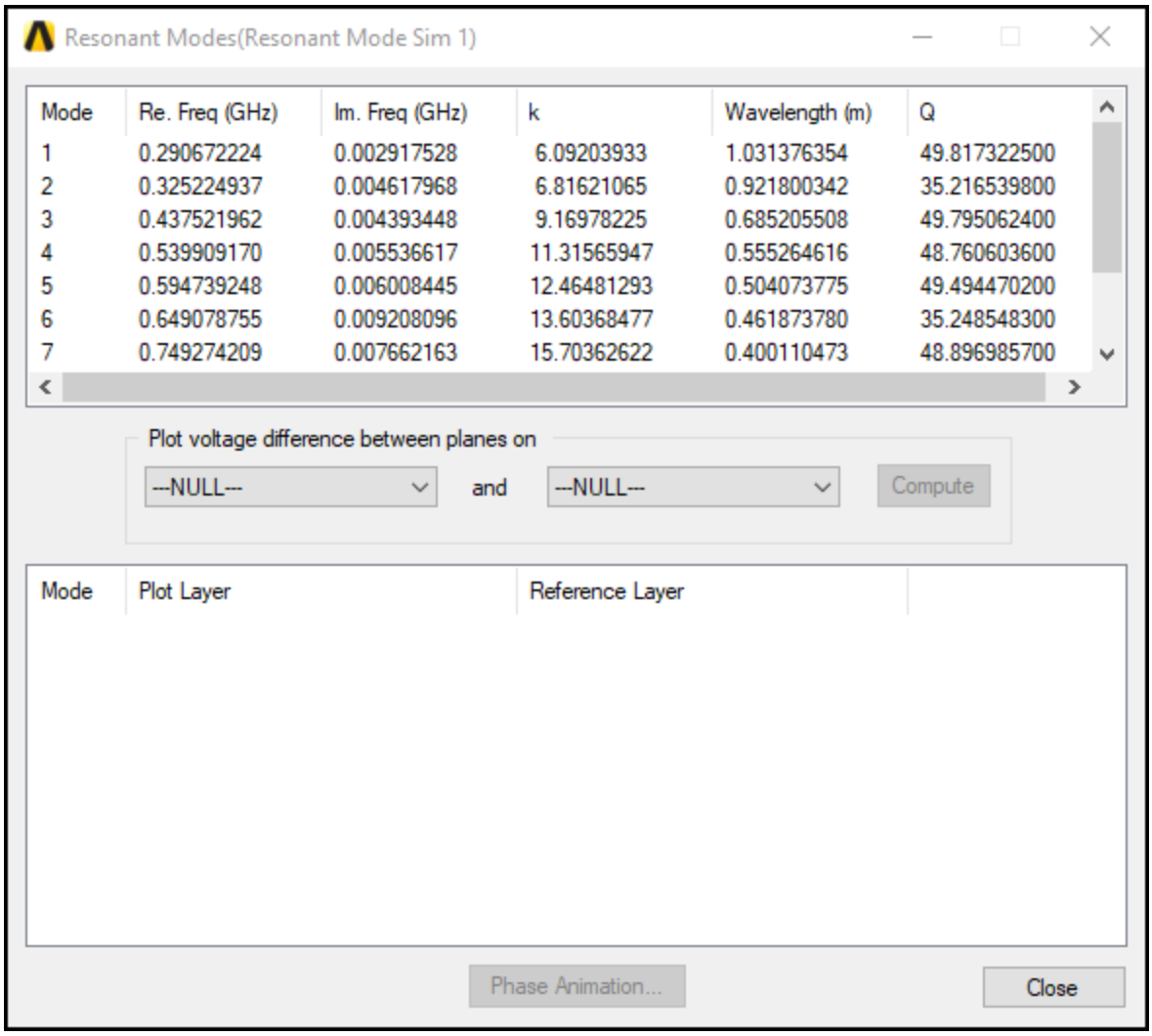


The **Resonant Modes** window appears.



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3. Select a mode from the list at the top. For more information on how the free space wave number (k) and quality factor (Q) are calculated, see Resonant Frequencies.
4. Use the **Plot voltage difference between planes on** drop-down menus to select metal layers between which voltage difference is to be viewed.
5. Click **Compute**.

   The **Messages** window displays the progress. When the process finishes, results are displayed in the Modeling Workspace and at the bottom of the **Resonant Modes** window.

   To view the resonant mode simulation profile in SIwave:

6. Click **Results**.
7. From the SIwave area, use the **Resonant Mode** drop-down menu to select **[Simulation Name] > View Profile**.

   The profile appears.

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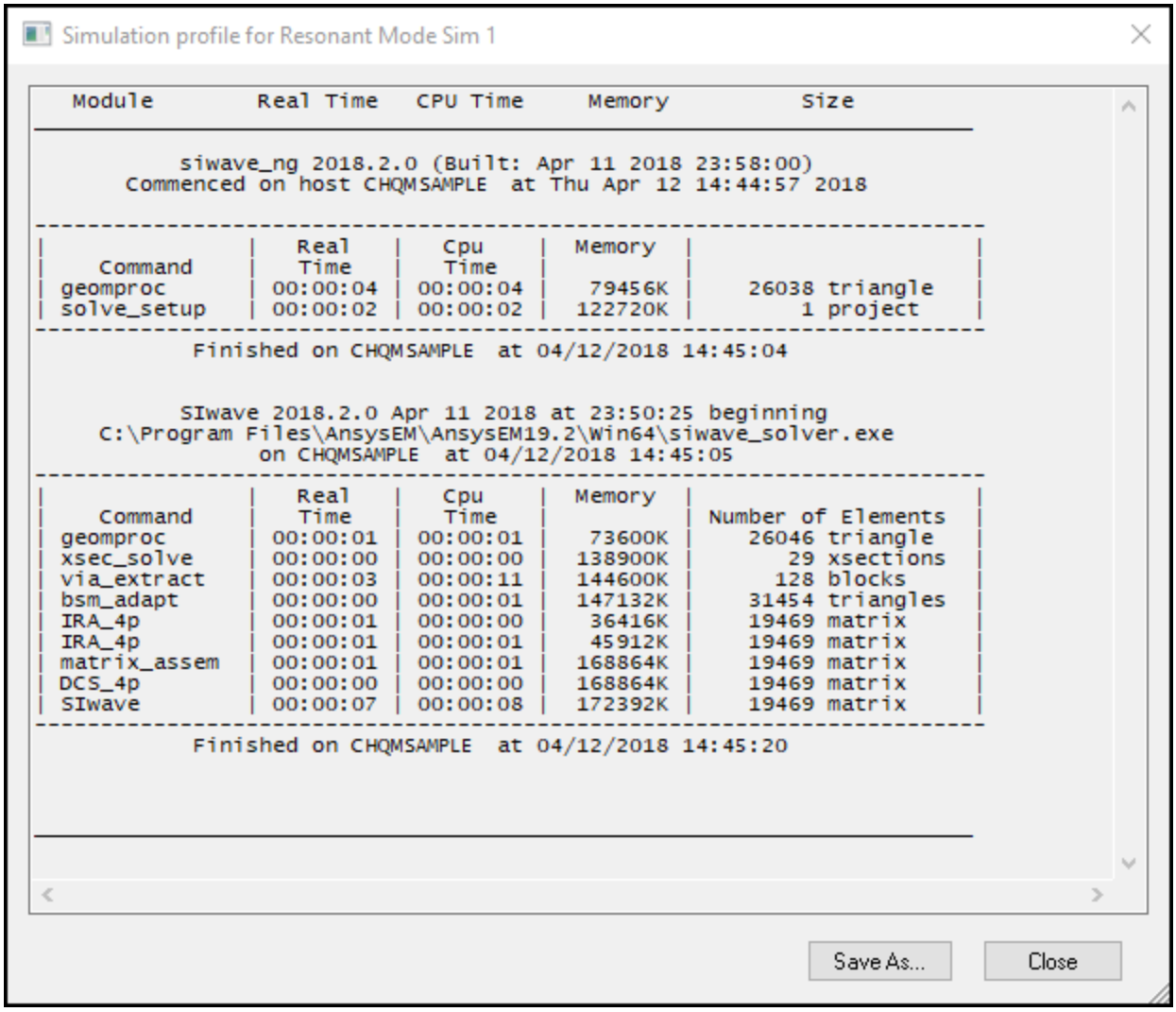

8. Click **Save As** to save the profile as a text file (*.txt).
9. Click **Close** to close the profile.

To view the resonant modes simulation properties:

1. From the **Results** window, right-click the simulation name and select **View Simulation Properties**.

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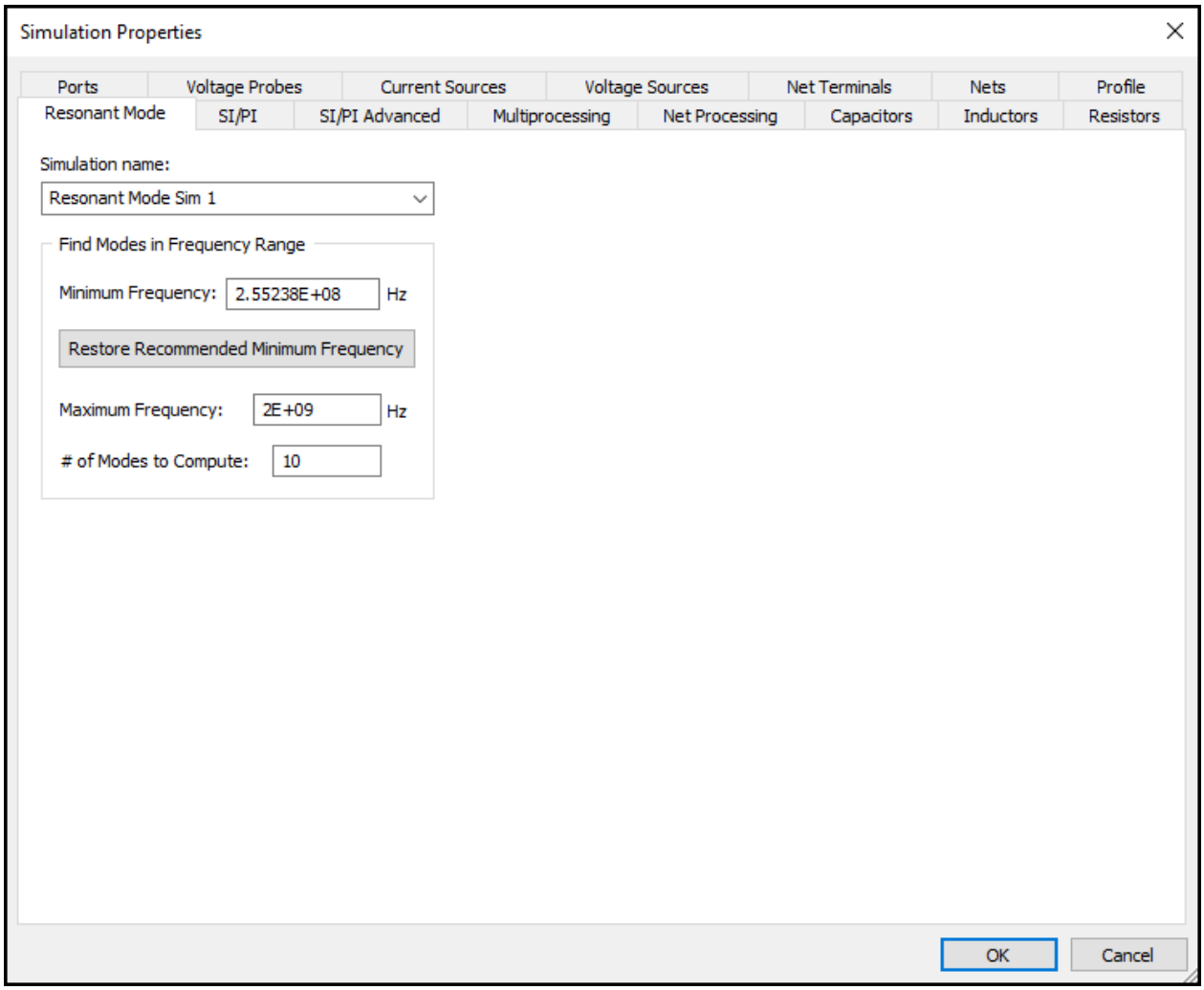
The **Simulation Properties** window appears, with the **Resonant Mode** tab selected.



To delete a resonant modes solution:

1. From the **Results** window, right-click the simulation name and select **Delete Solution**.

Viewing the Phase Animation

When you have finished computing resonant modes, you can view the phase animation.

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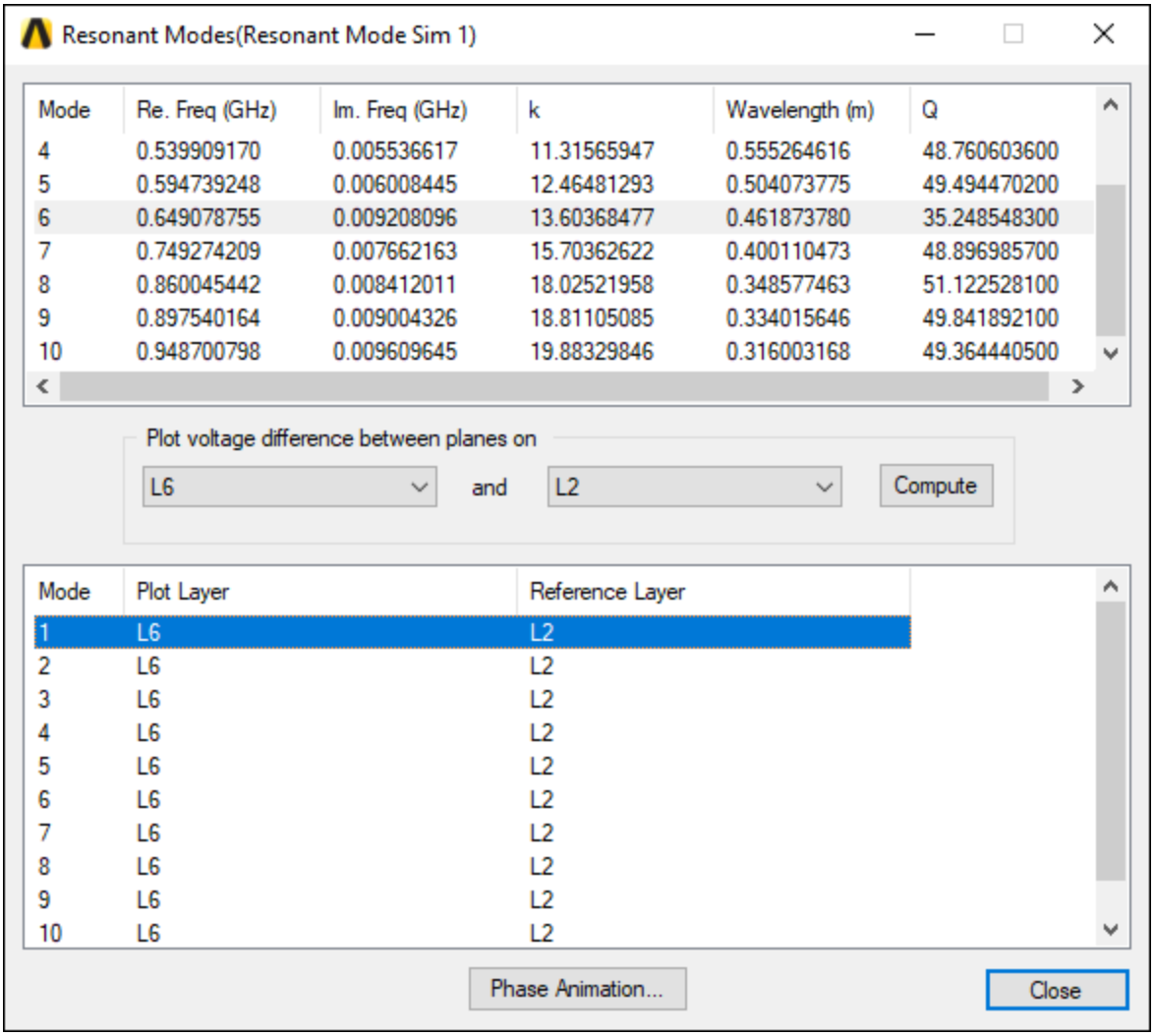

To view the phase animation:

1. Click **Phase Animation**.

   The **Phase Animation** window appears.

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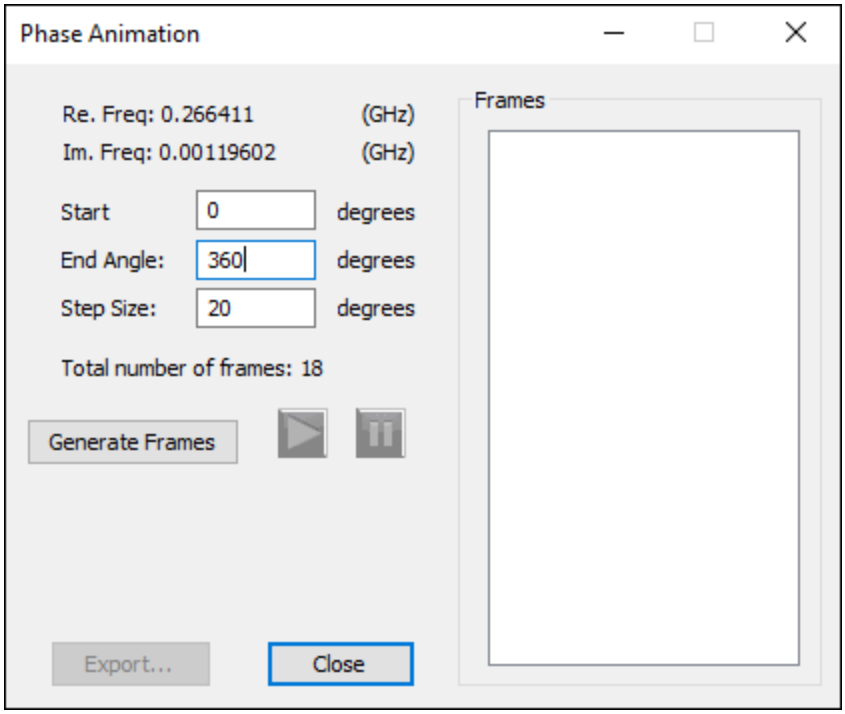

2. Enter an appropriate **Start Angle**, **End Angle**, and **Step Size**, in degrees.
3. Click **Generate Frames**.

   The frames are generated according to the values entered, and appear in the Frames area.

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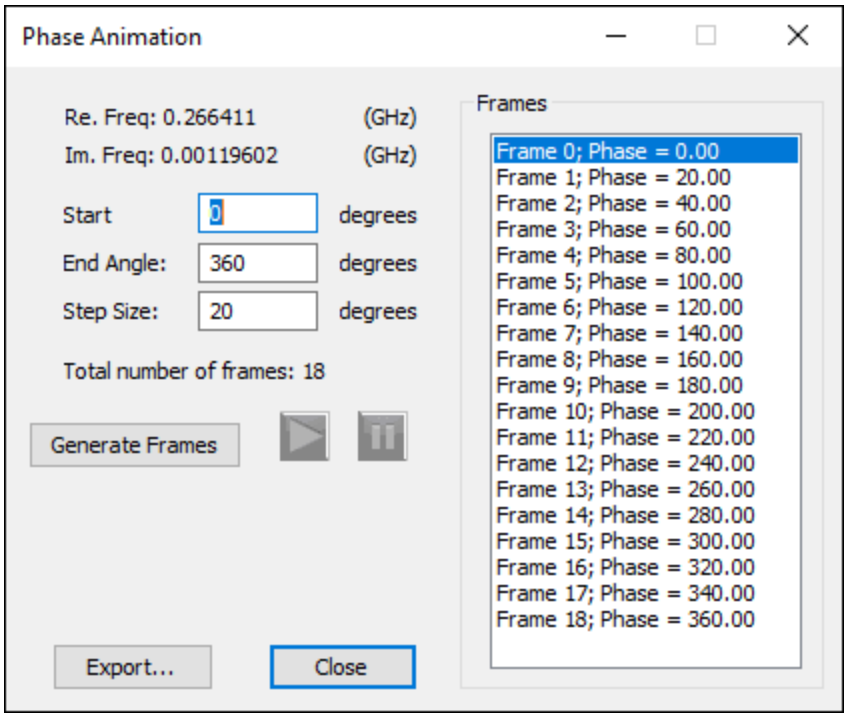

To view the frames as an animation in the Modeling workspace:

1. Click **Play** ( ) to begin the animation.
2. Click **Pause** ( ) to stop the animation.
3. Click **Close** to exit.

You can also export the animation to an ***.avi** or ***.gif** file.

Exporting the Phase Animation

From the Phase Animation window, you can export an *.avi or *.gif of the resonant modes analysis.

To export the animation from the Phase Animation window:

1. Click **Export**.
2. Select a file name and location.
3. From the **Save as Type** drop-down menu, select either **GIF Animation Files (*.gif)** or **Audio-Video Inteleave Files (*.avi)**.
4. Click **Save**.

   The **Animation Options** window appears.

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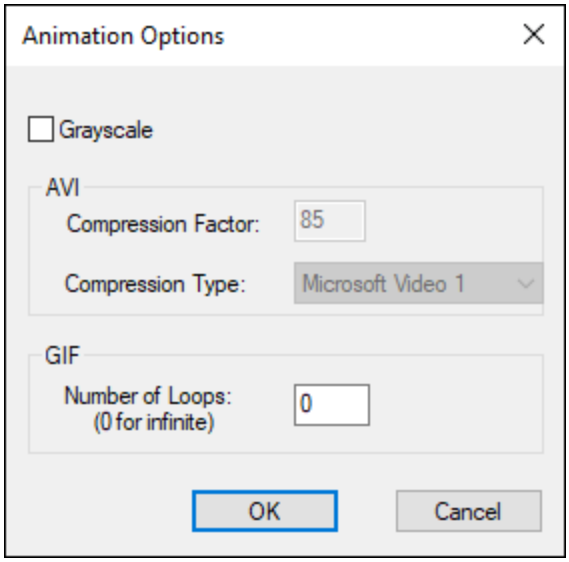

5. To replace colors in the file with 256 shades of gray, check the **Grayscale** check box. Grayscale animations use less memory than full color animations.
6. For **.avi** files:
   a. Specify the **Compression Factor**.
   b. Use the **Compression Types** drop-down menu to select from the following: INTEL Indeo, Cinepak, Microsoft Video 1, or None.
7. For **.gif** files, specify the number of times you want to play the animation in the **Number of Loops** box. The default (0) loops indefinitely.
8. Click **OK**.

   The animation is exported to the specified format.

Computing Frequency Sweep

Frequency sweep analysis allows you to evaluate the effects on the voltage and current distribution of applied AC voltage and current sources on your design across a specified frequency range. In a sweep operation, the frequency of the sources is swept from a minimum value to a maximum value. You can set the start frequency, stop frequency, and number of frequency points used. The analysis can use voltage/current sources defined in SIwave, or sources accessed via push excitations from Ansys Electronics Desktop.

Results are expressed graphically with the use of frequency response plots. Frequency responses show how the amplitude and phase of user-defined voltage probes change with different frequencies. The software also displays a 3D plot of the magnitude of the voltage difference between a specified pair of planes.

During a frequency sweep, voltage and current sources remain active, and all ports are ignored.

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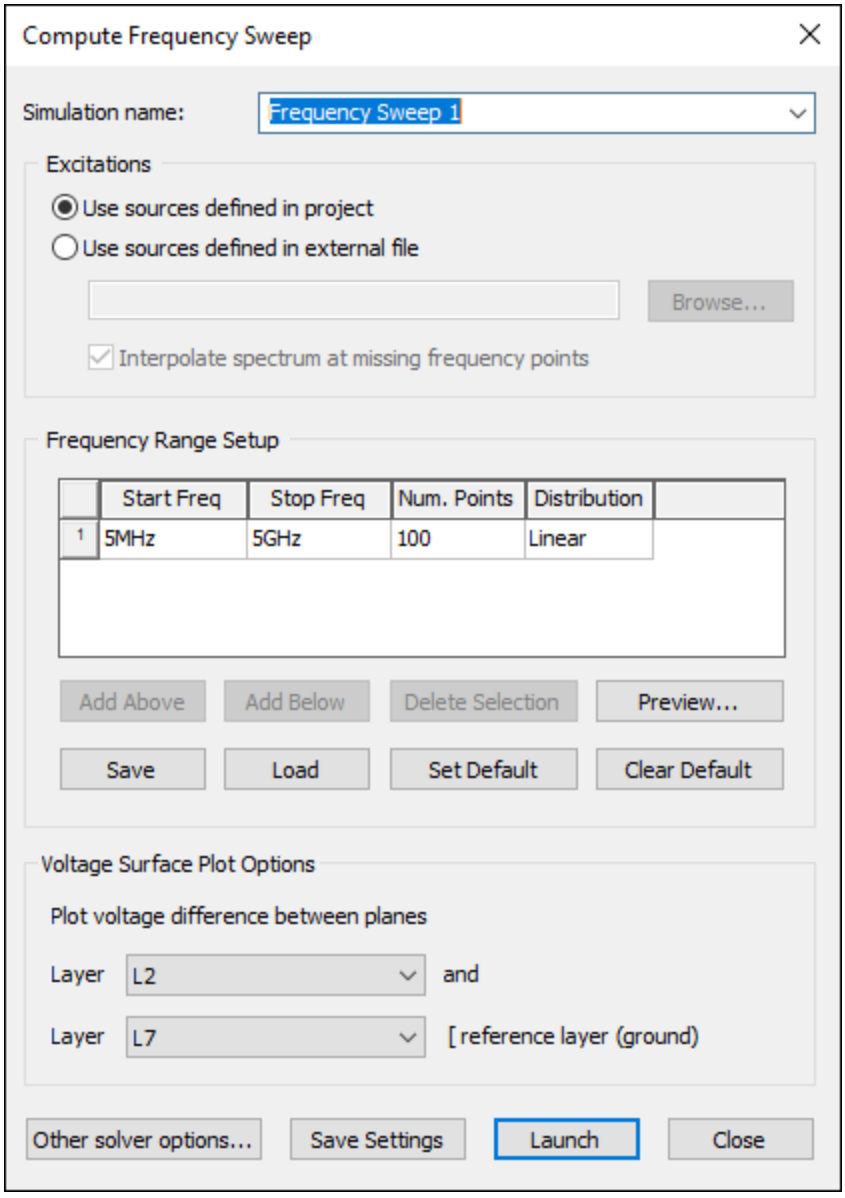
To generate a frequency sweep:

1. Click **Simulation**.
2. From the SIwave area, click **Compute Frequency Sweeps**.

   The **Compute Frequency Sweep** window appears.



3. Specify the source of the excitations. You can select one of the following options:

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- **Use sources defined in the project**
- **Use sources defined in an external file**. Click **Browse**and locate the external source file. This file specifies the ports at which the frequency dependent sources will be attached. If an external file is used, any sources you placed in the layout are ignored.

Additionally, you can also specify the termination resistors for other ports, voltage source resistance values, or current source resistance values in this file.

If you select an external file, the **Interpolate spectrum at missing frequency points** check box is enabled. If SIwave cannot find a value at a certain frequency *f* in the external excitation file during simulation, it generates a value by interpolating the data specified at the two closest frequency points straddling *f*. If this option is unchecked, no simulation data is computed at the frequency point *f* for which excitation data is absent.

4. Enter values for **Start Frequency**, **Stop Frequency**, and **Number of Solution Points**.
5. From the **Distribution** field, select one of:
   - **Linearly** – the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
   - **By Decade** – distributes the number of points specified logarithmically, over each decade.
6. To add or delete frequency points, use the **Add Above**, **Add Below**, and **Delete Selection** buttons.
7. To preview all frequency points, click **Preview**.

   The **Frequency List Preview** window appears, showing all the points.

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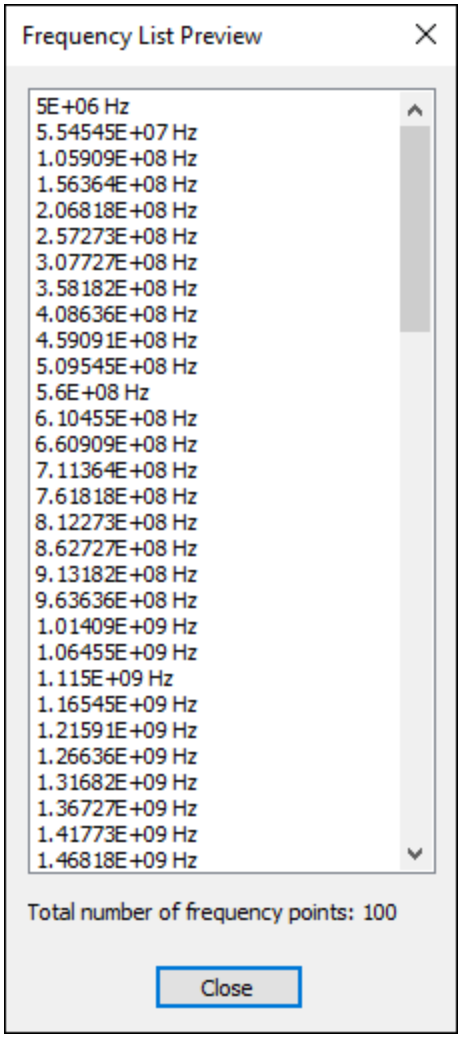

8. Clock **Close** to exit the **Frequency List Preview**.
9. To save grid values to a file, click **Save**. Choose a file name and location for your SIwave Frequency Sweep Distribution File (*.sfsdf).
10. To load grid values from an SIwave Frequency Sweep Distribution File (*.sfsdf), click **Load** and select your file.
11. To make the current settings the default, click **Set Default**. When a default value has been set, the window for that simulation type will always be populated with those settings when the window is opened.
12. To remove the default settings, click **Clear Default**.
13. From the **Voltage Surface Plot Options** area, use the drop-down menus to select the layers between which voltage difference is to be plotted.
14. If you want to save these settings for subsequent simulations, click **Save Settings**.
15. To see additional solver options, click **Other Solver Options**.

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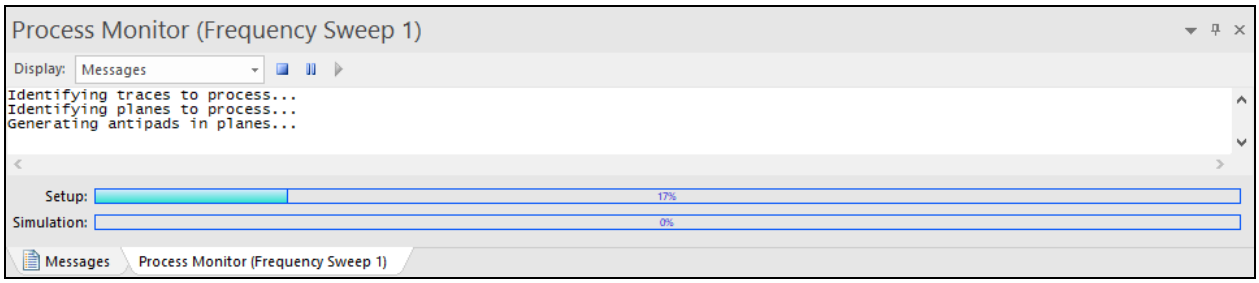
16. Click **Launch** to run the simulation.

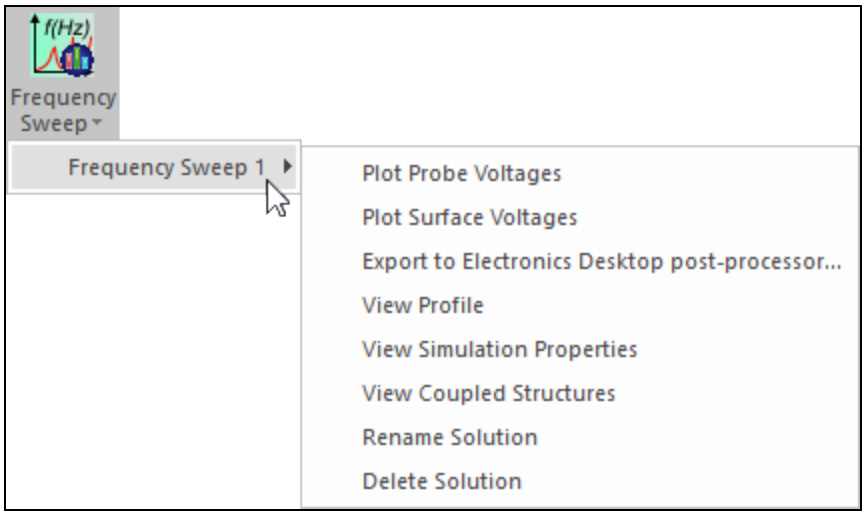
    The **Messages** window updates with a Process Monitor tab that displays the progress.



Viewing Frequency Sweep Results

To view frequency sweep results:

1. Click **Results**.
2. From the SIwave area, select **Frequency Sweep** > **[Simulation Name]**.
3. Select the type of results you would like to view.



Result options include:

- Plot Probe Voltages
- Plot Surface Voltages

Results display in the Modeling workspace, and a results window appears. Click a frequency to view it. You can also export a frequency sweep animation.

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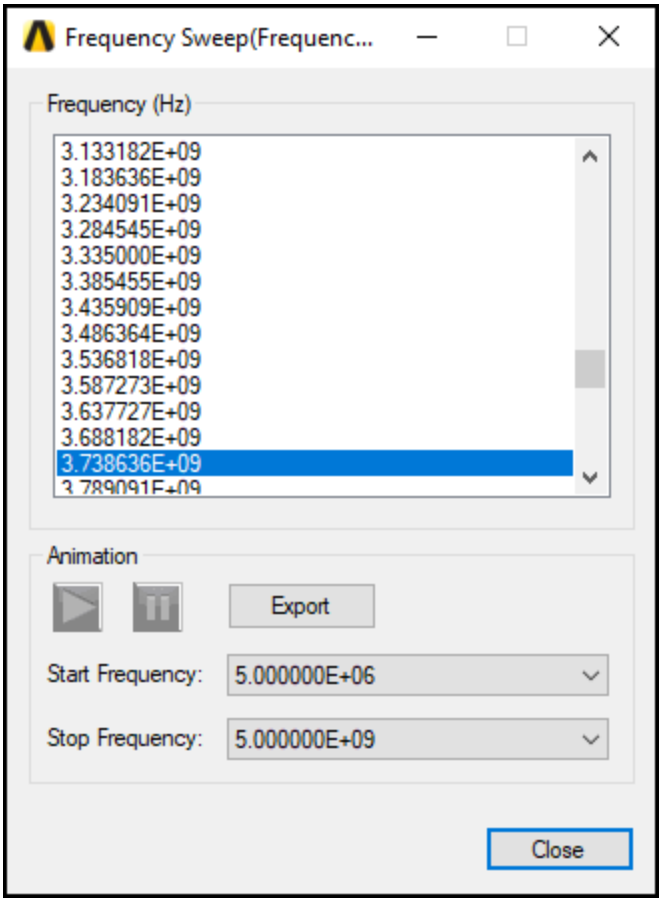

From the results menu, you can also access additional Frequency Sweep options.

Frequency Sweep Results Menu Options

Navigate to the Frequency Sweep Results menu:

1. Click **Results**.
2. From the SIwave area, select **Frequency Sweep** > **[Simulation Name]**.

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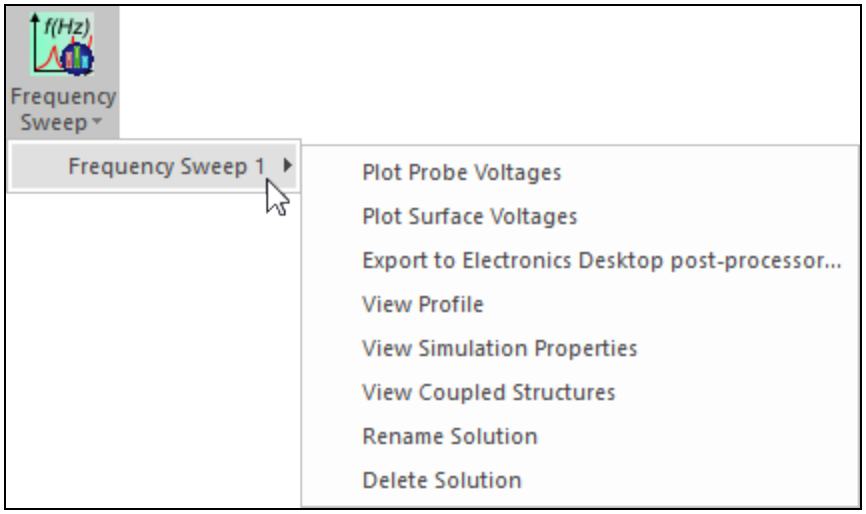

Menu options include:

- **Export to Electronics Desktop post-processor** – exports the solution to Ansys Electronics Desktop and opens it there.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the Freq. Sweep tab.
- **View Coupled Structures** – displays coupled structures in the Modeling workspace.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Simulation Profile:

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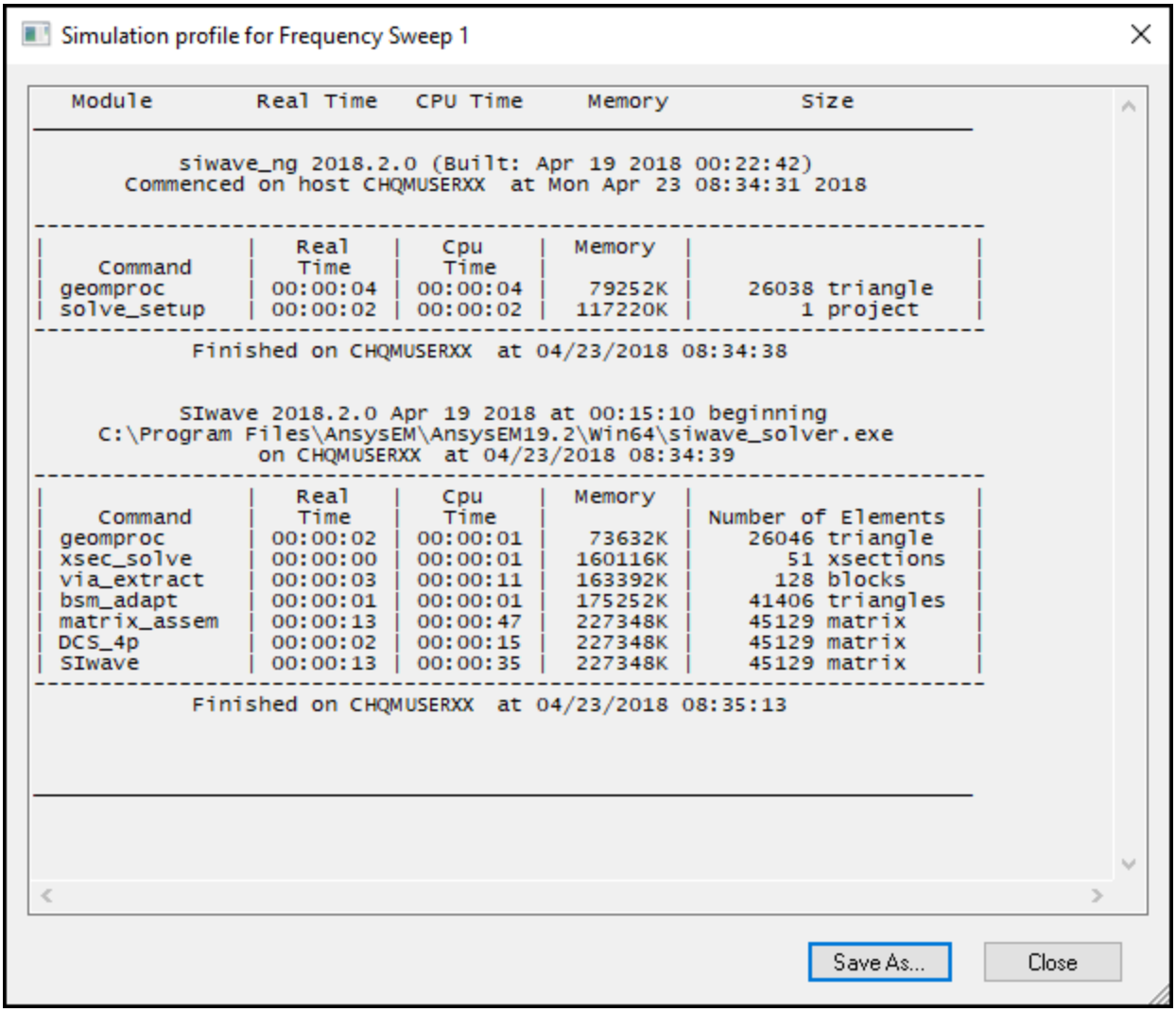

Simulation Properties:

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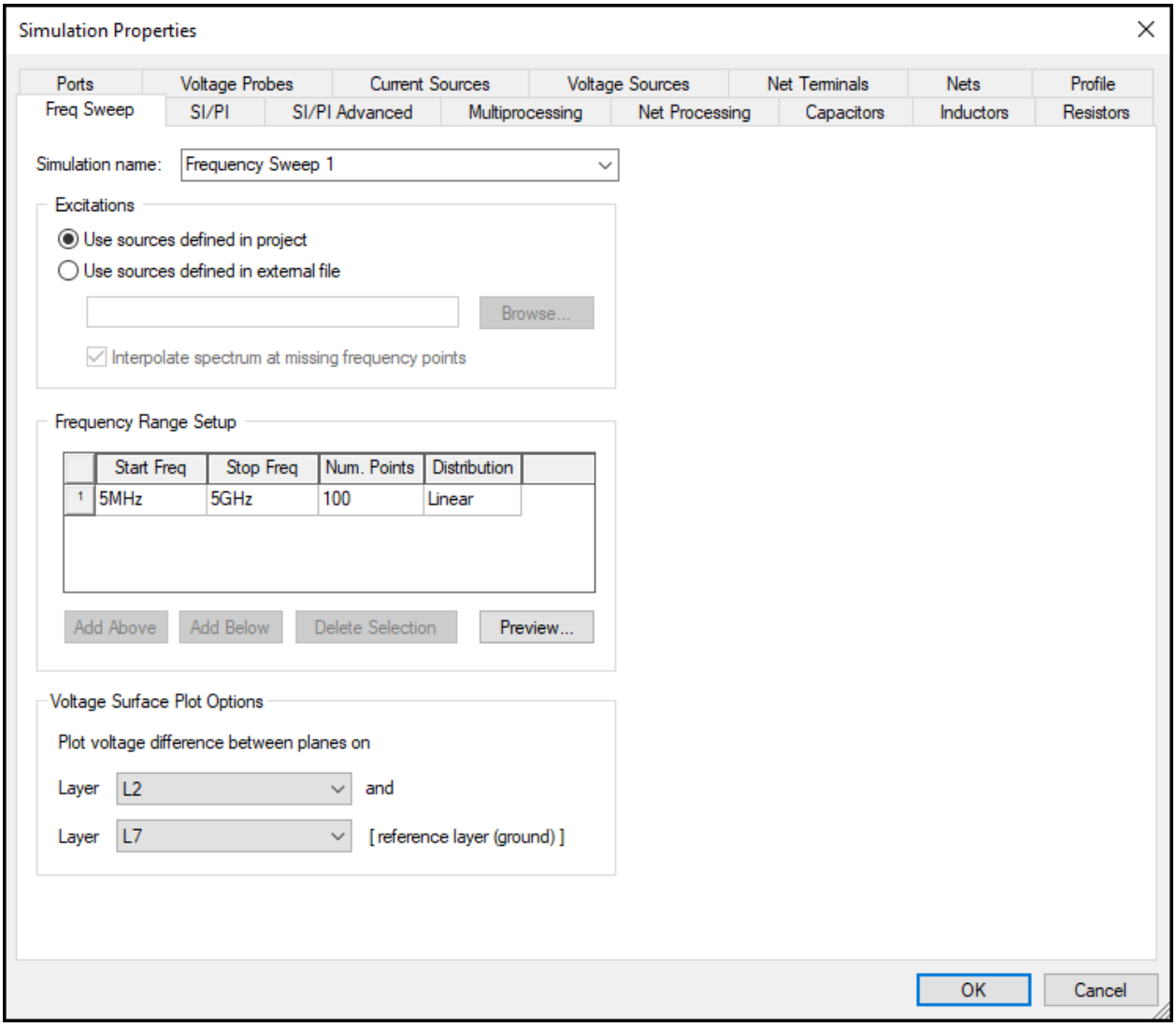

From this menu, you can also view frequency sweep results or export a frequency sweep animation.

Exporting a Frequency Sweep Animation

Navigate to the Frequency Sweep Results menu:

1. Click **Results**.
2. From the SIwave area, select **Frequency Sweep** > **[Simulation Name]**.

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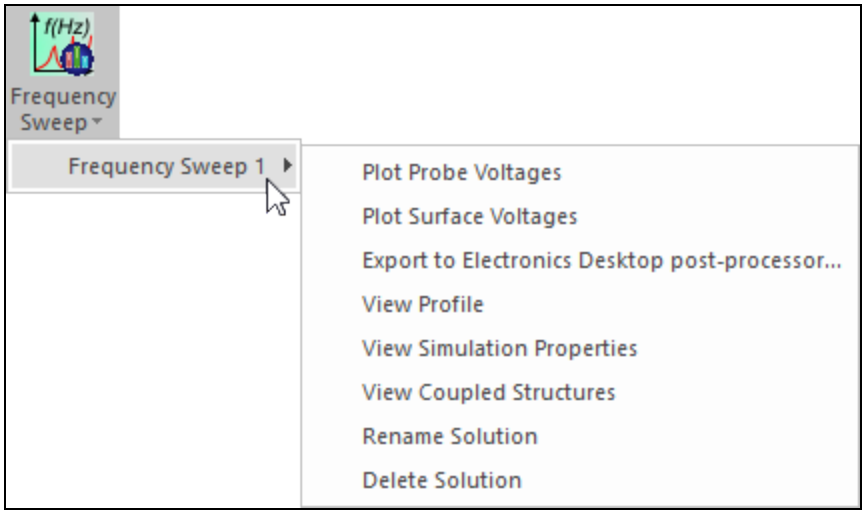

3. Select the result type you want to view (either **Plot Probe Voltages** or **Plot Surface Voltages**).

   The **Frequency Sweep Results** window appears.

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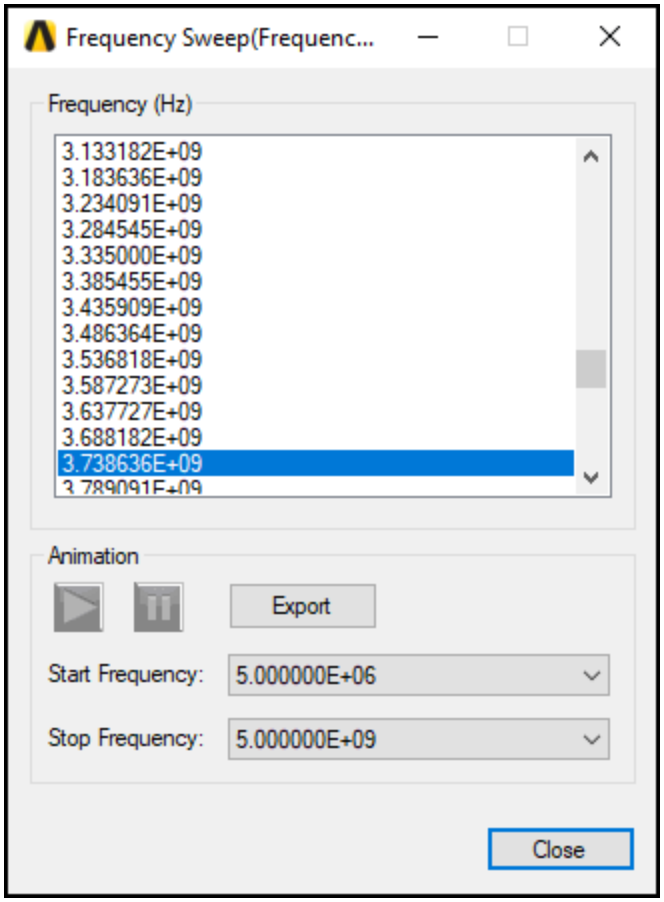

Use the **Play** and **Pause** icons to view the results as an animation in the Modeling workspace.

To export an animation:

1. Use the **Start Frequency** drop-down menu to select the first frequency in your animation.
2. Use the **Stop Frequency** drop-down menu to select the final frequency in your animation.
3. Click **Export**.

   The **Select file for Animation file output** window appears.

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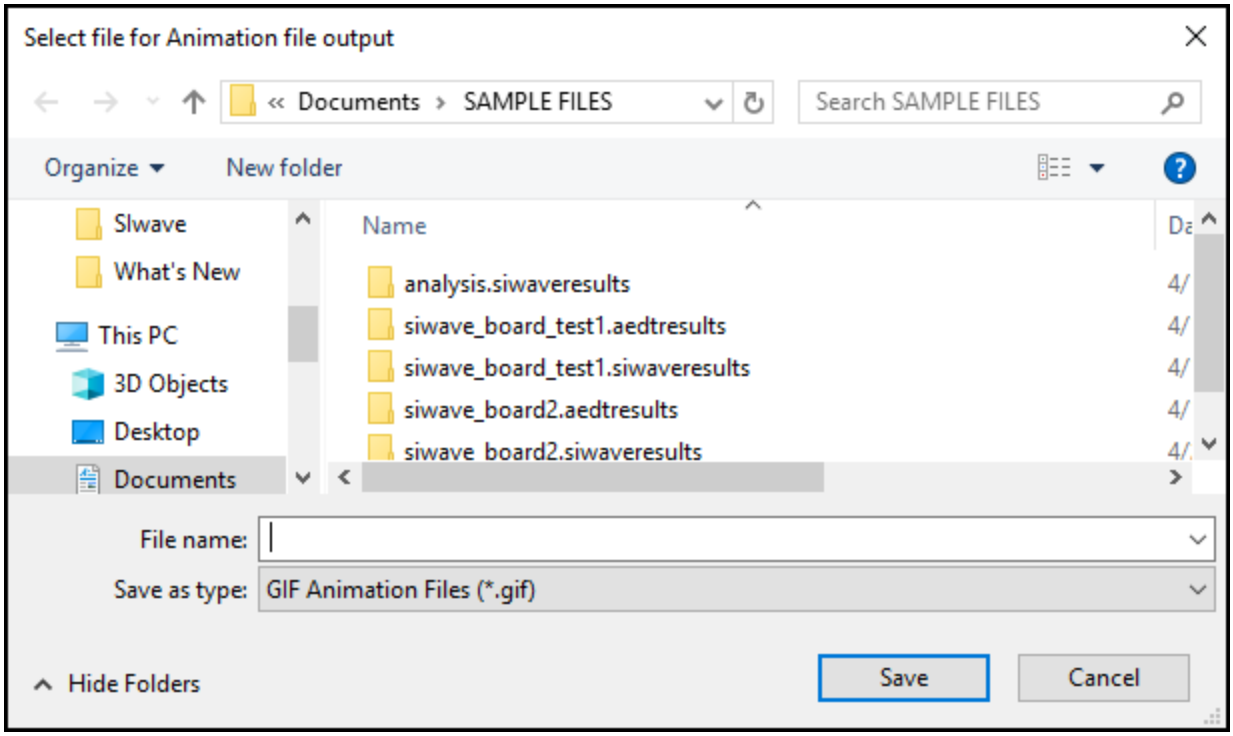

4. Select a location for the file.
5. From the **File name** field, enter a name for the file.
6. Use the **Save as type** drop-down menu to select either **GIF Animation Files (*.gif)** or **Audio-Video Inteleave Files (*.avi)**.
7. Click **Save**.

   The **Animation Options** window appears.

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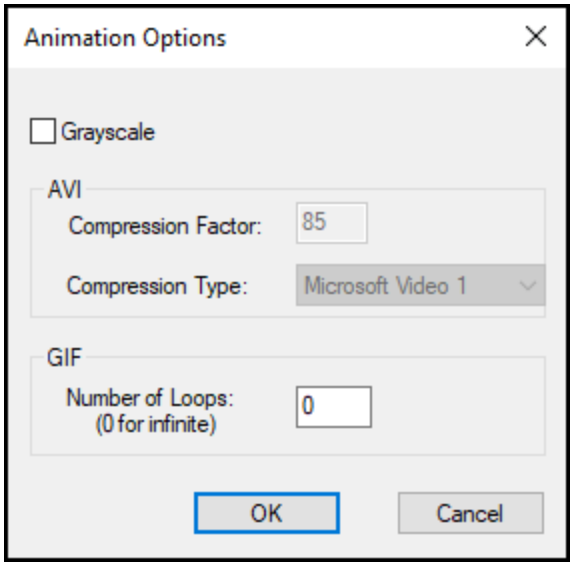

8. To replace colors in the file with 256 shades of gray, check the **Grayscale** check box. Grayscale animations use less memory than full color animations.
9. For **.avi** files:
   a. Specify the **Compression Factor**.
   b. Use the **Compression Types** drop-down menu to select from the following: INTEL Indeo, Cinepak, Microsoft Video 1, or None.
10. For **.gif** files, specify the number of times you want to play the animation in the **Number of Loops** box. The default (0) loops indefinitely.
11. Click **OK**.

    The animation is exported to the specified format.

Computing Near Fields

To analyze the radiated fields associated with a design, a radiation surface is defined over which the fields are calculated. The values of the fields over this surface are used to compute the fields in the space surrounding the device. This space is typically split into two regions: the near-field region and the far-field region. The near-field region exists at less than a wavelength from an energy source. The far-field region is where radiation occurs. Both near and far fields can play a role in EMI. Near and far field analyses can use sources defined in SIwave or via push excitations from Ansys Electronics Desktop.

To perform a near field simulation:

1. Click **Simulation**.
2. From the **SIwave** area, click **Compute Near Field**.

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The **Compute Near Field** window appears.

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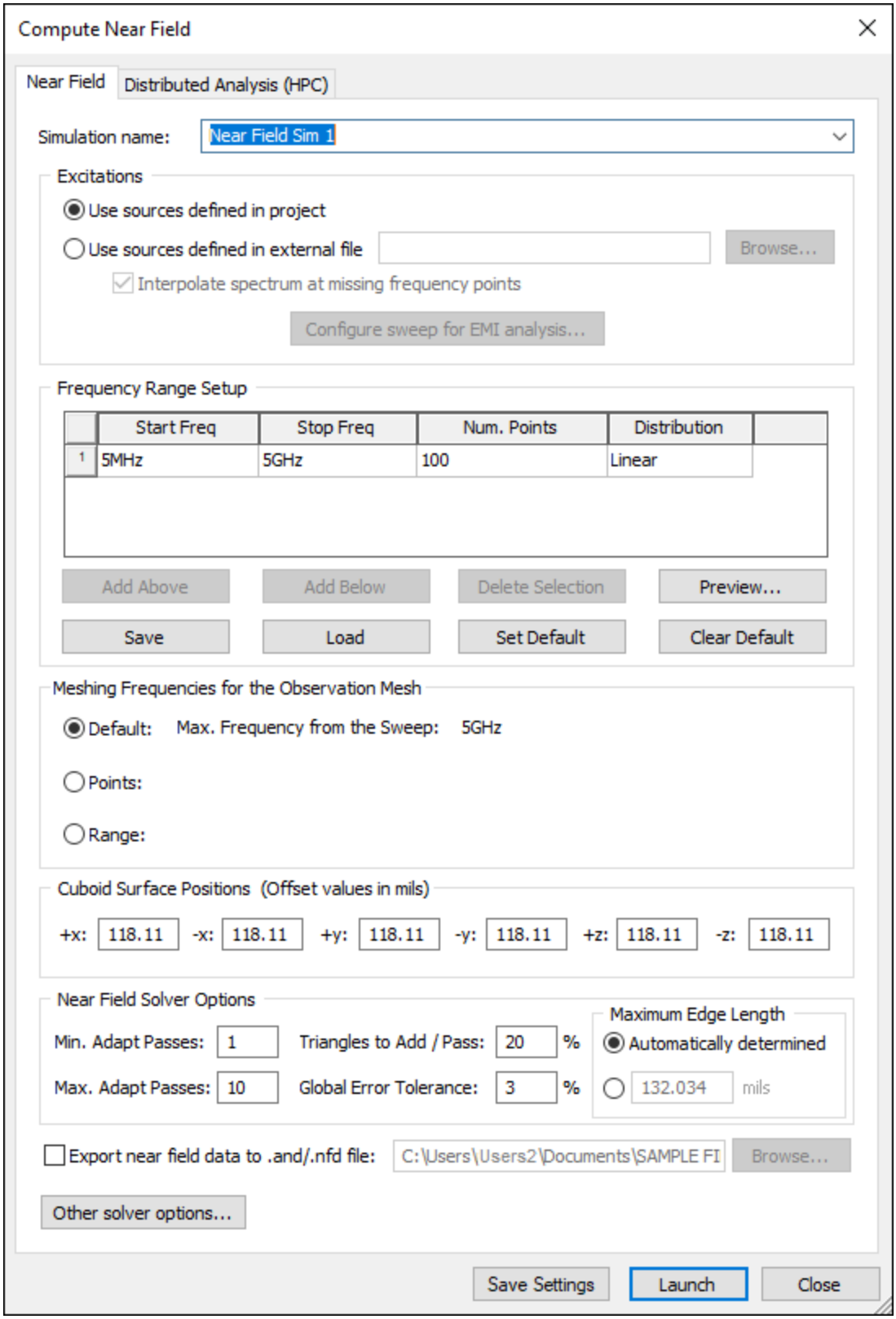

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3. From the **Simulation name** field, enter a name for the simulation.
4. From the **Excitations** area, select a source of excitations (i.e., **Use sources defined in the project** or **Use sources defined in external file**. If users select **Use source defined in external file**, **Browse** to an appropriate file and select it. Then, if appropriate, check the **Interpolate spectrum at missing frequency points** box.
5. From the **Frequency Range Setup** area, click the **Start Freq.**, **Stop Freq.**, and **Num. Points** fields to enter values.
6. Use the **Distribution** drop-down menu to select either **Linear** or **By Decade**.
   - **Linear** – the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
   - **By Decade** – distributes the number of points specified logarithmically, over each decade.
7. If appropriate, add or remove rows to the Frequency Range using the **Add Above**, **Add Below**, and **Delete Selection** buttons.
8. If appropriate, click **Save** to save the settings as a SIwave Frequency Sweep Distribution File (*.sfsdf). Click **Load** to choose previously saved settings.
9. If appropriate, click **Set Default** to set the current grid settings as a default value for that simulation type. When a default value has been set, the window for that simulation type will always be populated with those settings when the window is opened. Click **Clear Default** to remove the default setting and return the population of the grid to its normal behavior.
10. Click **Preview...** to open the **Frequency List Preview** window.

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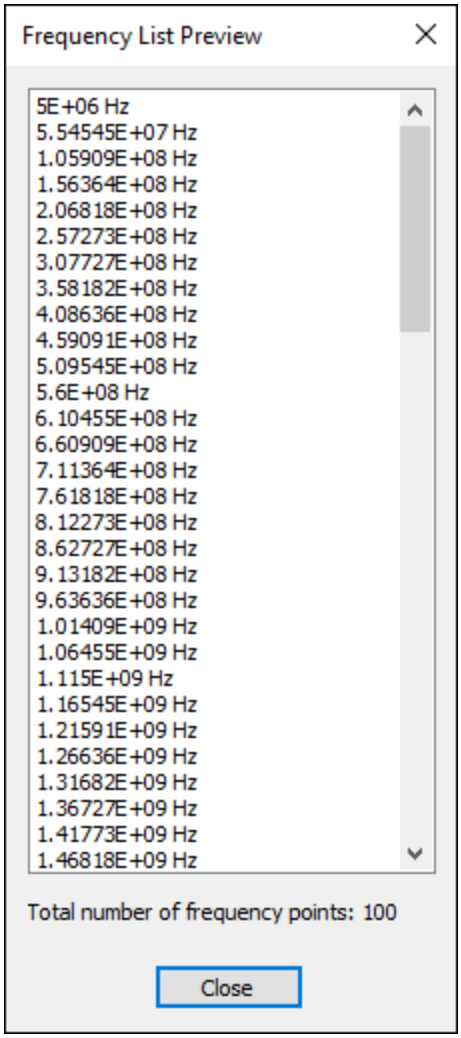

11. From the **Meshing Frequencies for the Observation Mesh** area, use the radio buttons to select which frequencies will be used for the observation mesh:
    - **Default** – uses the default max. frequency from the sweep (5Ghz).
    - **Points** – opens menu options that allow you to enter specific frequencies.
    - **Range** – opens menu options that allow you to select a start and stop frequency.
12. From the **Cuboid Surface Positions** area, enter values for **+x**, **-x**, **+y**, **-y**, **+z**, and **-z** offset. These values define a cuboid that completely encloses the design by specifying the cuboid face offset values from the design bounding box. The near field is evaluated on the surface of this cuboid.

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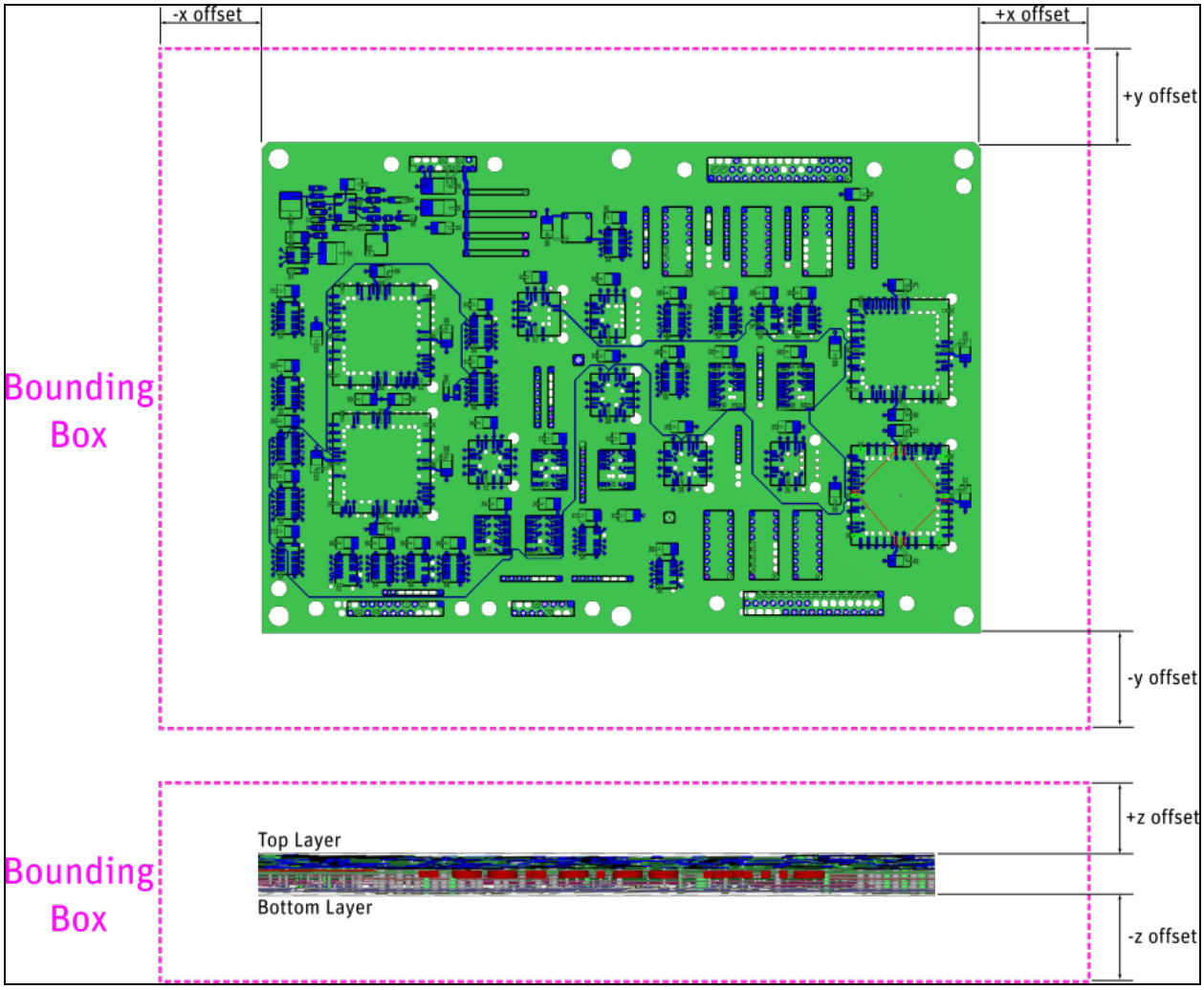

Note:

Offsets that are very small may increase simulation time.

13. From the **Near Field Solver Options** area, enter values for the following:
    a. **Min. Adapt Passes** – an adaptive analysis will not stop unless the minimum number of passes specified is completed, even if convergence criteria have been met.
    b. **Max. Adapt Passes**- this value is the maximum number of mesh refinement cycles SIwave will perform. This value is a stopping criterion for the adaptive solution; if the maximum number of passes has been completed, the adaptive analysis stops; otherwise, the adaptive analysis will continue unless the convergence criteria are reached.

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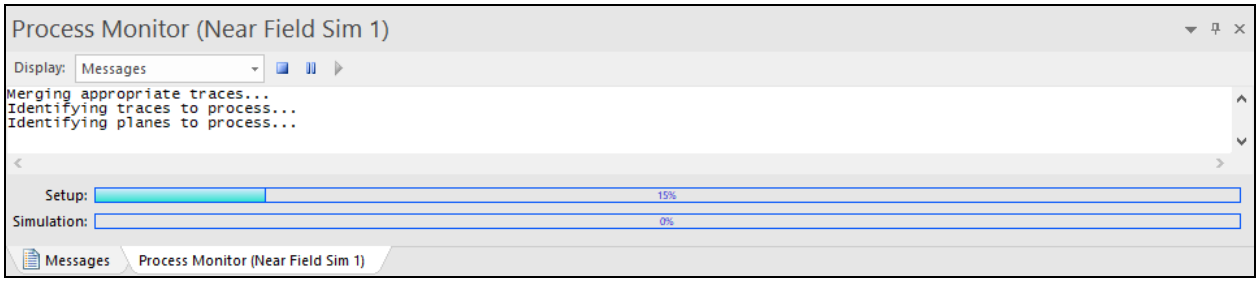
> **Note:**
>
> The size of the finite element mesh — and the amount of memory required to generate a solution — increases with each adaptive refinement of the mesh. Setting the maximum number of passes too high can result in SIwave requesting more memory than is available or taking excessive time to compute the solutions.

c. **Triangles to Add/Pass**

d. **Global Error Tolerance** – this is the maximum relative difference allowed between two successive passes.

14. From the **Maximum Edge Length** area, use the radio buttons to select **Automatically determined** or enter a value in mils. SIwave generates a surface triangular mesh such that the triangle edge lengths are equal to or less than the specified value.
15. If appropriate, check **Export near field data to .and/.nfd files after simulation completes** and select a location for the file. Near field data is exported in Ansys Nearfield Data (*.and) format, and can be used as external incident field data in Ansys HFSS simulations.
16. If appropriate, click **Save settings** to save these values.
17. If appropriate, click **Other solver options** to change general solver options.
18. Click **Launch** to begin simulation.

    The **Messages** window opens a Process Monitor tab that displays the progress.



Viewing Near Field Results in SIwave

To view near field results:

1. Click **Results**.
2. From the SIwave area, select **Near Field** > **[Simulation Name]**.

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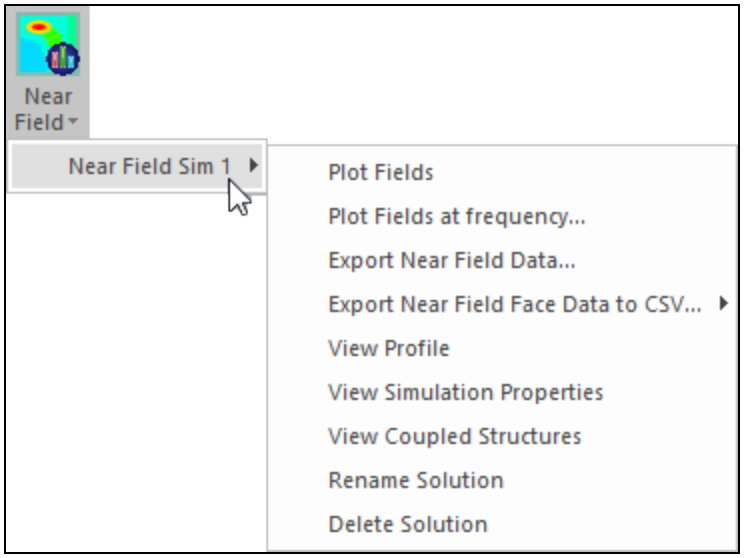

You can also access this menu by right-clicking **[Simulation Name]** in the Results window.

Plot options include:

- Plot Fields
- Plot Fields at Frequency

To plot fields:

1. Click **Plot Fields**.

   The **Near Field Sweep** results window appears.

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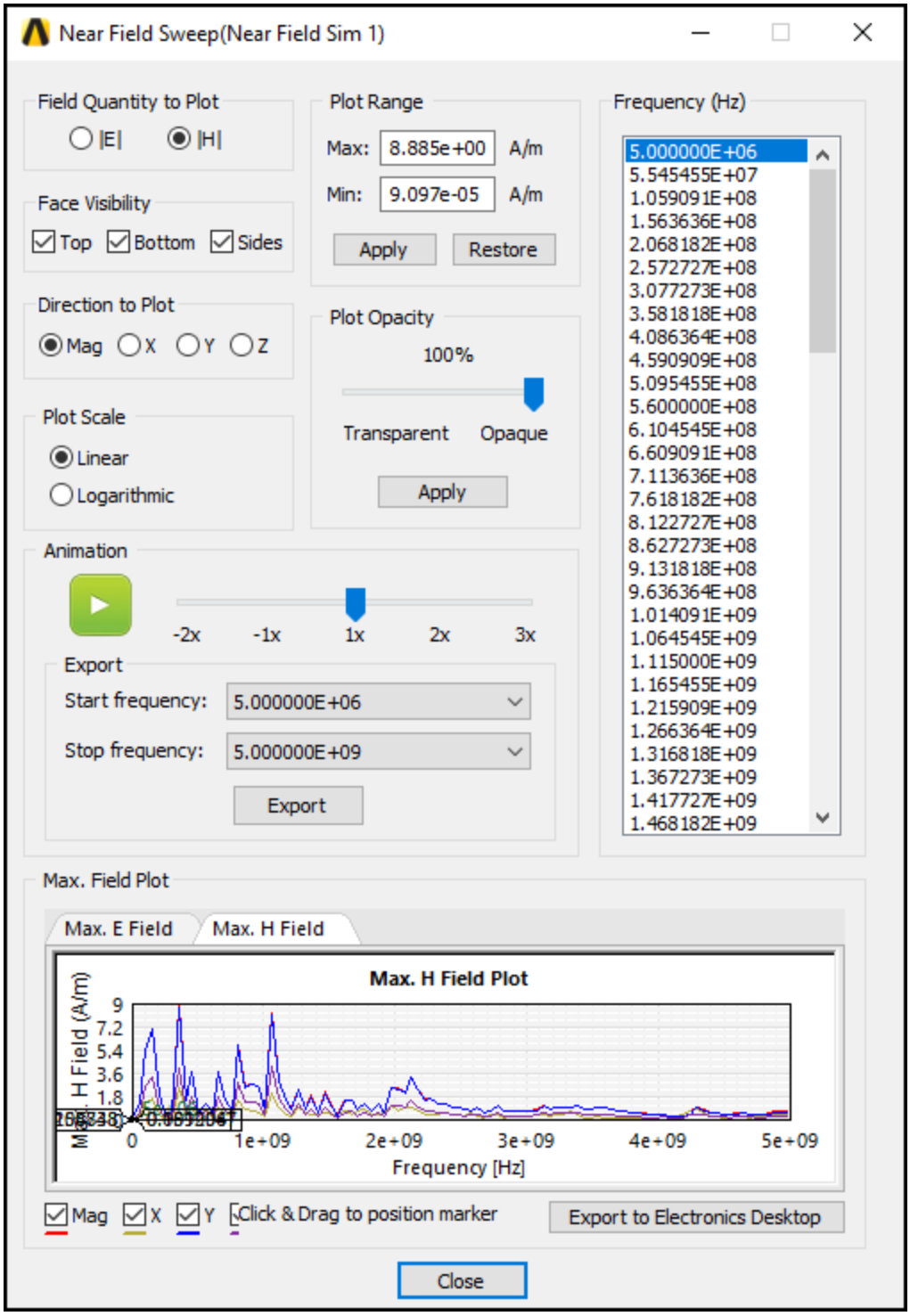

2. Select your appropriate options:
   - **Field Quantity to Plot** – select either **|E|** or **|H|** to plot that entire solution magnitude range.

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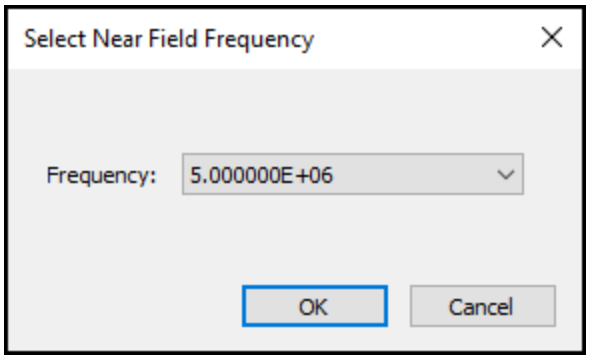
- **Plot Range** – use the **Max** and **Min** fields to restrict the plot scale to a sub-range. Areas where field magnitude is above the maximum value are drawn in red. Areas where field magnitude is below the minimum value are drawn in blue. Click **Apply** to apply the changes or **Restore** to revert them.
- **Face Visibility** – use the check boxes to determine E/H field visibility. Choose whether E/H fields on the **Top**, **Bottom**, and **Sides** are visible. When you move the cursor across a visible top or bottom face, a tool tip displays the E/H field value. If both the top and bottom faces are visible, the tool tip displays the value of the top face.
- **Direction to Plot** – choose **mag**, **x**, **y**, or **z** plot. Mag is the default.
- **Plot Scale** – choose between **Linear** and **Logarithmic** scale.
- **Plot Opacity** – use the slider to increase or decrease the transparency of the object. Click **Apply** to apply changes.

The **Max. Field Plot** displays at the bottom of the window. Use the **mag**, **x**, **y**, and **z** check boxes to view those plots.

Click **Export to Electronics Desktop** to export and open the plot in Ansys Electronics Desktop.

To plot fields at a specific frequency:

1. Click **Plot Fields at Frequency**.
2. The **Select Near Field Frequency** window appears.



3. Use the drop-down menu to select a frequency.
4. Click **OK**.

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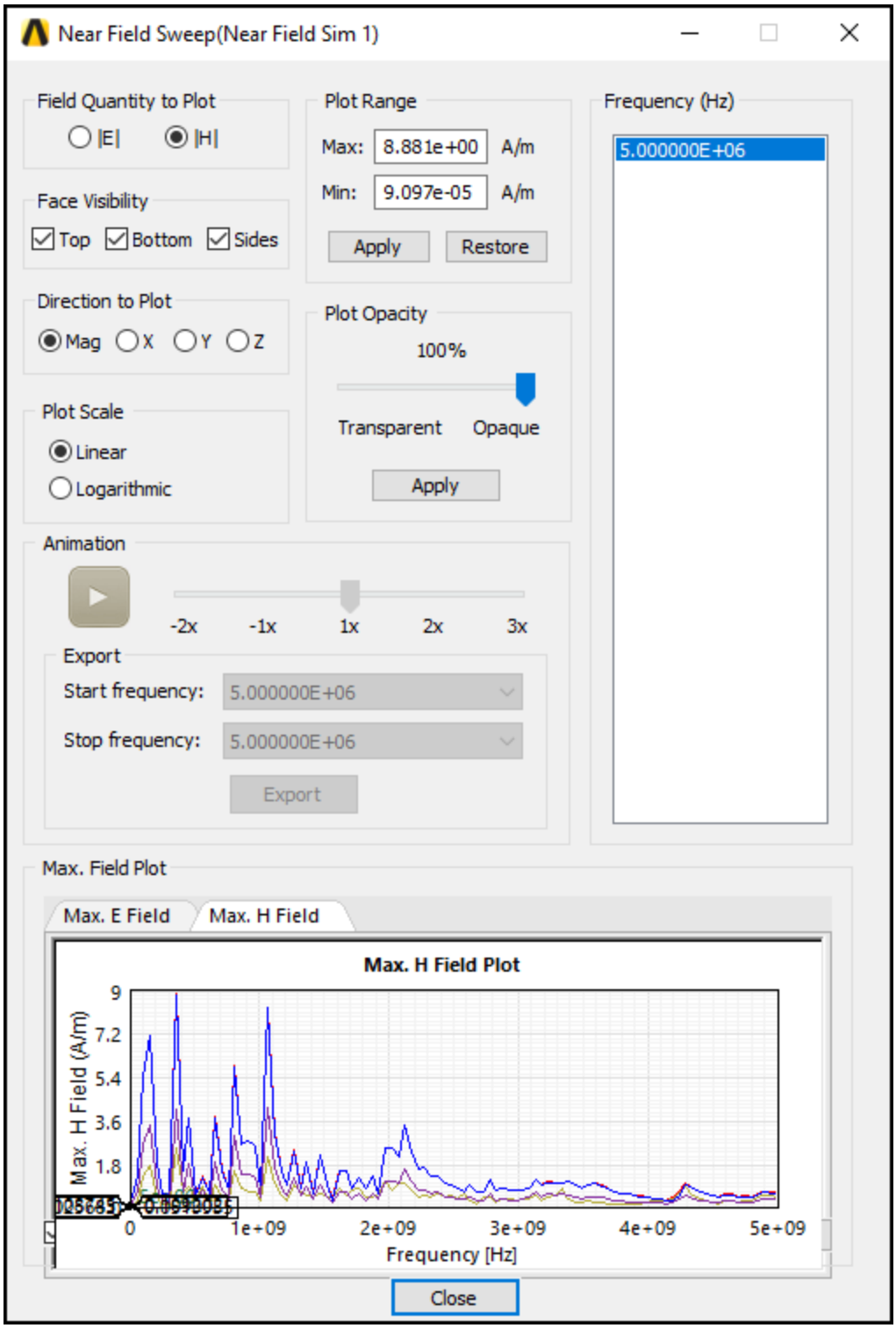
The **Near Field Sweep** results window appears, with only the selected frequency displayed.



From here, you can export the near fields animation.

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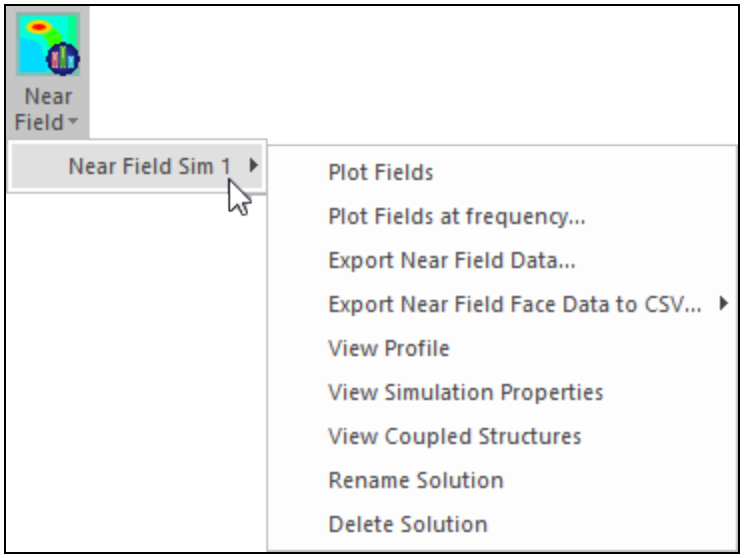
From the Near Field results menu, you can also access additional Near Fields options.

Near Field Results Menu Options

Navigate to the Near Field Results menu:

1. Click **Results**.
2. From the SIwave area, select **Near Field** > **[Simulation Name]**.



You can also access this menu by right-clicking **[Simulation Name]** in the Results window.

Menu options include:

- **Export Near Field Data** – exports the solution to Ansys Electronics Desktop and opens it there.
- **Export Near Field Face Data to CSV** – exports near field face data as a *.csv file.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the Near Field tab.
- **View Coupled Structures** – displays coupled structures in the Modeling workspace.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Simulation Profile:

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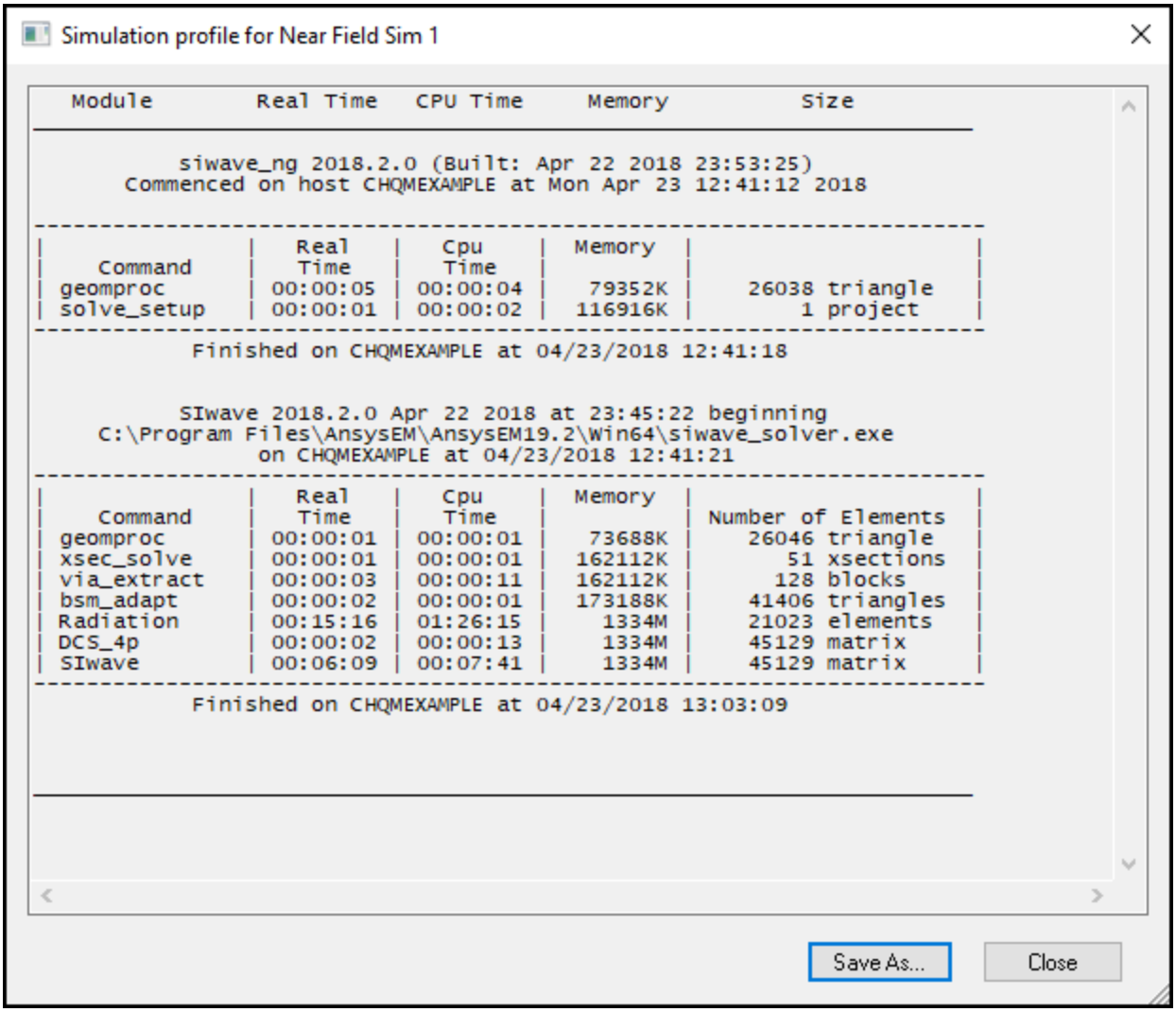

Simulation Properties:

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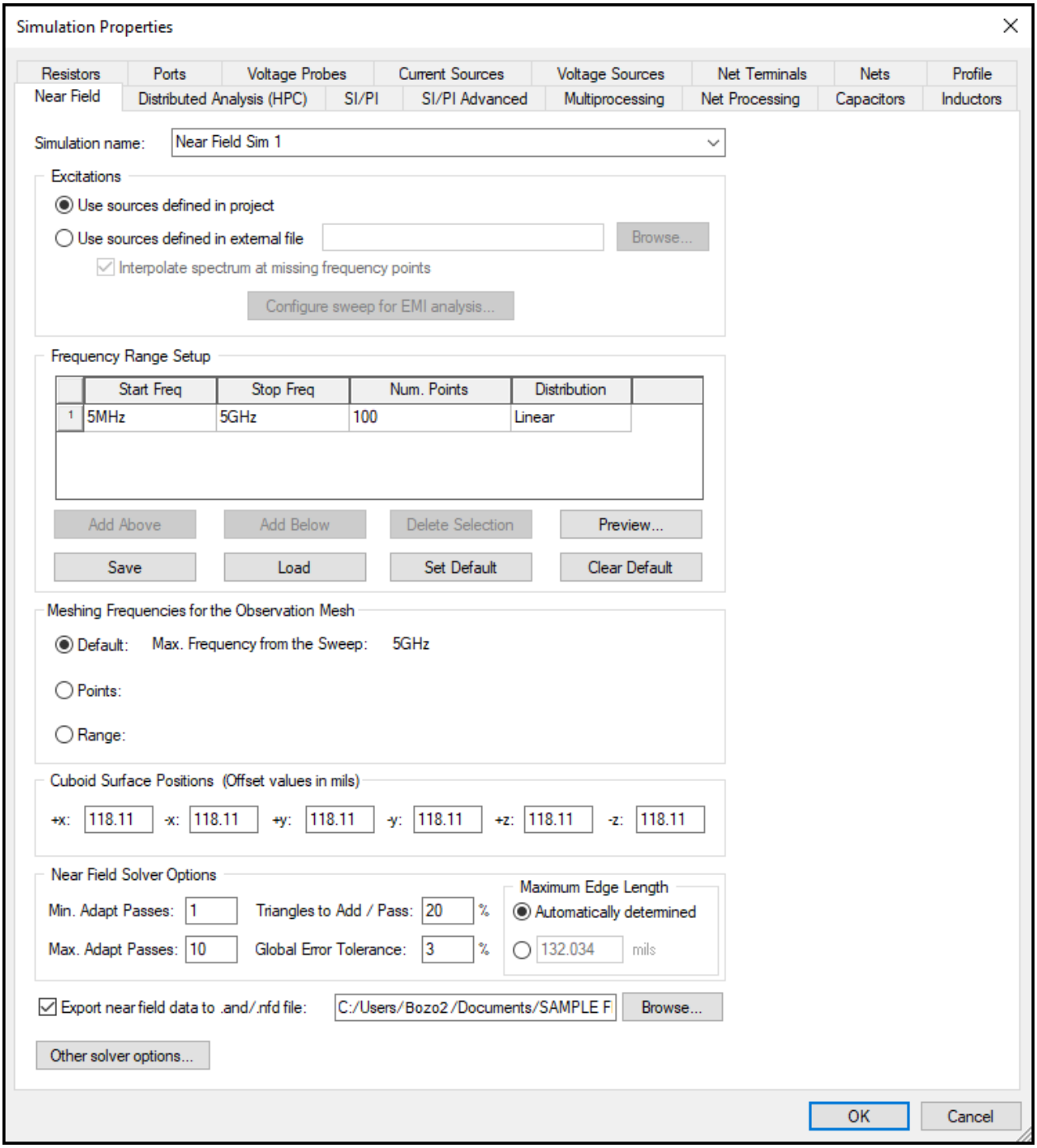

From this menu, you can also view near field results or export a near fields animation.

Exporting the Near Fields Animation

Navigate to the Near Field Results menu:

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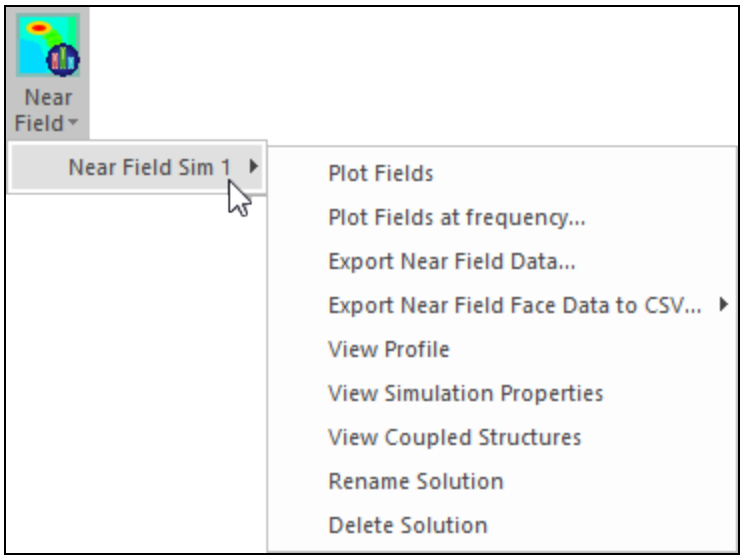
1. Click **Results**.
2. From the SIwave area, select **Near Field** > **[Simulation Name]** > **Plot Fields**.



You can also access this menu by right-clicking **[Simulation Name]** in the Results window.

The **Near Field Sweep** results window appears.

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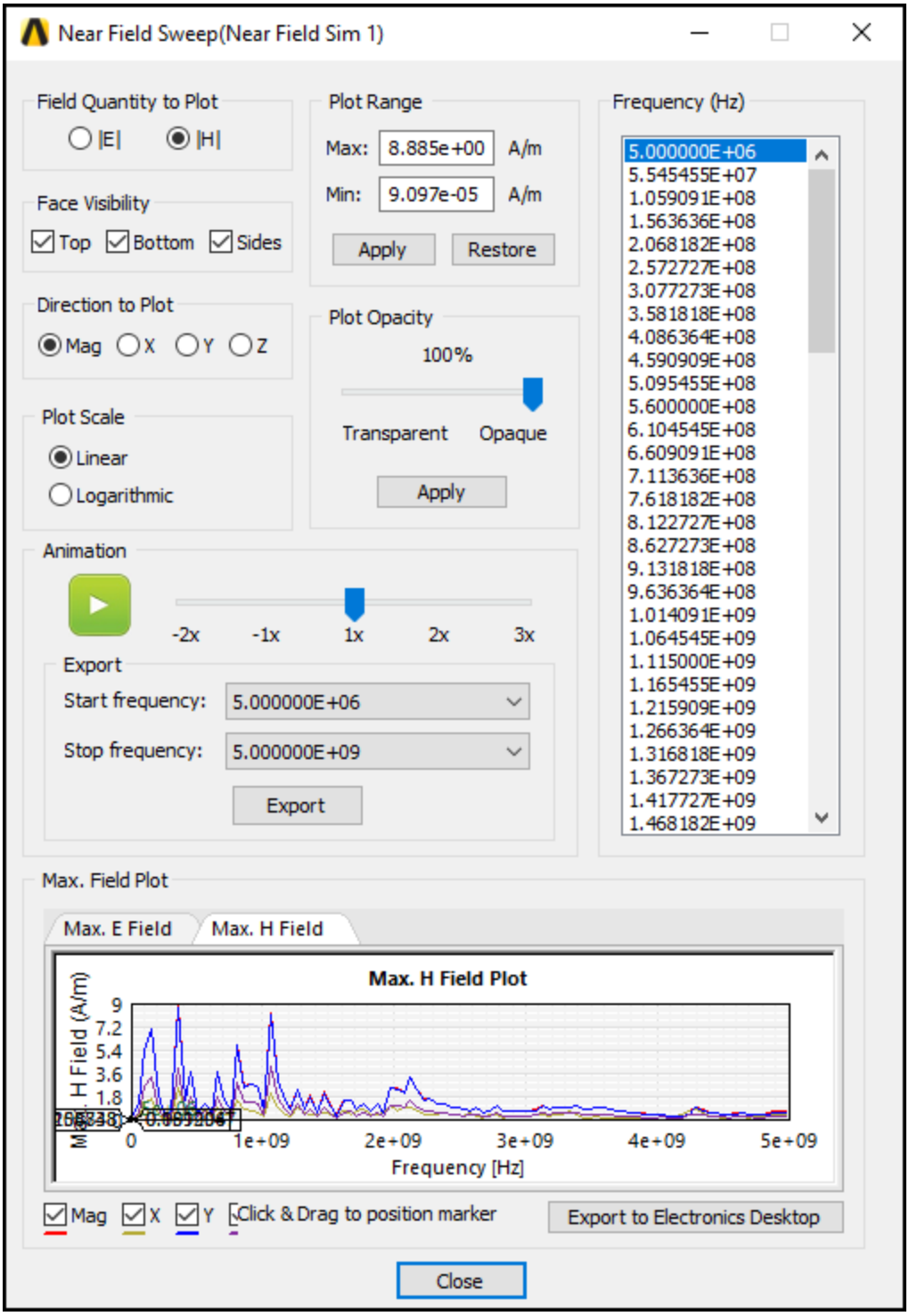

Use the **Play** icon to view the results as an animation in the Modeling workspace. While in playback, the icon becomes a Pause icon. Click **Pause** to stop the animation.

To export an animation:

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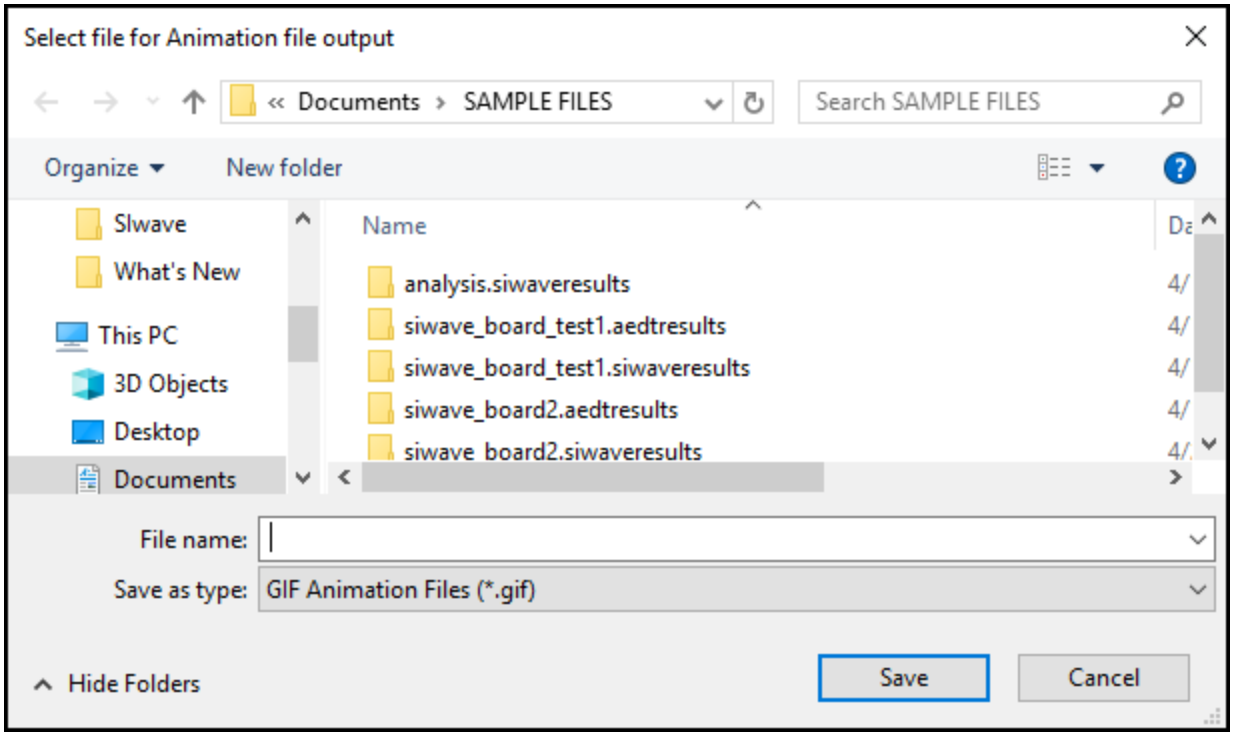
1. Use the **Start Frequency** drop-down menu to select the first frequency in your animation.
2. Use the **Stop Frequency** drop-down menu to select the final frequency in your animation.
3. Click **Export**.

   The **Select file for Animation file output** window appears.



4. Select a location for the file.
5. From the **File name** field, enter a name for the file.
6. Use the **Save as type** drop-down menu to select either **GIF Animation Files (*.gif)** or **Audio-Video Inteleave Files (*.avi)**.
7. Click **Save**.

   The **Animation Options** window appears.

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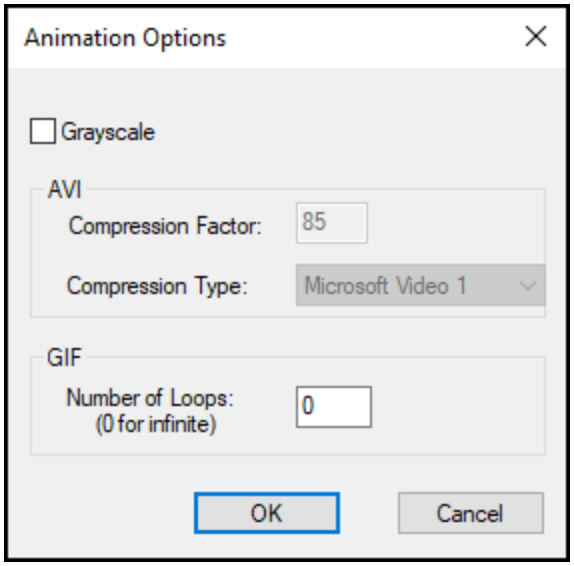

8. To replace colors in the file with 256 shades of gray, check the **Grayscale** check box. Grayscale animations use less memory than full color animations.
9. For **.avi** files:
   a. Specify the **Compression Factor**.
   b. Use the **Compression Types** drop-down menu to select from the following: INTEL Indeo, Cinepak, Microsoft Video 1, or None.
10. For **.gif** files, specify the number of times you want to play the animation in the **Number of Loops** box. The default (0) loops indefinitely.
11. Click **OK**.

    The animation is exported to the specified format.

Computing Far Fields

To analyze the radiated fields associated with a design, a radiation surface is defined over which the fields are calculated. The values of the fields over this surface are used to compute the fields in the space surrounding the device. This space is typically split into two regions: the near-field region and the far-field region. The near-field region exists at less than a wavelength from an energy source. The far-field region is where radiation occurs. Both near and far fields can play a role in EMI. Near and far field analyses can use sources defined in SIwave or via push excitations from Ansys Electronics Desktop.

To perform a far field simulation:

1. Click **Simulation**.
2. From the SIwave area, click **Compute Far Field**.

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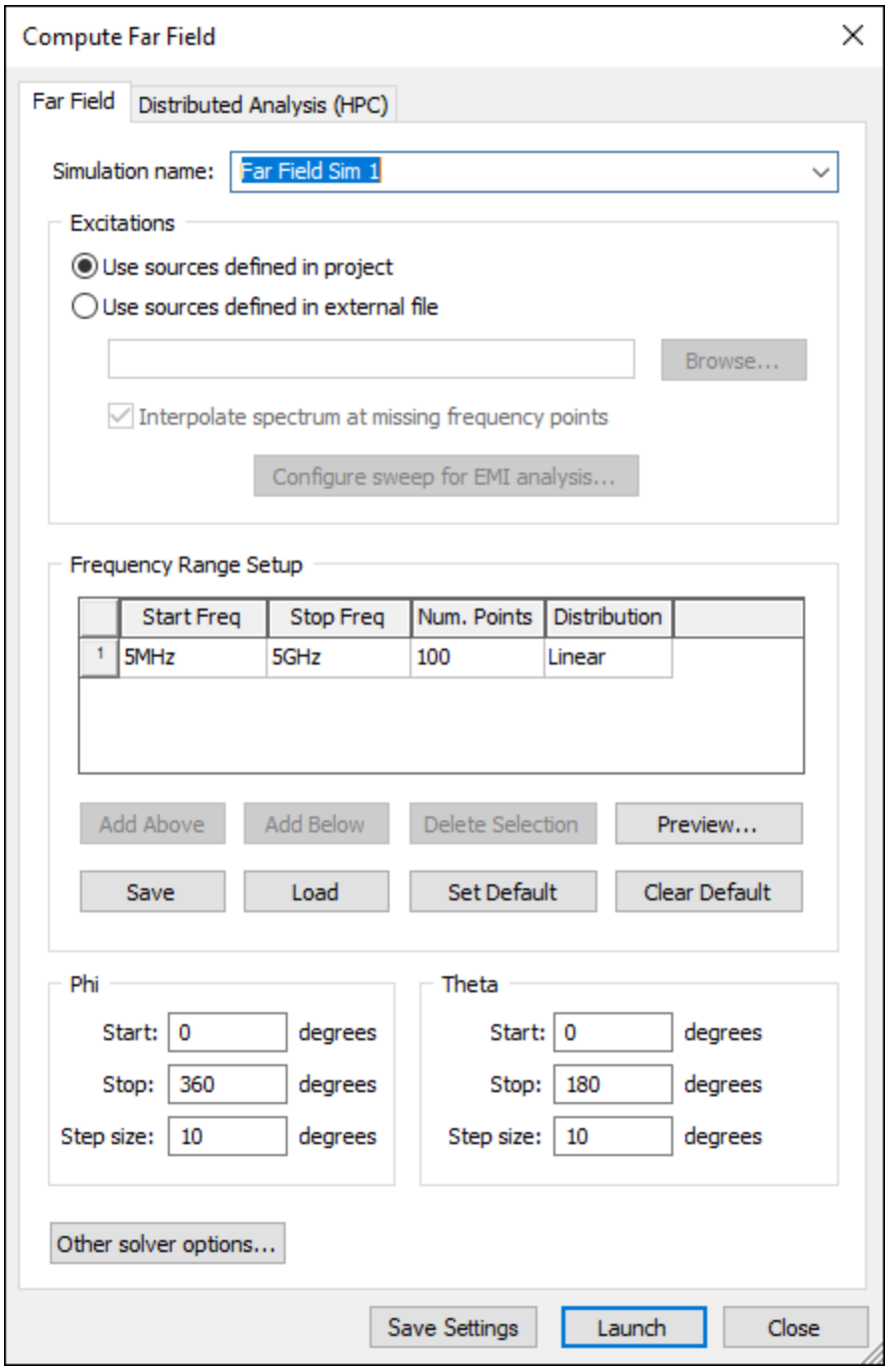
The **Compute Far Field** window appears.



3. From the **Simulation Name** field, enter a name for the simulation.
4. From the Excitations area, use the radio buttons to select whether to **use sources defined in the project** or **use sources defined in external file**. Click **Browse** to select an external file.

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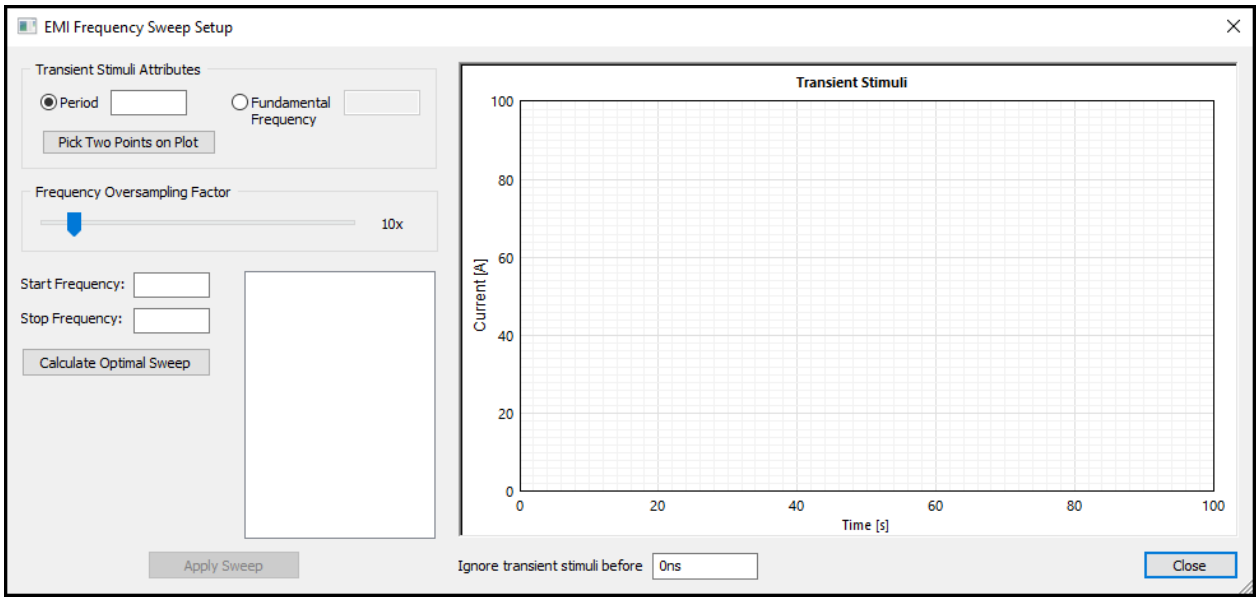
5. If appropriate, click **Configure sweep for EMI analysis** to set up the EMI sweep. This option is only enabled when using an external file.

   The **EMI Frequency Sweep Setup** window appears.



   a. From the Transient Stimuli Attributes area, use the radio buttons to select either **Period** or **Fundamental Frequency**. Period is the measured period information (T). The Fundamental Frequency is defined as $f_0 = 1/T$ where T is the period information.
   b. Use the **Frequency Oversampling Factor** slider to select the frequency range sampling density. A higher oversampling factor results in more frequency points being introduced between the selected sweep start and stop frequencies, and may result in longer simulation time.
   c. Enter a value for the minimum frequency to sweep in the **Start Frequency** box.
   d. Enter a value for a sweep maximum frequency in the **Stop Frequency** box.
   e. Click **Calculate Optimal Sweep** to generate the sweeps. They appear as a list in the box to the right.
   f. Click **Apply Sweep**. A new sweep line is added to the table in the **Compute Far Field** window.
   g. If appropriate, enter a value in the **Ignore transient stimuli before** box. This allows SIwave to filter out any non-periodic start-up transient ripple when computing the Fourier transform during simulation. The ignored time period is represented by a shaded rectangle on the plot.
   h. Click **Close** to return to the **Compute Far Field** window.

6. Specify the **Frequency Range Setup**. SIwave solves the solution beginning with the frequency entered in the Start box and ending with the frequency entered in the Stop box.

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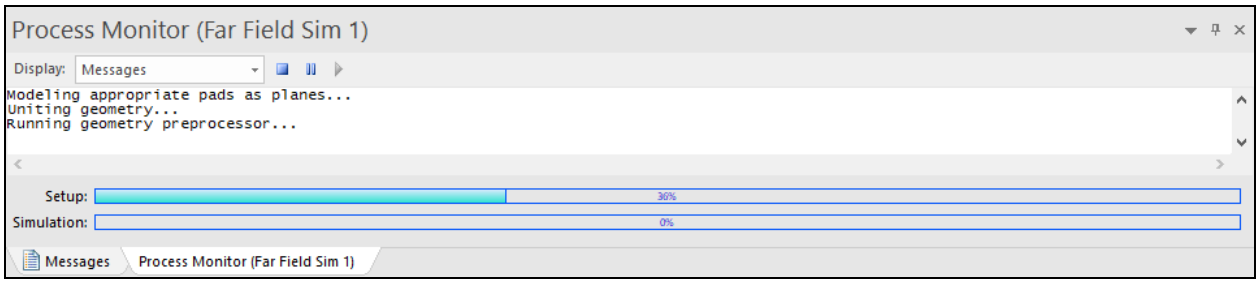
a. From the **Start Freq** text boxes, type the starting frequency of the frequency sweep.
b. From the **Stop Freq** text boxes, type the ending frequency of the frequency sweep.
c. From the **Num Points** boxes, type the number of points.
d. Use the **Distribution** drop-down menu to select either **Linear** or **By Decade**. Linear distributes the number of points specified over the entire specified range. By Decade distributes the number of points specified logarithmically over each decade.
e. If appropriate, click **Add Above** or **Add Below** to add a row in an appropriate position. Click **Delete Selection** to delete the selected rows.
f. Click **Preview** to see the frequency range in the **Frequency List Preview** window.
g. Click **Save** to save the grid values to SIwave Frequency Sweep Distribution File (*.sfsdf).
h. Click **Load** to load the grid values from a *.sfsdf file.
i. Click **Set Default** to set the current grid settings as a default value for that simulation type.
j. Click **Clear Default** to remove the default setting and return the population of the grid to its normal behavior.

7. Specify the range of angles to include in the sphere. Specify the following for Phi:
   - **Start** – The point where rotation of phi begins.
   - **Stop** – The point where rotation of phi ends.
   - **Step Size** – The number of angular subdivisions between the Start and Stop angles.
8. Specify the following for Theta:
   - **Start** – The point where rotation of theta begins.
   - **Stop** – The point where rotation of theta ends.
   - **Step Size** – The number of angular subdivisions between the Start and Stop angles.
9. If appropriate, click **Save Settings** to save the settings.
10. Click **Launch** to begin the Far Field simulation.

    The **Messages** window opens a Process Monitor tab that displays the progress.



Viewing Far Field Results in SIwave

To view far field results:

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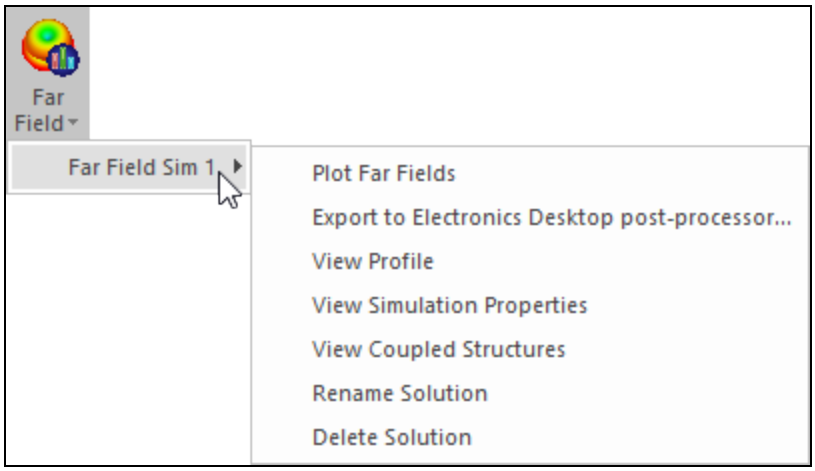
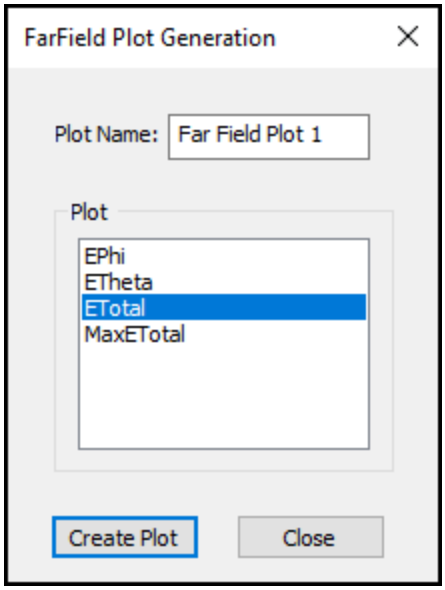
1. Click **Results**.
2. From the SIwave area, select **Far Field** > **[Simulation Name]** > **Plot Fields**.



The **FarField Plot Generation** window appears.



3. From the **Plot Name** field, enter a name for the plot.
4. From the **Plot** field, choose from the available options.

   The far field quantities measure the product r*E, where r is the radial distance from the origin and E is the electric field vector. For far fields, r*E does not depend on r; or equivalently, E is proportional to 1/r. Also, for far fields the radial (r) component of the E field is zero. The units of r*E are Volts.

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ePhi, eTheta	spherical (phi, theta) components of the quantity r*E. These are complex numbers.
eTotal	eTotal is a real number, and is the square root of the sum of the magnitudes of the vector components of r*E. It can be expressed either as: $\sqrt{\lvert\mathbf{E_x}\rvert^2 + \lvert\mathbf{E_y}\rvert^2 + \lvert\mathbf{E_z}\rvert^2}$ or $\sqrt{\lvert\mathbf{E_\Phi}\rvert^2 + \lvert\mathbf{E_\theta}\rvert^2}$
eX, eY, and eZ	Cartesian (x, y, z) components of the quantity r*E. These are complex numbers.
ELeft	The dominant component for a left-hand, circularly polarized field.
ERight	The dominant component for a right-hand, circularly polarized field.
MaxEX	A real-valued quantity. It is the maximum value (across all values of phi and theta on a sphere) of the magnitude of the x-component of r*E.
MaxEY	A real-valued quantity. It is the maximum value (across all values of phi and theta on a sphere) of the magnitude of the y-component of r*E.
MaxEZ	A real-valued quantity. It is the maximum value (across all values of phi and theta on a sphere) of the magnitude of the z-component of r*E.
MaxEPHI	A real-valued quantity. It is the maximum value (across all values of phi and theta on a sphere) of the magnitude of the phi-component of r*E.
MaxETheta	A real-valued quantity. It is the maximum value (across all values of phi and theta on a sphere) of the magnitude of the theta-component of r*E.
MaxETotal	The maximum value (across all values of phi and theta) of eTotal.
MaxELeft	Maximum values for the dominant component for a left-hand, circularly polarized field.
MaxERight	Maximum values for the dominant component for a right-hand, circularly polarized field.

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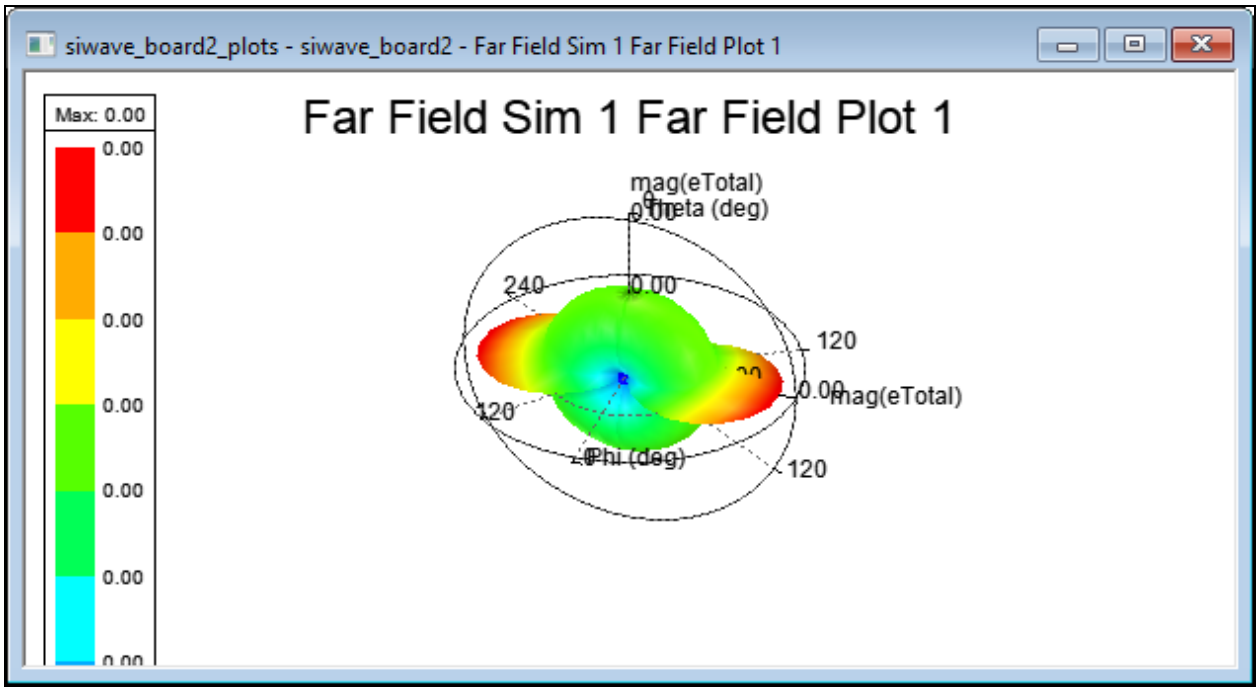
5. Click **Create Plot**.

   Ansys Electronics Desktop launches to display the plot.



From the Far Field results menu, you can also access additional menu options.

Far Field Results Menu Options

Navigate to the Far Field Results menu:

1. Click **Results**.
2. From the SIwave area, select **Far Field** > **[Simulation Name]**.

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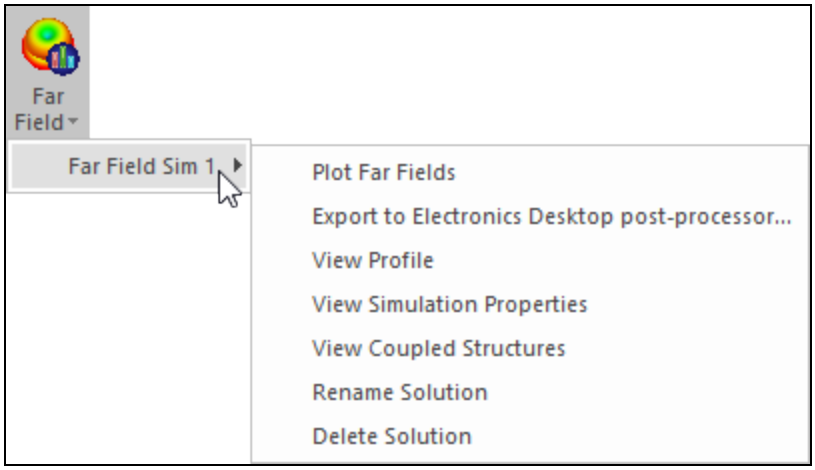

Menu options include:

- **Export to Electronics Desktop post-processor** – exports the solution to Ansys Electronics Desktop and opens it there.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the Far Field tab.
- **View Coupled Structures** – displays coupled structures in the Modeling workspace.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Simulation Profile:

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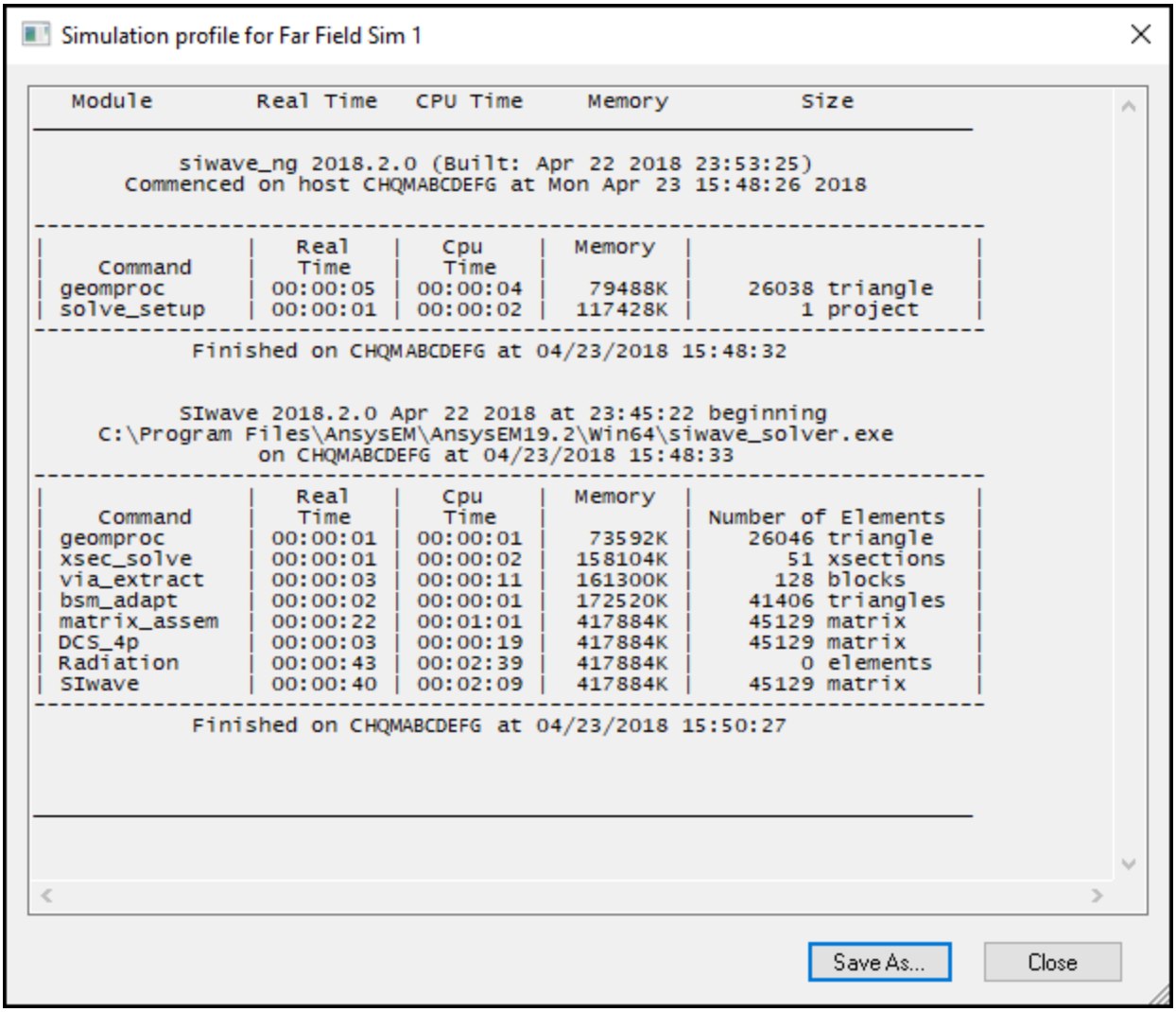

Simulation Properties:

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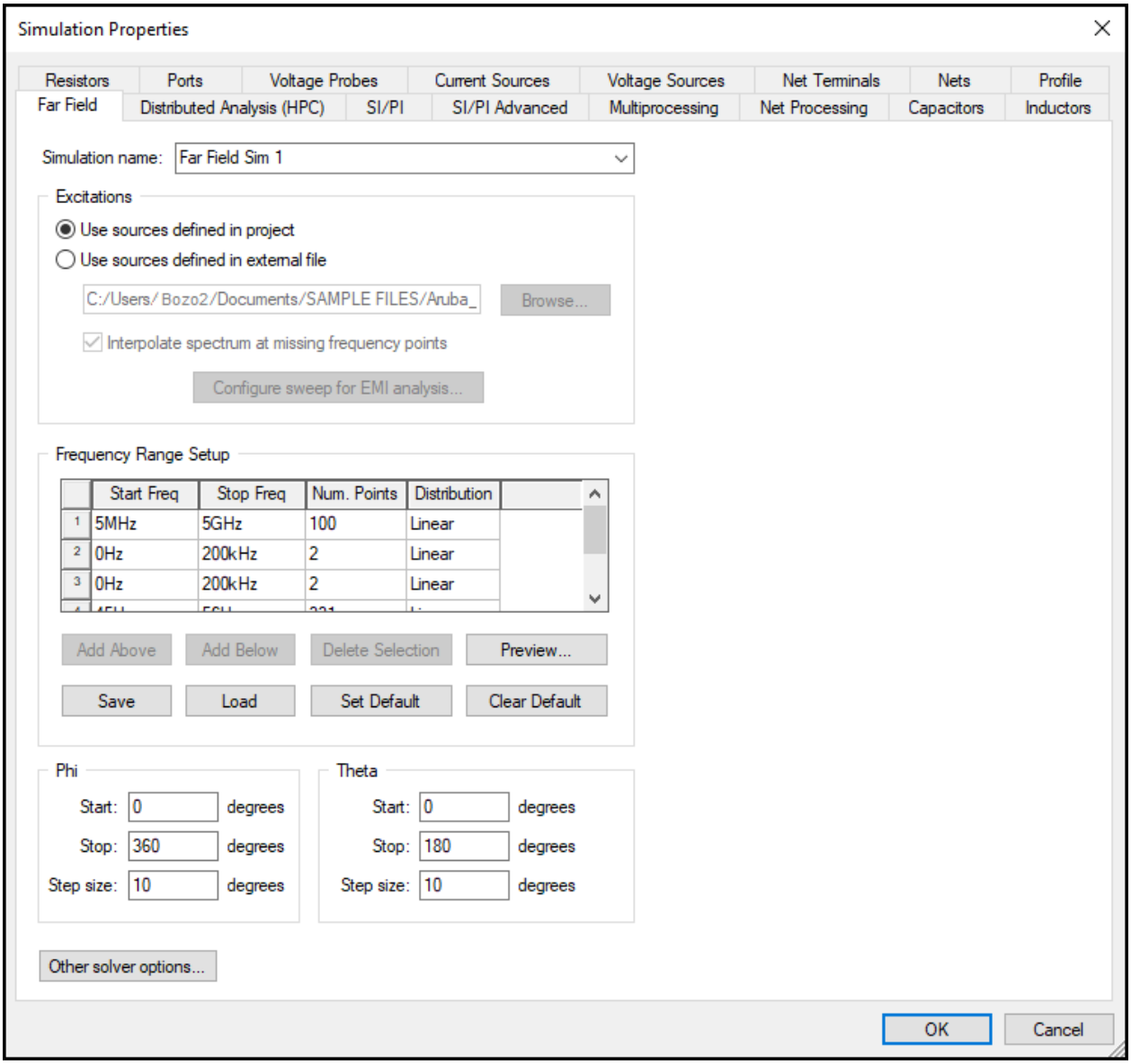

From this menu, you can also view far field results.

Computing DC IR Simulations

DC IR analysis solves for the voltage drop across the power plane. The DC solution provides important information pertaining to power delivery, including:

- Status of the voltage regulator to determine if it is functioning and supplying the proper DC voltage to all active components attached to power rails
- DC current density information to warn where board or via damage may occur

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SIwave makes use of a dedicated DC solver that is based on a well-known formulation and produces an efficient DC solution.

SIwave can perform the following actions:

- Compute DC voltage and current density for a given source configuration
- Compute IR-drop and current flow within each element in a PCB model (resistor, inductor, via, trace, plane, bondwire, source, etc.)
- Perform adaptive mesh refinement for increased accuracy

The DC IR simulation provides a connection to the thermal solver Ansys Icepak. If appropriate, export the DC IR data to Icepak after analysis, or import a temperature map from Icepak to use in the DC IR simulation.

> **Note:**
>
> As a preliminary step, users may want to define equipotential regions.

Users can configure component parameters prior to simulation from the **SIwave Workflow Wizard** or skip directly to "Setting Up the Compute DC Current and Voltage Distribution Window" on page 9-86.

Beginning Simulation From the SIwave Workflow Wizard

Complete the following steps to begin configuring a simulation from the **SIwave Workflow Wizard**.

1. From the **SIwave Workflow Wizard**, select **Configure DC IR Drop Analysis** to open the **DC IR Configuration** window.

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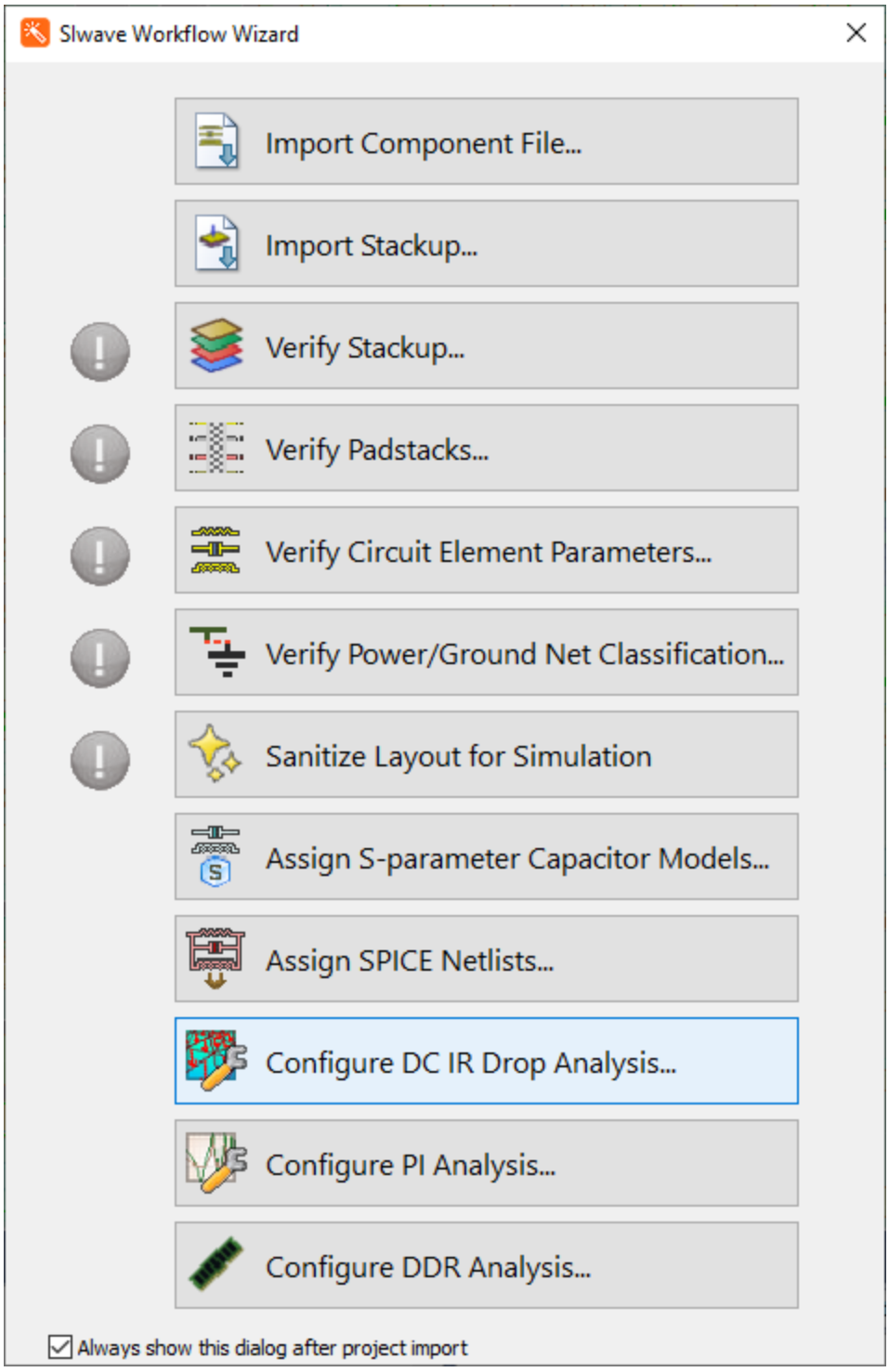

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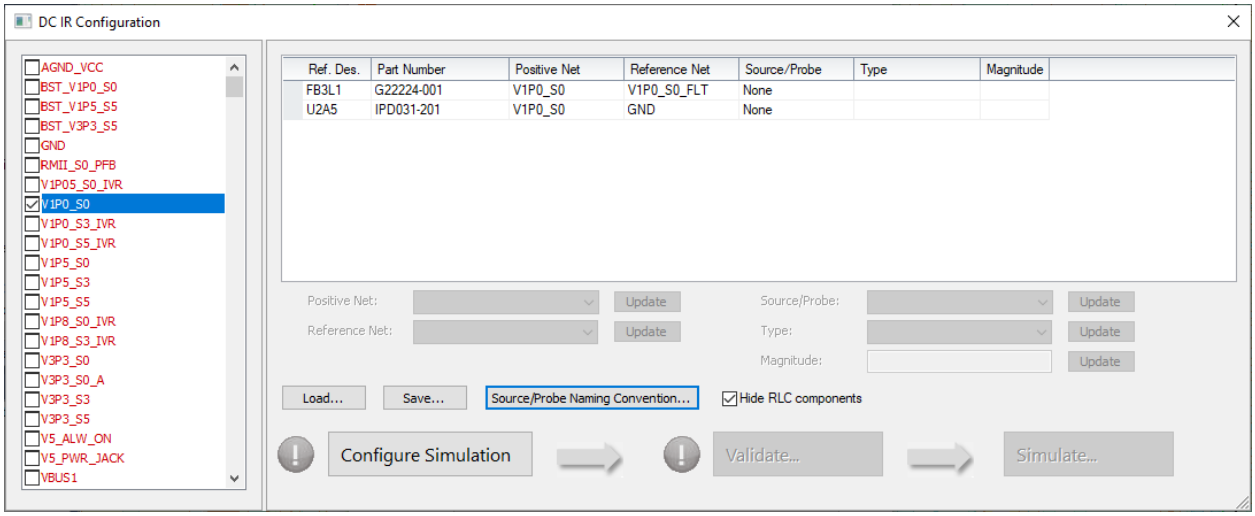
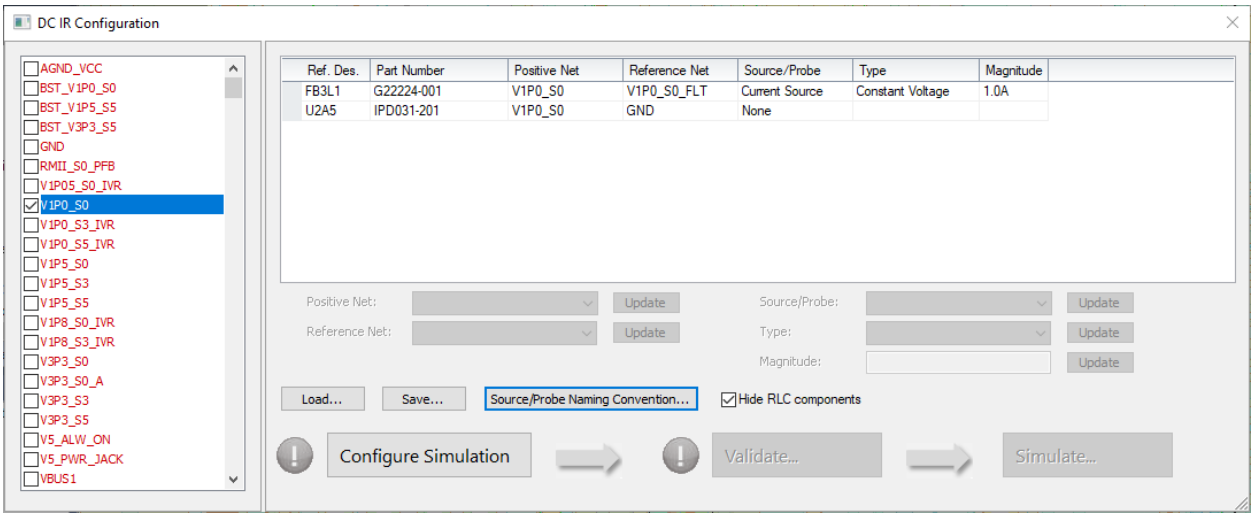
2. From the list on the left, check the box adjacent to an appropriate net (e.g., **V1P0_S0**).



3. From the table, do the following:

   a. Make selections from the **Source/Probe**drop-down menu (i.e, select **None**, **Current Source**, **Voltage Source**, **Voltage Probe**, or **Terminal**) .

   b. The **Type** drop-down menu is enabled if **Current Source** or **Voltage Probe** are selected from the **Source/Probe** drop-down menu. Select either **Constant Voltage** (i.e., adding one circuit element) or **Distributed Current** (i.e., adding a circuit element on every pin) from the **Type** drop-down menu.



   c. Enter a **Magnitude** in the field or accept the default parameter, if any.

   d. Select the left-most empty cell in the component's row to populate the fields beneath the

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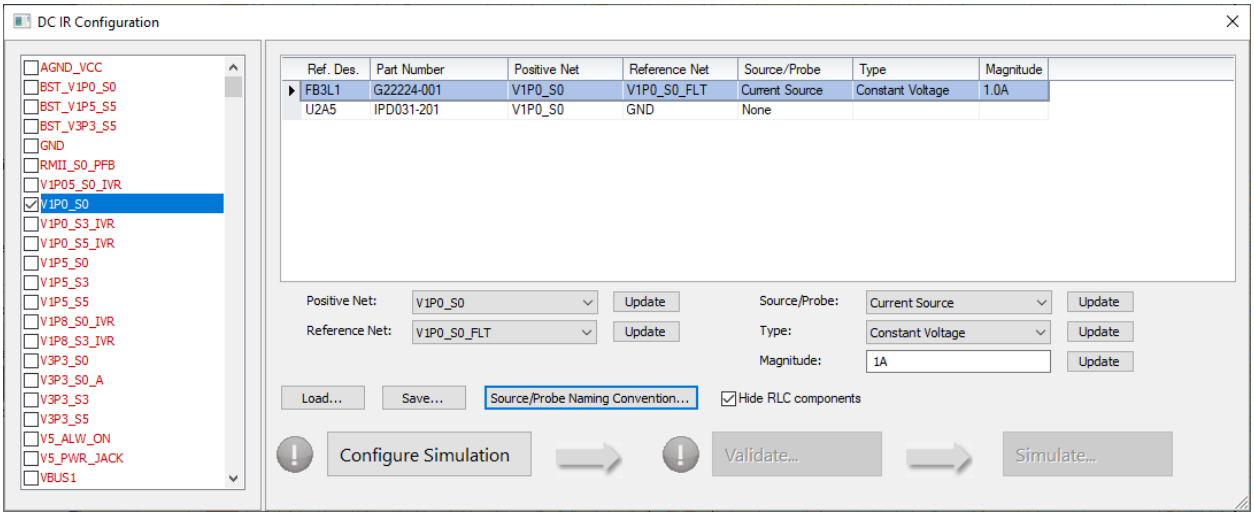
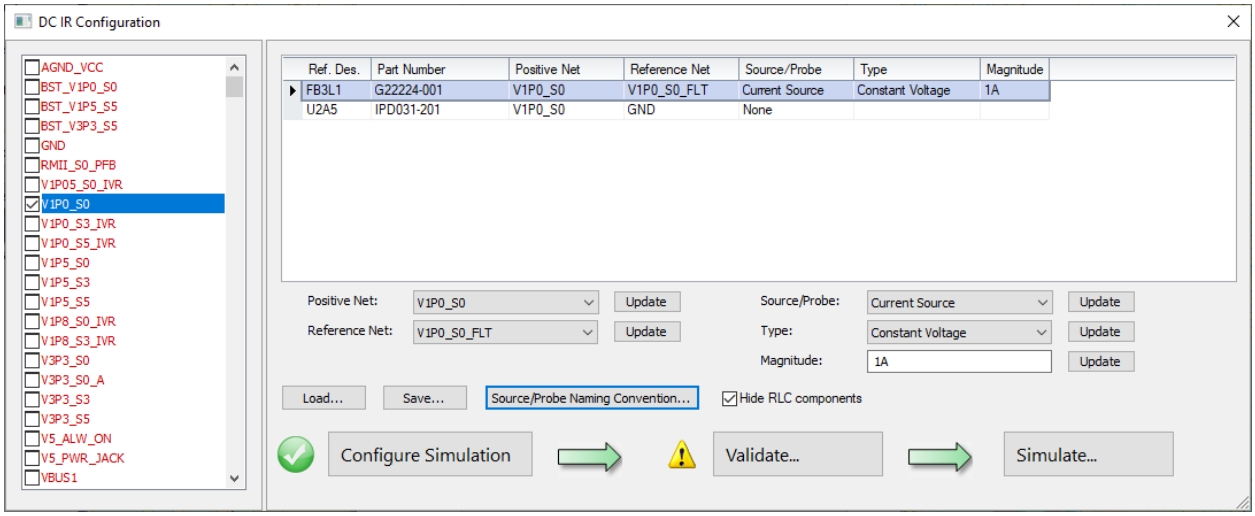
table. Then make further adjustments, as appropriate.



4. Click **Configure Simulation**.



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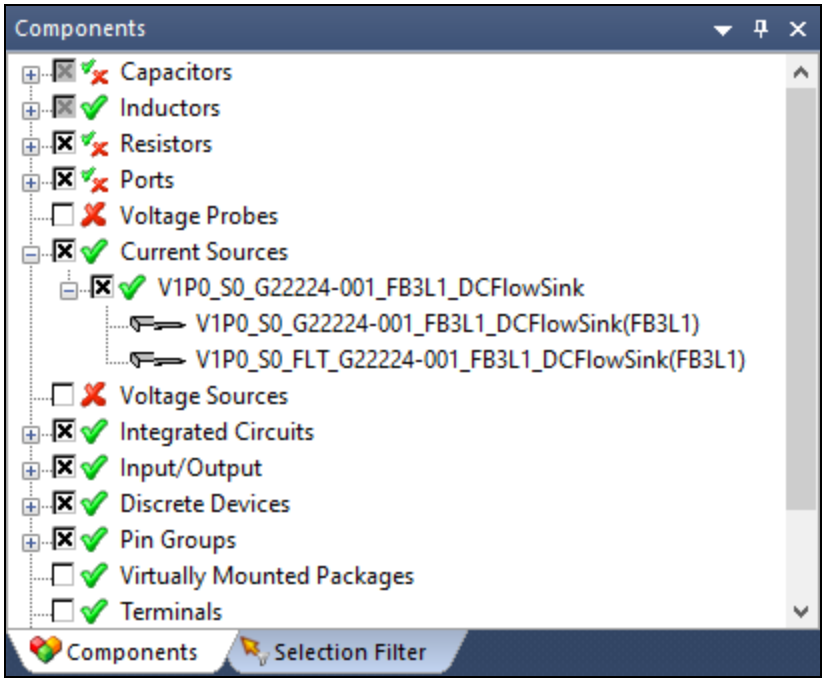
The **Components** window will populate with an appropriate sources/probes.



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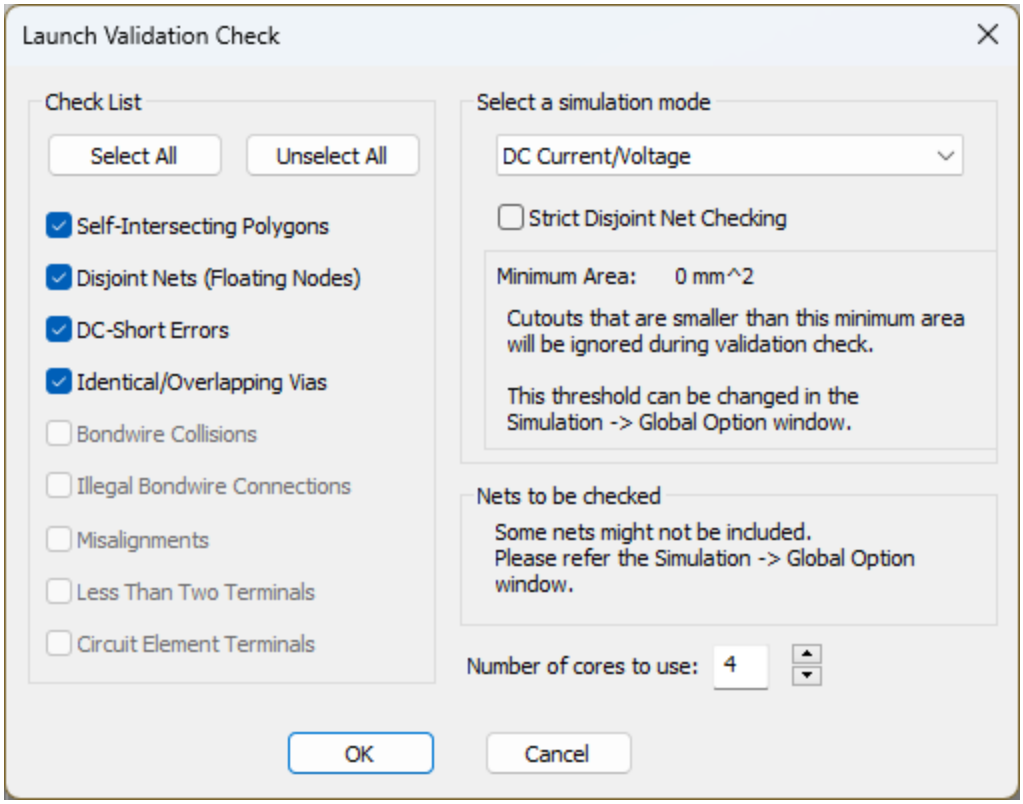
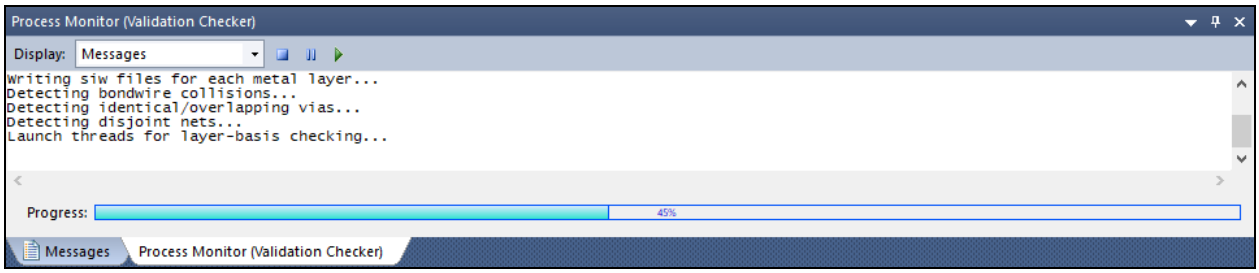
5. Click **Validate** to open the **Launch Validation Check** window.



6. If appropriate, configure the validation check. Then click **OK** to begin validation. View progress in the **Process Monitor (Validation Checker)**.



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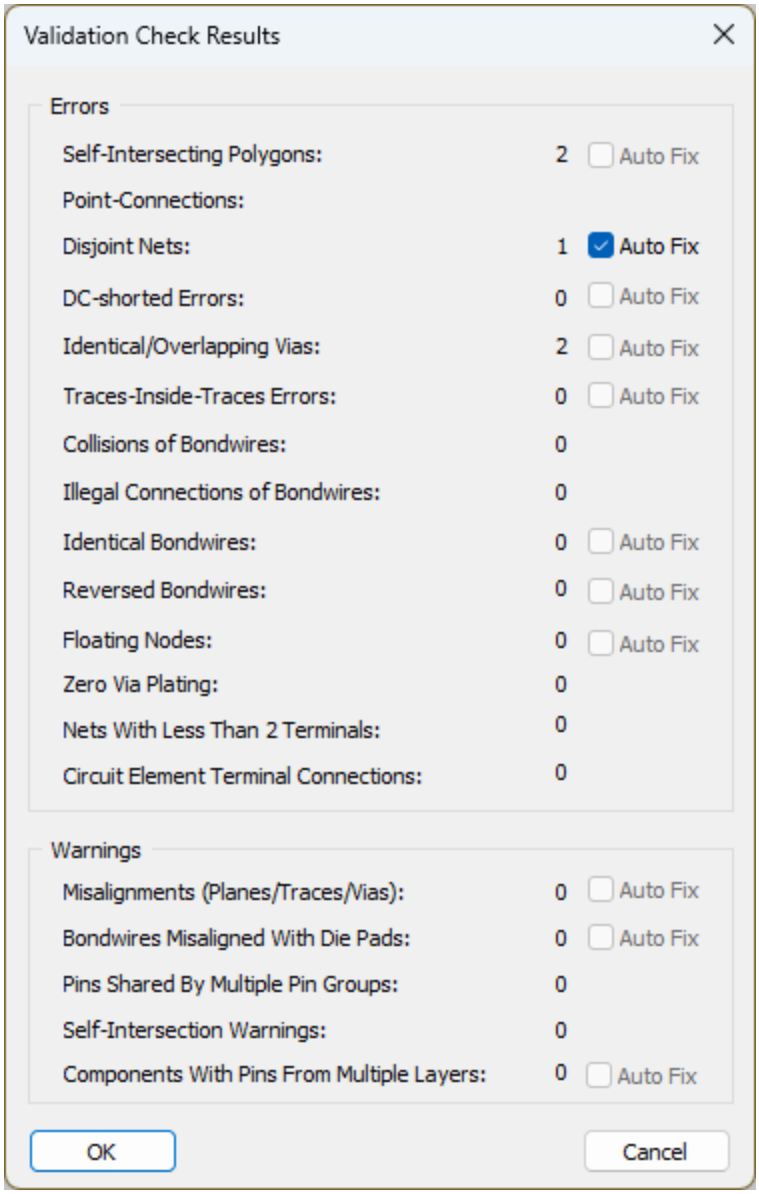
7. After the validation check is complete, a **Validation Check Results** window appears.



8. Assuming the simulation has passed validation, click **OK** to return to the **DC IR Configuration** window.

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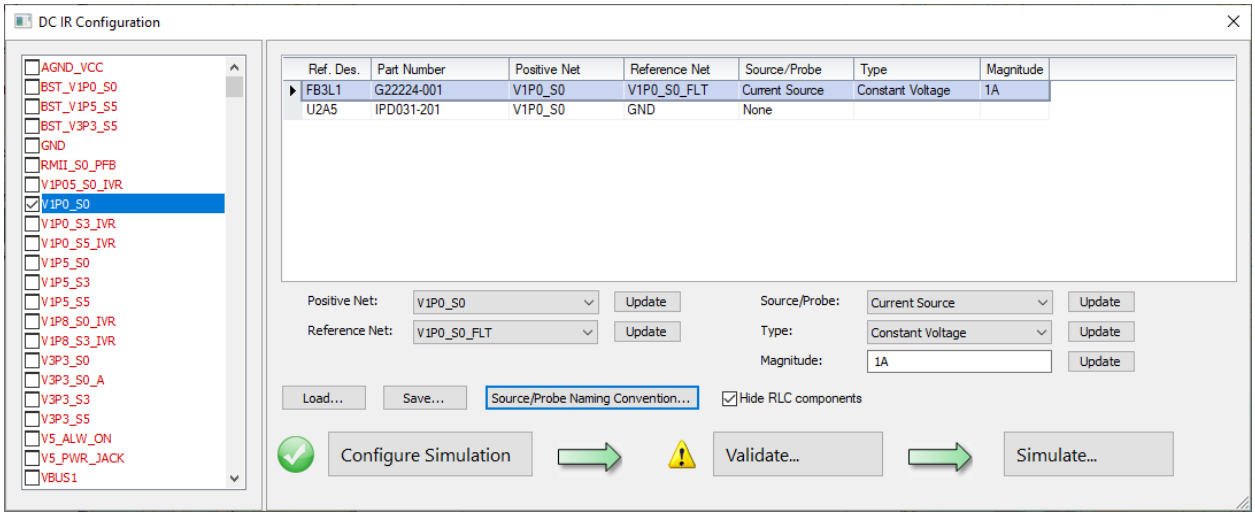
9. Click **Simulate** to open the **Compute DC Current and Voltage Distribution** window.

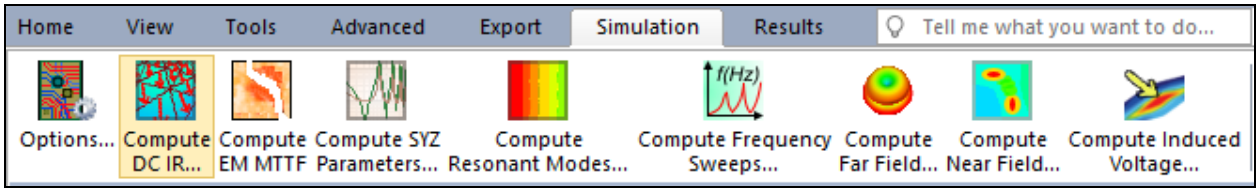


10. Continue to step 2 of "Setting Up the Compute DC Current and Voltage Distribution Window" below.

Setting Up the Compute DC Current and Voltage Distribution Window

Complete the following steps to finalize simulation solver setup and run a simulation.

1. From the **Simulation** tab, click **Compute DC IR** to open the **Compute DC Current and Voltage Distribution** window.



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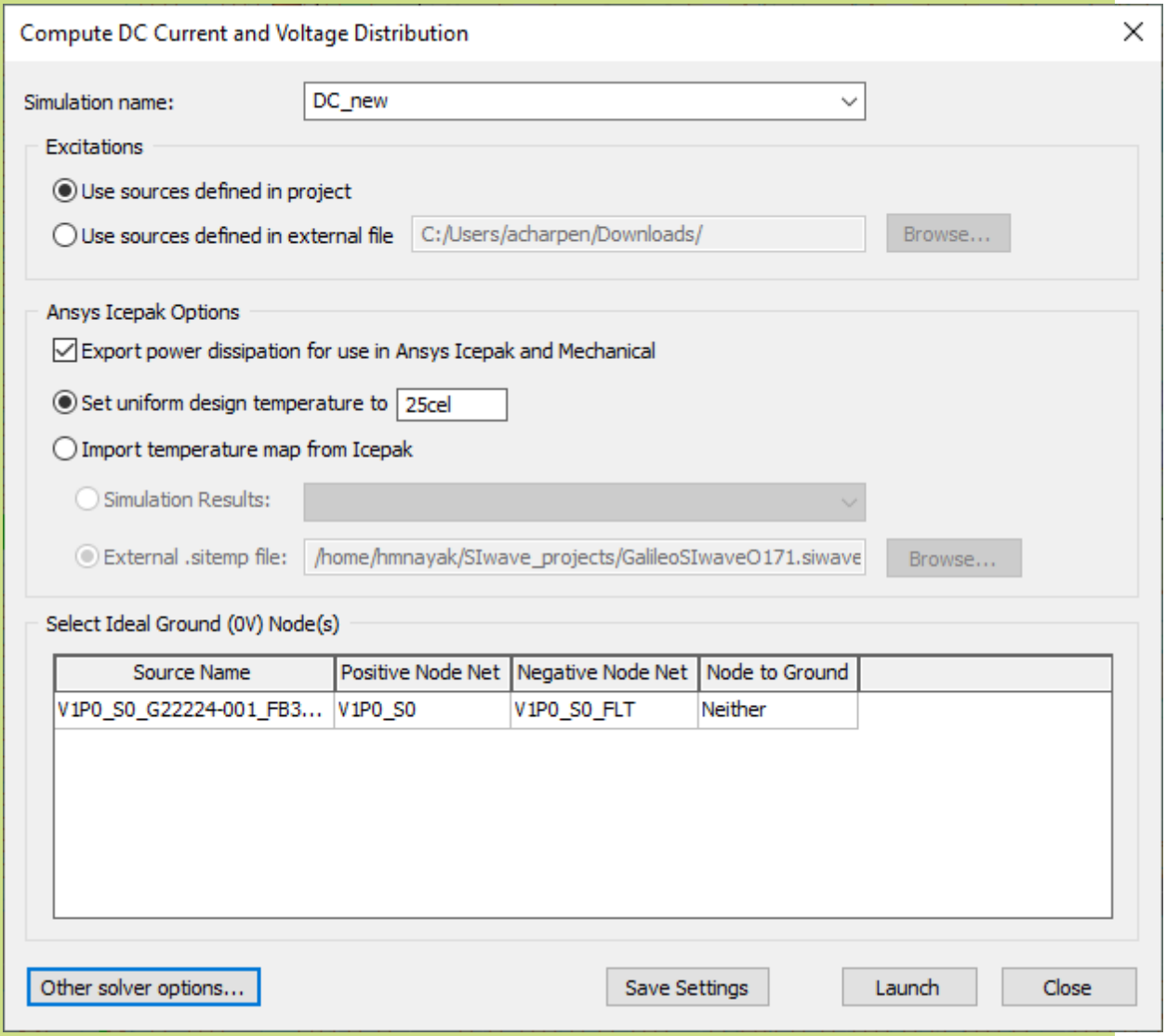
Note:

DC thermal information is provided when requested for use in Icepak simulations using a full-resolution meshed power map.



2. From the **Simulation Name** field, enter a name for the DC IR simulation.
3. From the **Ansys Icepak Options** area:
   - Check **Export power dissipation...** if users want to export data to Ansys Icepak or Mechanical.

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- Select either:
  - **Set uniform design temperature...** and enter a value, in celsius. This sets a global design temperature and is used to modify the conductivity of metallization during the DC IR simulation. In general, the higher the temperature, the lower the conductivity (implying a higher resistance).
  - **Import temperature map...** and select an Icepak temperature distribution file, either from a previous simulation or from an external *.sitemp file. The temperature data can locally adjust DC conductivity.

    Resistivity of conductors is adjusted by:

    $$R = R_{ref}\left[1 + \alpha\left(T - T_{ref}\right)\right]$$

    Where:

    - R is the conductor resistance at temperature T.
    - R_{ref} is the conductor resistance at reference temperature T_{ref}.
    - α is the temperature coefficient of resistance for conductor material (4e-3 per degree Celsius for all materials in SIwave).
    - T is the conductor temperature in degrees Celsius.
    - T_{ref} is the reference conductor temperature in degrees Celsius at which the resistivity of a metal in the material definition is assumed to be taken (20 degrees Celsius in SIwave).

4. From the **Select Ideal Ground Node(s)** area, choose a ground node from the table. Select a current or voltage source at 0 volts (ideal ground). All other voltages are computed with respect to this node. If no ideal ground node is selected, SIwave automatically picks a source terminal to ground.
5. Use the **Node to Ground** drop-down menu to select **Neither**, **Negative**, or **Positive**.

   If users select **Negative** on a voltage source, the voltage display on its ground pin will be 0 V.

   If users select **Positive** on a voltage source, the voltage display on its ground pin will be negative.

   Consider this as being the 0 node in a SPICE simulation. This is the node to which all voltages should be referenced. Since SIwave includes the return paths of all planes (including the ground), we cannot assume that all of the sources reference that 0 node. Thus we have to pick one to be the absolute 0 node reference. So if we put the 0 node on the positive side of a voltage plane, the "ground" or return path would show as negative.
6. Click **Save Settings**.
7. To view additional solver options, click **Other solver options**.

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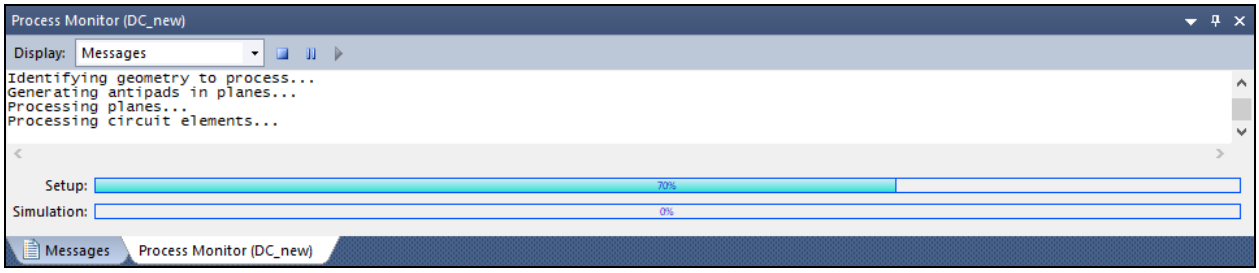
8. Click **Launch** to begin the simulation. View progress in the **Process Monitor**.



> **Note:**
>
> If the simulation is canceled while it is running, and even if one iteration has been completed, the last refinement iteration will display.

Viewing DC IR Results in SIwave

After performing a DC IR simulation, view the following result types from the DC IR Results Menu:

- Currents/Voltages Plot
- Icepak Power Map
- Voltage Probes Plot
- Element Data
- Loop Resistance Info
- Path Resistance Matrix
- RL Table
- Plot Solver Convergence

Complete these steps to view any of the following results.

1. From the **Results** window, expand **DC IR Drop Simulations**.
2. Right-click an appropriate simulation.

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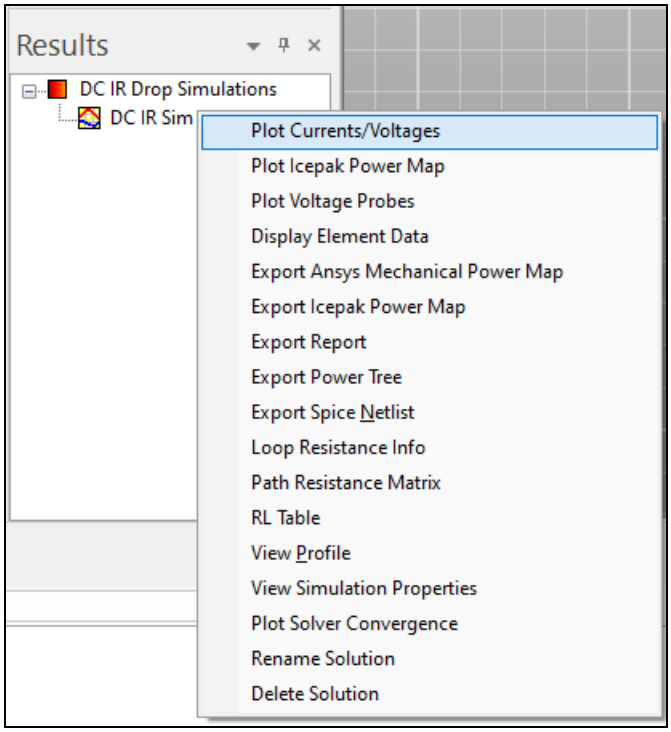
3. Click a result type to open.



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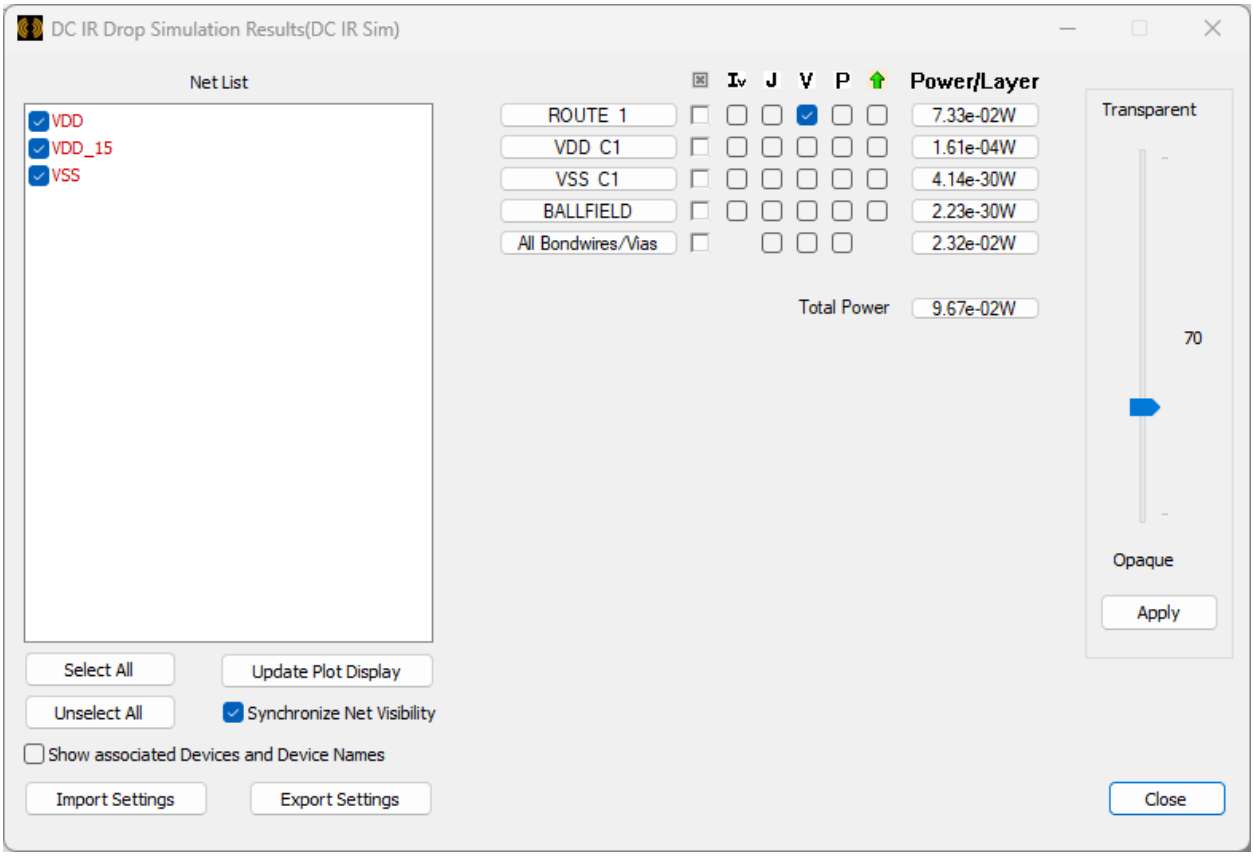
Plot Currents/Voltages



From the **DC IR Drop Simulation Results** window, select from the following combination of nets, layers, and element parameters to view plot overlays in the **Modeling** workspace:

- **Net List** area — check boxes to view nets with associated plots.
- **Power Layer** table — check boxes to view field quantities on any combination of layers. Only one type of field quantity (i.e., **Iv** (via current), **J** (current density), **V** (voltage), or **P** (power)) can be viewed at a time, but any combination of layers can be active. The **Modeling** workspace updates dynamically to show selected currents/voltages.

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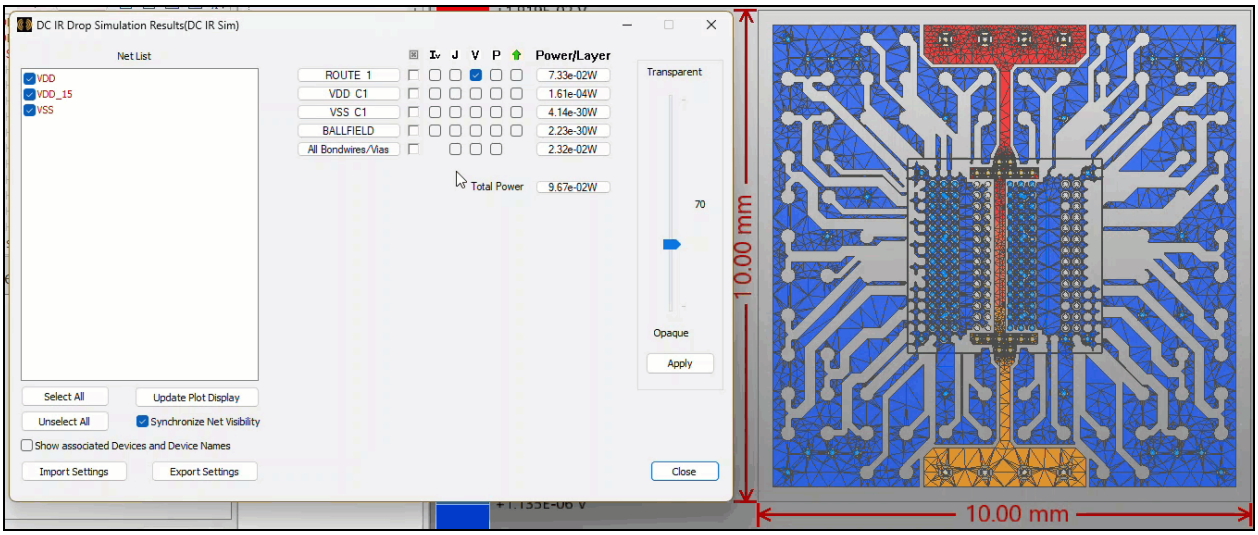
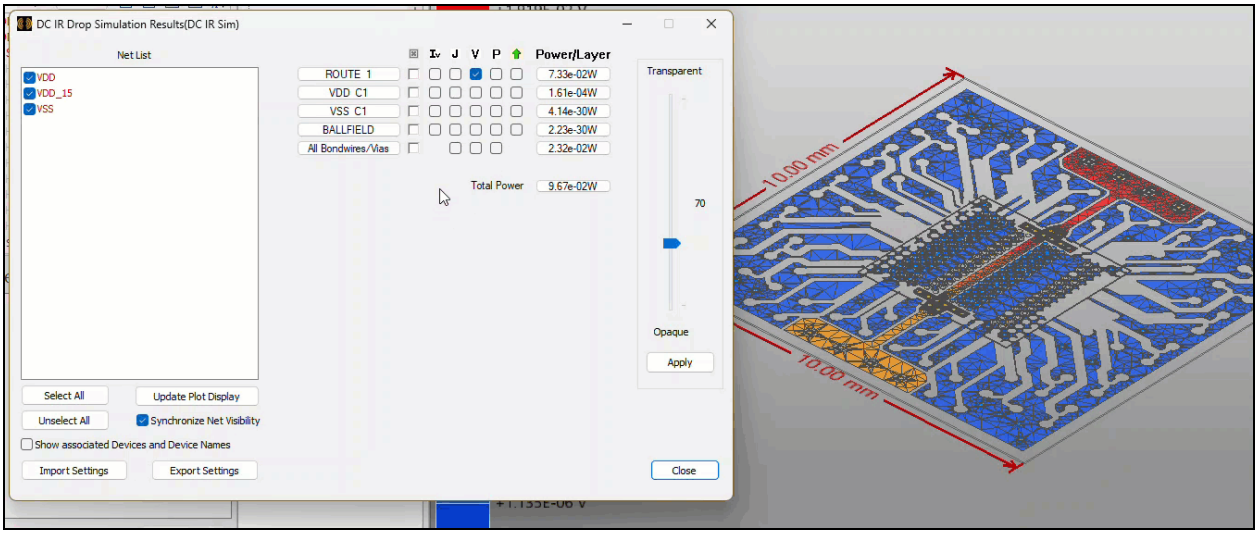


Check any box in the elevation column (i.e., the green arrow) to raise the component mesh in the **Modeling** workspace. Only available for components on metal layers.



- **Synchronize Net Visibility** checkbox — check to return to default settings.
- **Transparent**slider — adjust the slider and click **Apply** to set element visibility.
- **Import Settings** — import previously saved settings as an XML file.
- **Export Settings** — save the current settings as an XML file.

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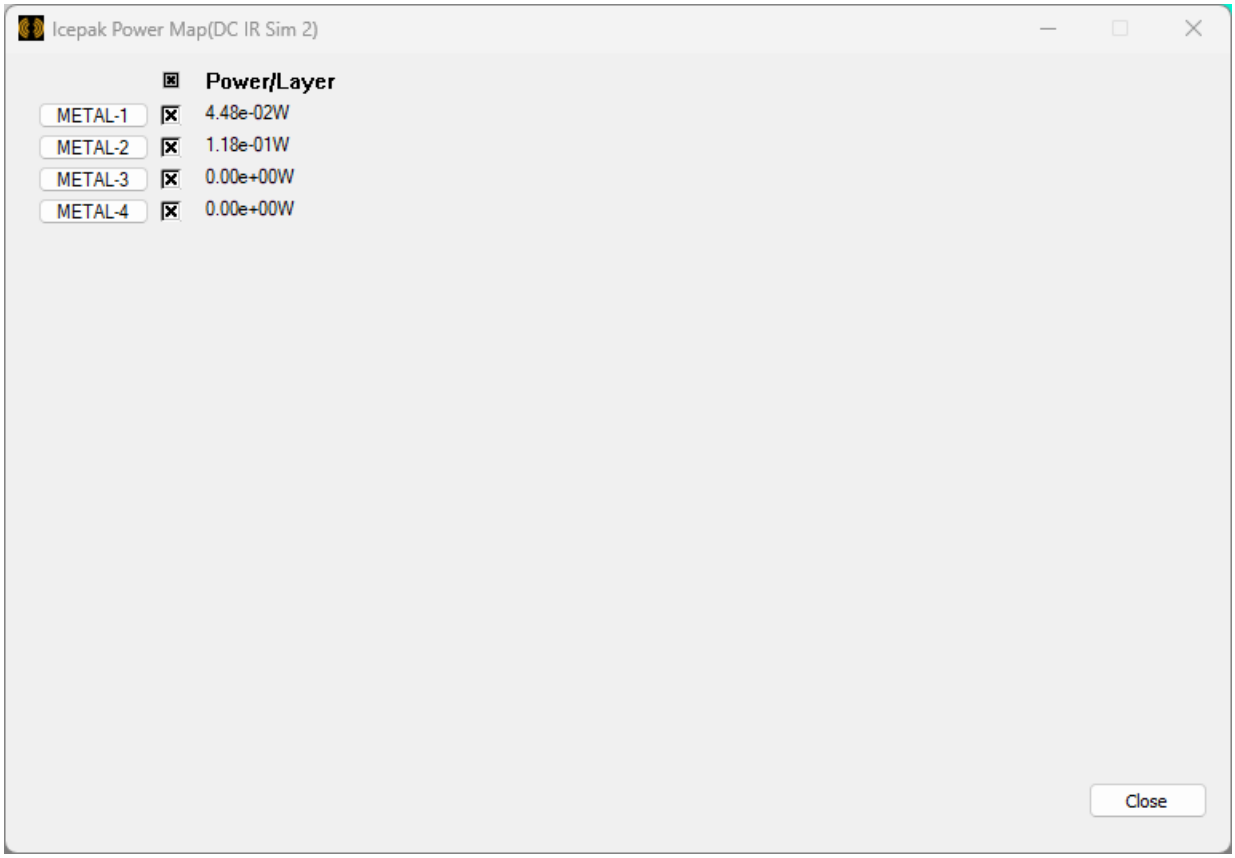
Plot Icepak Power Map



From the **Icepak Power Map** window, check boxes to select layers for which Icepak results display.

> **Note:**
>
> **Plot Icepak Power Map** only works if, during simulation setup, users check the **Export power dissipation for use in Ansys Icepak and Mechanical** box (i.e., located in the **Compute DC Current and Voltage Distribution** window > **Ansys Icepak Options** area. Refer to Computing DC IR Simulations.

Voltage Probe Plot

To immediately overlay a voltage probe plot in the **Modeling** workspace, click **Plot Voltage Probes**.

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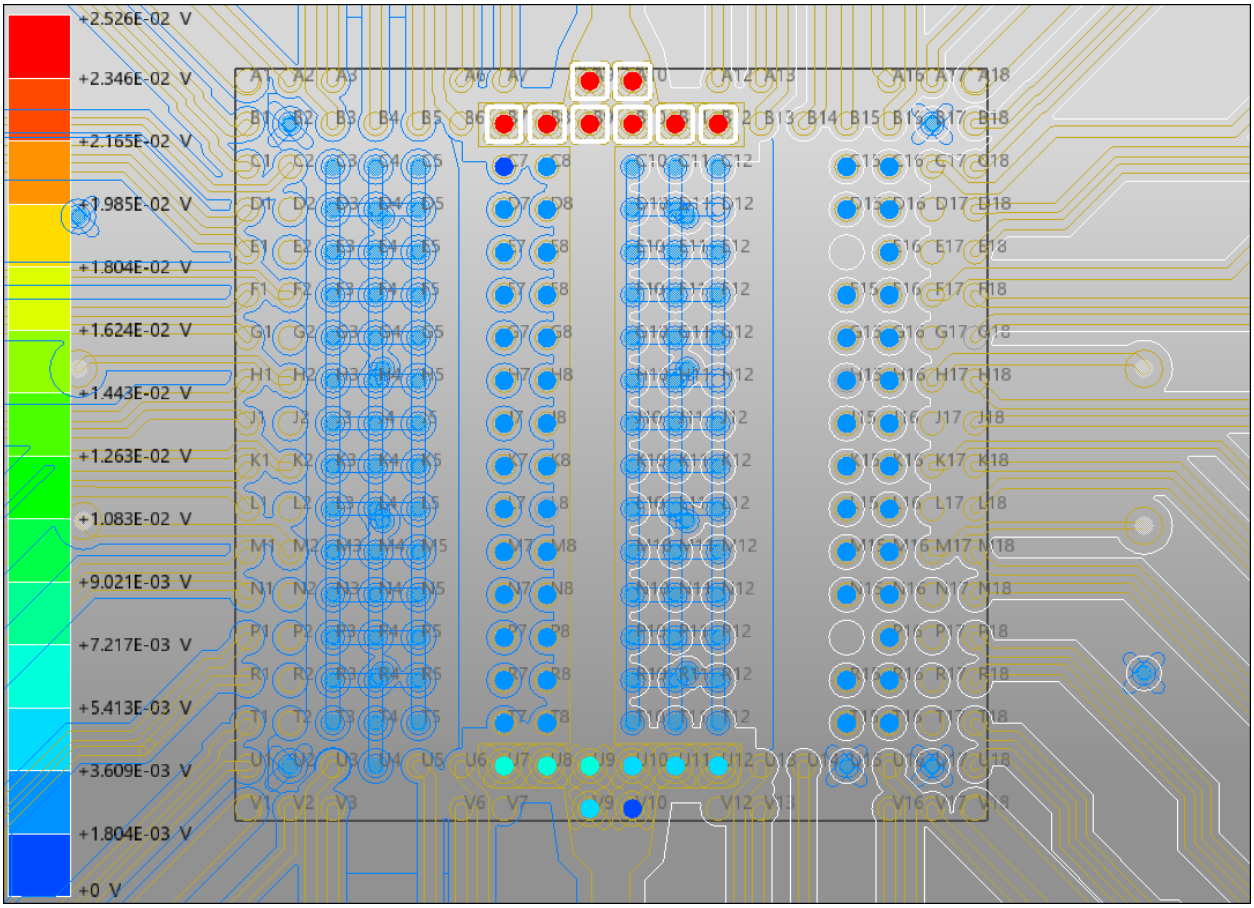

Right-click any voltage to highlight probes with that voltage (e.g., in the previous screenshot, the +2.526E-02 V probes are highlighted in white).

Display Element Data

From the **DC Simulation Element Data** window, select any combination of nets, layers, and element parameters to view plot overlays in the **Modeling** workspace:

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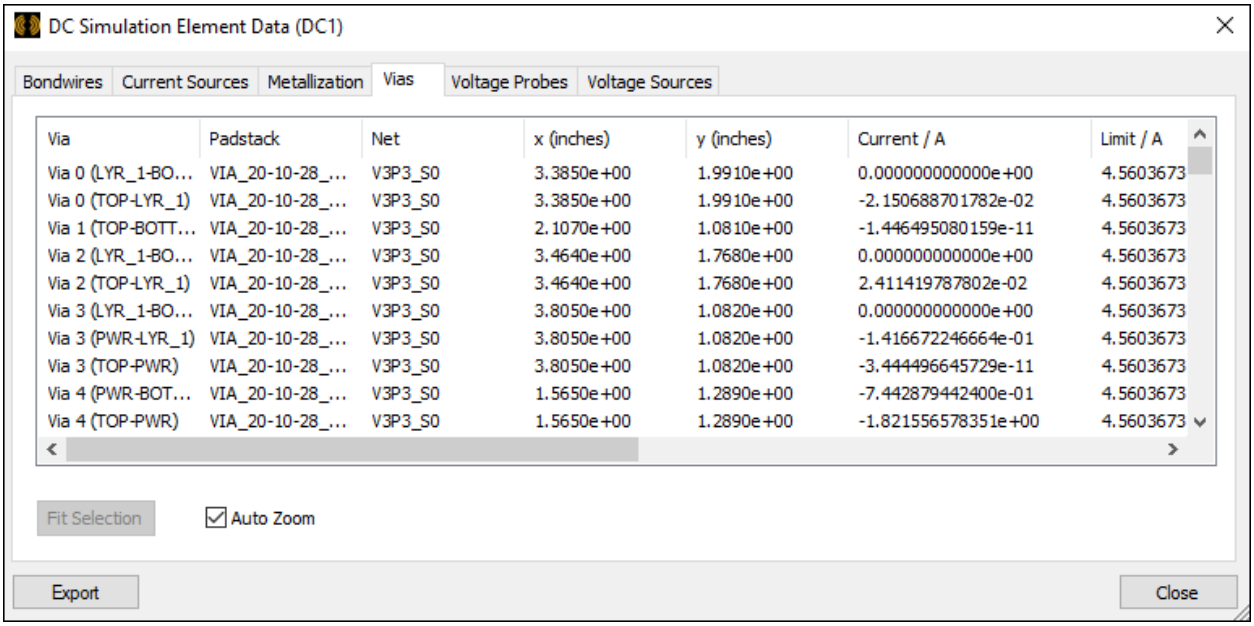

Selecting an element populates the **Properties** window with information about it. When **Auto Zoom** is enabled, selecting an element also zooms the Modeling workspace to that element. Elements are sorted into the following tabs:

- **Bondwires** — displays a list of bondwires. The Pass/Fail column displays **Pass** if the total current is less than or equal to the current limit flowing through the element (see: Technical Notes).
- **Current Sources** — displays a list of current sources, along with their voltage and current.
- **Metallization** — displays a list of areas with a specified voltage, current density, or power density. To populate the list, enter an appropriate information and click **Find**.
- **Vias** — displays a list of vias. The Pass/Fail column displays **Pass** if the total current is less than or equal to the current limit flowing through the element (see: Technical Notes).
- **Voltage Probes** — displays a list of voltage probes.
- **Voltage Sources** — displays a list of voltage sources.

Use the tabs to move between elements, and click column headers to sort the data. Click **Export** to save the data as a DC Element Data File (*.dc).

Loop Resistance Info

From the **Loop Resistance** window, make selections to see how the loop resistance is computed per pair of sources where the first source is the location of the measurement, and the second is the return path of the current loop. Note the source used as return path is shorted and the internal resistance is ignored.

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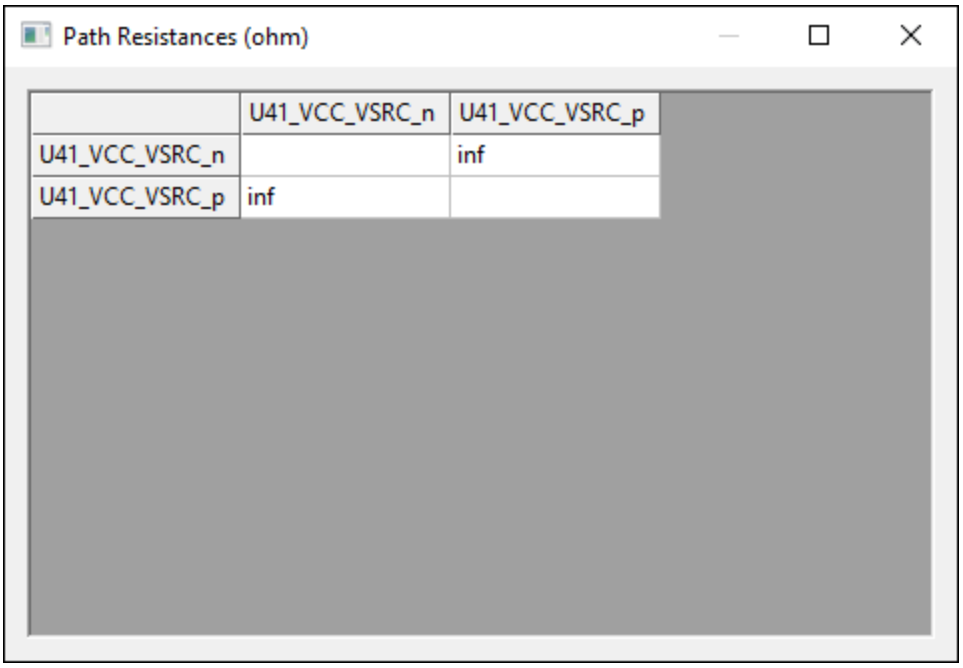
Path Resistance Matrix

From the **Path Resistances** window, view the resistances between pairs of terminals.



RL Table

Select **RL Table** to open the **DC RL Table** window.

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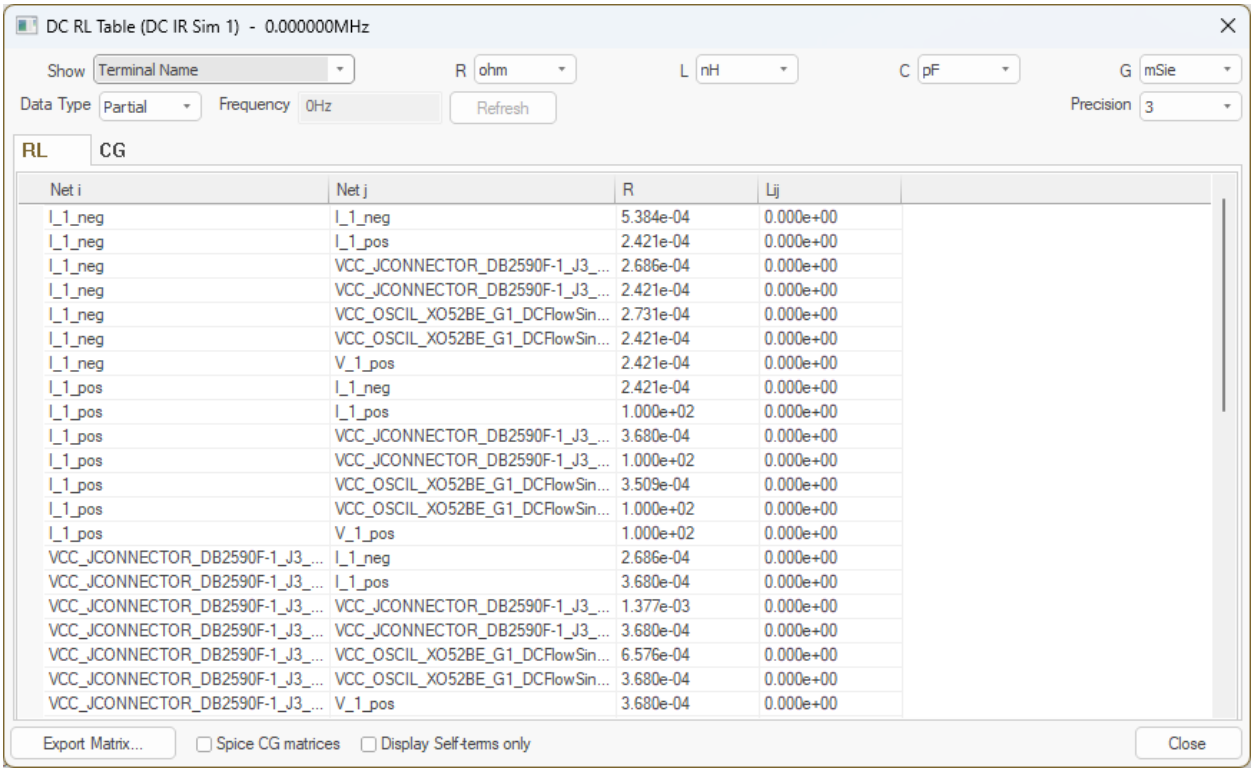

The RL table displays Q3D-like self and mutual resistance and inductance values computed by the DCIR solver in a list format. Every voltage and current source-based (i.e., driven) DCIR simulation includes a source with both a positive and a negative node, which are treated as terminals. During simulation, the solver selects one terminal on each net to designate as a sink, while the remaining $n-1$ terminals on that net are treated as sources. In DCIR terminal-based simulations, the terminal locations are set by the user, but the classification of source vs. sink follows the same logic as in driven simulations.

To measure resistance and inductance on a net, the solver injects 1 ampere (A) into each source terminal in turn and measures the voltage at all the source terminals, including the injection point, as the current flows to the designated single sink terminal.

Plot Solver Convergence

Select **Plot Solver Convergence** to open the **DCIR Solver Convergence Information** window.

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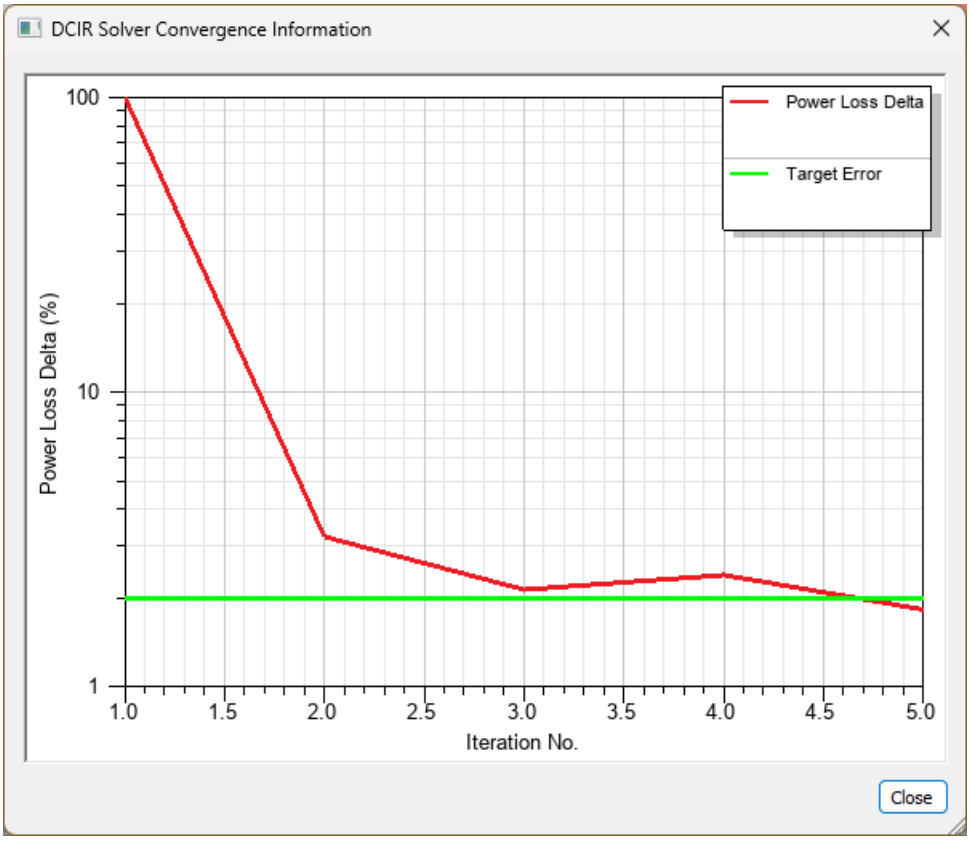

DC IR Results Menu Options

Navigate to the DC IR Results menu:

1. Click **Results**.
2. From the SIwave area, select **DC IR** > **[Simulation Name]**.

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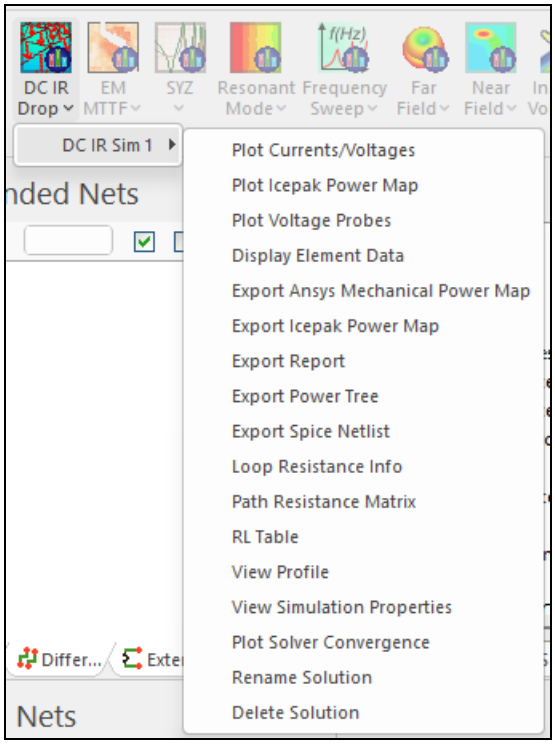

Menu options include:

- **Plot Currents/Voltages** – see Viewing DC IR Results.
- **Plot Icepak Power Map** – see Viewing DC IR Results.
- **Plot Voltage Probes** – see Viewing DC IR Results.
- **Display Element Data** – see Viewing DC IR Results.
- **Export Ansys Mechanical Power Map** – see Exporting DC IR Information.
- **Export Icepak Power Map** – see Exporting DC IR Information.
- **Export Report** – see Exporting DC IR Information.
- **Export Power Tree** – see Exporting DC IR Information.
- **Export Spice Netlist** – see Exporting DC IR Information.
- **Loop Resistance Info** – see Viewing DC IR Results.
- **Path Resistance Matrix** – see Viewing DC IR Results.
- **RL Table** – see Viewing DC IR Results.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the DC IR tab.
- **Plot Solver Convergence** – opens a window displaying DCIR solver convergence in a 2D AnsPlot.
- **Refinement Statistics** – opens a window displaying power loss statistics.

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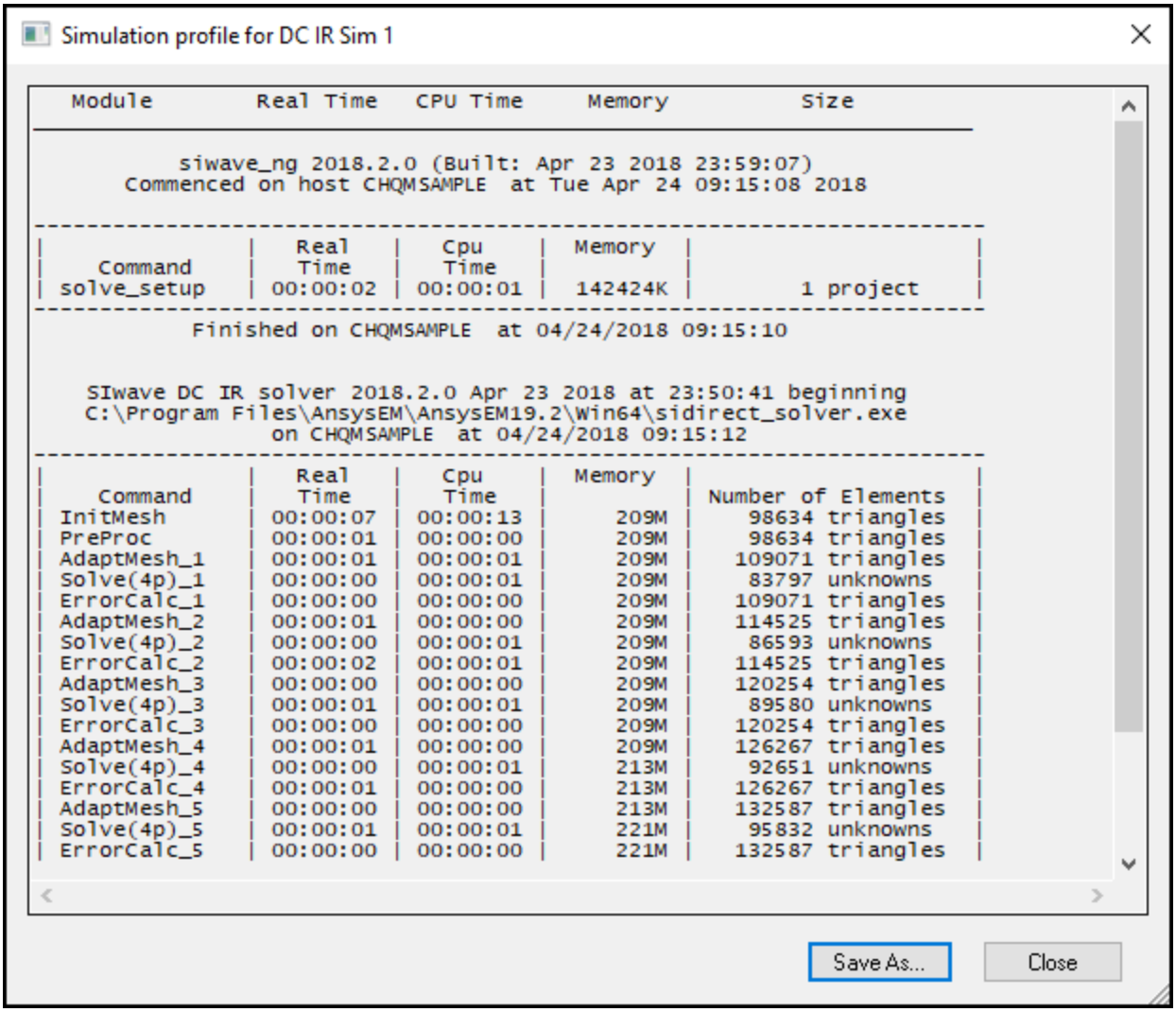
- **Rename Solution** – allows the user to rename the solution.
- **Delete Solution** – deletes the solution.
- Provide an option to plot DCIR solver convergence in a 2D (AnsPlot) graph

Simulation Profile:



Simulation Properties:

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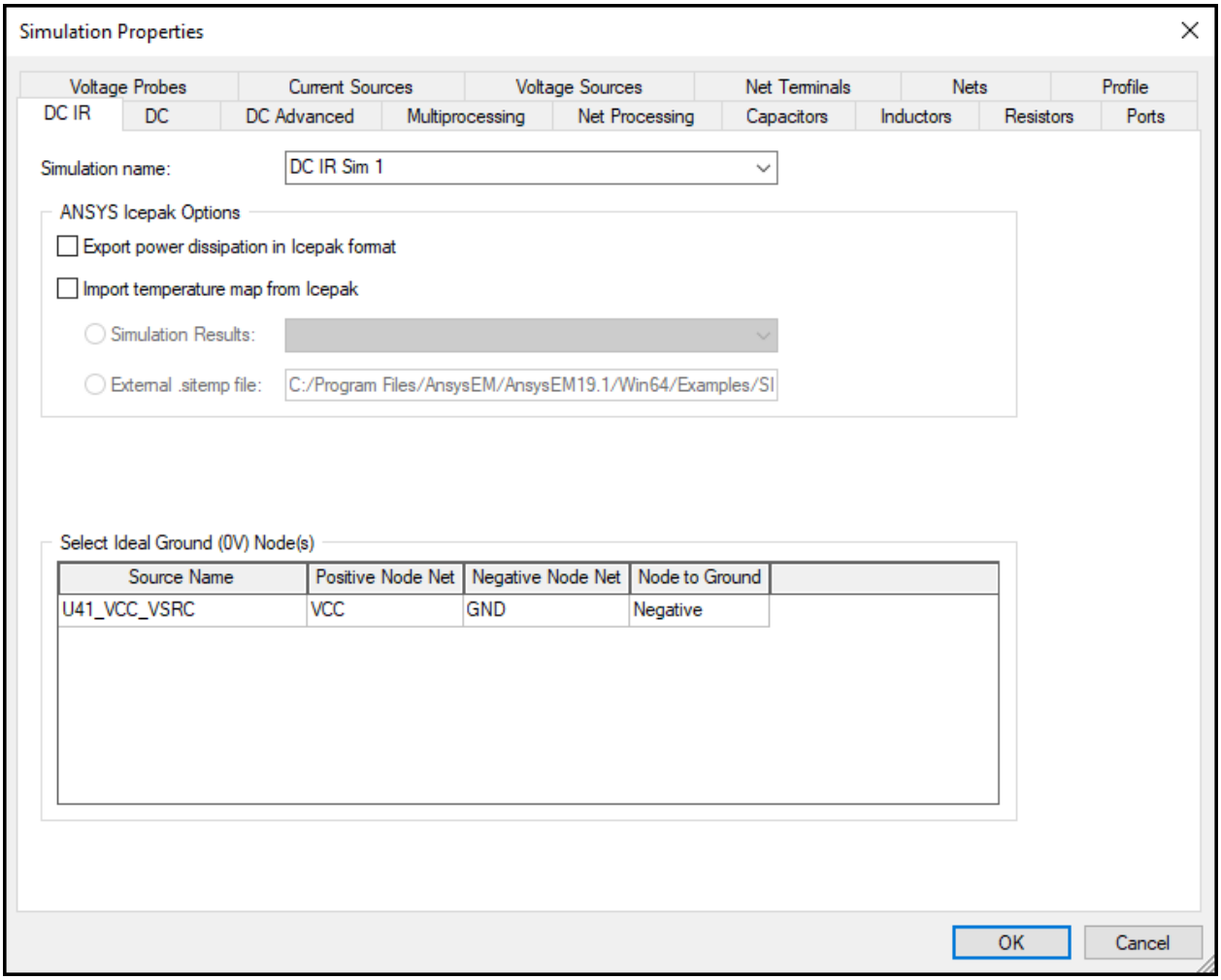

DCIR Solver Convergence Information Window:

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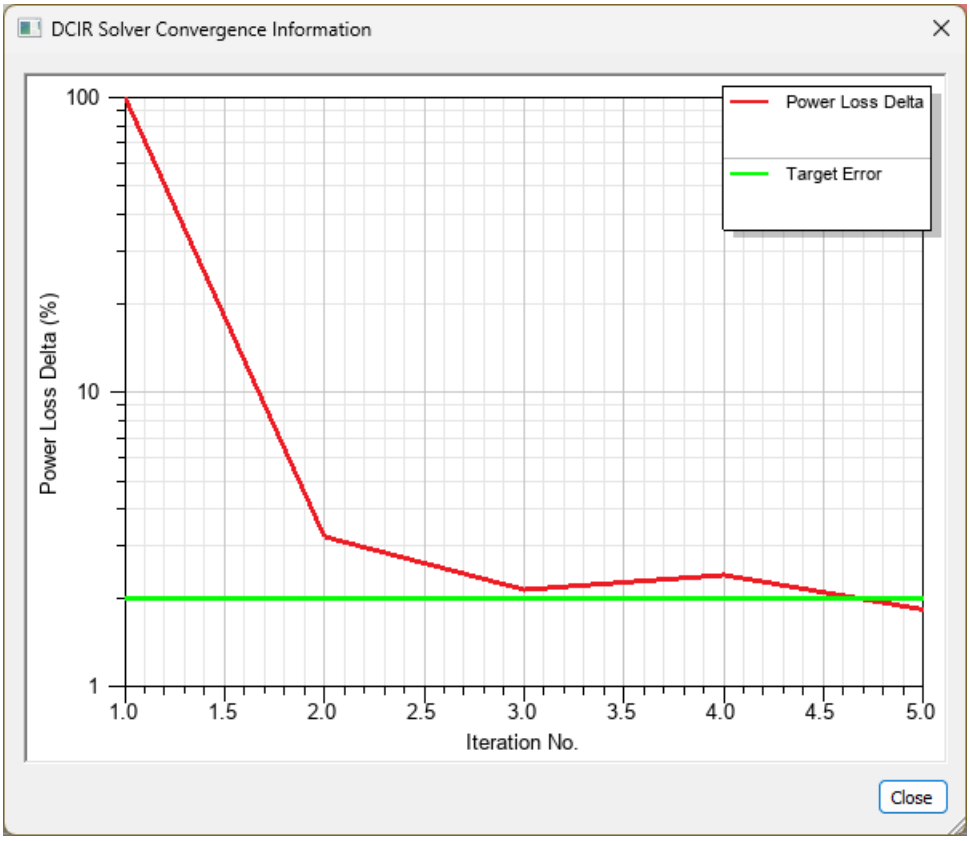

Exporting DC IR Information

Complete these steps to export DC IR information.

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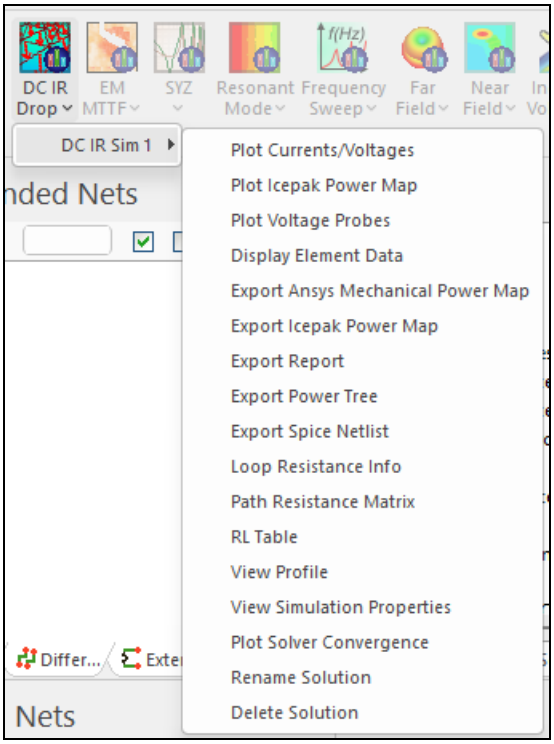
1. Do one of the following:
   - From the **Results** tab, select **DC IR Drop** > **[*Simulation Name*]** (e.g., **DC IR Sim 1**).



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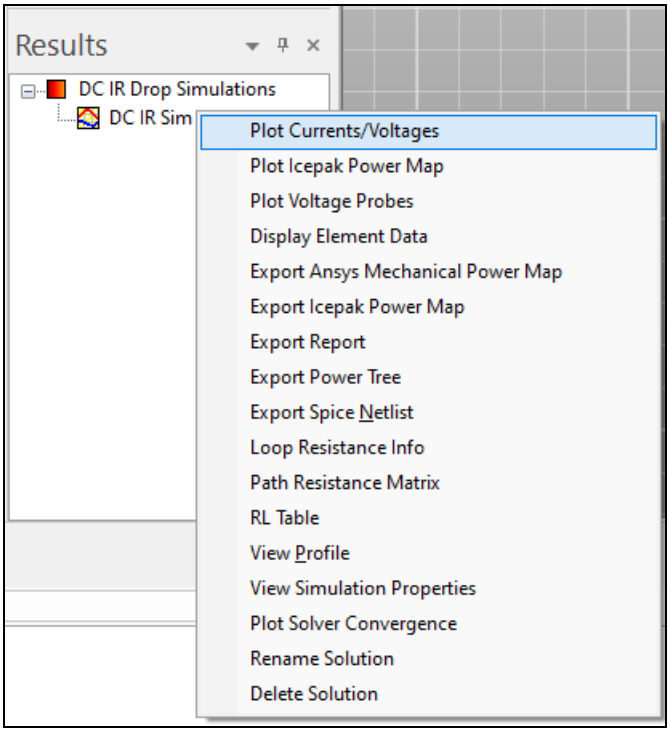
- From the **Results** window, right-click **[*Simulation Name*]** (e.g., **DC IR Sim 1**).



2. Select an appropriate export option. Export options include (but are not limited to) the following:
   - **Export Ansys Mechanical Power Map** – exports a power map.
   - **Export Icepak Power Map** – copies power dissipation files to a specified folder. These files can be opened using Icepak.
   - **Export Report** – exports a report in *.html format.
   - **Export Power Tree** – exports a power tree in *.png format (*.bmp on Linux). The power tree shows the current and voltage drop across each branch and component. Actual values are compared with the user's expected values, and determines the Pass/Fail result of each terminating component.
   - **Export Spice Netlist** – exports a SPICE Netlist in *.sp format.
3. A settings window opens with an appropriate options for the selected export type, such as the following examples.

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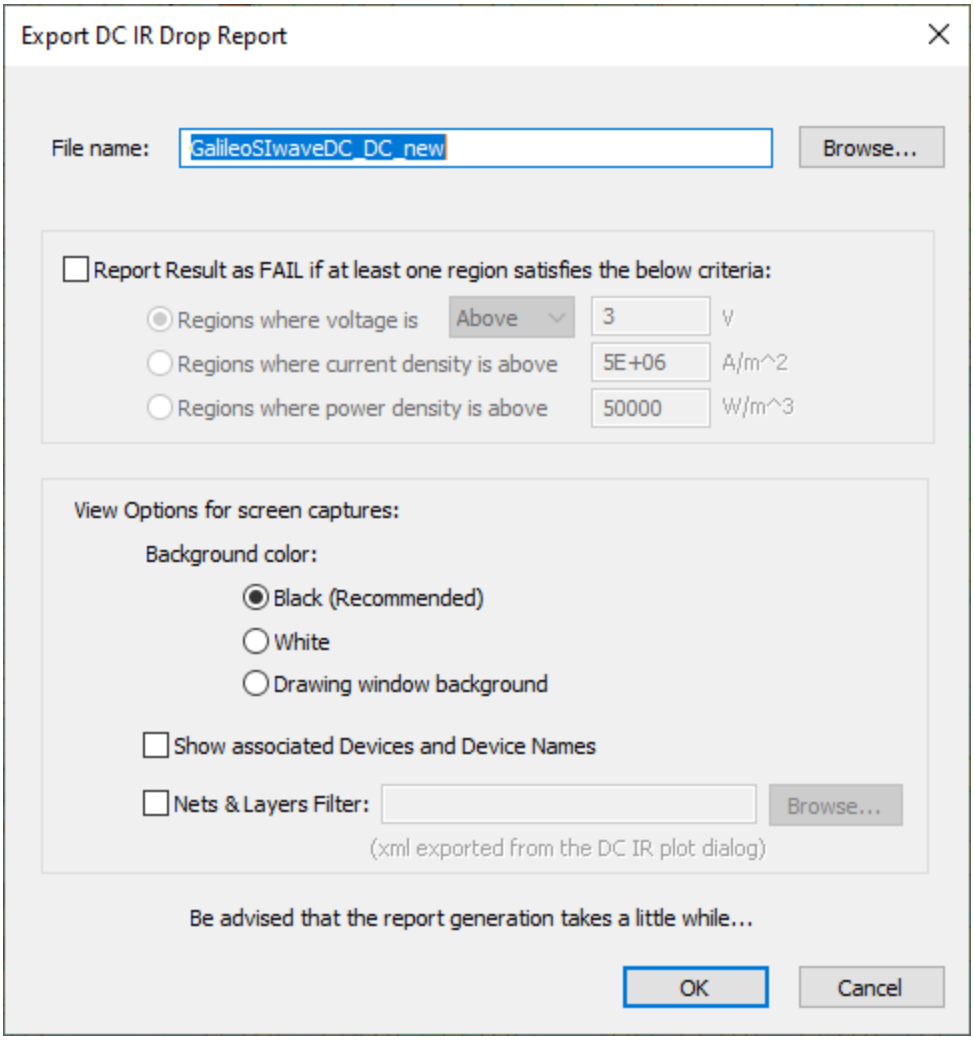
Export Report > Export DC IR Drop Report Window



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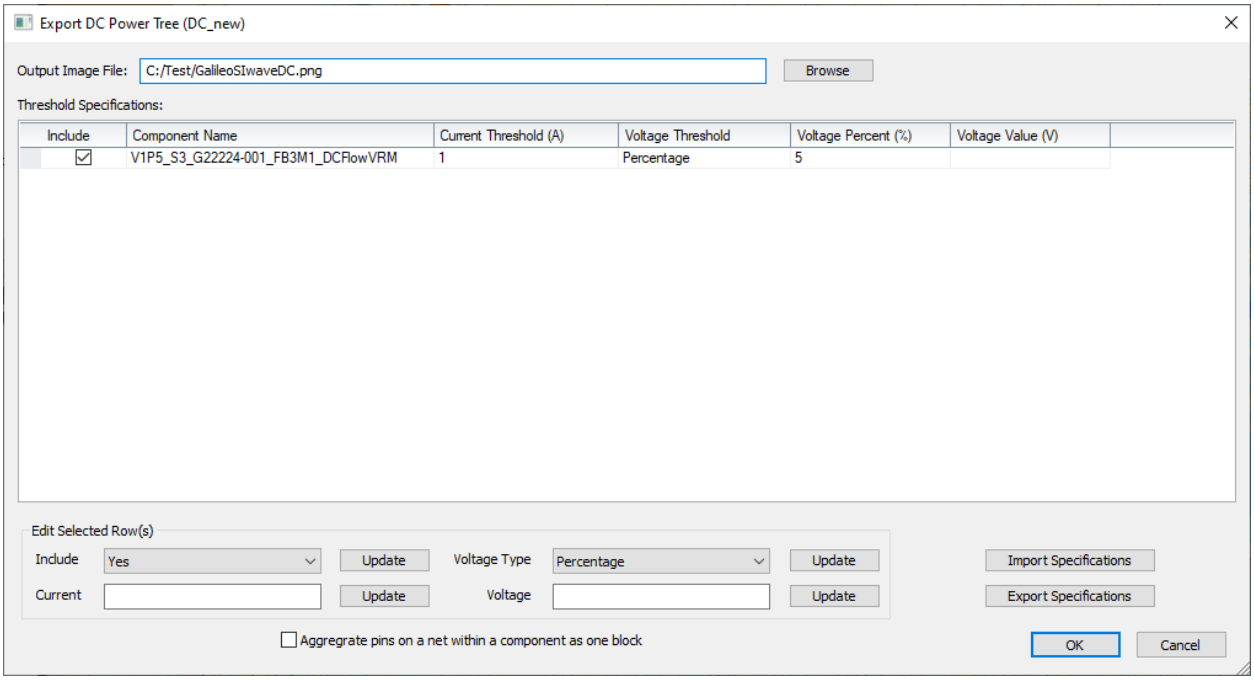
Export Power Tree > Export DC Power TreeWindow



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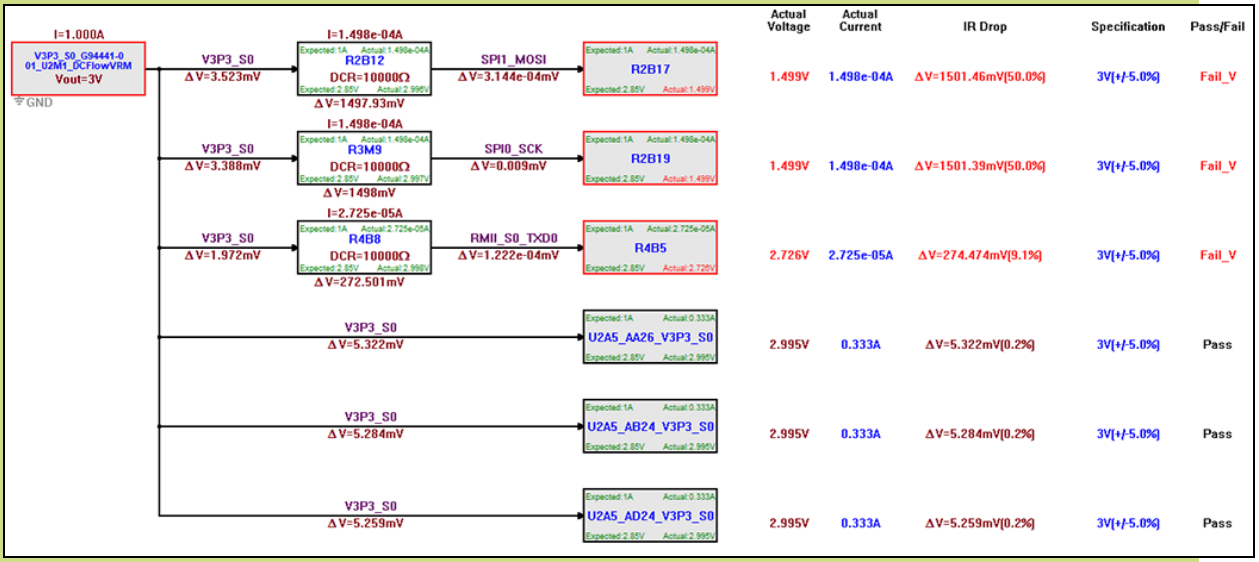
Note:

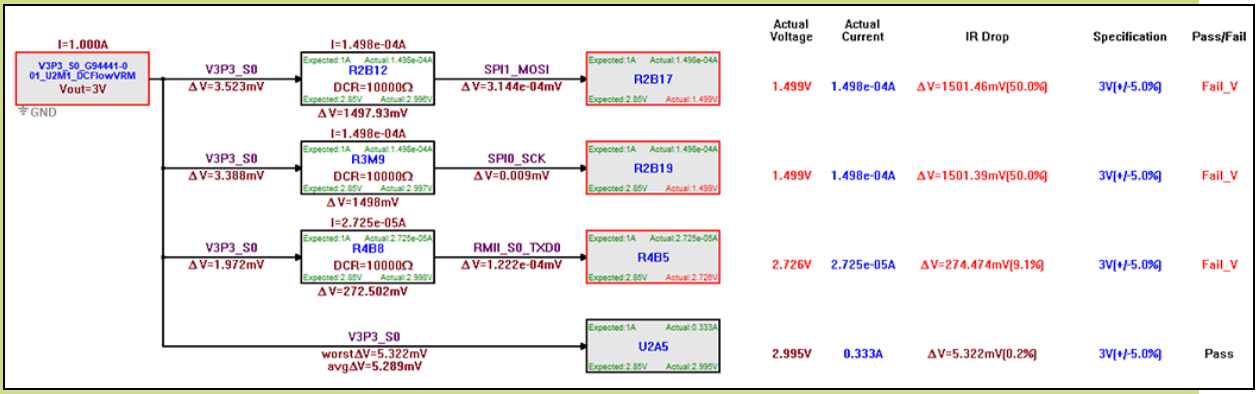
If the source/probe is a distributed current, all of the pins from a single component can be combined into one block for general analysis. Check the **Aggregate pins on a net within a component as one block** box beneath the **Edit Selected Row(s)** area to proceed.

Before Pin Aggregation



The result will display the combined pins' average voltage loss as well as the most significant voltage loss experienced by any of the pins.

After Pin Aggregation



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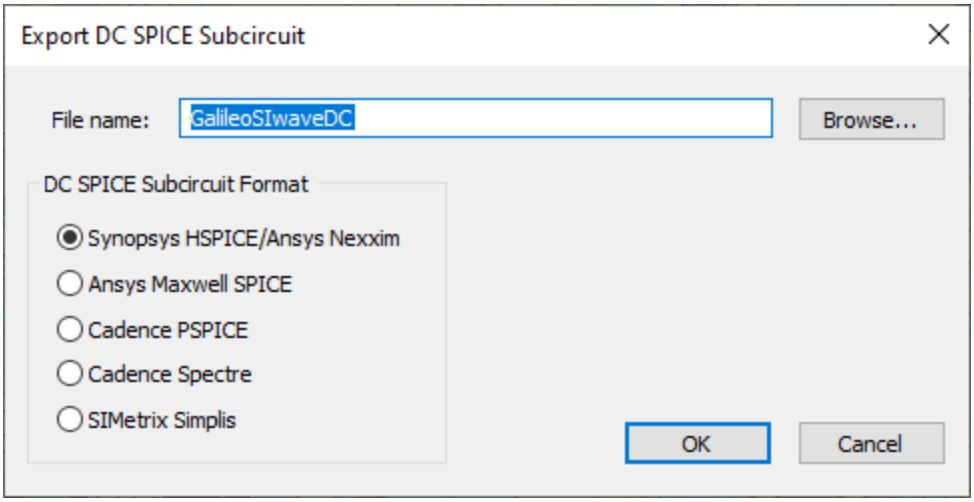
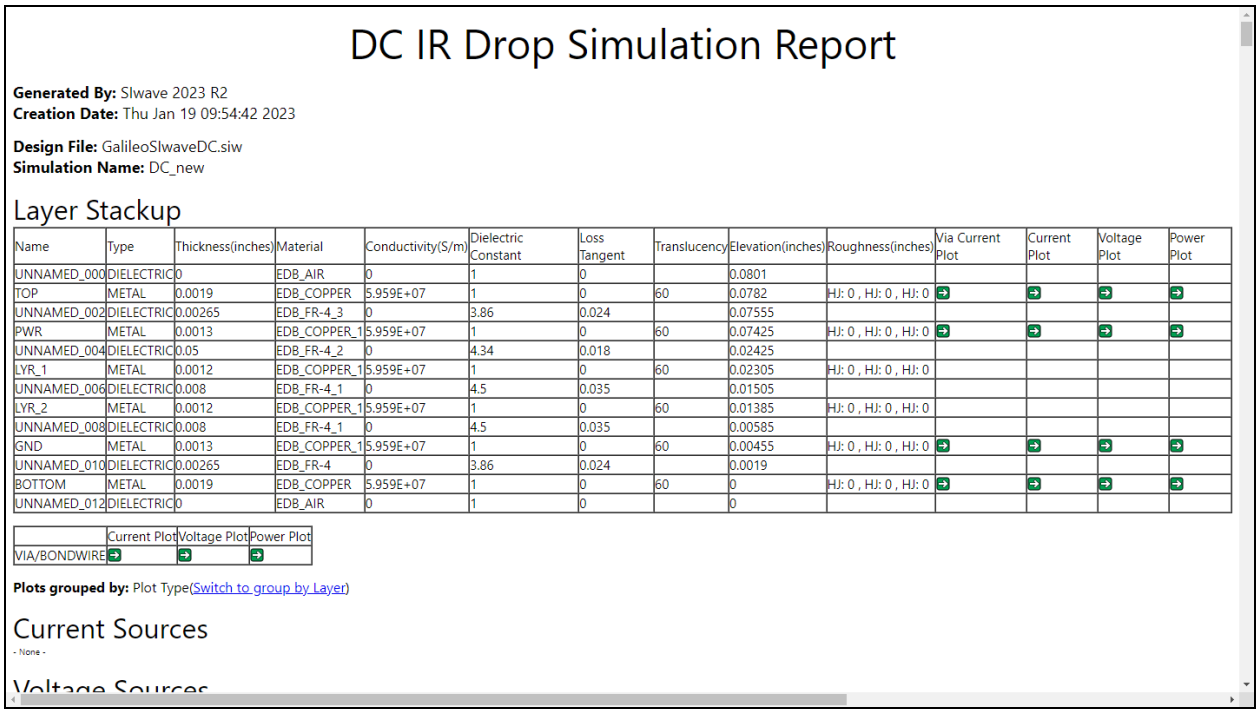
Export Spice Netlist > Export DC SPICE Subcircuit Window



4. After finalizing the configuration, click **OK** to generate the export (e.g., produce and open a report in ***.html** format).



DC IR Drop Simulation Report

Generated By: SIwave 2023 R2
Creation Date: Thu Jan 19 09:54:42 2023

Design File: GalileoSIwaveDC.siw
Simulation Name: DC_new

Layer Stackup

Name	Type	Thickness(inches)	Material	Conductivity(S/m)	Dielectric Constant	Loss Tangent	Translucency	Elevation(inches)	Roughness(inches)	Via Current Plot	Current Plot	Voltage Plot	Power Plot
UNNAMED_000	DIELECTRIC	0	EDB_AIR	0	1	0		0.0801					
TOP	METAL	0.0019	EDB_COPPER	5.959E+07	1	0	60	0.0782	HJ: 0 , HJ: 0 , HJ: 0				
UNNAMED_002	DIELECTRIC	0.00265	EDB_FR-4_3	0	3.86	0.024		0.07555					
PWR	METAL	0.0013	EDB_COPPER_1	5.959E+07	1	0	60	0.07425	HJ: 0 , HJ: 0 , HJ: 0				
UNNAMED_004	DIELECTRIC	0.05	EDB_FR-4_2	0	4.34	0.018		0.02425					
LYR_1	METAL	0.0012	EDB_COPPER_1	5.959E+07	1	0	60	0.02305	HJ: 0 , HJ: 0 , HJ: 0				
UNNAMED_006	DIELECTRIC	0.008	EDB_FR-4_1	0	4.5	0.035		0.01505					
LYR_2	METAL	0.0012	EDB_COPPER_1	5.959E+07	1	0	60	0.01385	HJ: 0 , HJ: 0 , HJ: 0				
UNNAMED_008	DIELECTRIC	0.008	EDB_FR-4_1	0	4.5	0.035		0.00585					
GND	METAL	0.0013	EDB_COPPER_1	5.959E+07	1	0	60	0.00455	HJ: 0 , HJ: 0 , HJ: 0				
UNNAMED_010	DIELECTRIC	0.00265	EDB_FR-4	0	3.86	0.024		0.0019					
BOTTOM	METAL	0.0019	EDB_COPPER	5.959E+07	1	0	60	0	HJ: 0 , HJ: 0 , HJ: 0				
UNNAMED_012	DIELECTRIC	0	EDB_AIR	0	1	0		0					

	Current Plot	Voltage Plot	Power Plot
VIA/BONDWIRE			

Plots grouped by: Plot Type(Switch to group by Layer)

Current Sources

- None -

Voltage Sources

From the DC IR results menu, you can also view DC IR results and view and change DC IR properties.

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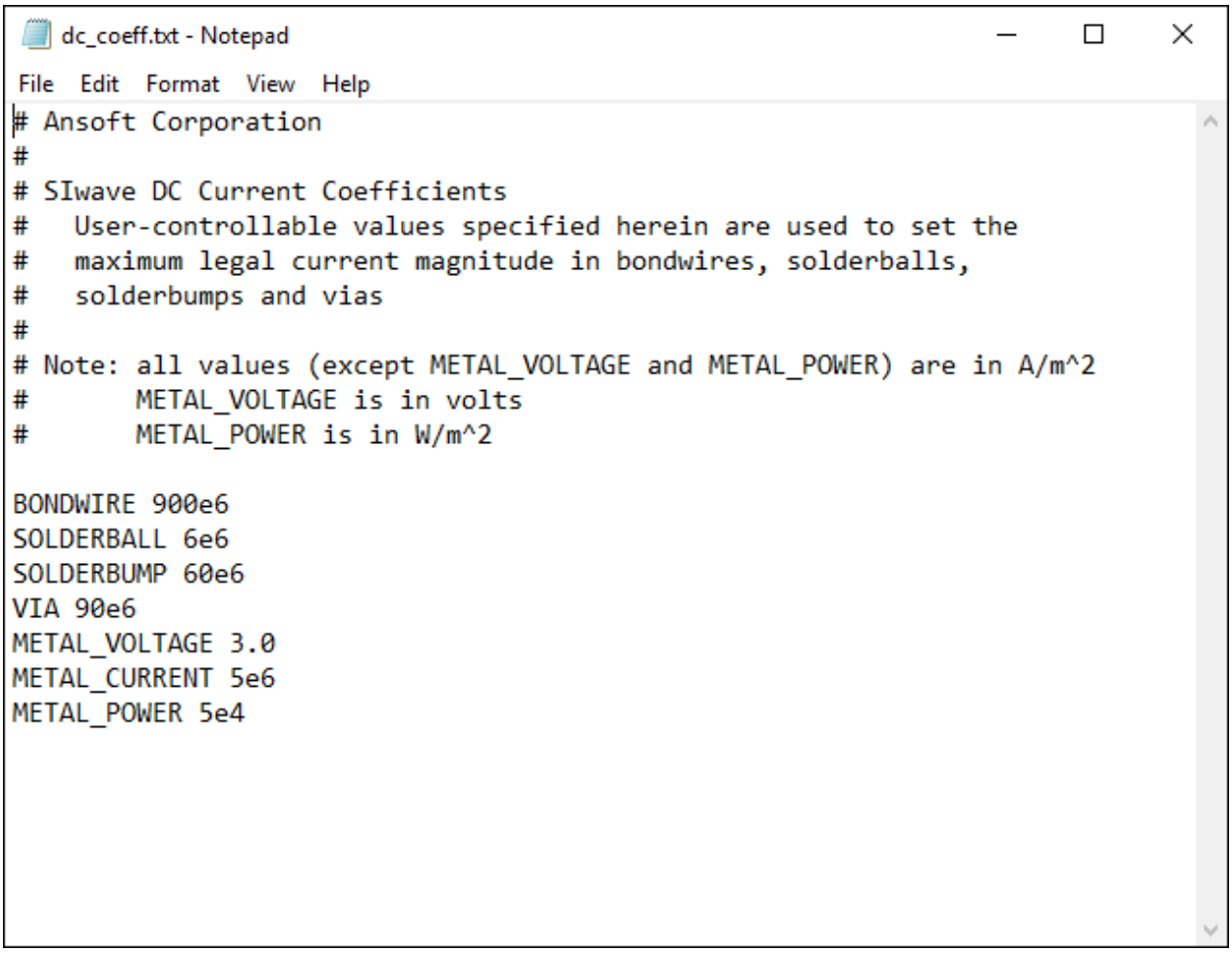
Editing the DC Coefficient Text File

By default, the DC Coefficient text file (**dc_coeff.txt**) is automatically installed in the <install_root>\v251\Win64 (or Linux64) directory. In this file, you can set the threshold values for bondwires, solderballs, solderbumps and vias, as well as for metal voltage, metal current and metal power. All values must be positive.



Changing the DC Coefficient Text File Installation Directory

To change the DC_coeff.txt file's installation directory, create the environment variable `SIWAVE_DC_COEFF_FILE_PATH`. From the value field, enter the dc_coeff.txt file's new directory path.

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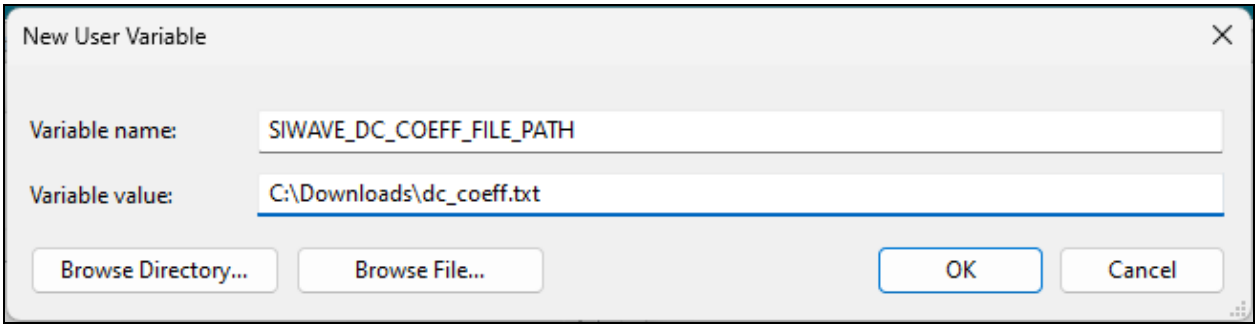

Thermal Cosimulation with Icepak

You can perform a cosimulation between SIwave and Icepak (thermal analysis tool). The cosimulation is performed in conjunction with the DC IR simulation.

- Run the DC simulation within SIwave.
- Export the data to Ansys Icepak.

> **Note:**
>
> The **Export Power Dissipation in Icepak format** option must be selected.

- Run Icepak to analyze the PCB including the power dissipation data.
- The temperature map generated by Icepak imports automatically.
- The DC simulation automatically runs again to update the power analysis.

Multiphase VRM

Voltage Regulator Modules (VRMs) supply near-constant DC voltage to subsystems on a board, such as the CPU or memory. Some VRMs make use of remote sense lines to monitor the voltage at their load. This allows them to use feedback to maintain a more stable voltage at the point in the power delivery network where current is being drawn, even if that current varies widely depending on the system's activity level. Some VRMs use multiple phases, and have more than one chip (power module) supplying current to the load. This has advantages in terms of component prices, heat management, and failure tolerance. VRMs with multiple phases try to balance the currents across phases and try to keep the current in each phase nearly the same.

Some VRMs also have a separate chip (control module) that monitors the load voltage as well as the phase currents and sends out control signals to adjust the output voltage and balance the phase currents. In some designs this control capability is built into the power modules themselves.

You can define multiphase VRMs and run the DC IR simulation. SIwave can compare current and power output at each VRM phase to ensure that values are in balance. These values can

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also be compared against the simulation results generated by modeling the VRMs using voltage sources.

To create a multiphase VRM:

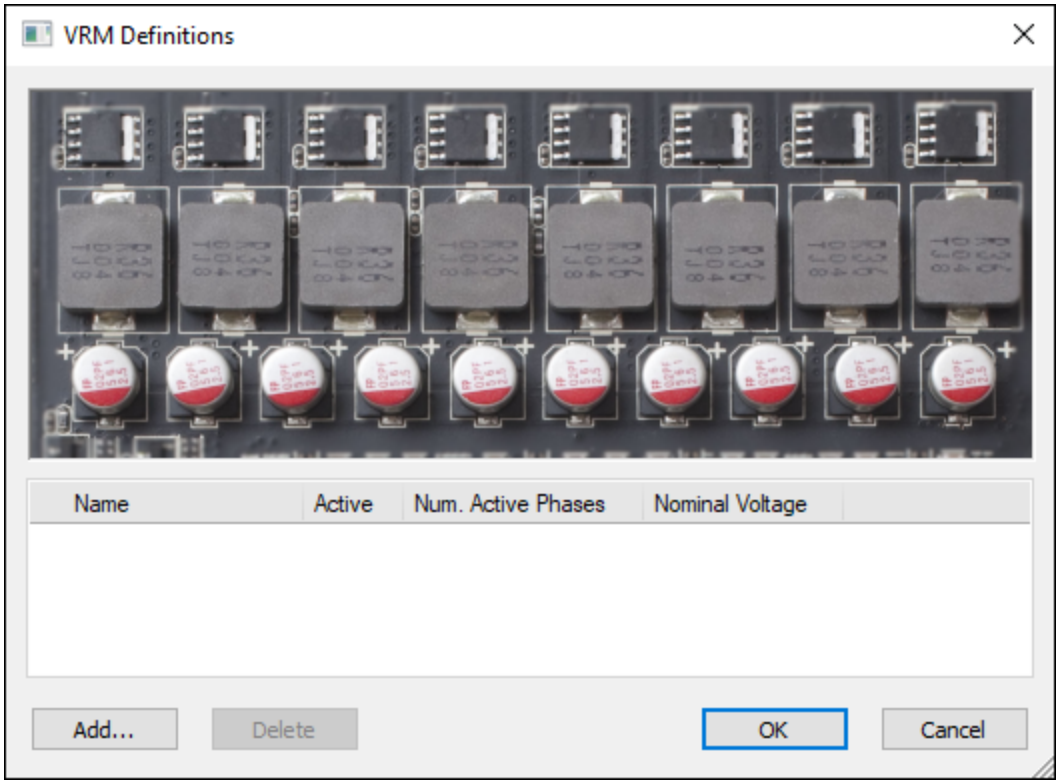
1. At each VRM component, combine the positive output pins into a pin group. Combine the negative output pins into another pin group.
2. Select each VRM reference designator by clicking on the component bounding box.
3. Right-click and select **Create Multiphase VRM**.

> **Note:**
>
> If this option is not enabled, ensure that only reference designators with the same part name are selected.

Alternate method to create a multiphase VRM:

1. Click **Advanced**.
2. From the Other Edit Tools area, click **Multiphase VRMs**.

   The **VRM Definitions** window appears.



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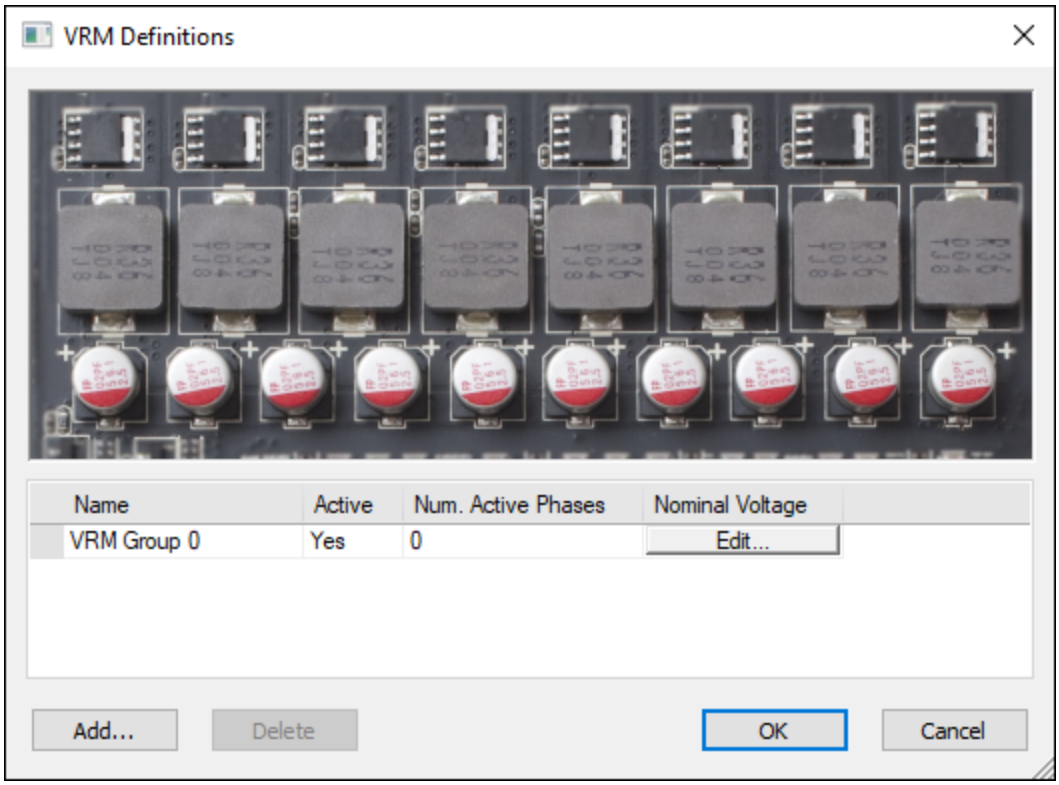
3. Click **Add**.

   A VRM group is added and appears in the list.



To edit a multiphase VRM from the VRM Definitions window:

1. Click **Edit** next to the group you would like to edit.

   The **Multiphase VRM Definition** window appears.

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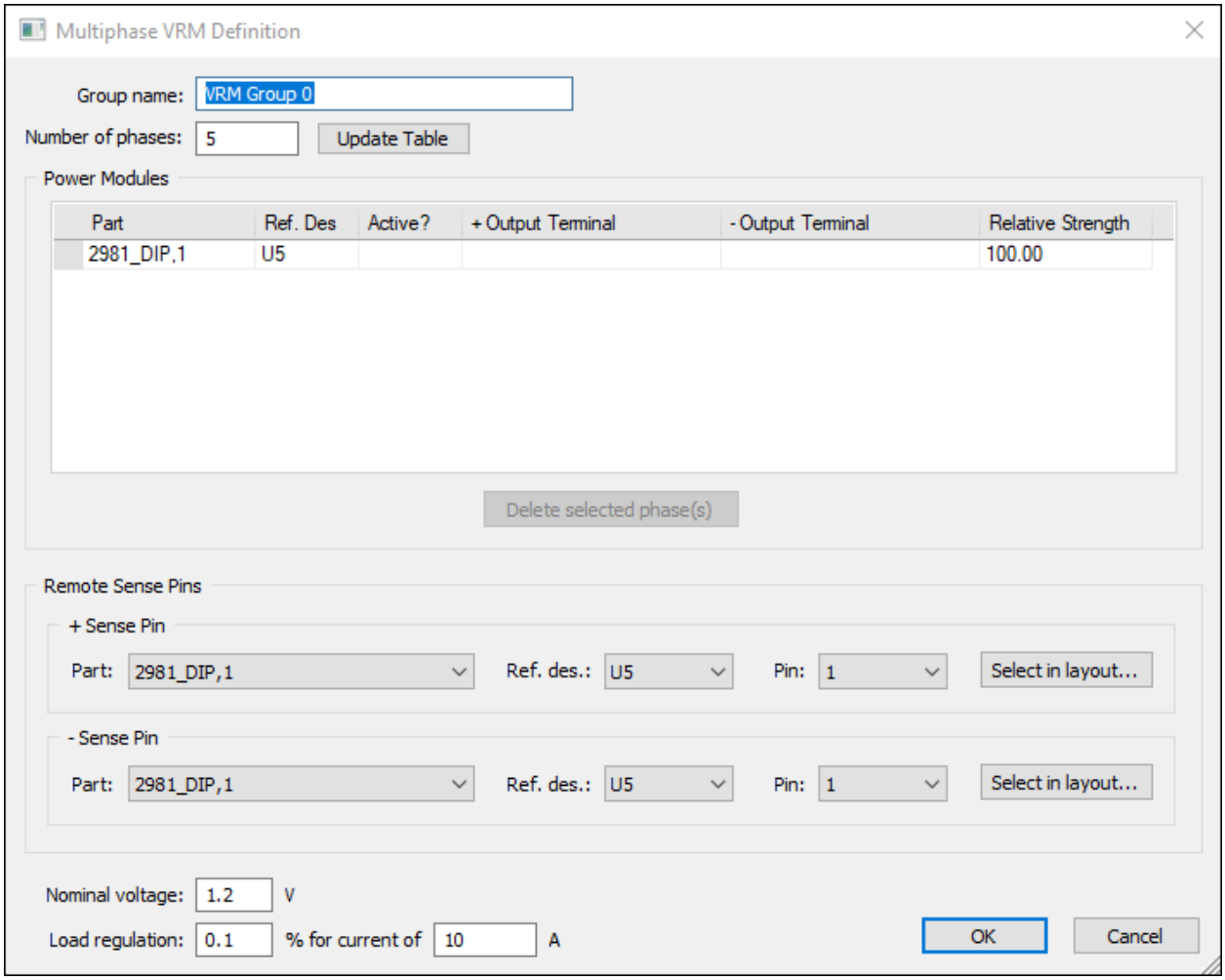

If positive and negative net names are recognized, the **+ Output Terminal** and **- Output Terminal** columns automatically populate VRM pin groups.

2. From the **Group name** field, enter a name.

   This group is a collection of ICs that constitutes a multiphase voltage regulator. Typically, it consists of several power module ICs (one per phase) that source the output currents to the load. In some designs there may be a controller IC that monitors the load voltage and phase currents and sends out control signals to the power modules.

3. Specify the **Number of phases**. Phases appear as rows in the Power Modules list.
4. For each phase, click the cells to define the **Part**, **Reference Designator**, **Active/Inactive** status, pin numbers for the **Positive (+) Output Terminal** and **Negative (-) Output Terminal**, and a **Relative Strength**.

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For **Relative Strength**, all power modules are nominally expected to supply the same output current, but in reality will have small differences. Manufacturers often specify a current sharing accuracy (example: +/- 10%). Different relative strengths for each phase allow you to model such differences. These are expressed as a percentage, with a default value of 100% (exactly matched strength). You can raise or lower these percentages as needed, even dropping them to zero to model a failure of one power module. A strength of 100% is normal strength; a phase with 90% strength will supply only 0.9 times the normal current. The voltage actually produced by the VRM will vary from the nominal value depending on how much load current is being drawn and how many phases are used. The variation can be estimated from the load regulation data entered:

Change in V_{out} = (load regulation fraction) x (nominal voltage) x (actual output current) / ((current in load regulation spec) x (number of phases))

5. From the **Remote Sense Pins** area, use the drop-down menus to select the positive and negative remote sense pins. Alternatively, click **Select in layout** and click the pin in the Modeling workspace.

   Each VRM group has remote sense lines to monitor the load voltage. There is both a positive and negative sense line and they are connected to pins of a component. You can specify the part number and reference designator for the control module IC (if a separate one is used; otherwise, identify one of the power modules) and the pins that are used for remote voltage sensing.

6. If appropriate, change the values for **Nominal voltage** and **Load regulation**.
   - **Nominal Voltage** is what the output voltage should be with zero load current. It is an appropriate voltage difference between the positive and negative sense pins; the VRMs adjust their output voltage to meet this value within tolerance.
   - **Load regulation** is how much the output voltage of a single power module varies from its nominal value for a given load current. The voltage variation is entered as a percentage of the output voltage.
7. Click **OK** to complete the multiphase VRM definition.
8. Run the DC simulation.

The current and power output at each active VRM phase should match.

Electrothermal Flow For Power Electronics

When simulating the PCBs of power electronics converters, most cases deal with Pulse Width Modulated (PWM) voltage and current sources. From these cases, it is impossible to configure a DC IR setup that both accurately represents power losses and satisfies the current balance in accordance with Kirchhoff's first law. Therefore, an advanced workflow is required to accurately estimate losses on PCB traces for power electronics.

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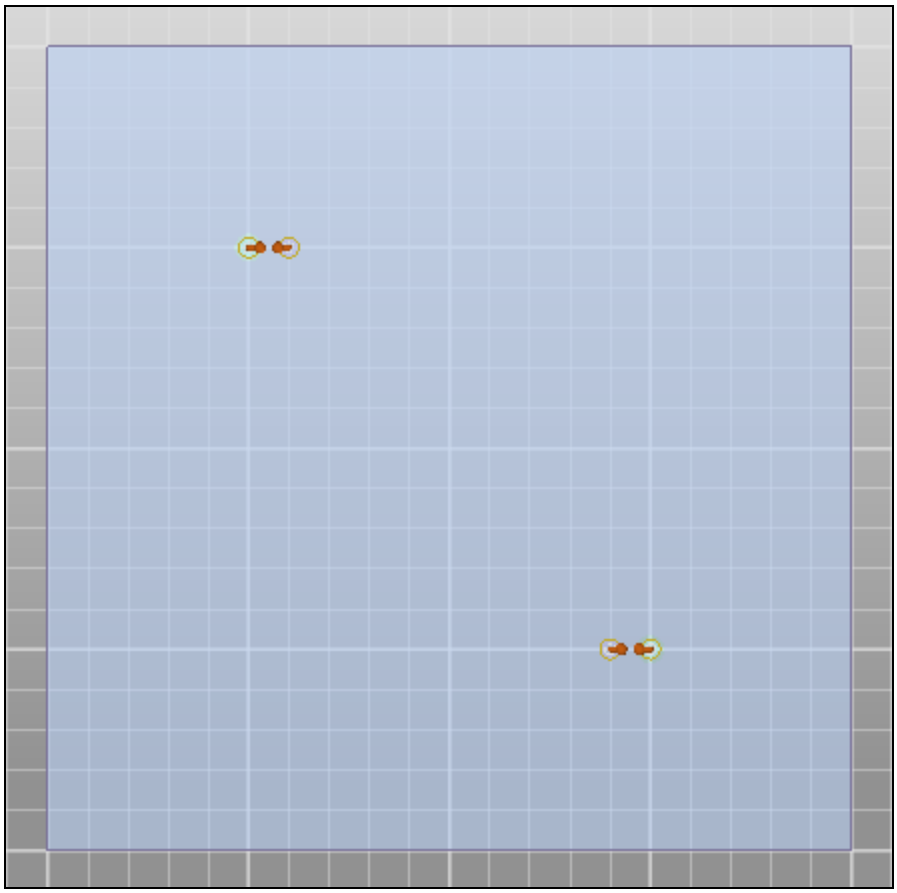
Frequency Domain Workflow Using SIwave and Circuit

Complete the following steps for at least one period of power converter output frequency.

> **Note:**
>
> This workflow can be conducted using excitations from a Circuit/Nexxim source file or from a user-generated frequency dependent source file. Refer to the frequency dependent workflow to generate a frequency dependent source file.

1. Set up a PCB design in SIwave.



2. Set up and run an SYZ simulation to compute and extract S-parameters.

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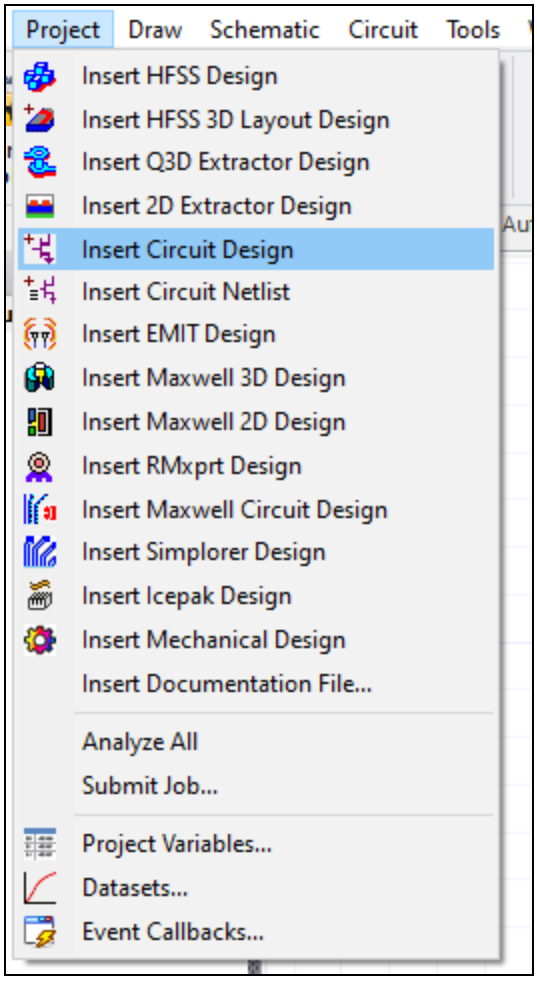
3. **Save** and **Close** the project.
4. Open **Electronics Desktop** and insert a Circuit Design. Refer to the Circuit Help.



5. Create an SIwave dynamic link in Circuit/Nexxim. Refer to the Circuit Help.
6. Create an appropriate Circuit design (Refer to the Nexxim Design Examples available in the Circuit Help.).

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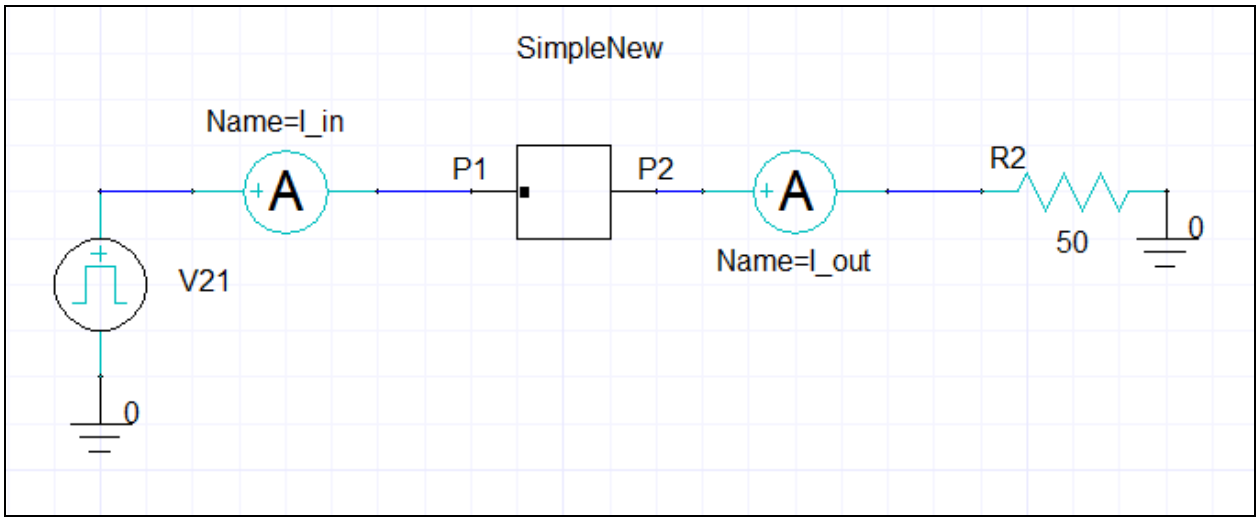
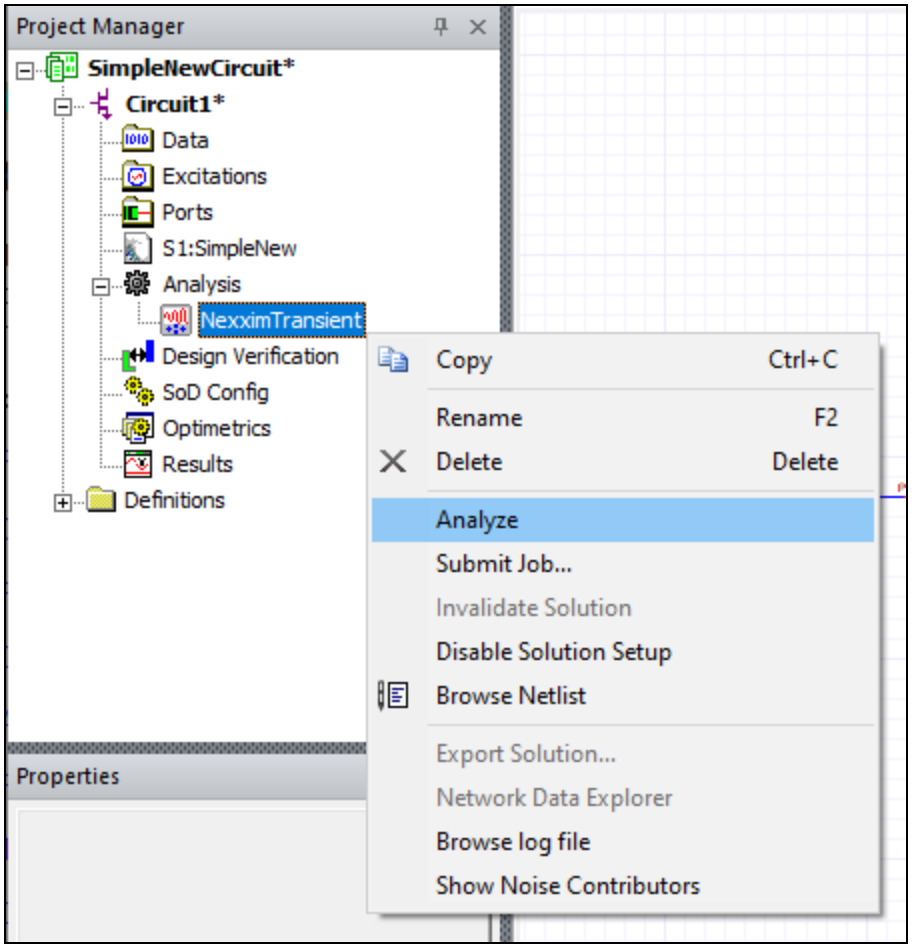


7. Run a Nexxim Transient analysis with appropriate **Step** and **Stop** values. Refer to the Circuit Help.



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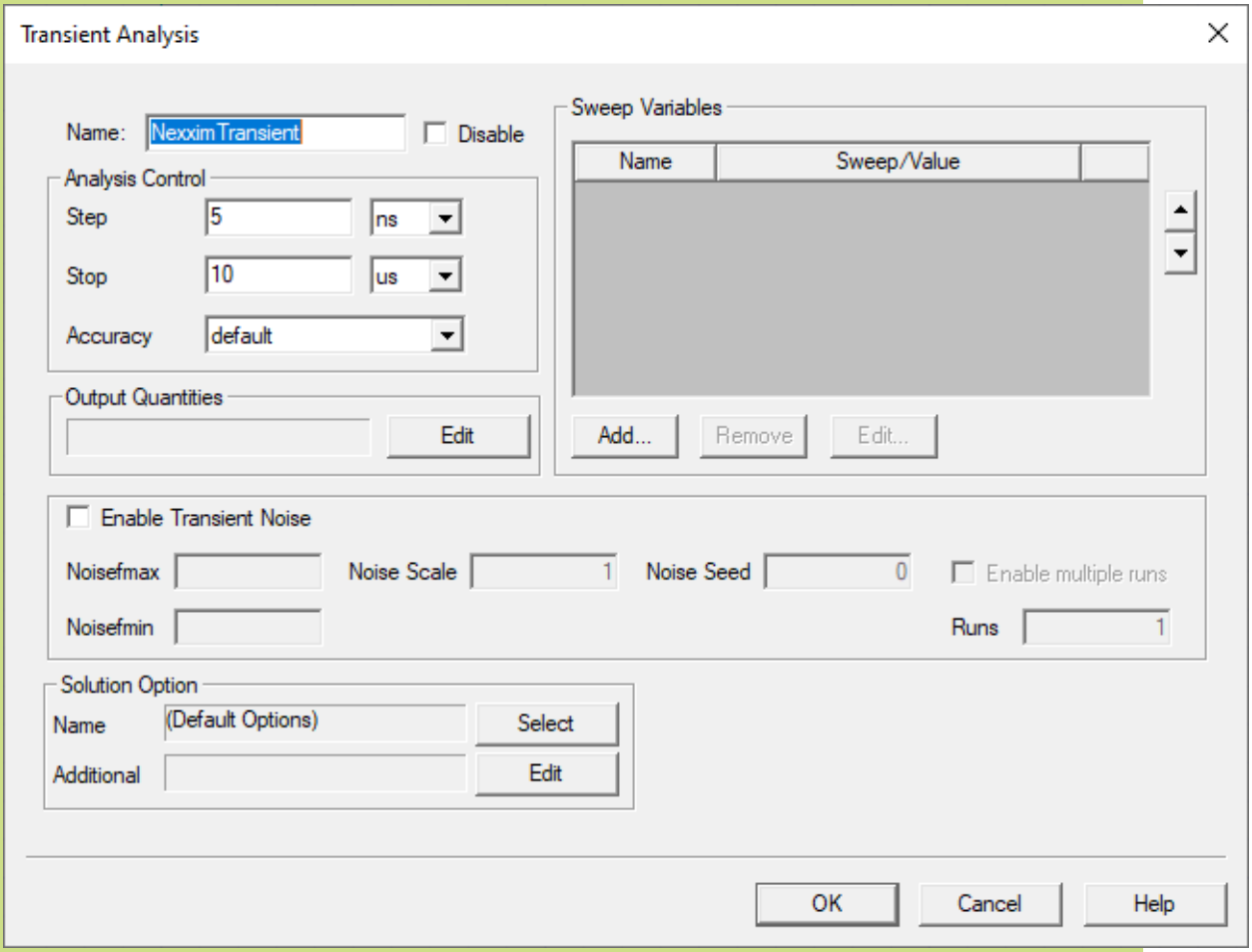
Note:

SIwave uses Fourier Transform to convert a transient source into a frequency domain source. If users set a high **Step** variable during the transient analysis, simulation time may increase when run as a DC IR Drop simulation (i.e., step 10).



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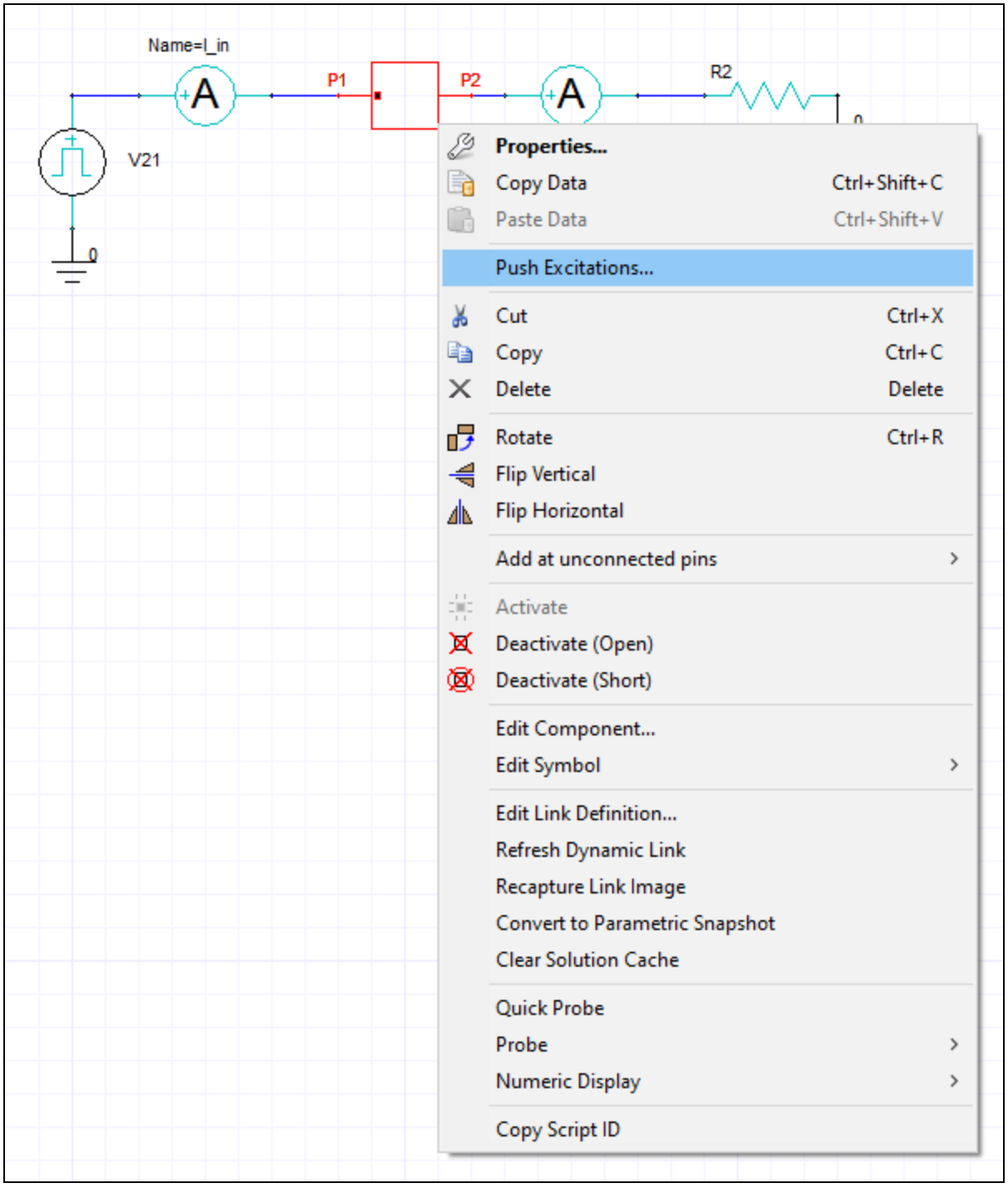
8. Push the analysis excitations from Circuit/Nexxim to SIwave. Refer to the Circuit Help.



9. Return to **SIwave** and reopen the project.
10. Create and run a DC IR Drop simulation. The excitation output from Circuit/Nexxim will be automatically used as the source file (e.g., **4685_NexximTransient_sources.tmp**).

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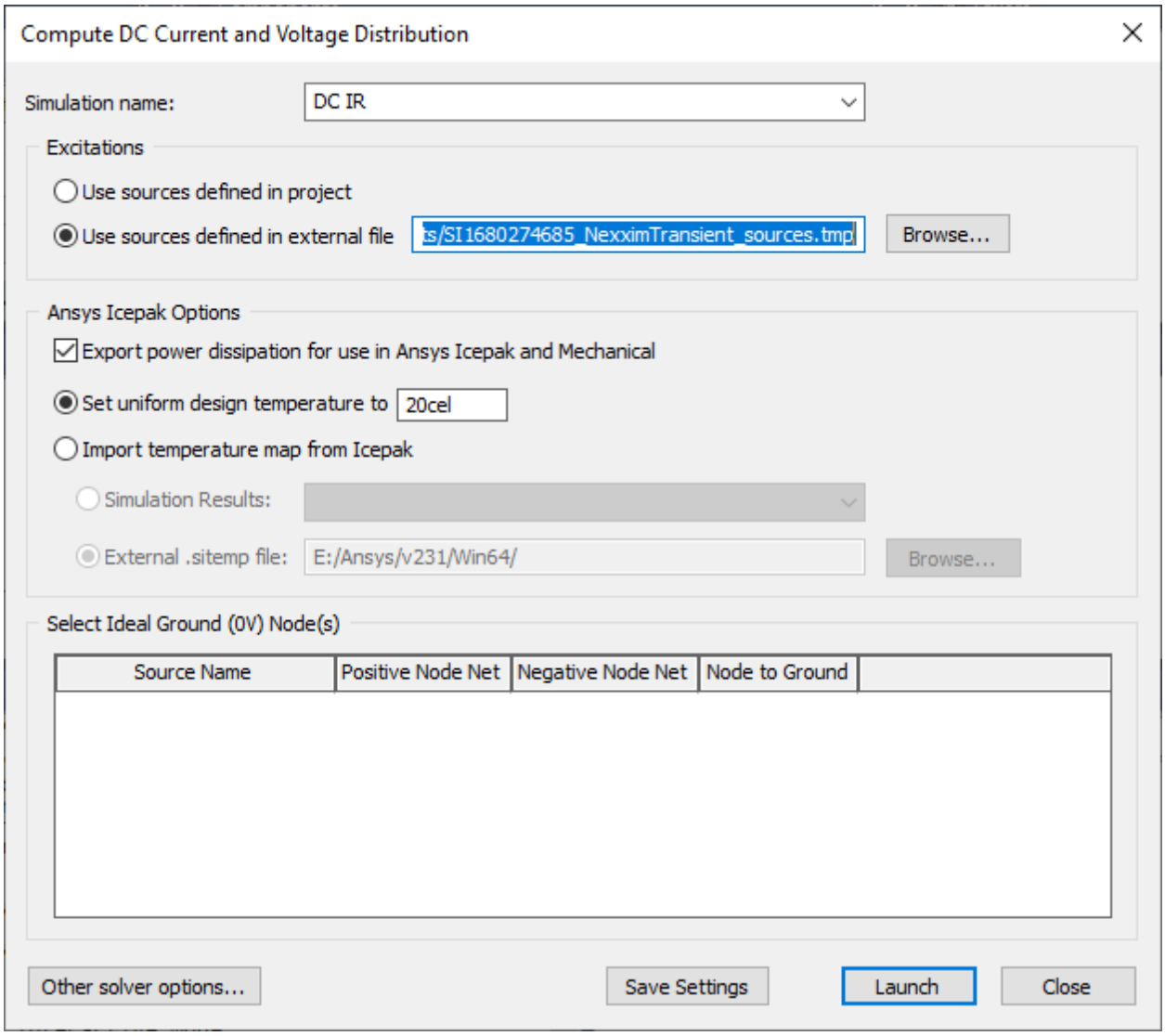

Note:

Passive components (e.g., capacitors and inductors) should be removed from the layout and modeled in the Circuit design.

11. Once the DC IR Drop simulation is complete, navigate to the **Results** folder. Then right-click the completed simulation (e.g., **DC IR**) and select one or more of the following:

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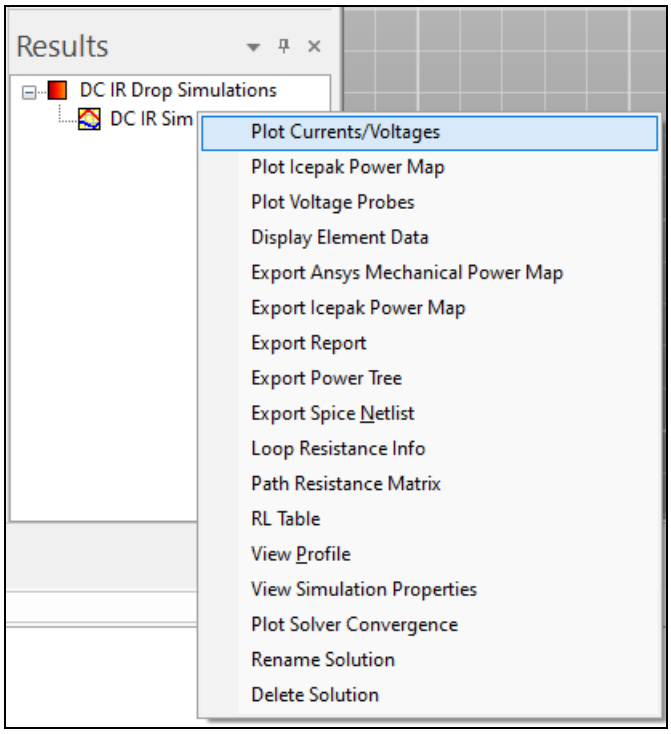

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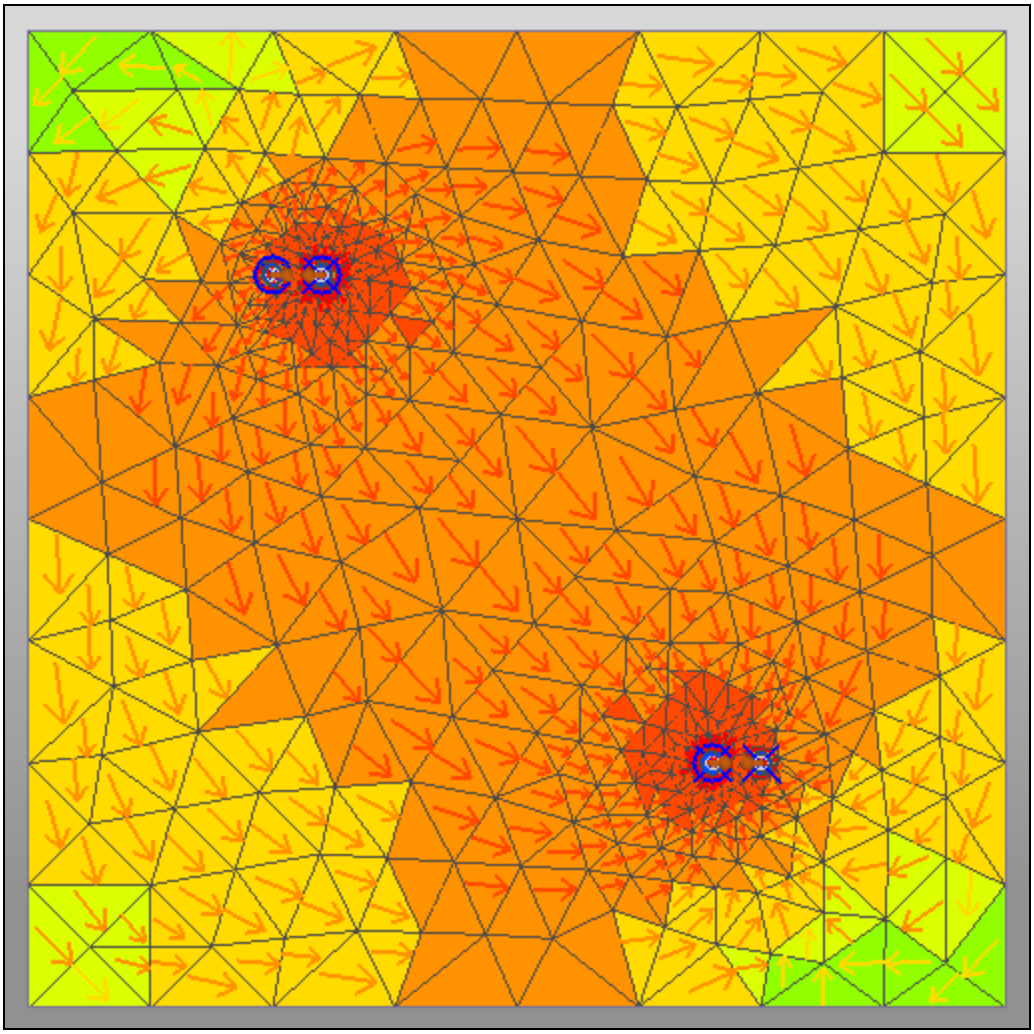
- **Plot Currents/Voltages**



- **Plot Icepak Power Map**

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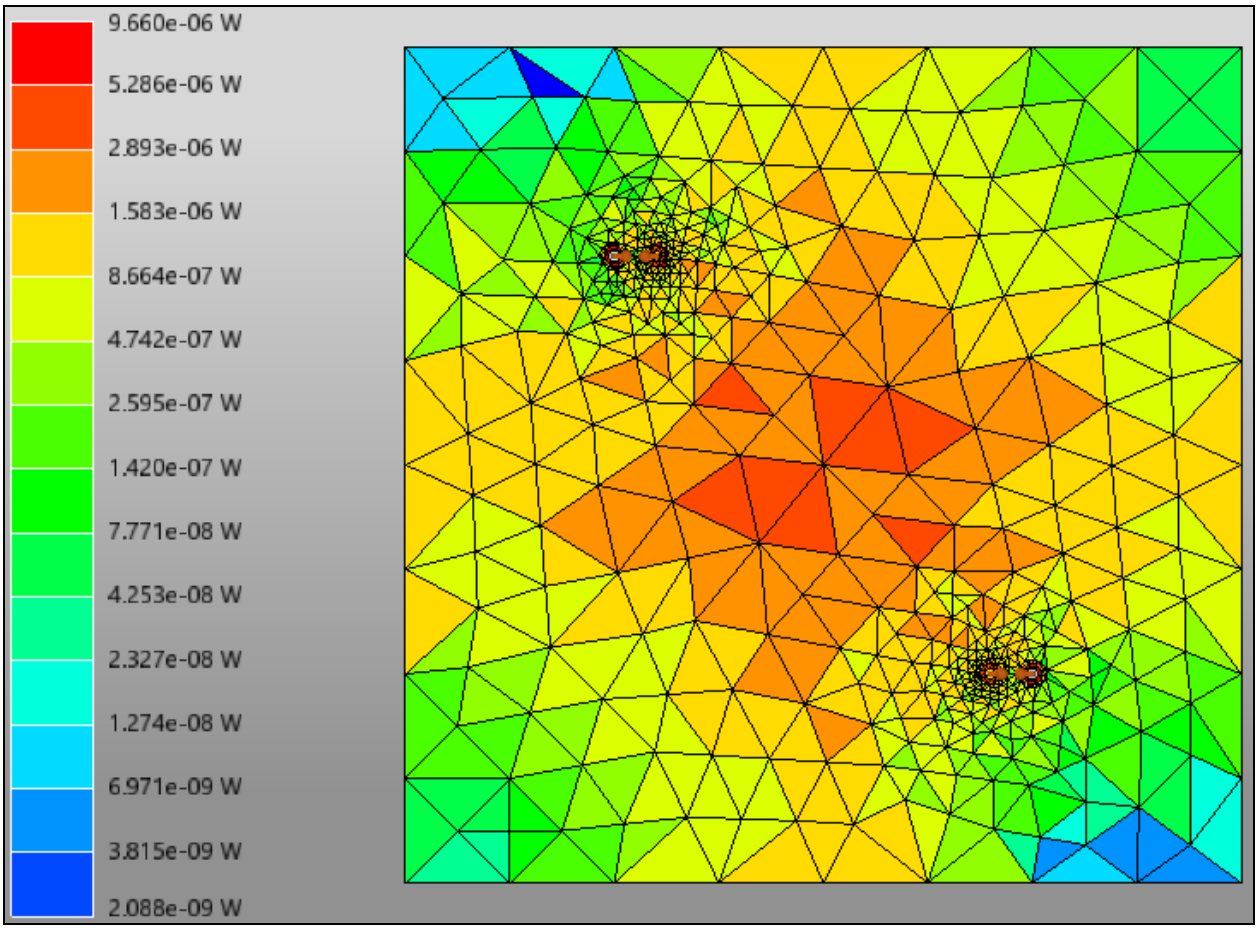

- **Plot Solver Convergence**

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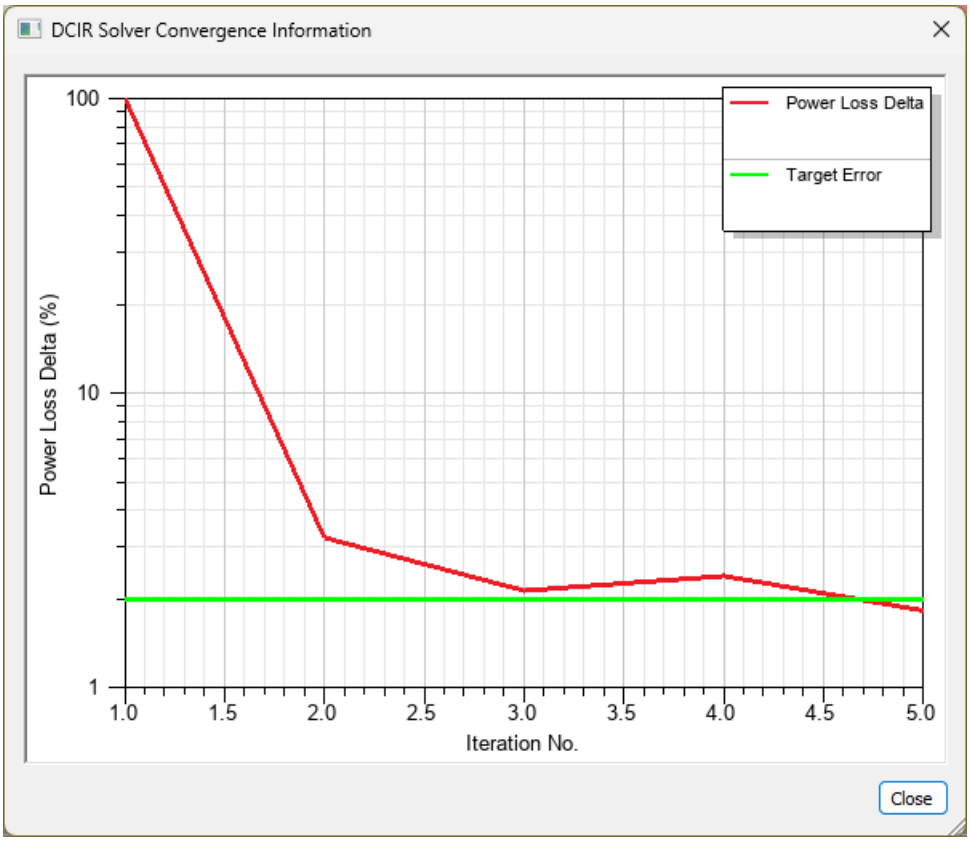

Note:

Power loss is the total loss generated by the transient source. Current and voltage correspond with the value at time t= 0s.

Refer to Viewing DC IR Results in SIwave for more information.

Frequency Domain Workflow Using Frequency Dependent Current in SIwave DC IR Solver

Complete the following steps if users intend to use a frequency dependent source file. Generate the data for the frequency dependent current course by performing a Fourier transformation on a transient current obtained from a circuit simulation for at least one period of power converter output frequency.

1. Create a frequency dependent source file (i.e., a **.txt* file), adhering to the following guidelines:

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- The file must contain the frequency domain excitations (i.e., Freq, Re, Im).

```
SOURCE_RESISTANCE <resistance value of the source (e.g., 5e7)>
0                 -1                              0
1e9               0                               -1
5e9               -1                              0
```

- If there is more than one frequency dependent current source used for a DC IR setup in a project, all source files must contain the same frequency points.

2. Add the frequency dependent source to the design.
3. Return to step 10 in the **Frequency Domain Workflow** to run a DC IR simulation. At the **Compute DC Current and Voltage Distribution** window, ensure **Use sources defined in project** is selected.

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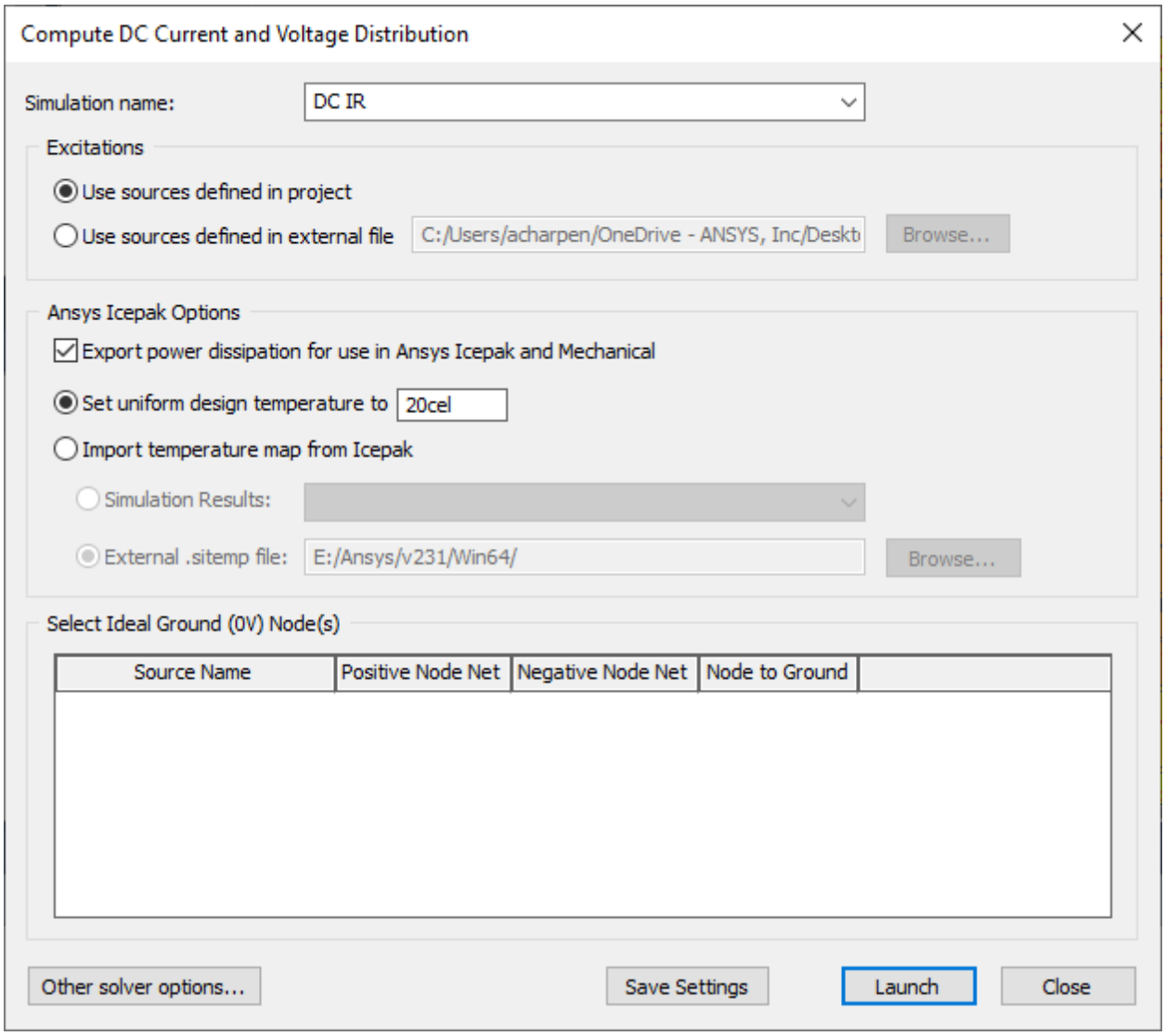

Technical Notes: How Frequency-Dependent Resistance is Calculated for the DC IR Solver

If a project includes a DC IR setup with frequency-dependent current sources or excitations pushed from a Dynamic SIwave component in a Circuit Design, the frequencies from the current sources are used in an SYZ analysis, which is run as part of the DC IR simulation. Since the DC IR simulation does not compute frequency-dependent resistance (i.e., RAC), the SYZ analysis computes the RAC. The resistance from the DC IR analysis (i.e., RDC) and the RAC from the SYZ analysis are used to calculate the power loss generated by the AC current source.

Utilizing DC correction to compute the exact DC point (i.e., the ZDC matrix generated by the DC IR solver), the simulation will then compute the power loss density for each frequency point with constant resistance obtained from the SYZ analysis. The final frequency-dependent power loss

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is the sum of the points generated by each current source using Re and Im current values at different frequencies, incorporating the ratio of the power loss calculated by RAC and RDC.

In summation, for DC point, power loss is computed by the DC IR solver as

$$P_{dc} = I_0 R_{dc} I_0$$

where I_0 is DC current and R_{dc} is resistance at DC point, calculated by the DC IR solver. The AC solver yields an equivalent resistance matrix that is used to compute power loss as

$$P_{n_Rf} = \frac{1}{2} I_{n_re} R_{fn} I_{n_re} + \frac{1}{2} I_{n_im} R_{fn} I_{n_im}$$

where R_{fn} is equivalent to the resistance matrix of the model at the frequency f_n, I_{n_re} and I_{n_im} are vectors of real and imaginary parts of the current sources at the frequency f_n. If a coefficient (e.g., k_n) is defined as $R_f n = k_n^2 Rdc$, the AC power loss at the frequency f_n can be rewritten as

$$P_{n_Rf} = k_n^2 \left(\frac{1}{2} I_{n_re} R_{dc} kn I_{n_re} + \frac{1}{2} I_{n_im} R_{dc} I_{n_im} \right) = k_n^2 P_{n_Rdc}$$

where P_{n_Rdc} is the AC power loss at the frequency f_n computed with constant resistance R_{dc}, leading to $k_n = \sqrt{\frac{P_{n_Rf}}{P_{n_Rdc}}}$. Since both P_{n_Rf} and P_{n_Rdc} can be computed for the frequency f_n, utilizing the AC solver (i.e., SYZ analysis) and the DC IR solver, k_n can be computed for all frequencies. Finally, the coefficient k_n is incorporated into the current sources as $I_n^{'} = k_n I_n$. The power loss result of modified current sources accounts for frequency dependent resistance behavior.

> **Note:**
>
> The ZDC matrix is the result of DC port simulation, which has different mesh refinement logistics from the DC IR simulation. In order to ensure agreement of power loss results calculated by equivalent resistance and results calculated by DC IR simulation, it is appropriate to have similar mesh (e.g., the same mesh is ideal), so the DC port and DC IR simulations run the same number of iterations. The number of iterations is beholden to the DC Port simulation automatically as part of the analysis.

Version 2025 R1 and Beyond

Prior to version 2025 R1, when computing power loss on the design, the DC IR solver considers capacitors open elements and inductors zero impedance elements. Starting with version 2025 R1, if the design contains frequency-dependent or time domain sources, the DC IR solver treats capacitors and inductors as active elements when solving the problem and computing power loss in the design.

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When addressing frequency-dependent sources in DC IR, a parasitic resistor of 10 MΩ is introduced in parallel with each capacitor, and a parasitic resistor of 9 μΩ is added in series with each inductor.

> **Note:**
>
> The parasitic capacitance of inductors and resistors, as well as the parasitic inductance of capacitors, are ignored during simulation. Any parasitic resistor values specified in the UI for capacitors and inductors are overridden by the DC solver with the values mentioned above.

The impedance of capacitors and inductors is calculated as in AC mode:

$$Z_c = \frac{1}{j2\pi fC}$$

$$Z_L = j2\pi fL$$

where Z_C and Z_L represent the impedance of the capacitor and inductor, respectively; C and L are the capacitance and inductance, and f is the frequency under study. The impedances of capacitors and inductors are ignored at DC (i.e., f=0.0).

For designs that include RLC components, the DC IR solver uses the constant resistance of the metal at DC to compute power loss. To optimize computation time, the Schur complement method is used to solve the matrix system when frequency-dependent or time domain sources are involved.

Computing EM MTTF Simulations

The EM MTTF simulation provides an estimate of Mean Time to Failure (MTTF) of metallization due to electron flow.

It is represented by the equation:

$$MTTF = Aj^{-n}e^{\left(\frac{E_a}{kT}\right)}$$

Where:

- A is an experimental constant
- j is the current density
- n is a value between 1 and 2

  n is close to 1 when current density is low (<=0.1MA/cm^2), and gradually trends toward 2 as current density increases.

  n = 1.5 for 0.1MA/cm^2 < j < 1MA/cm^2

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n = 2 for j >= 1MA/cm^2

- *Ea* is the activation energy
- *k* is the Boltzmann Constant
  1.38064852 x 10^{-23} m^2 kg s^{-2} K^{-1}
- *T* is the temperature in Kelvin

Note:

Sample activation energy (*Ea*) and current density exponent values can be found in the following publication:

Lou Nicholls et al. "Comparative Electromigration Performance of Pb Free Flip Chip Joints with Varying Board Surface Condition." Electronic Components and Technology Conference, 2009. https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5074122.

Important:

You cannot run an EM MTTF simulation without first running a DC IR simulation, as the calculation uses DC IR-generated current density. In order to map MTTF data to individual bondwires and vias during post-processing, ensure that the "Mesh Bondwires" and "Mesh Vias" options are selected when running the DC simulation.

Users may want to run an Icepak simulation first to generate the temperature distribution.

To compute an EM MTTF simulation:

1. Compute a DC IR simulation.
2. Click **Simulation**.
3. From the **SIwave** area, click **Compute EM MTTF**.
   The **Compute Electromigration Induced Failures** window appears.

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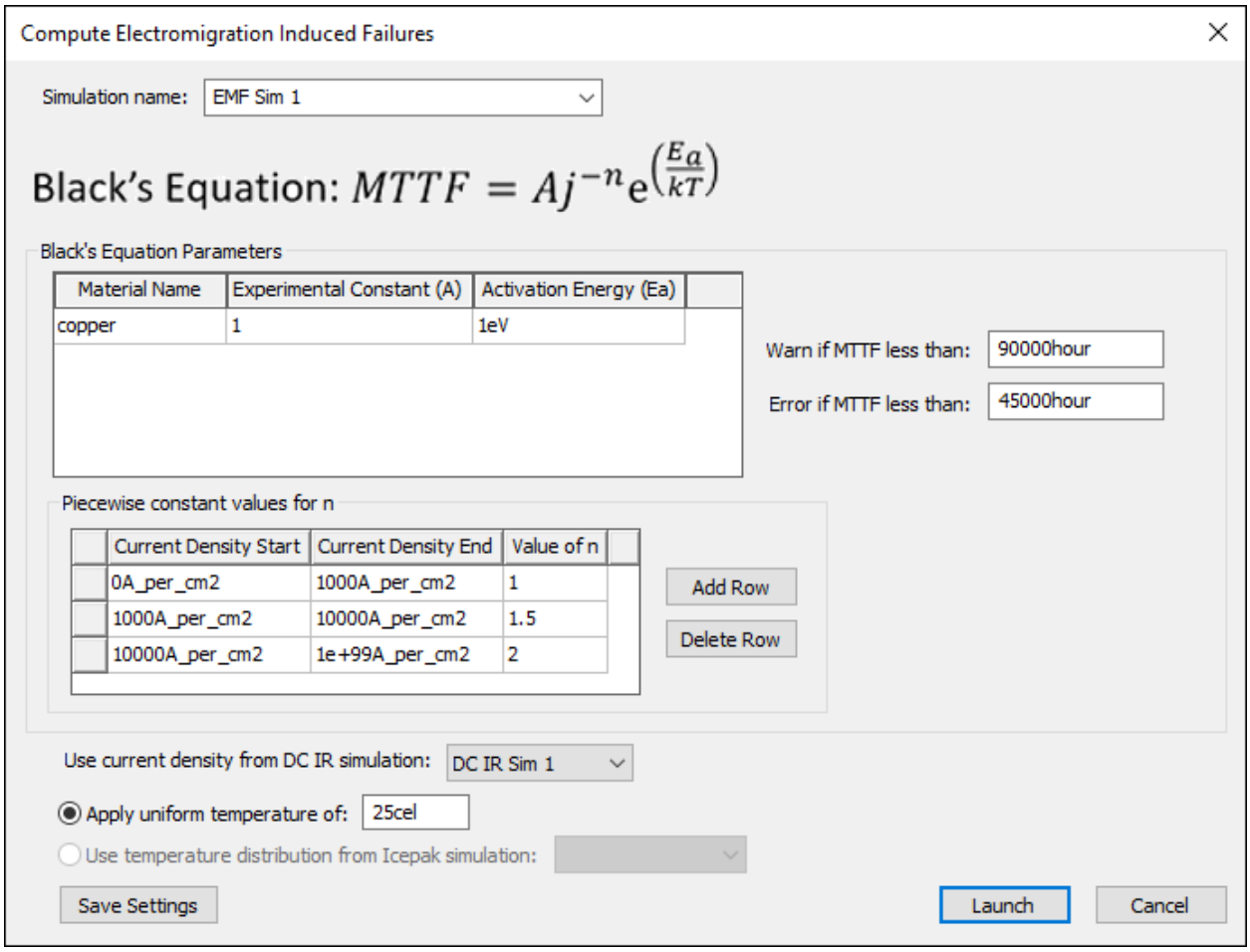

4. From the **Simulation Name** field, enter a name for the EM MTTF simulation.
5. From the **Black's Equation Parameters** area, enter equation parameters and the MTTF time (in hours) you want to cause a warning or an error.
6. From the **Piecewise constant values for n** area, enter a start and end current density, as well as the *n* value for Black's Equation. You can use **Add Row** and **Delete Row** to change the number of *n* values.
7. From the **Use current density from DC IR simulation** drop-down menu, select the DC IR simulation you previously ran.
8. Select **Apply uniform temperature of** and enter a temperature in Celsius, or select **Use temperature distribution from Icepak simulation** and use the drop-down menu to select a previously run Icepak simulation.
9. Click **Launch** to run the simulation.

   The **Messages** window updates with a Process Monitor tab that displays the progress.

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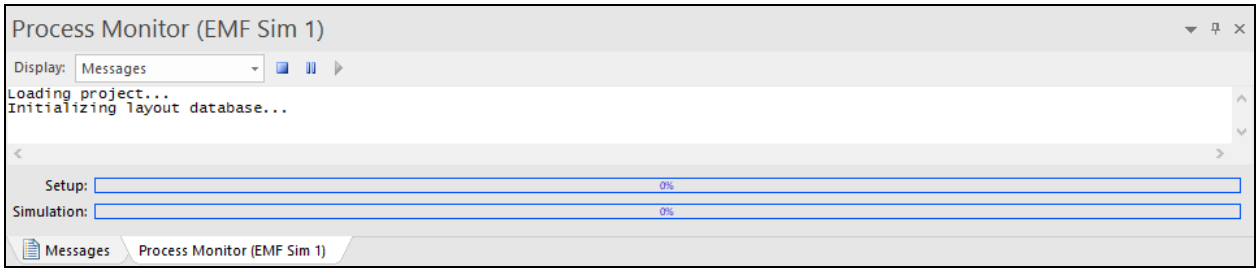

When the simulation has finished, you can view the results.

Viewing EM MTTF Simulation Results

To view EM MTTF results:

1. Compute an EM MTTF simulation.
2. Click **Results**.
3. From the **SIwave** area, click **EM MTTF** and select **[Simulation Name]** .

Results menu options include:

- **Plot MTTF** – plots estimated failure times in the Modeling workspace.
- **Plot MTTF (Warnings/Errors)** – plots estimated failure times, by severity, in the Modeling workspace.
- **Display MTTF Location Table** – opens a table displaying MTTF locations.
- **Delete Solution** – deletes the EM MTTF results.

You can plot **MTTF**, which displays estimated failure times, or **MTTF Warnings/Errors**, which plots estimated failure times by severity.

Plotting MTTF

To plot estimated failure times:

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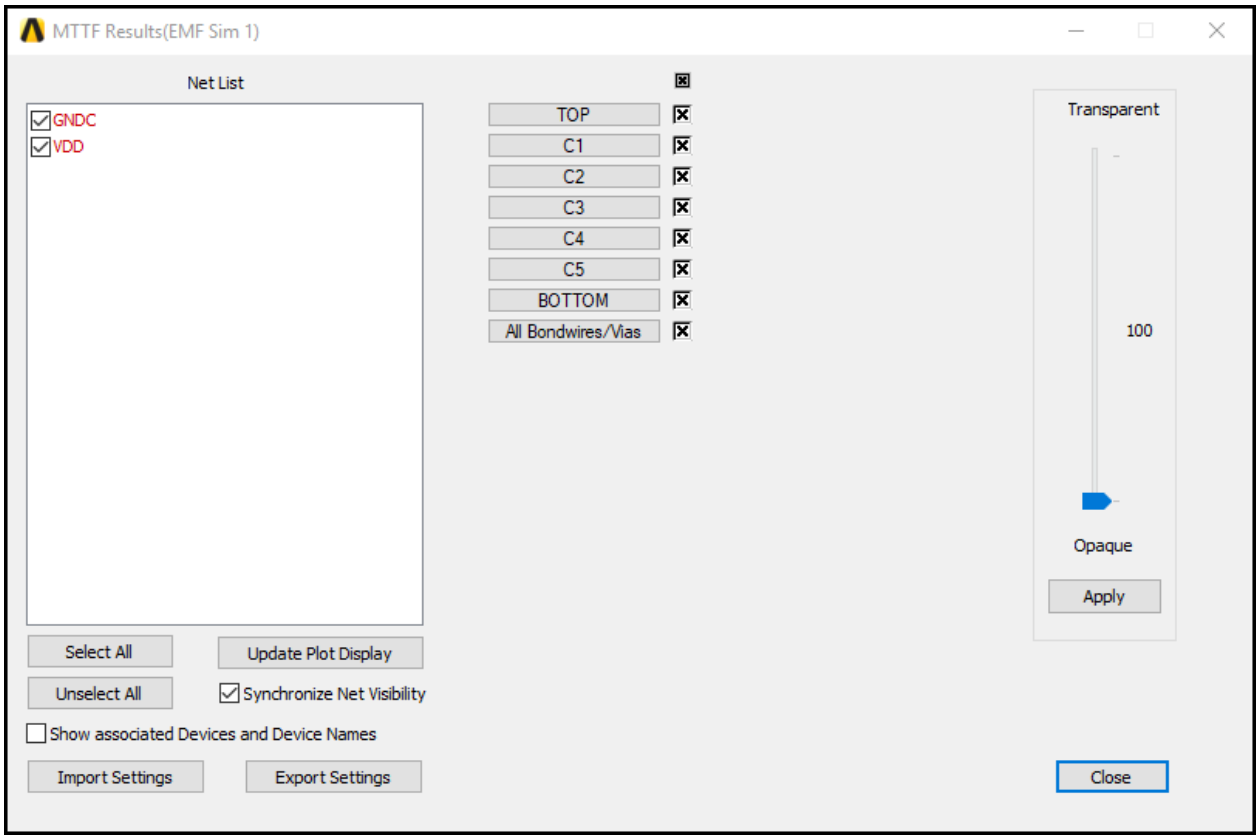
1. Compute an EM MTTF simulation.
2. Click **Results**.
3. From the **SIwave** area, click **EM MTTF** and select **[Simulation Name] > Plot MTTF**.

   The **MTTF Results** window appears, and the Modeling workspace updates to display MTTF.



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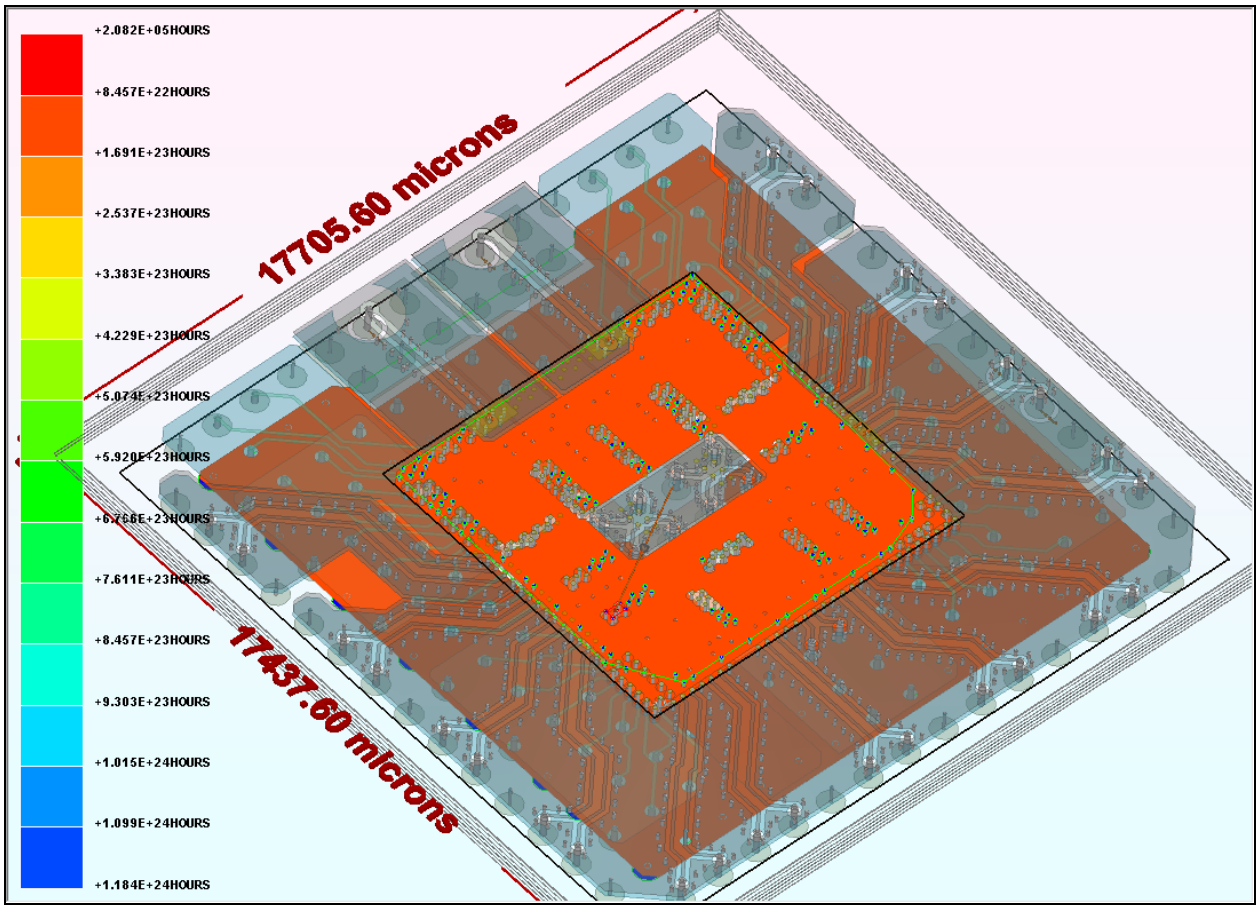

Use the **Net List** to select or deselect nets for display. Use the layers list to do the same for layers. Click **Update Plot Display** to apply changes.

Use the Transparent/Opaque slider to adjust the MTTF plot's transparency, and click **Apply**.

You can also **Export Settings** in *.xml format, or **Import Settings** from a previously saved *.xml file.

Plotting MTTF (Warnings/Errors)

To plot MTTF Warnings/Errors:

1. Compute an EM MTTF simulation.
2. Click **Results**.
3. From the **SIwave** area, click **EM MTTF** and select **[Simulation Name] > Plot MTTF (Warnings/Errors)**.

   The **MTTF Results** window appears, and the Modeling workspace updates to display MTTF Warnings and Errors.

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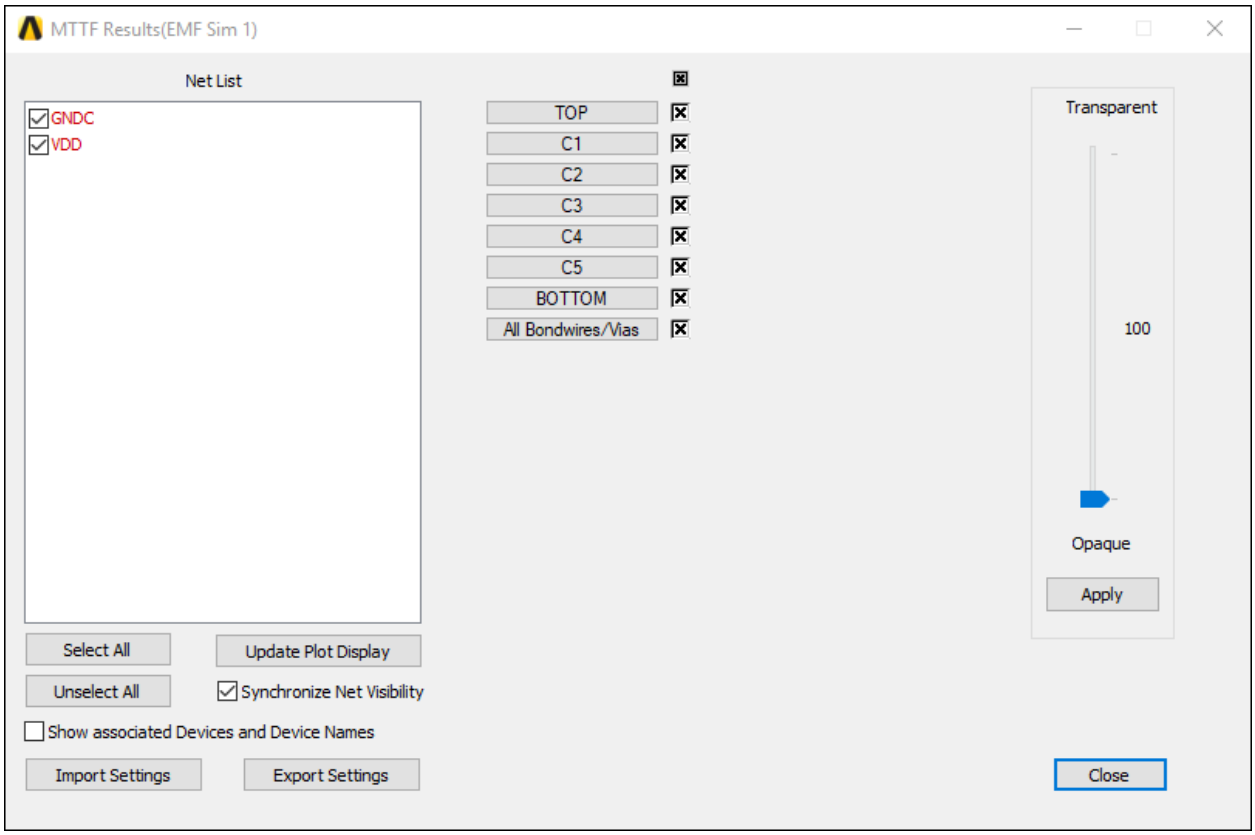

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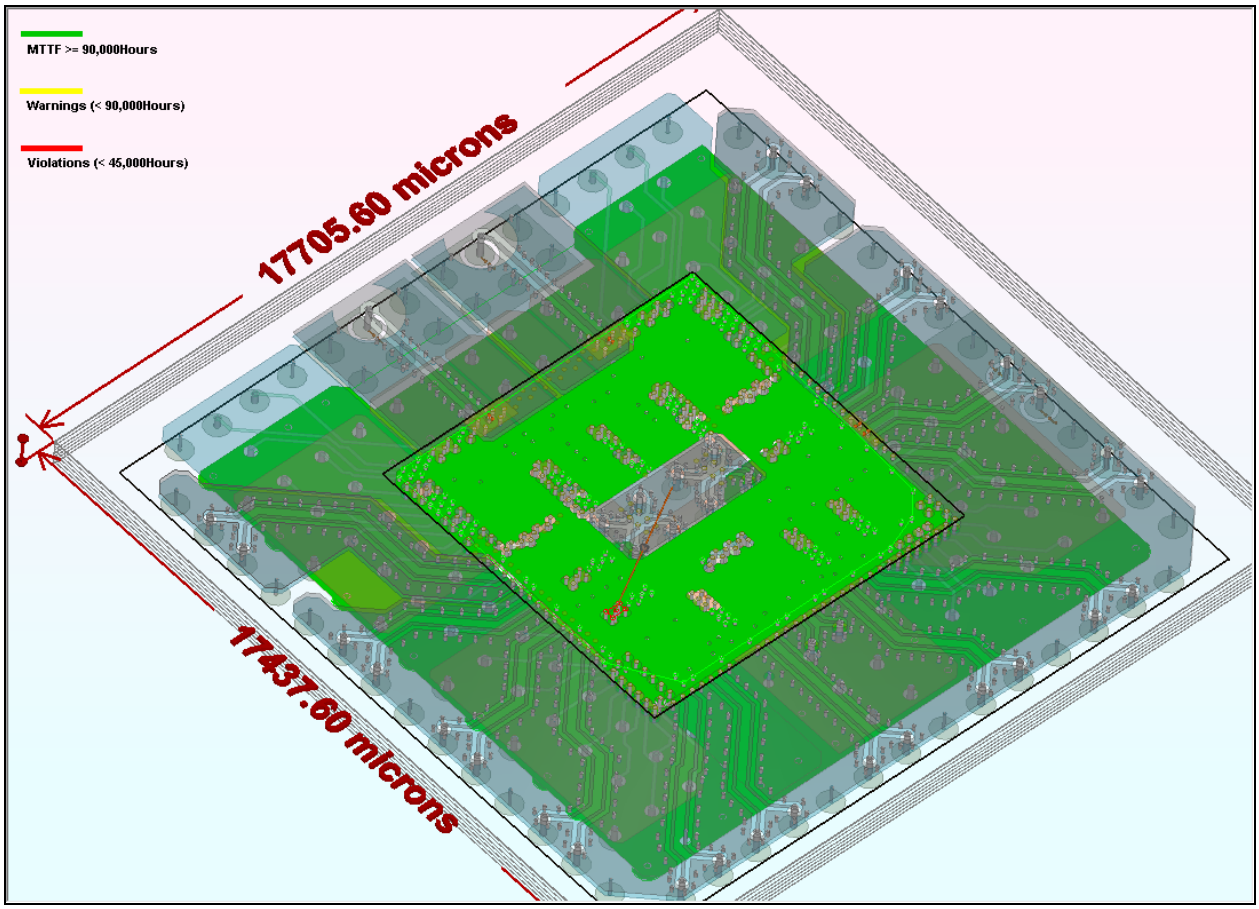

Green indicates an acceptable MTTF (>90000 hours), Yellow indicates a warning (<90000 hours), and Red indicates violations (<45000 hours).

Use the **Net List** to select or deselect nets for display. Use the layers list to do the same for layers. Click **Update Plot Display** to apply changes.

Use the Transparent/Opaque slider to adjust the MTTF plot's transparency, and click **Apply**.

You can also **Export Settings** in *.xml format, or **Import Settings** from a previously saved *.xml file.

Displaying MTTF Location Table

MTTF simulation results can be visualized in a tabular format that allows users to quickly navigate to regions on metal layers where MTTF is above/below a user-specified threshold, or navigate to individual vias and bondwires.

To display the MTTF Location Table:

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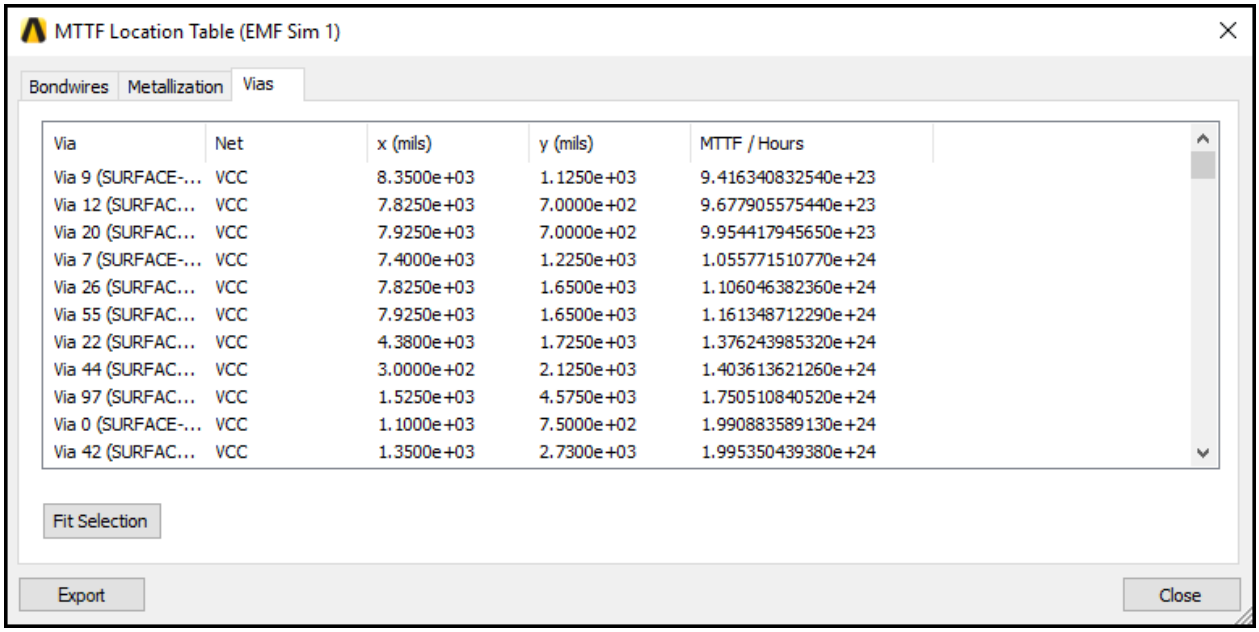
1. Compute an EM MTTF simulation.
2. Click **Results**.
3. From the **SIwave** area, click **EM MTTF** and select **Display MTTF Location Table**.

   The **MTTF Location Table** window appears.



   Use the **Bondwires**, **Metallization**, and **Vias** tabs to find the element you're looking for.

   Click an element to highlight it in yellow in the Modeling workspace.

   Click **Fit Selection** to zoom the Modeling workspace in or out to the area containing the selected element(s).

   Click **Export** to export MTTF information in MTTF Data (*.mttf) format.

EM MTTF Simulation Automation

You can use an XML configuration file to control the EM MTTF simulation flow non-graphically using siwave_ng.

Reference an XML file in the exec file passed as a command line argument to siwave_ng through an **`MTTFSimConfigFile`** directive:

```
MTTFSimConfigFile "C:/users/ansys/mttf_config.xml"
```

The following sample file shows the XML file syntax:

```
<?xml version="1.0" encoding="utf-8"?>

<SIwaveElectromigrationSimConfig>
```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```
  <Thresholds>
    <Warning MTTF="100000hour"/>
    <Error MTTF="50000hour"/>
  </Thresholds>
  <MaterialParameters>
    <Material Name="EDB_COPPER" ExperimentalConstant="1.1"
ActivationEnergy="0.8eV"/>
    <Material Name="EDB_GOLD" ExperimentalConstant="1.2"
ActivationEnergy="0.9eV"/>
    <Material Name="EDB_SOLDER" ExperimentalConstant="1.3"
ActivationEnergy="1.1eV"/>
    <Material Name="copper" ExperimentalConstant="1.4"
ActivationEnergy="0.7eV"/>
    <Material Name="gold" ExperimentalConstant="1.5"
ActivationEnergy="0.6eV"/>
    <Material Name="solder" ExperimentalConstant="1.6"
ActivationEnergy="0.89eV"/>
  </MaterialParameters>
  <CurrentDensityExponentRange>
    <CurrentDensity Start="0A_per_cm2" End="50A_per_cm2" n="1.2"/>
    <CurrentDensity Start="50A_per_cm2" End="200A_per_cm2" n="1.5"/>
    <CurrentDensity Start="200A_per_cm2" End="1e+99A_per_cm2" n="2"/>
    </CurrentDensityExponentRange>
  <DCSim Name="DC"/>
  <ApplyIcepakTemperature IcepakSimName="Icepak"/>
  <ApplyUniformTemperature Value="20cel"/>
</SIwaveElectromigrationSimConfig>
```

Computing Induced Voltage

SIwave can calculate the voltage at ports using plane wave excitation. The induced voltage will be measured at the ports. The incident wave can be a single incidence where it is described in

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spherical or Cartesian system. The incident wave can also be multiple where it is described only in spherical system with start and stop angles having a specific step.

To compute the induced voltage generated on the board by a plane wave incident at a particular angle with a specific polarization:

1. Click **Simulation**.
2. From the SIwave area, click **Compute Induced Voltage**.

   The **Compute Induced Voltage** window appears.

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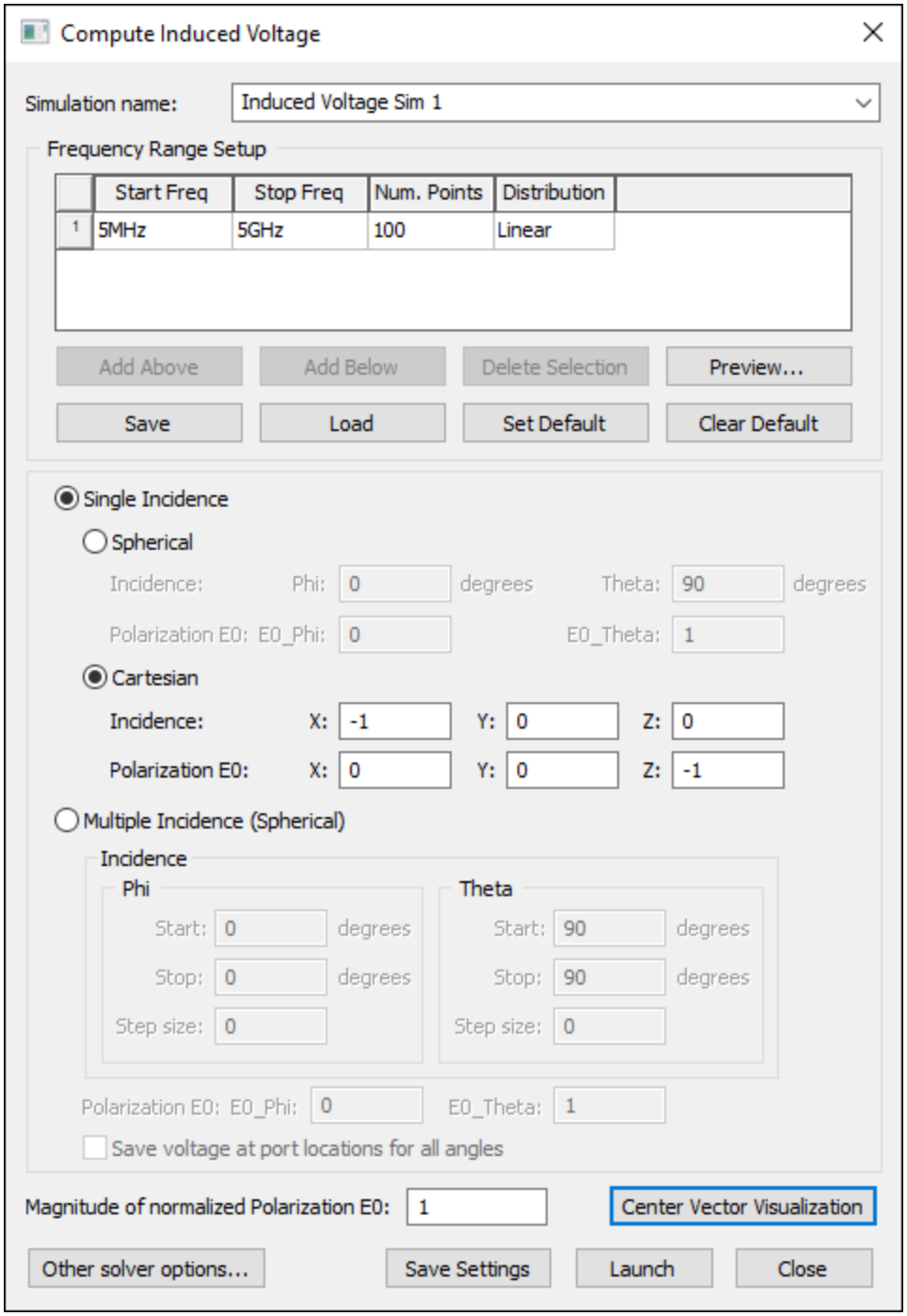

When the **Compute Induced Voltage** window is opened, a visualization of the incident wave (k) direction vector and the polarization wave (E0) direction vector will be visible in the drawing window at the bottom-left corner of the design. When **Single Incidence** is selected, there will be one k and one E0 vector. When **Multiple Incidence** is selected, there will be multiple vectors. The visualization updates as you make changes.

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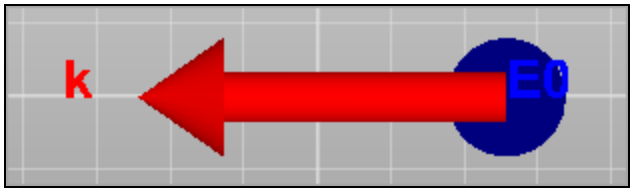

You can center the visualization by clicking **Center Vector Visualization**.

3. From the **Simulation name** field, enter a name for the simulation.
4. From the **Frequency Range Setup** area, enter values for the **Start Freq.**, **Stop Freq.**, and **Number of Points**.
5. Use the drop-down menu to select a **Distribution** method:
   - **Linear**– the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
   - **By Decade** – distributes the number of points specified logarithmically, over each decade.
6. If appropriate, add frequency points at an appropriate location using the **Add Above** and **Add Below** buttons. Delete a point by selecting its row and clicking **Delete Selection**. You can also **Save** your settings as an SIwave Frequency Sweep Distribution File (*.sfsdf) or **Load** previously saved settings from an *.sfsdf file.
7. If appropriate, click **Set Default** to set the current grid settings as a default value for that simulation type. Click **Clear Default** to return to the original default settings.
8. To preview all frequency points, click **Preview**. The **Frequency List Preview** window appears, showing all points.

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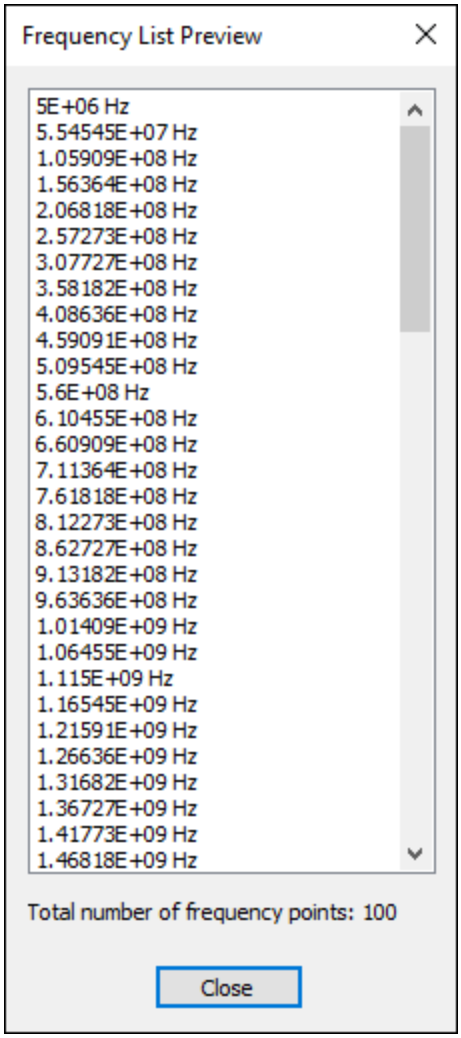

9. Click **Close** to return to the Compute Induced Voltage window.
10. From the **Frequency Range Setup** area, select one or more rows.
11. Select the incidence type you want. You can select either single or multiple incidence.
    - **Single Incidence** – choose either **Spherical** or **Cartesian**, then specify the **Incidence** wave vector and the **Polarization** vector of the plane wave.
    - **Multiple Incidence (Spherical)** – enter the sweep on the angle on of incidence under **Phi** and **Theta**. Specify the **Polarization**. Check the **Save Voltage at port locations for all angles** check box to save and plot induced voltage at every sweep in angle for every frequency, instead of max induced voltage for every frequency plotted.
12. If you want to save these settings and use them for subsequent simulations, click **Save Settings**.
13. If you want to change additional simulation options, click **Other solver options**.
14. Click **Launch** to begin the simulation.

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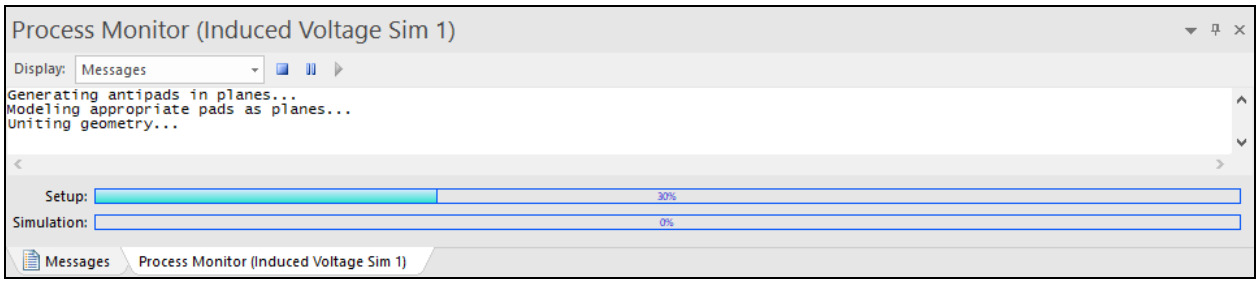
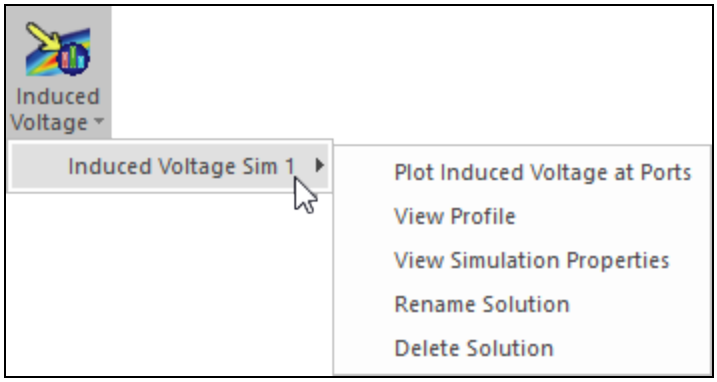
The **Messages** window updates with a Process Monitor tab that displays the progress.



Viewing Induced Voltage Results in SIwave

To view the results of an induced voltage analysis:

1. Click **Results**.
2. From the SIwave area, select **Induced Voltage** > **[Simulation Name]**.



3. Click **Plot Induced Voltage at Ports**.

   The **Induced Voltage Plot Generation** window appears.

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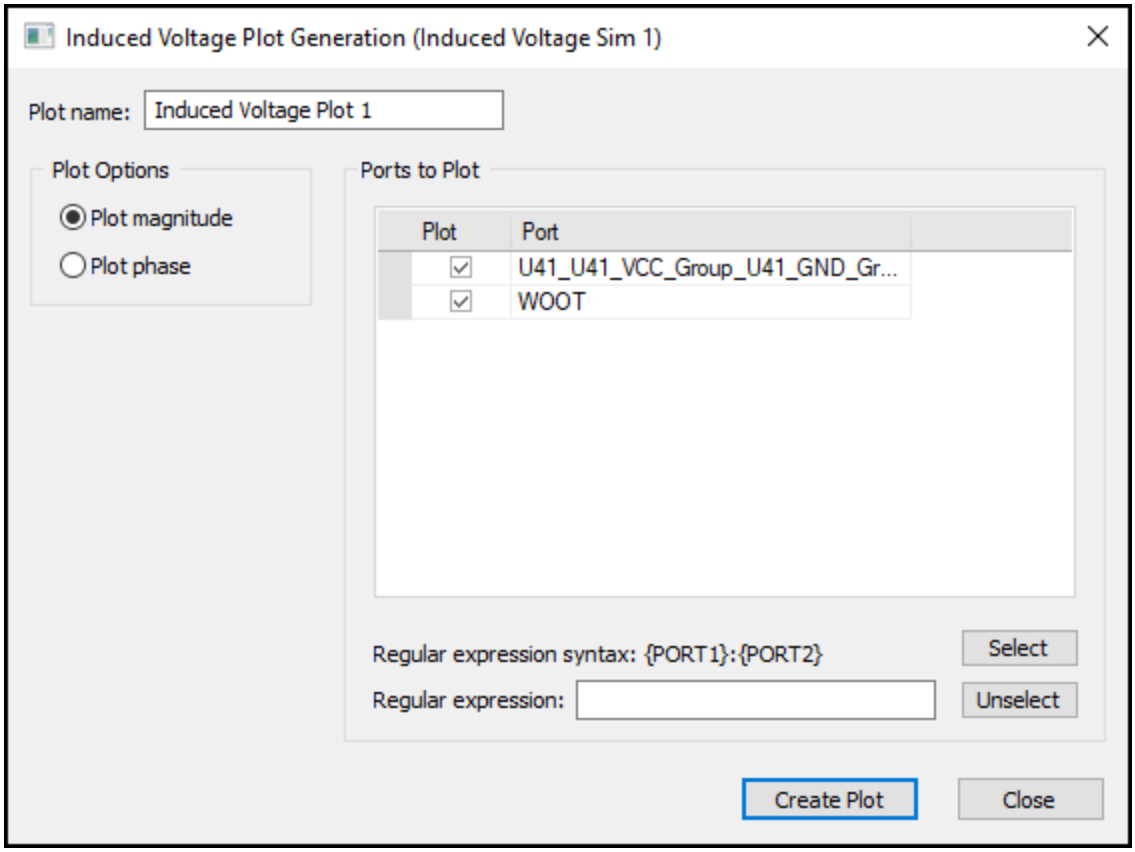

4. From the **Plot Name** field, enter a name for the plot.
5. From the **Plot Options** area, use the radio buttons to select whether to plot magnitude or phase.
6. From the **Ports to Plot** area, use the check boxes to select or deselect ports. You can also use a **regular expression** to select or deselect ports.
7. Click **Create Plot**.

   Ansys Electronics Desktop launches and displays the plot.

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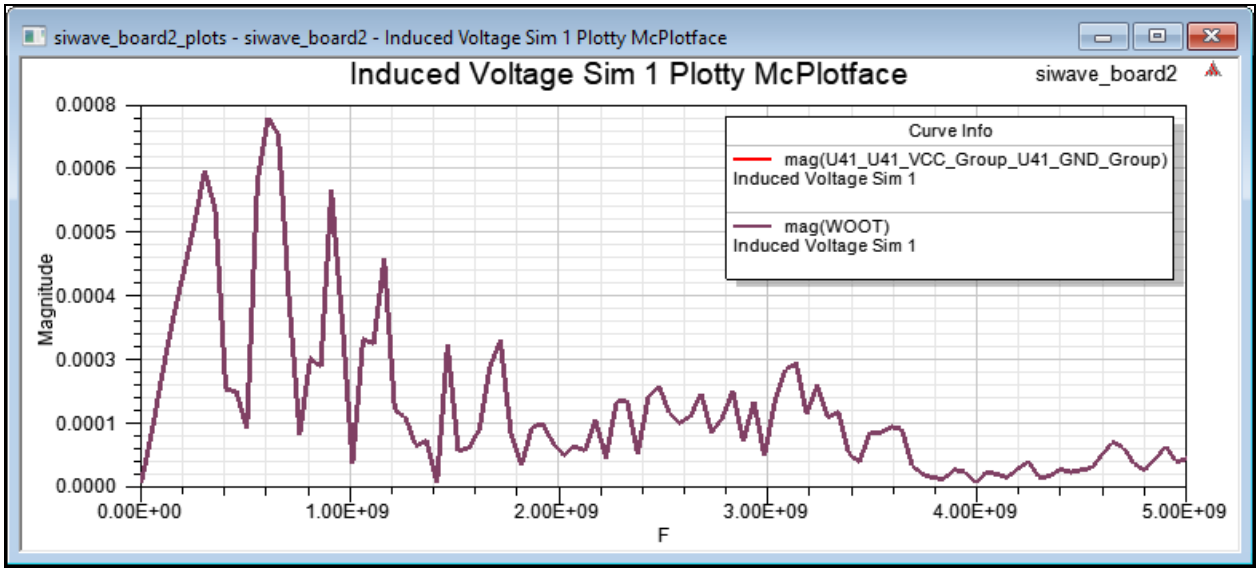
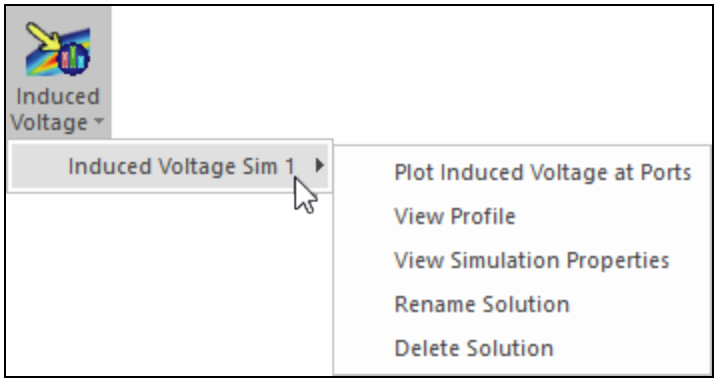


From the Induced Voltage Results menu, you can also access additional menu options.

Induced Voltage Results Menu Options

Navigate to the Induced Voltage Results menu:

1. Click **Results**.
2. From the SIwave area, select **Induced Voltage** > **[Simulation Name]**.



Menu options include:

- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the **Simulation Properties** window on the **Induced Voltage** tab, and generates a visualization of the incident wave (k) direction vector and the polarization wave (E0) direction vector in the lower-left corner of the design. See: Computing Induced Voltage.

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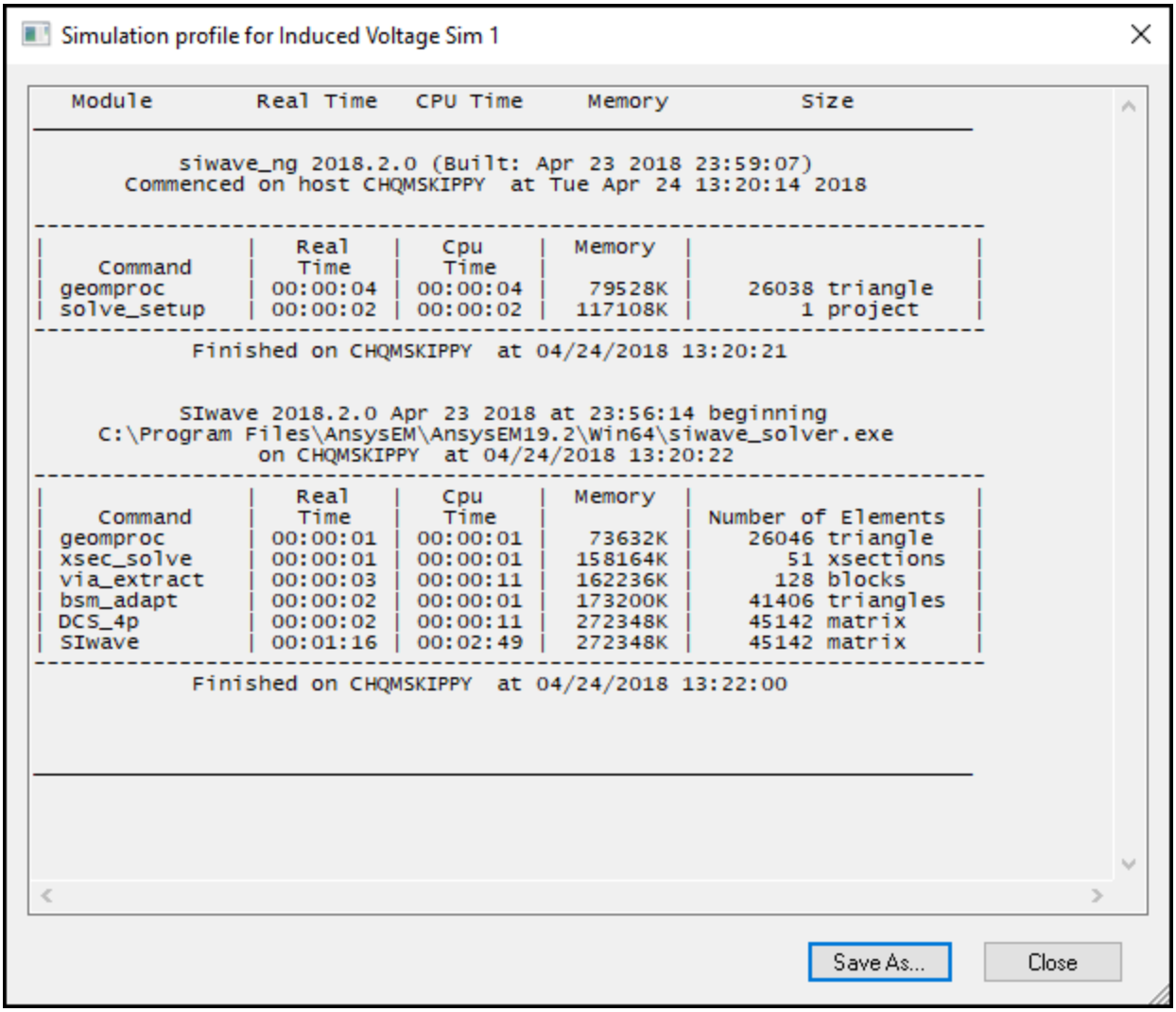
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Simulation Profile:



Simulation Properties:

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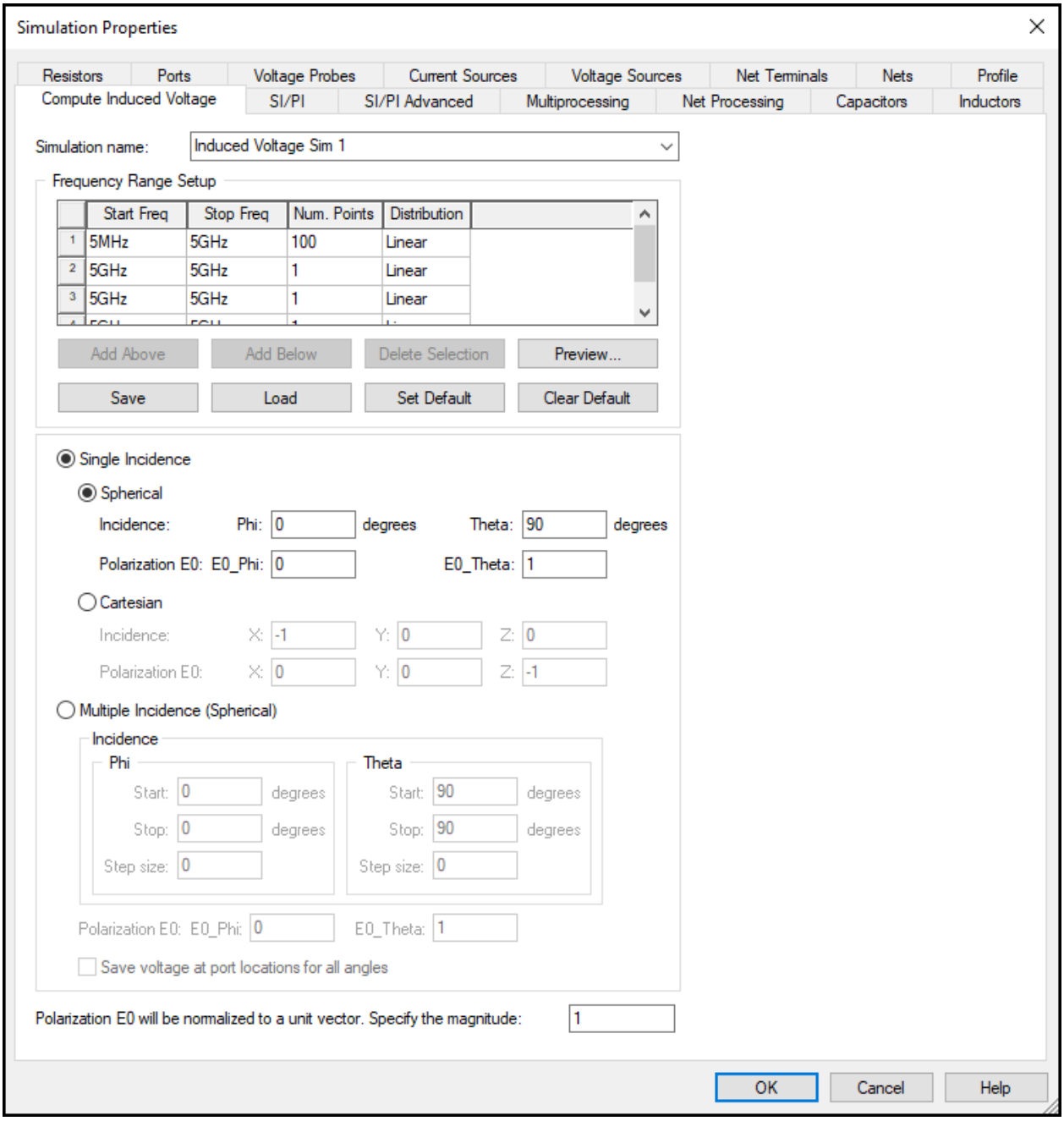

From the Induced Voltage results menu, you can also view Induced Voltage results.

Crosstalk Scans

The Crosstalk Scanner allows you to quickly detect near and far-end signal line crosstalk violations.

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When you select a set of nets, SIwave checks every possible pair of coupled lines within that set. SIwave then compares all crosstalk coefficients to determine whether a line is an aggressor or victim and reports the maximum NEXT or FEXT coefficient that the line can possibly experience.

> **Note:**
>
> It is not possible to specify aggressor or victim lines, as the scan must cover all specified nets in order to report maximum values.

Topics in this section:

- Crosstalk Scan - Frequency Domain
- Crosstalk Scan - Time Domain
- Crosstalk Scan Automation

Computing a Crosstalk Scan - Frequency Domain

To run the frequency domain crosstalk scan in SIwave:

1. Click **Simulation**.
2. From the SIwave area, select **Crosstalk Scan** > **Frequency Domain**.

   The **FEXT/NEXT Crosstalk Scan** window appears, on the **Single Ended** tab.

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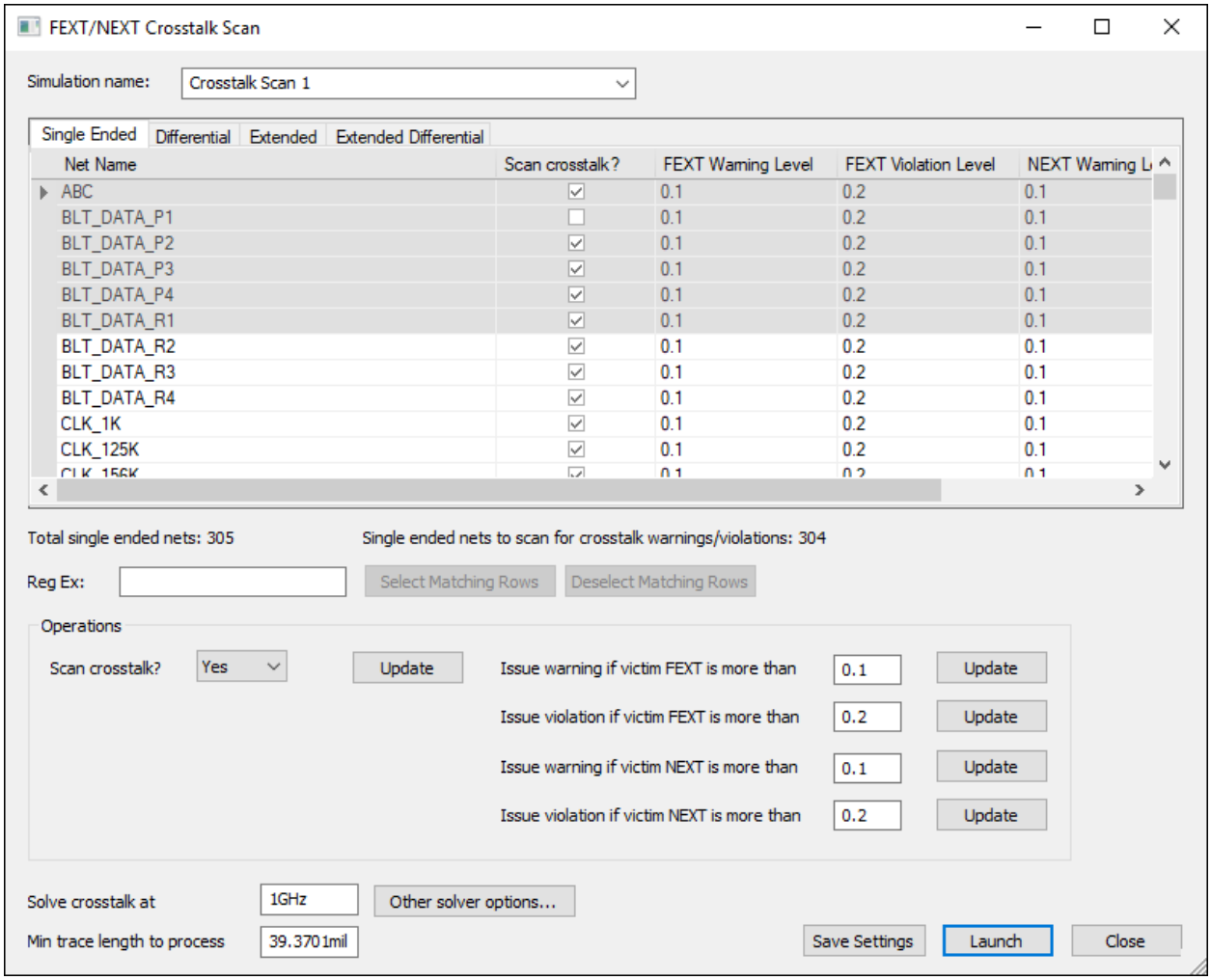

3. Navigate using the tabs and select one or more **Single Ended**, **Differential**, **Extended**, or **Extended Differential** nets. You can also use **regular expressions** to select and deselect nets.
4. Use the **Scan crosstalk?** check boxes to denote which nets will be scanned.
5. From the **Operations** area, enter values the NEXT and FEXT warning and violation thresholds.
6. If appropriate, update the **Solve crosstalk at** and **Min trace length to process** fields.
7. If appropriate, click Save Settings to save your settings.
8. Click **Launch** to run the simulation.

   The **Messages** window updates with a Process Monitor tab that displays the progress.

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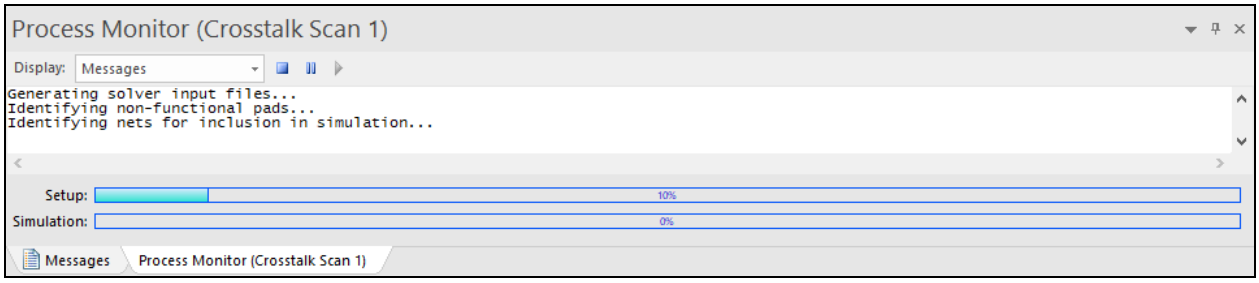
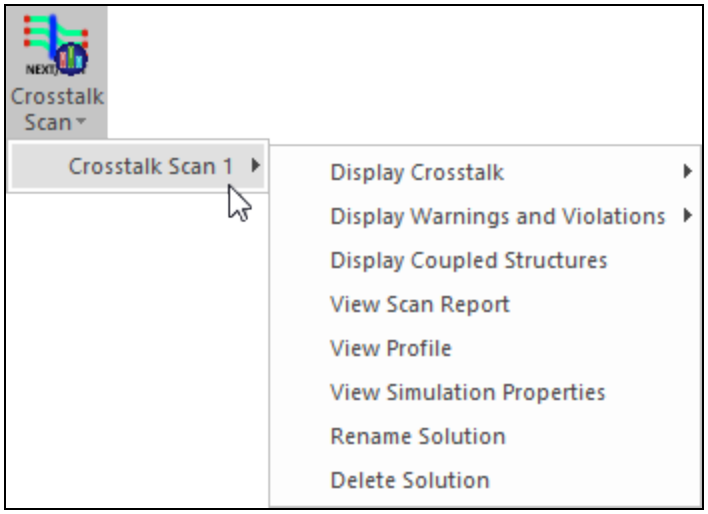


You can view crosstalk scan results, access additional results menu options, or automate crosstalk scans.

Viewing Crosstalk Scan Results in SIwave

To view the results of a crosstalk scan:

1. Click **Results**.
2. From the SIwave area, select **Crosstalk Scan** > **[Simulation Name]**.



3. Select the results you want to display.

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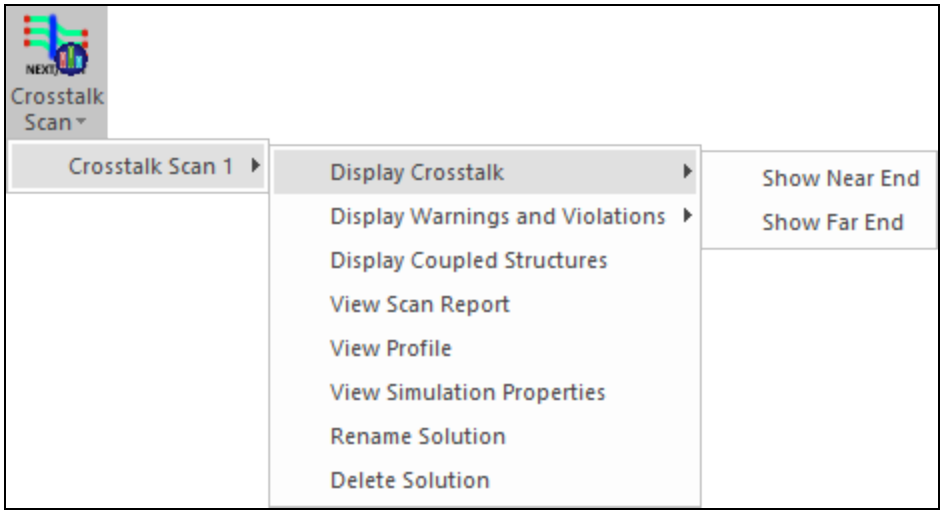

Result menu options include:

- Display Crosstalk>Show Near End
- Display Crosstalk>Show Far End
- Display Warnings and Violations>Show Near End
- Display Warnings and Violations>Show Far End

The applicable **Trace Crosstalk** window appears.

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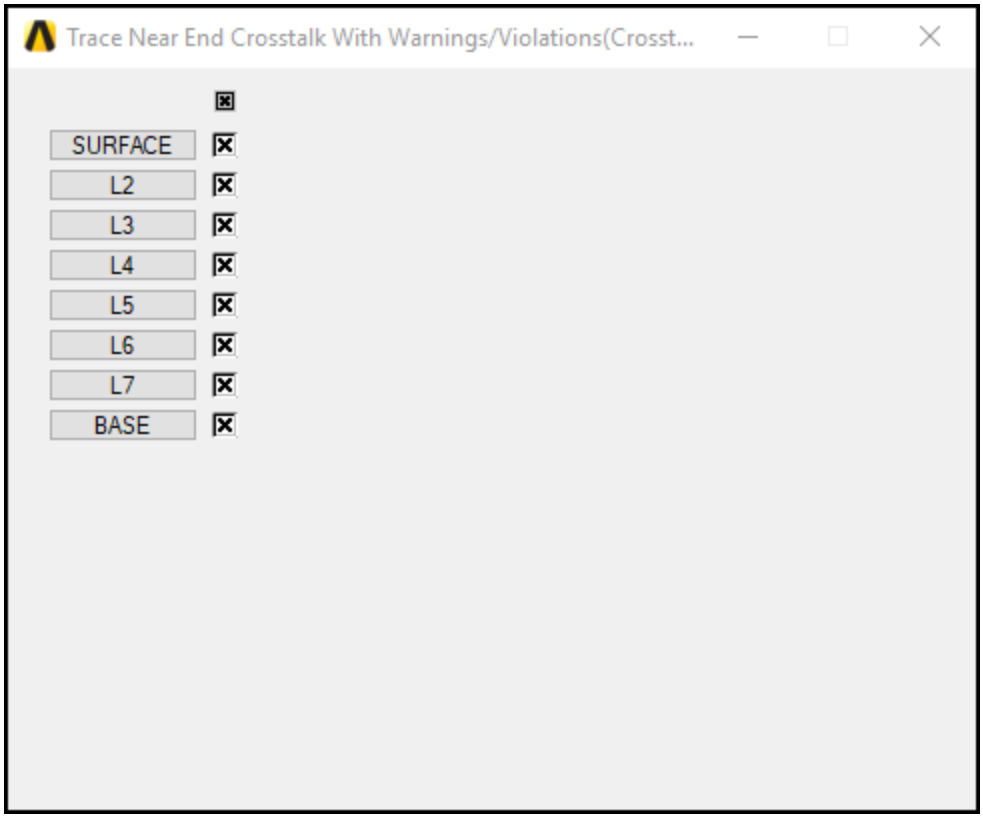

Use the check boxes to select layers on which to display crosstalk information.

Results display in the Modeling workspace. Hover the mouse pointer over a trace section in the layout. Crosstalk coefficients are overlaid on top of the layouts.

Warnings and Violations are indicated by color overlays. Traces within threshold are green, those with a warning are orange, those with a violation are red, and those belonging to differential but that are not coupled appear gray.

From the Crosstalk Scan Results menu, you can also access additional menu options.

Crosstalk Scan Results Menu Options

Navigate to the Crosstalk Scan Results menu:

1. Click **Results**.
2. From the SIwave area, select **Crosstalk Scan** > **[Simulation Name]**.

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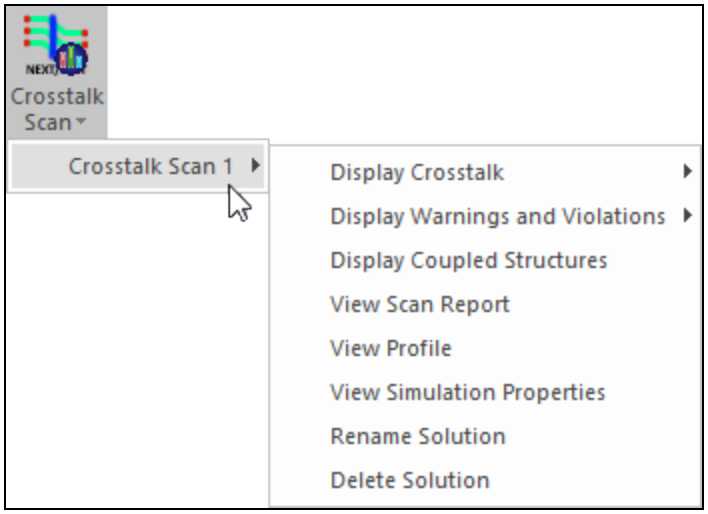

Menu options include:

- **Display Coupled Structures** – displays coupled structures in the Modeling workspace.
- **View Scan Report** – opens an *.html file detailing the scan properties and results.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the SI/PI tab.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Scan Report:

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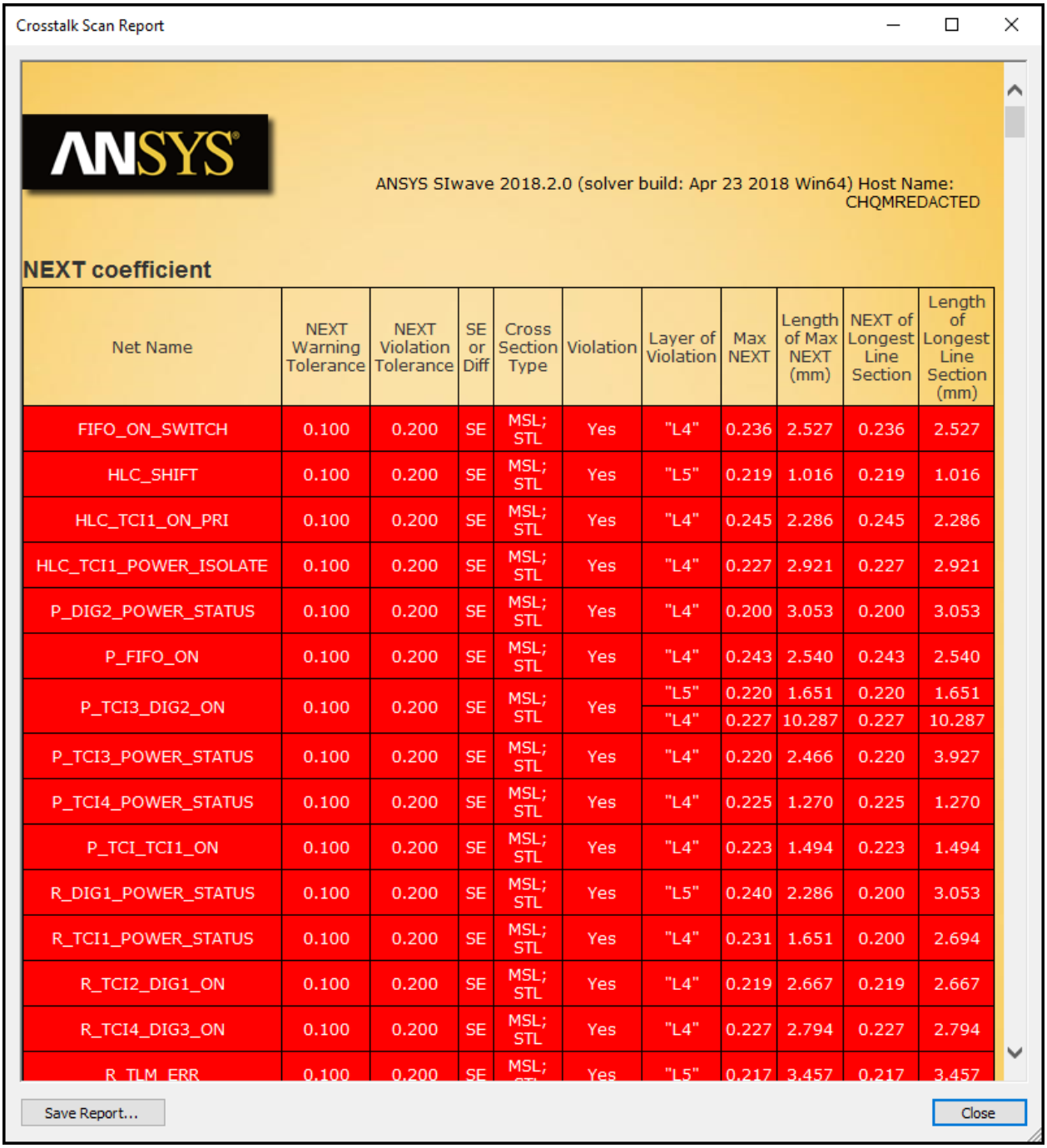
Crosstalk Scan Report

ANSYS SIwave 2018.2.0 (solver build: Apr 23 2018 Win64) Host Name: CHQMREDACTED

NEXT coefficient

Net Name	NEXT Warning Tolerance	NEXT Violation Tolerance	SE or Diff	Cross Section Type	Violation	Layer of Violation	Max NEXT	Length of Max NEXT (mm)	NEXT of Longest Line Section	Length of Longest Line Section (mm)
FIFO_ON_SWITCH	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.236	2.527	0.236	2.527
HLC_SHIFT	0.100	0.200	SE	MSL; STL	Yes	"L5"	0.219	1.016	0.219	1.016
HLC_TCI1_ON_PRI	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.245	2.286	0.245	2.286
HLC_TCI1_POWER_ISOLATE	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.227	2.921	0.227	2.921
P_DIG2_POWER_STATUS	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.200	3.053	0.200	3.053
P_FIFO_ON	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.243	2.540	0.243	2.540
P_TCI3_DIG2_ON	0.100	0.200	SE	MSL; STL	Yes	"L5"	0.220	1.651	0.220	1.651
						"L4"	0.227	10.287	0.227	10.287
P_TCI3_POWER_STATUS	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.220	2.466	0.220	3.927
P_TCI4_POWER_STATUS	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.225	1.270	0.225	1.270
P_TCI_TCI1_ON	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.223	1.494	0.223	1.494
R_DIG1_POWER_STATUS	0.100	0.200	SE	MSL; STL	Yes	"L5"	0.240	2.286	0.200	3.053
R_TCI1_POWER_STATUS	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.231	1.651	0.200	2.694
R_TCI2_DIG1_ON	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.219	2.667	0.219	2.667
R_TCI4_DIG3_ON	0.100	0.200	SE	MSL; STL	Yes	"L4"	0.227	2.794	0.227	2.794
R_TLM_ERR	0.100	0.200	SE	MSL;	Yes	"L5"	0.217	3.457	0.217	3.457

Save Report...

Close

Simulation Profile:

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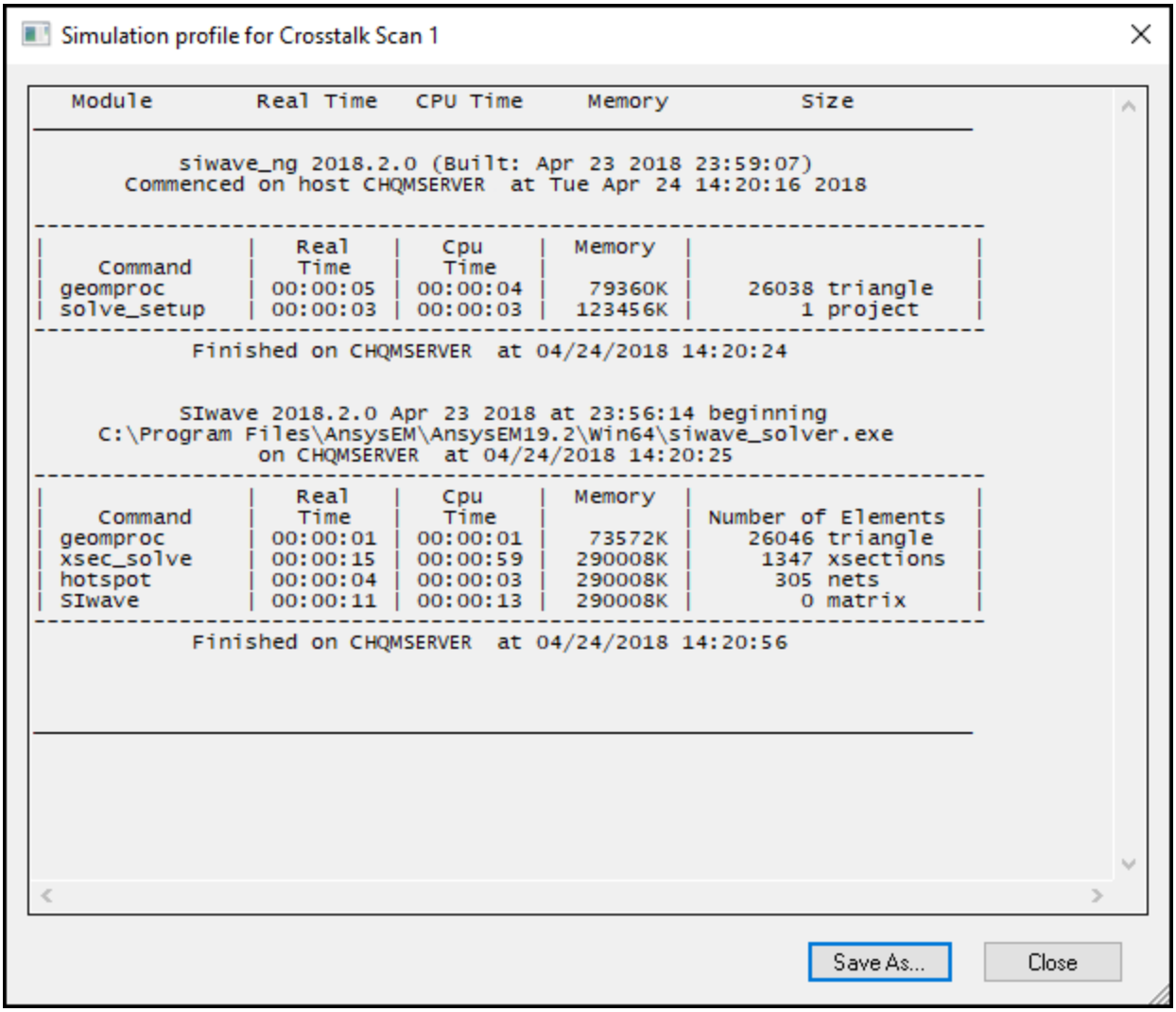

Simulation Properties:

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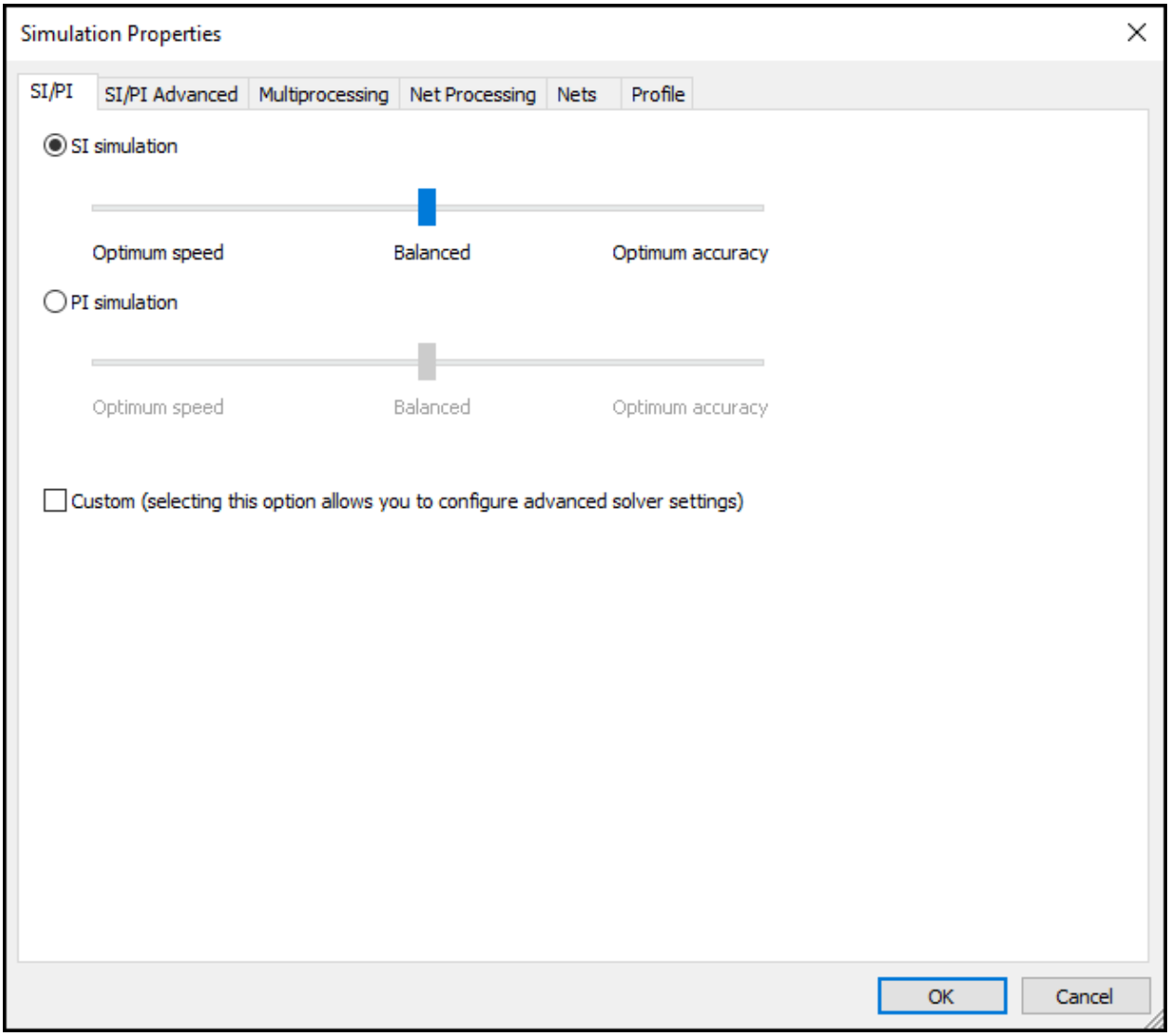

From the Crosstalk Scan results menu, you can also view Crosstalk Scan results.

Computing a Crosstalk Scan - Time Domain

You can perform a time domain crosstalk scan on either a single-ended net or on a differential pair.

> **Note:**
>
> Signal and impedance settings for differential pairs refer only to the differential signal.
>
> Likewise, differential pair results refer only to the differential signal.

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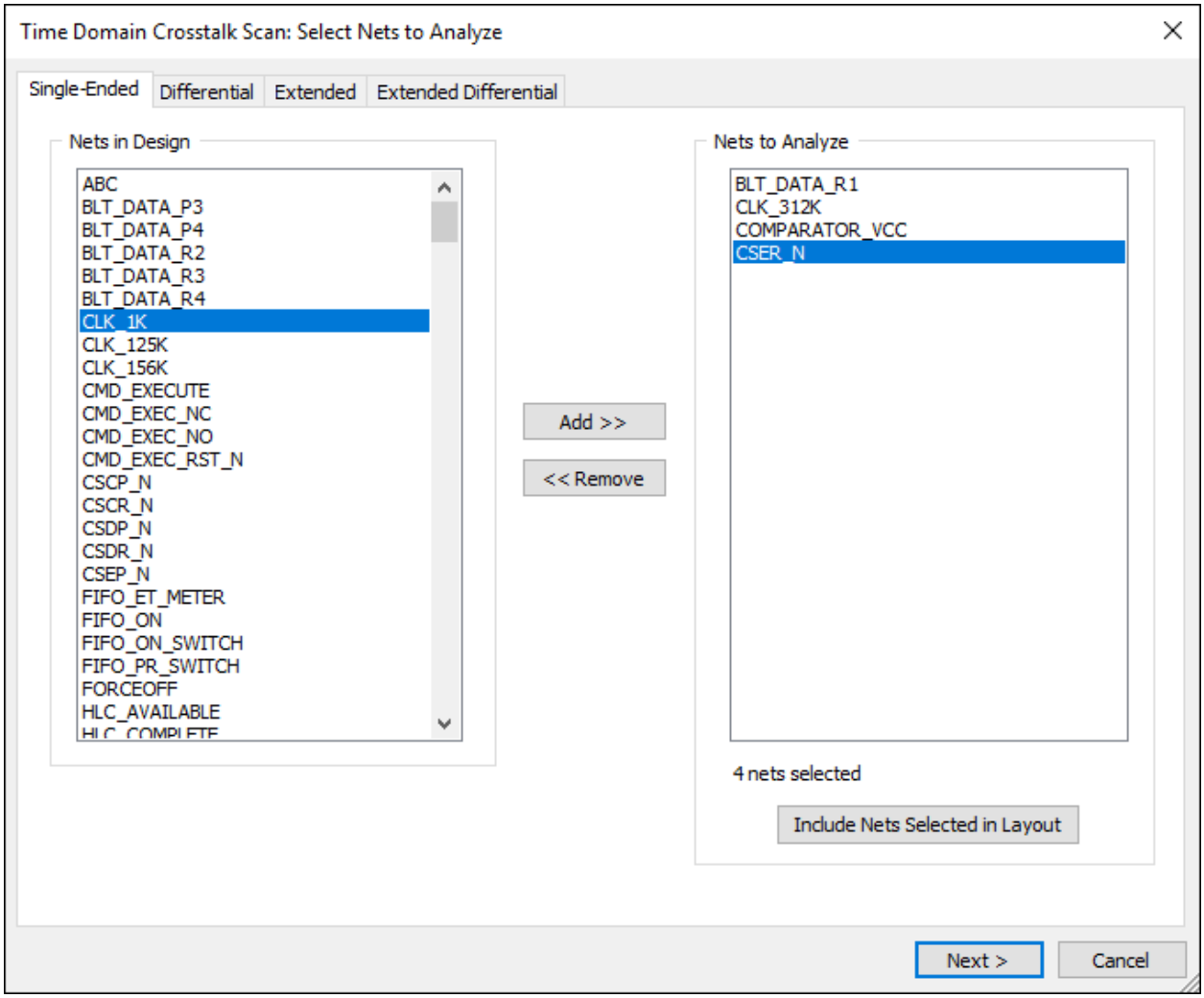
To run the time domain crosstalk scan in SIwave:

1. Click **Simulation**.
2. From the SIwave area, select **Crosstalk Scan** > **Time Domain**.

   The **Time Domain Crosstalk Scan** window appears, on the **Single-Ended** nets tab.



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3. Find the nets you want to analyze:
   - For single-ended nets, select the **Single-Ended** or **Extended** tab.
   - For differential pairs, select the **Differential** or **Extended Differential** tab.

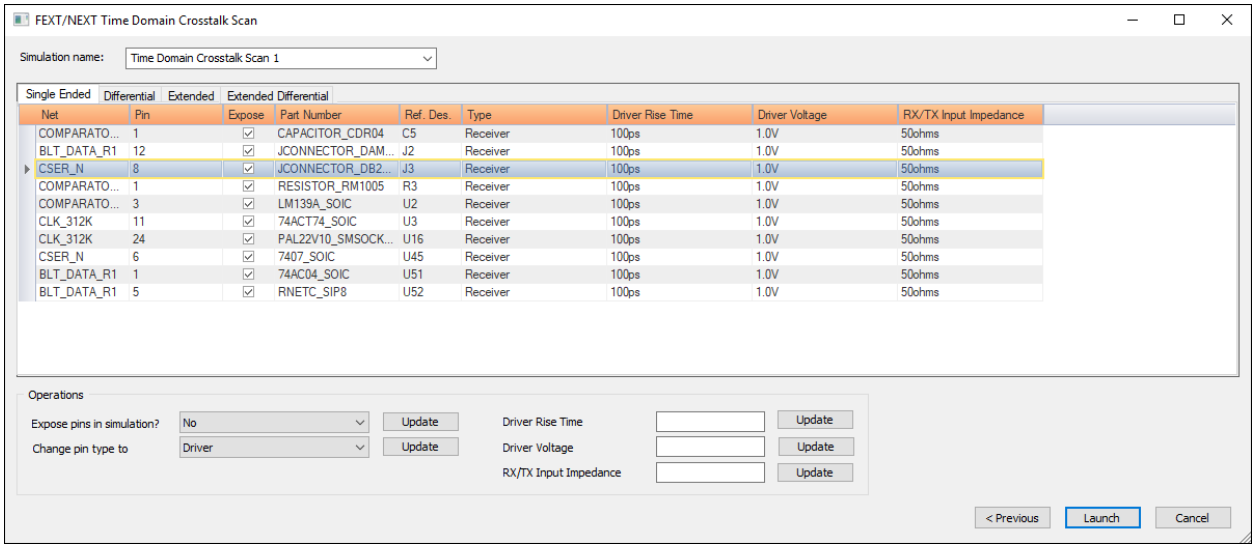
   > **Note:**
   >
   > An extended differential net must have *both* a corresponding extended net definition pair *and* a corresponding differential net definition set containing at least 2 entries.

4. Select nets and use the **Add** and **Remove** buttons to determine which will be analyzed.

   If you want to include all nets selected in the layout, click **Include Nets Selected in Layout**.

5. Click **Next**.

   The **FEXT/NEXT Time Domain Crosstalk Scan** window appears.



6. User the **Single Ended**, **Differential**, **Extended**, and **Extended Differential** tabs to find nets.
7. Select a net by clicking to the left of its row, then select your appropriate options.
8. Click **Launch** to run the simulation.

To view peak voltages:

1. Click **Results**.
2. From the SIwave area, select **Time Domain Crosstalk Scan** > **[Simulation Name]**.
3. Click **View Peak Voltages**.

   The **Crosstalk Peak Voltage Viewer** window appears.

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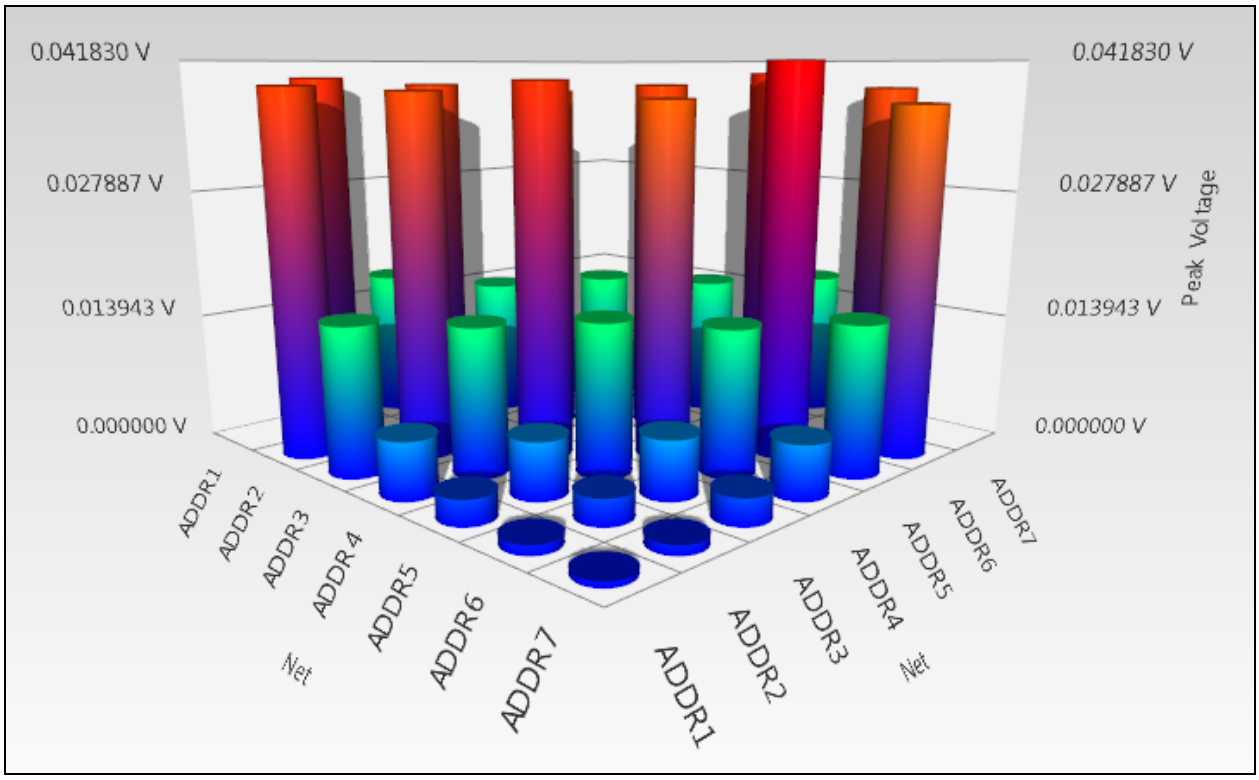
If appropriate, click **Show Voltage** to display the plot.

At any time, use the check box to **Maintain original net selections on close**.

The 3D Peak Voltage Plot appears with the 3D bar chart representing peak voltages in the upper section of the display. One axis of the 3D plot represents aggressor nets and the other represents victim nets.



Use the **Plot type** menu to select **Near End Peak Voltage** or **Far End Peak Voltage** to be displayed.

Use the check boxes and menus in the **Bar graph settings** panel to control the plot appearance:

- **Show background** toggles the shadowing behind the bars.
- **Show grid** toggles the grid lines.
- **Axes titles visible** toggles the display of the axis titles.
- **Show color scale** toggles the display of a color scale used for the voltage.
- To select a pair of nets, click on the bar. **Select nets in main frame** causes any selected net pairs to be selected in the SIwave Modeling workspace. The names of the selected nets are displayed in the **Current selected nets** field, and the voltage is displayed in the **Voltage** field; these fields are just below the **Select nets in the main frame** check box.

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- **Change bar style** toggles between **Cylinder** (circular) and **Bar** (rectangular) shapes.
- **Change plot view** selects one of four views: **Isometric view** (3D effect with perspective), **X-axis view**, **Y-axis view**, or **Top view**.
- **Change color scheme** selects the color pattern used for the bars: **Smooth gradient**, **Heat map** (lower voltages cooler, higher voltages hotter), and **Primary color** (all bars the same color).
- **Change selection mode** provides a menu in two parts. The first six options determine how much gets selected when you click on a bar: **Bar**, **Row**, **Bar and Row**, **Column**, or **Bar and Column**. Then the last four options allow you to change the display from 3D to 2D slice of the selected bar, row, or column: **Slice into Row**; **Slice into Column**; **Slice into Row, Item**; or **Slice into Colum, Item**. You must have something selected to get the 2D slice.
- The **Adjust label orientation** slider controls the positions of the net names.
- The **Adjust label font size** slider controls the size of the font used for the net names.
- The **Rotate horizontally** and **Rotate vertically** sliders control the orientation of the 3D plot.

> **Note:**
>
> You can also rotate the plot by holding down the middle mouse button and dragging, or by pressing Alt plus the left mouse button and dragging.

- You can zoom the display by rotating the mouse wheel or by pressing Shift Alt plus the left mouse button and dragging.
- You can reset the view by pressing Shift Alt plus double-clicking the left mouse button.

The lower portion of the Peak Voltage display is a 2D time domain **Waveform** of the voltages. Click on a bar to display the corresponding waveform:

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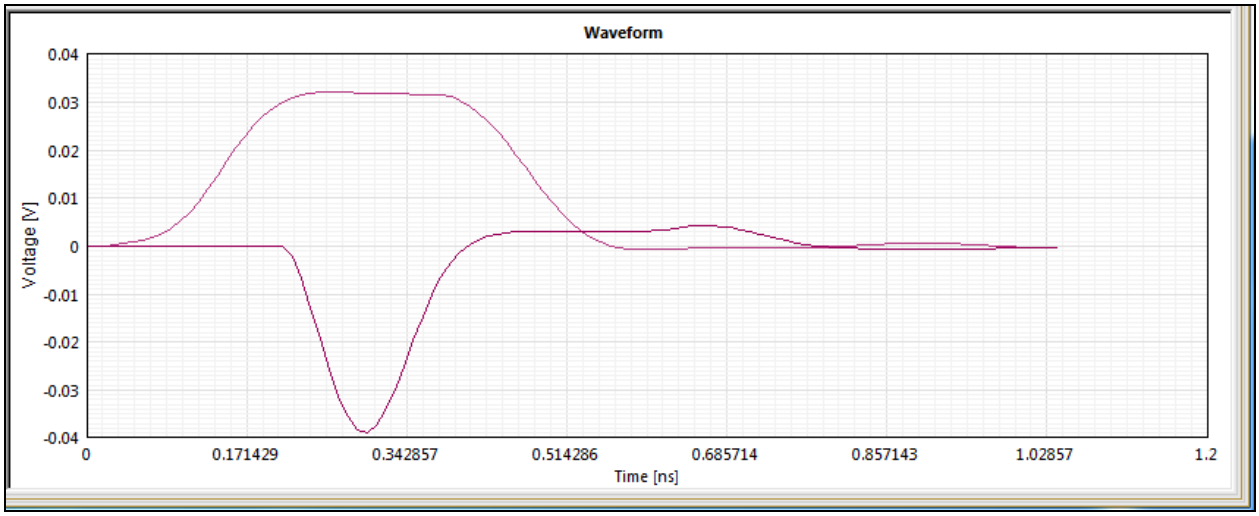

The titles of the traces display when you move the cursor over the traces.

- By default, the **Curve type** shows the near end voltage [V(next)] and the far end voltage [V(fext)]. Use the check boxes in the **Curve type** panel to display the input voltage [V(in)] or the output voltage [V(out)].
- the check box **Show curves for multiple bars** allows you to accumulate traces from multiple bars as you select each one in turn.
- The **Axis settings** panel controls the range and units to be used for the X- and Y-axes in the waveform plot.
- Click **Clear plot** to clear the waveform plot.

To view time domain crosstalk maximum voltages, click **Results** > **SIwave** > **Time Domain Crosstalk Scan**. Then select the simulation name and click **Display Time Domain crosstalk max voltages**.

To see what portions of the geometry are being coupled, click **Results** > **SIwave** > **Time Domain Crosstalk Scan**. Then select the simulation name and click **Display Coupled Structures**. Thick and thin colored lines are visible along with thick gray lines. The gray color signifies that a portion is not coupled to anything, while other colors signify coupling to other traces or planes. Thick lines represent traces, and thin lines show plane edges. A colored (thick or thin) line signifies that it is coupled to another trace or plane edge. Gray lines (trace only) are not coupled. Uncoupled plane edges are not visible, so there are no thin gray lines. When this option is selected, you can toggle it off by selecting **Hide Coupled Structures**.

To display a summary of CPU and memory usage during the crosstalk scan, select the simulation name and click **View Profile**.

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To view nets and pins that were selected for the simulation, click **Results** > **SIwave** > **Time Domain Crosstalk Scan**. Then select the simulation name and click **View Simulation Properties**.

To rename the simulation, click **Results** > **SIwave** > **Time Domain Crosstalk Scan**. Then select the simulation name and click **Rename Solution**.

To delete the simulation, click **Results** > **SIwave** > **Time Domain Crosstalk Scan**. Then select the simulation name and click **Delete Solution**.

You can also automate crosstalk scanning.

Crosstalk Scan Automation

You can use an XML configuration file to control the simulation flow to drive impedance, frequency and time domain scans non-graphically using siwave_ng.

Reference an XML file in the exec file passed as a command line argument to siwave_ng through a **`CrosstalkScanConfigFile`** directive:

```
CrosstalkScanConfigFile "C:/users/ansys/siwave_scan.xml"
```

> **Note:**
>
> In all of the examples given below, net names can be specified using Perl regular expressions.

To run an **impedance scan**, use an XML file to specify the nets to include in the simulation along with the percentage values indicating impedance warning and violation thresholds. See example below:

```
<?xml version="1.0" encoding="utf-8"?>
<SIwaveScanConfig xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">
      <Z0ScanConfig MinTlineSegmentLength="0.33mm" Z0Frequency="2e9Hz">
      <SingleEndedNets>
         <Net Name="RAMADD.*" NominalZ0="50.0" WarningThreshold="17.0"
         ViolationThreshold="32.0" />
         <Net Name="RAMD.*" NominalZ0="60.0" WarningThreshold="27.0"
         ViolationThreshold="37.0" />
      </SingleEndedNets>
      </Z0ScanConfig>
 </SIwaveScanConfig>
```


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To run a **frequency domain crosstalk scan**, the XML file should specify the nets to include in the simulation along with the percentage values indicating far and near end crosstalk warning and violation thresholds. See example below:

```
<?xml version="1.0" encoding="utf-8"?>
<SIwaveScanConfig xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">
     <FdXtalkConfig MinTlineSegmentLength="0.25mm"
        XtalkFrequency="2.25e9Hz">
        <SingleEndedNets>
             <Net Name="M_DQ_.*" FEXTWarningThreshold="7"
             FEXTViolationThreshold="17" NEXTWarningThreshold="7"
             NEXTViolationThreshold="17" />
             <Net Name="M_MA_.*" FEXTWarningThreshold="11"
             FEXTViolationThreshold="22" NEXTWarningThreshold="11"
             NEXTViolationThreshold="22" />
        </SingleEndedNets>
     </FdXtalkConfig>
</SIwaveScanConfig>
```

To run a **time domain crosstalk scan**, you can specify nets to simulate in one (or both) ways:

- Listing the nets to include - for each such net, SIwave automatically sets the lower-most/left-most pin to be the driver and the upper-most/right-most pin to be the receiver.
- Explicitly list and classify driver and receiver pins.

You can also specify the driver voltage, driver signal rise time, driver impedance and termination/receiver impedance. If these attributes are omitted, SIwave assigns reasonable defaults (1.0V for the driver voltage, 100ps for the driver rise time and 50ohm for the impedances) and proceeds with the simulation. See example below:

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```
<?xml version="1.0" encoding="utf-8"?>

<SIwaveScanConfig xmlns:xsi="http://www.w3.org/2001/XMLSchema-instance">

     <TdXtalkConfig>

        <SingleEndedNets>

             <!-- for each specified net, the lowermost/leftmost pin is set
             as the driver -->

             <!-- and the uppermost/rightmost pin is set as the receiver -->

             <Net Name="A0.*" DriverRiseTime="125ps" Voltage="3300mV"
             DriverImpedance="44.0ohm" TerminationImpedance="50.0ohm" />

        </SingleEndedNets>

        <DriverPins>

             <Pin Name="2" RefDes="U4" DriverRiseTime="50e-12s"
             Voltage="1.0V" DriverImpedance="50.0ohm" />

             <Pin Name="1" RefDes="U4" DriverRiseTime="75e-12s"
             Voltage="1.0V" DriverImpedance="50.0ohm" />

        </DriverPins>

        <ReceiverPins>

             <Pin Name="39" RefDes="U8" ReceiverImpedance="50.0ohm" />

             <Pin Name="10" RefDes="U8" ReceiverImpedance="50.0ohm" />

        </ReceiverPins>

     </TdXtalkConfig>

</SIwaveScanConfig>
```

Computing Icepak Simulations

The Icepak simulation type is useful for spotting potential thermal trouble spots in designs and can be used to improve accuracy of DC simulation results. Users can run the simulation and export the results. The Icepak simulation type is only accessible when there are DC simulation results that exported power dissipation data.

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Important:

The Icepak simulation will not run if the **File name** or **path** contains spaces or special characters.

Complete these steps to perform an Icepak simulation in SIwave.

1. From **Simulation**, select **Icepak** to open the **Icepak Simulation Setup** window. Navigate through the five tabs and make all appropriate selections (i.e., **Simulation Setup**, **Thermal Environment**, **Component Configuration**, **Component Materials**, and **Icepak Cabinet Size**).

   Note:

   Tabs are enabled depending on selection(s) made in the **Thermal Simulation Type** area of the **Simulation Setup** tab:

   - **Conduction** — **Simulation Setup** and **Thermal Environment**
   - **Conduction** and **Include Components (AEDT Only)** — **Simulation Setup**, **Thermal Environment**, **Component Configuration**, and **Component Materials**
   - **Convection** — **Simulation Setup**, **Thermal Environment**, **Component Configuration**, **Component Materials**, and **Icepak Cabinet Size**

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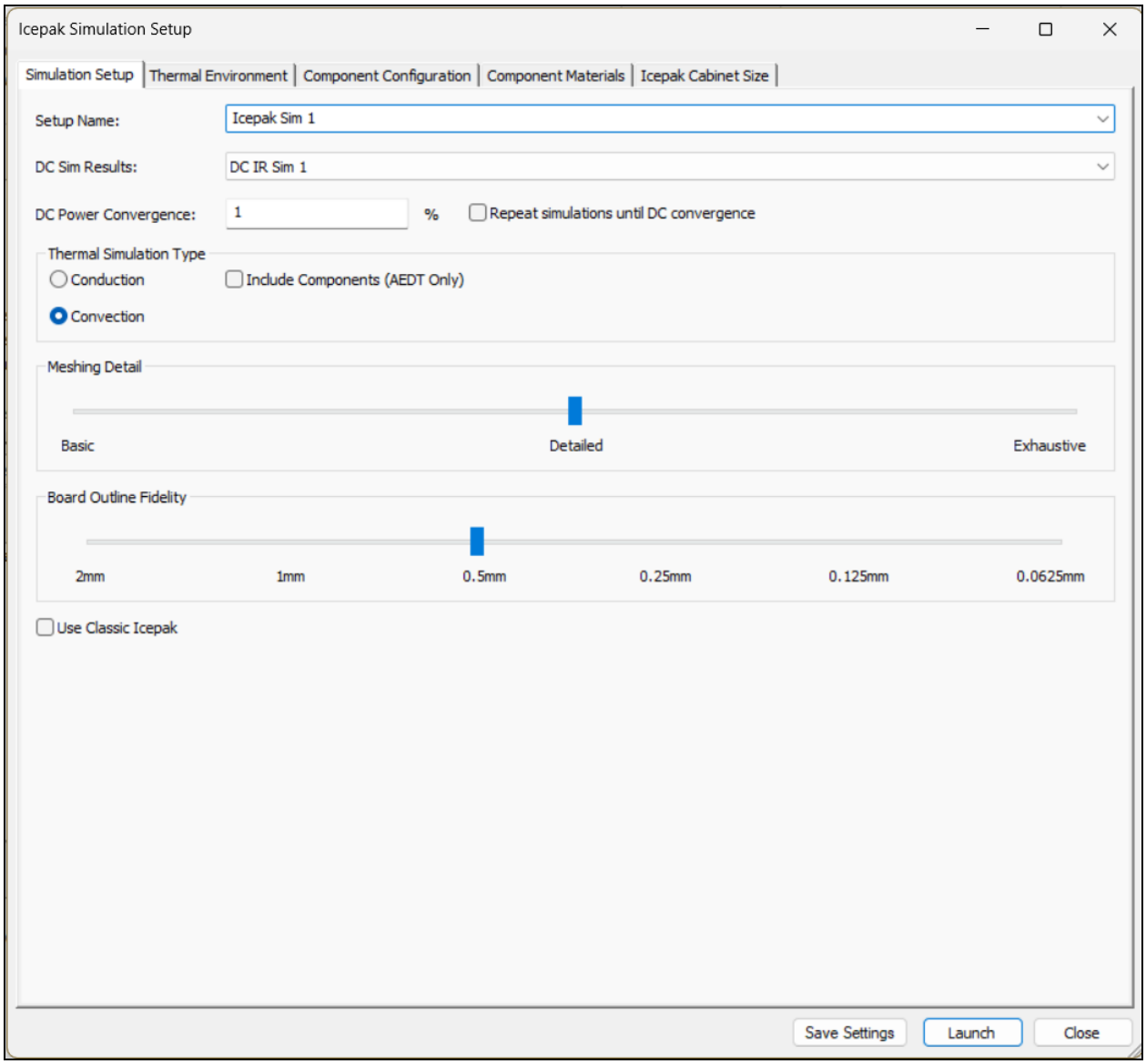

2. From the **Simulation Setup** tab, do the following:
   a. **Setup Name** field — enter a name for the simulation.
   b. **DC Sim Results** drop-down menu — select the previously run DC simulation.
   c. **DC Power Convergence** field — enter a percentage value.
   d. **Repeat simulations until DC convergence** check box:
      - To have SIwave alternate between running Icepak and DC simulations, check the **Repeat simulations until DC convergence**box. The output of each simulation is fed into the next in order to refine results. The loop ends when a DC simulation completes with a total power dissipation which differs from the previous DC simulation by less than the user-specified percentage. Results from all simulations in the loop are kept.

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Simulation names for each stage are based on the name of the previous run (i.e., if the previous name ended in a number, the number is incremented; otherwise, 2 is appended to the name).

- To run a single Icepak simulation, ensure the **Repeat simulations until DC convergence** box is not checked.

e. **Thermal Simulation Type** area — use the radio buttons to select **Conduction** (i.e., a simpler, faster form of thermal simulation that only considers the power dissipation from the DC results) or **Convection** (i.e., a more complicated form of thermal simulation which models airflow around the board).

f. **Include Components (AEDT Only)** check box — check the box to include components in conduction simulations, with the following caveats:

- heat sinks are prohibited
- only available in **Electronics Desktop**

g. **Meshing Detail** area — move the slider to **Basic**, **Detailed**, or **Exhaustive** to control the minimum size of various Icepak meshing parameters.

- **Basic** — the coarsest setting, intended for fast simulations or large projects where the higher mesh settings are too demanding.
- **Detailed** — the recommended setting, provides a good balance of speed and accuracy.
- **Exhaustive** — the most detailed setting and the most time consuming. **Exhaustive** should generally only be used when a **Detailed** run has not provided fine enough detail for an area of interest.

h. **Board Outline Fidelity** — move the slider to specify a minimum edge length when modifying the board outline for the exported project. This minimum edge length is used when discretizing arcs into a series of straight lines and when simplifying the outline to remove very small edges.

3. Click the **Thermal Environment** tab. The available options differ depending on whether **Conduction** or **Convection** is selected in step **2e**.

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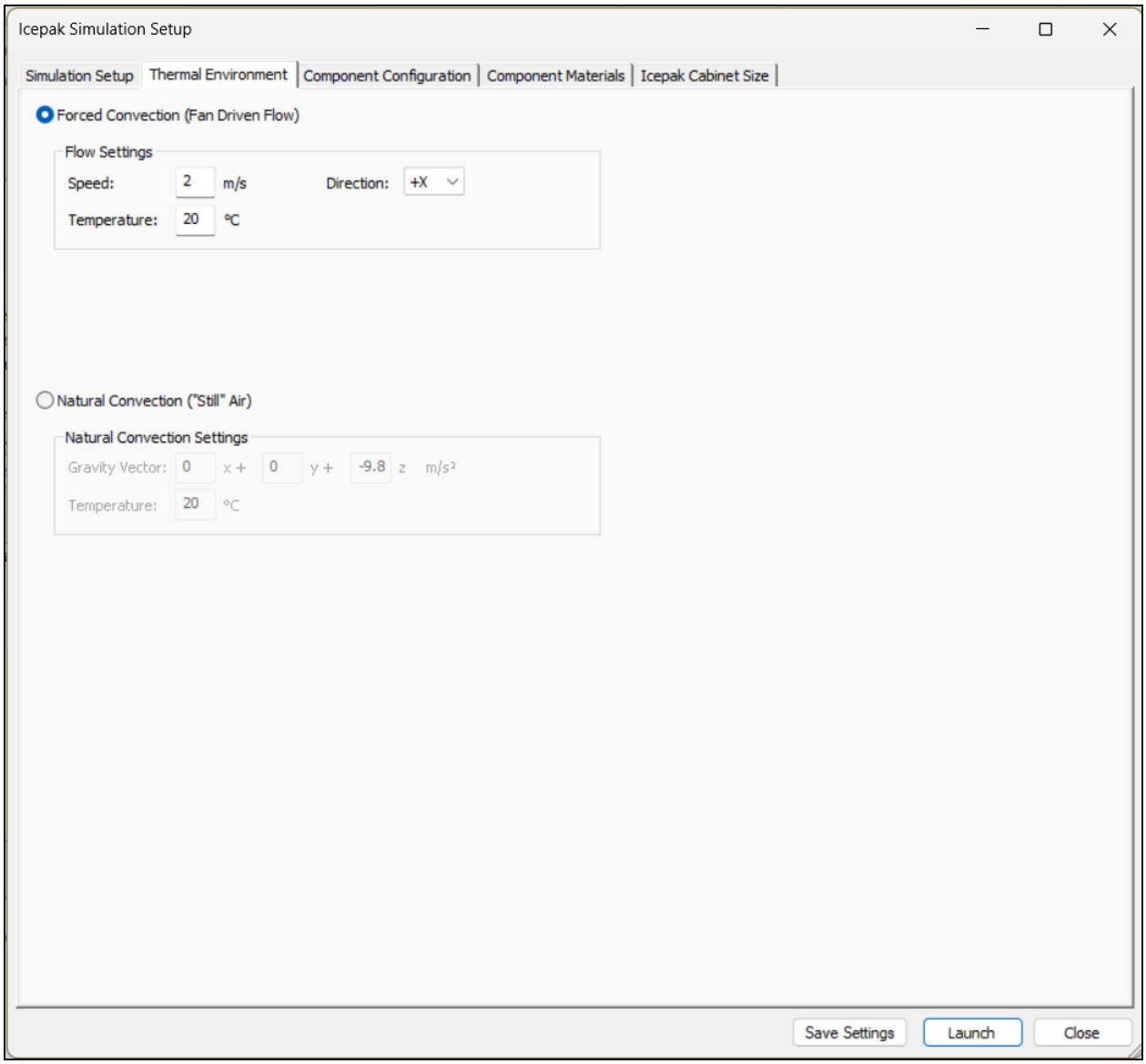

or

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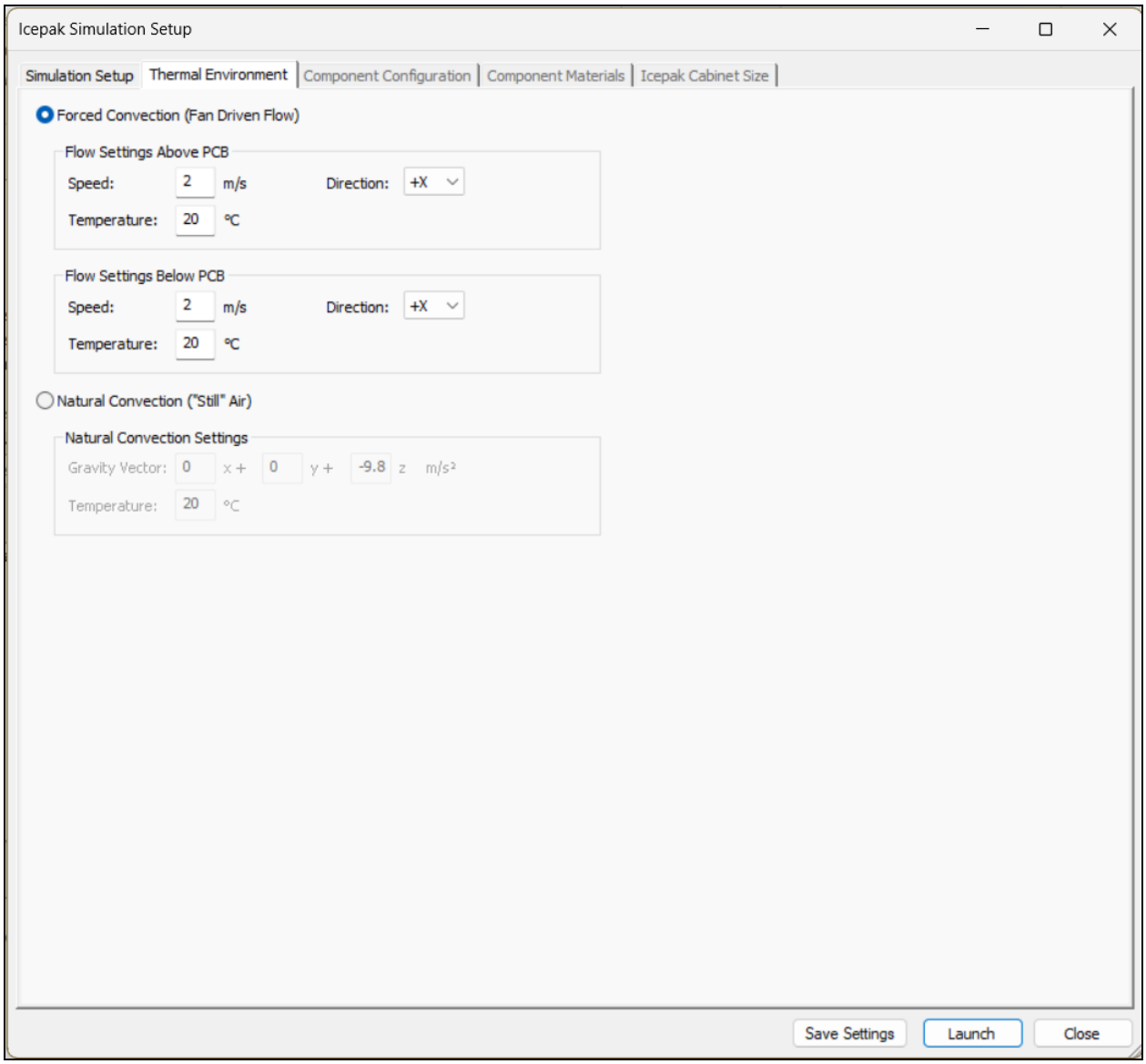

4. From the **Thermal Environment** tab, select from the following:
   - **Forced Convection (Fan Driven Flow)** — for thermal simulations where the board is intended to be used in an environment in which a fan will be blowing the air.
     - If applicable, specify the **Speed**, **Direction**, and **Temperature** in the **Flow Settings** area. If the primary simulation type is conduction, differing flow settings may be set **Above** and **Below** the PCB surfaces.
   - **Natural Convection ("Still" Air)** — to simulate environments in which no fans are present and the air flow will be determined by the heat distribution of the board and its orientation relative to gravity.

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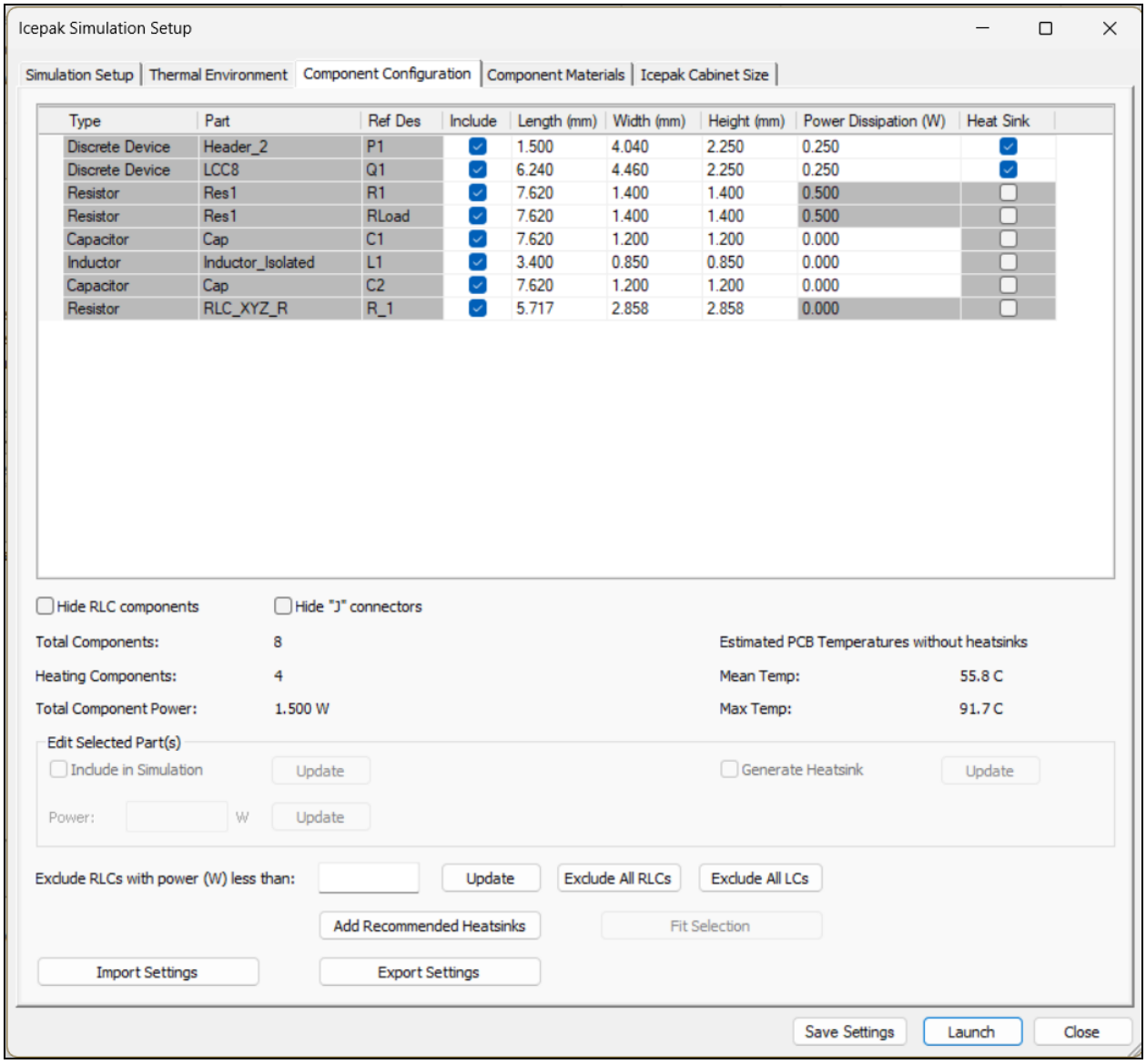
- If applicable, specify the **Gravity Vector** and **Temperature** in the **Natural Convection Settings** area. If the primary simulation type is conduction, only the cardinal direction with the largest magnitude is used from the **Gravity Vector**. A gravity vector in the Z direction is equivalent to an environment with the board flat on a horizontal surface (e.g., such as lying on a desk). A gravity vector in the X or Y direction is equivalent to an environment where the board is mounted standing on its edge.

5. If users are running a **Conduction** and **Include Components (AEDT Only)** or **Convection** simulation, click the **Component Configuration** tab. Otherwise, proceed to Launch.



6. From the **Component Configuration** tab, do the following:

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a. From the table, do the following:
   i. Click a column header to sort alphabetically by that column (i.e., **Type**, **Part**, **Ref Des**, **Include**, **Length (mm)**, **Width (mm)**, **Height (mm)**, **Power Dissipation (W)**, or **Heat Sink**).
   ii. Check any/all of the **Include** boxes to include components in the Icepak simulation.

> **Note:**
>
> Edit more than one part by selecting them and entering new values in the **Edit Selected Part(s)** area.

   iii. If appropriate, enter new values for **Length**, **Width**, **Height**, and **Power Dissipation**. Inductors and capacitors are set to **0** power by default. Power dissipation of resistors is automatically calculated from DC simulation results. All other components default to .25 Watts.
   iv. Check any/all of the **Heat Sink** boxes to designate components as heat sinks.

b. **Hide RLC Components**checkbox — check the box to temporarily suppress the display of resistors, inductors, and capacitors in the table.

c. **Hide "J" Connectors** checkbox — check the box to temporarily suppress the display of IOs and Discrete Devices with reference designators that start with **"J"**.

d. **Exclude RLCs with power (W) less than** field — if appropriate, enter a value in Watts. Click **Update** to exclude components with less power than the specified value. Alternatively, click **Exclude All RLCs** or **Exclude All LCs**.

e. **Add Recommended Heatsink** — click to assign heat sinks to components that are estimated to get significantly hot.

f. If appropriate, click **Import Settings** to load settings from a previously saved *.pwrd file.

g. If appropriate, click **Export Settings** to save the settings as an SIwave Power Dissipation File (*.pwrd).

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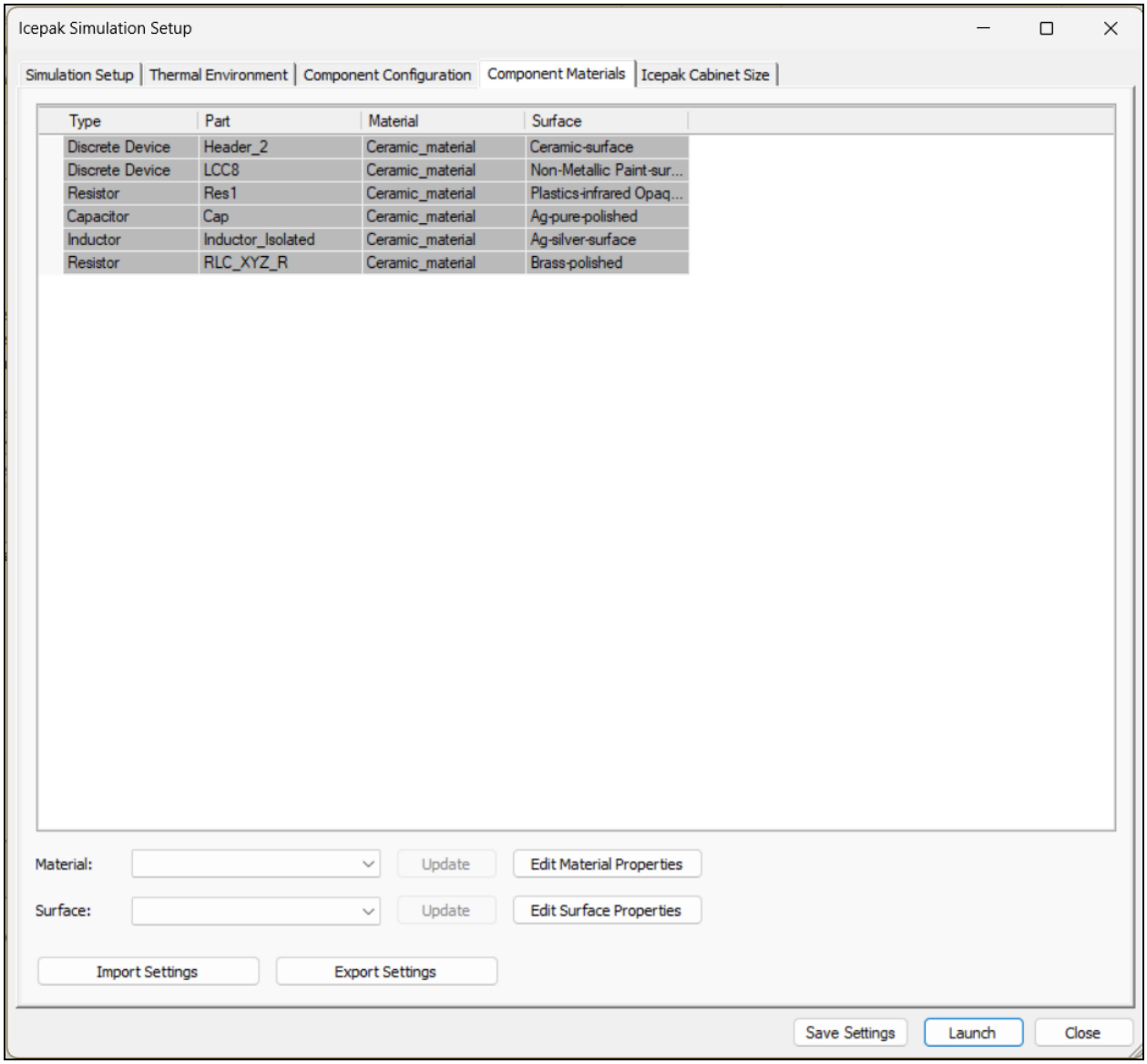
7. Click the **Component Materials** tab.



> **Note:**
>
> The **Component Materials** tab is restricted to only relevant materials (i.e., materials with defined thermal properties, project-level materials, and a subset of of system surface materials.

8. From the **Component Materials** tab, do the following:

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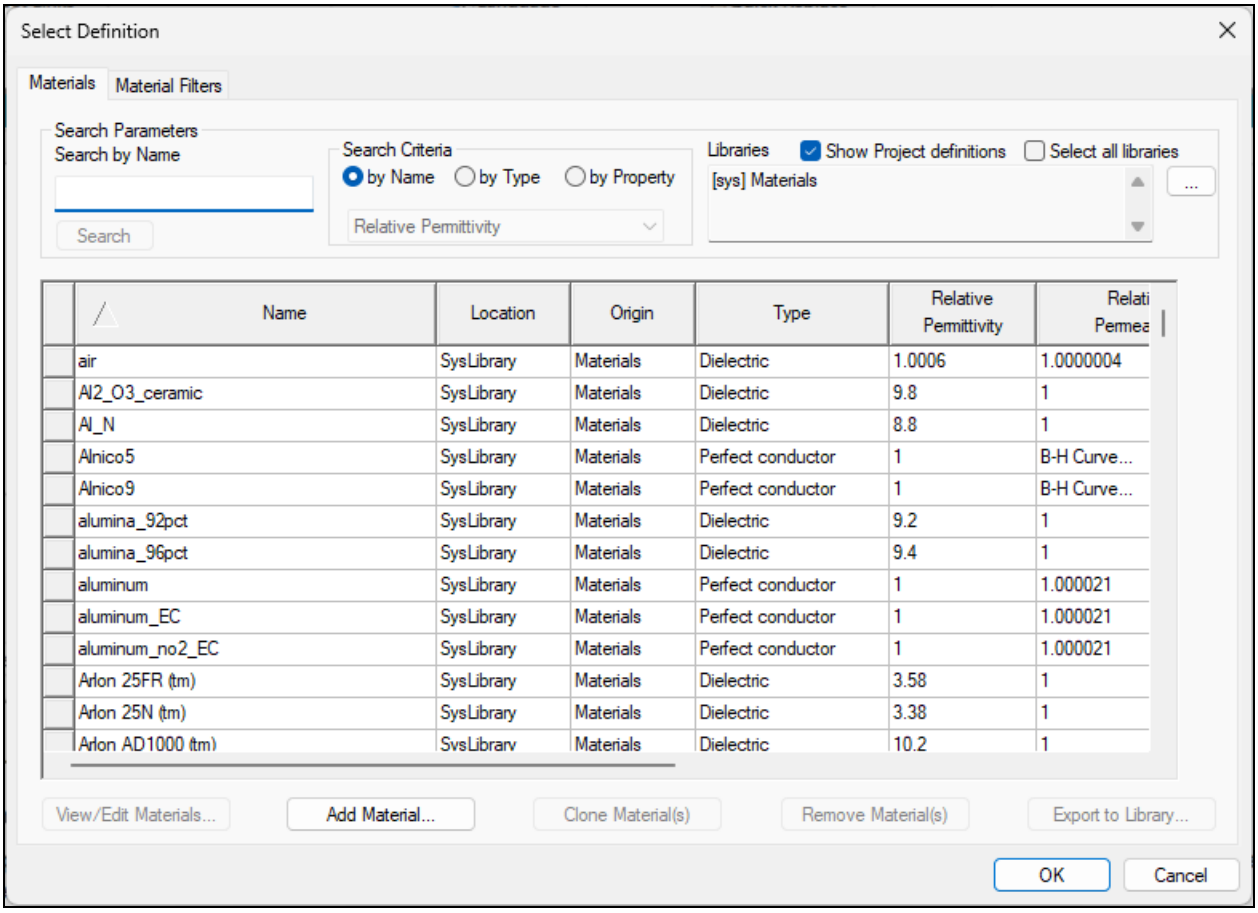
a. Click a column header to sort alphabetically by that column (i.e., **Type**, **Part**, **Material**, or **Surface**).

b. Click anywhere within a row to populate the **Material** and **Surface** drop-down menus with the selected row's contents. If appropriate, select a new **Material** and/or **Surface** from the drop-down menus and click the adjacent **Update** button(s) to push the new selection to the corresponding field in the table.

c. Click **Edit Material**/**Edit Surface Properties** to open a **Select Definition** window.



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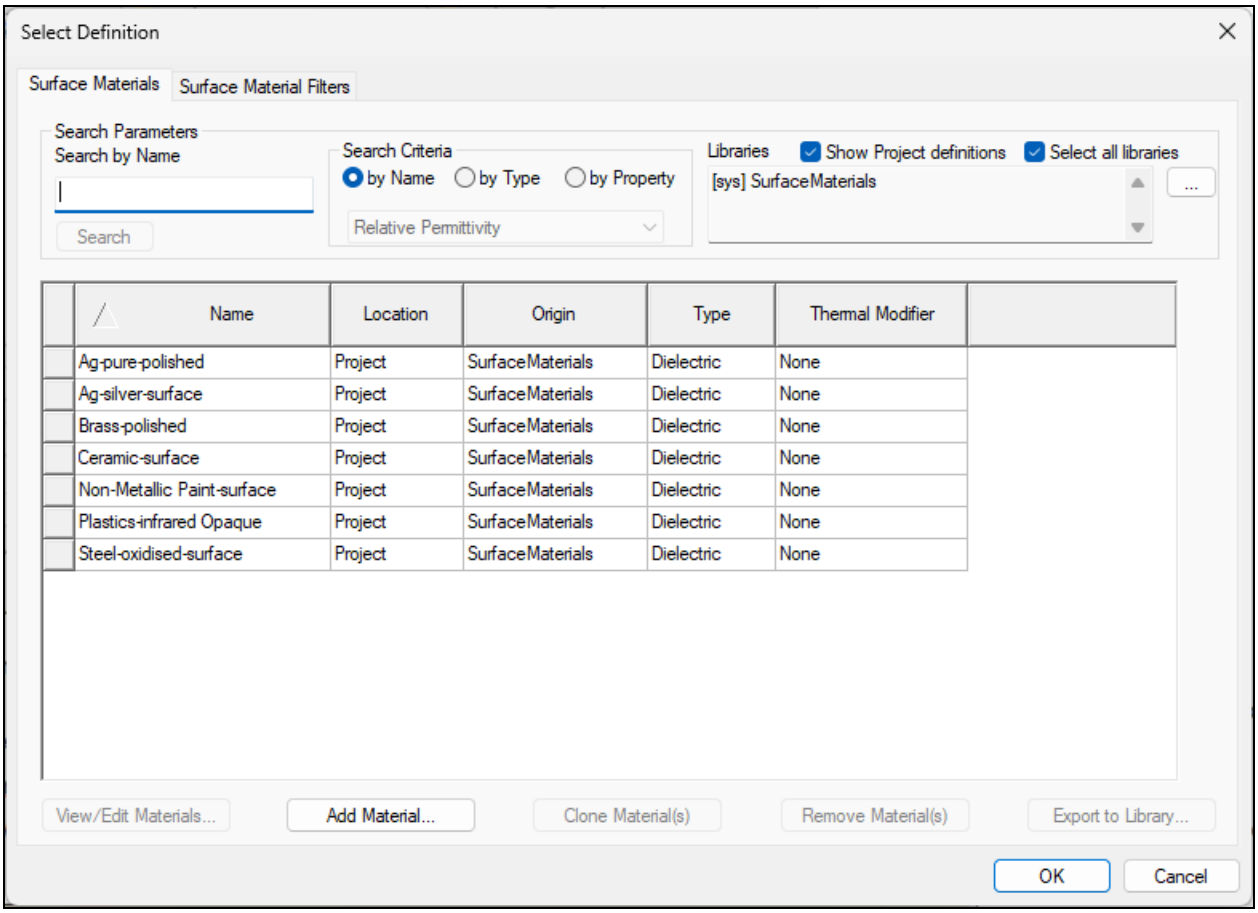

d. From the **Select Definition** window(s), search for existing materials, edit, clone, or remove materials within the available databases, or add new materials. Both windows function identically to those elsewhere in **SIwave** and **Electronics Desktop** (e.g., the **Select Definition** window accessible through the **Layer Stackup Editor** window > **Edit Material Properties**). Refer to Adding a New Material, Editing an Existing Material, and Material Properties.

> **Note:**
>
> By default, the **Selection Definition** windows also show a limited selection of materials. To access all material definitions, click the **Materials/Surface Material Filters** tab and select **All Materials and Properties** from the **Show Materials and Properties for** area.

e. If appropriate, click **Import Settings** or **Export Settings**.

9. Click the **Icepak Cabinet Size** tab. The available options differ depending on whether **Forced Convection** or **Natural Convection** is selected in step **4**.

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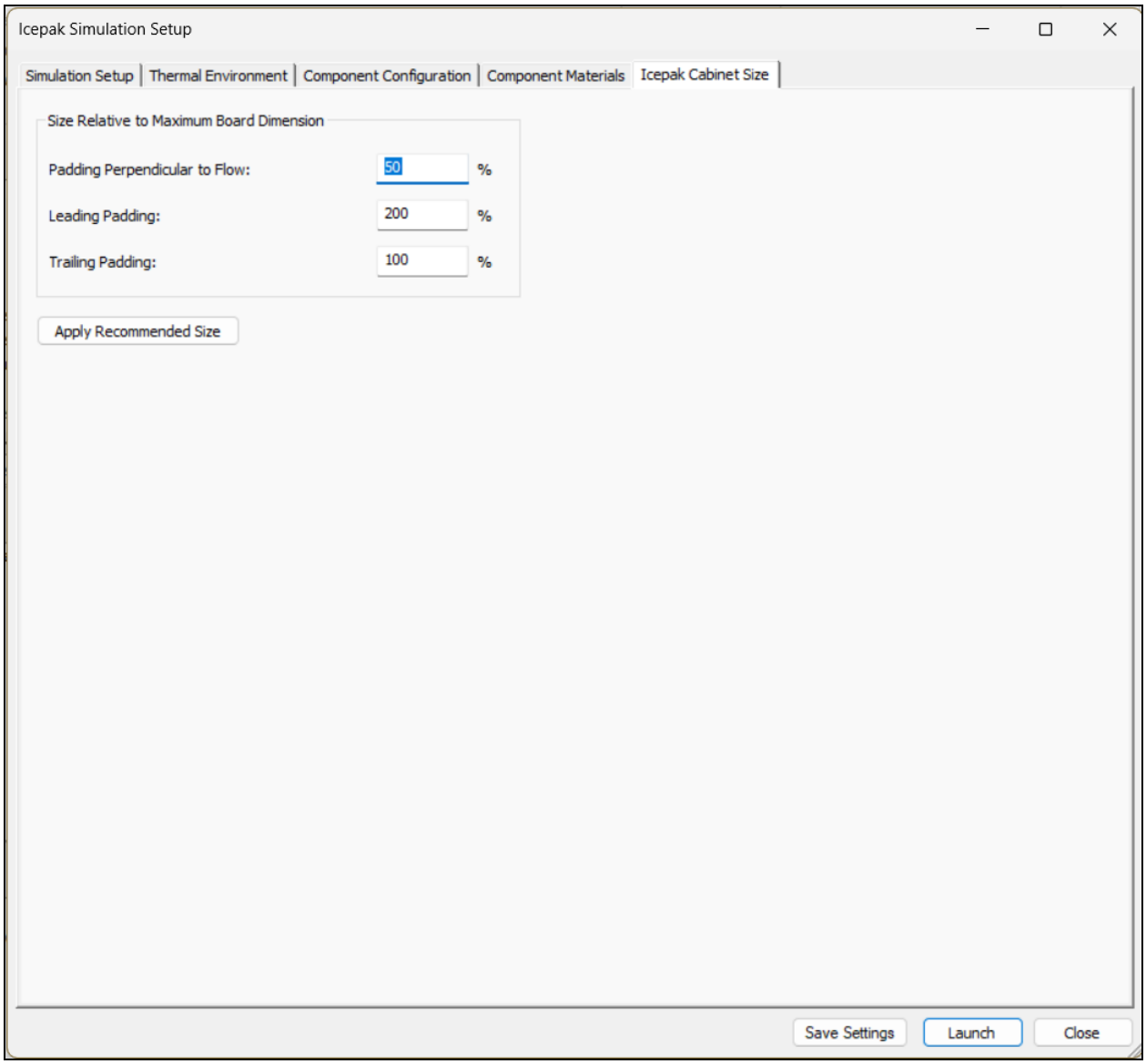

or

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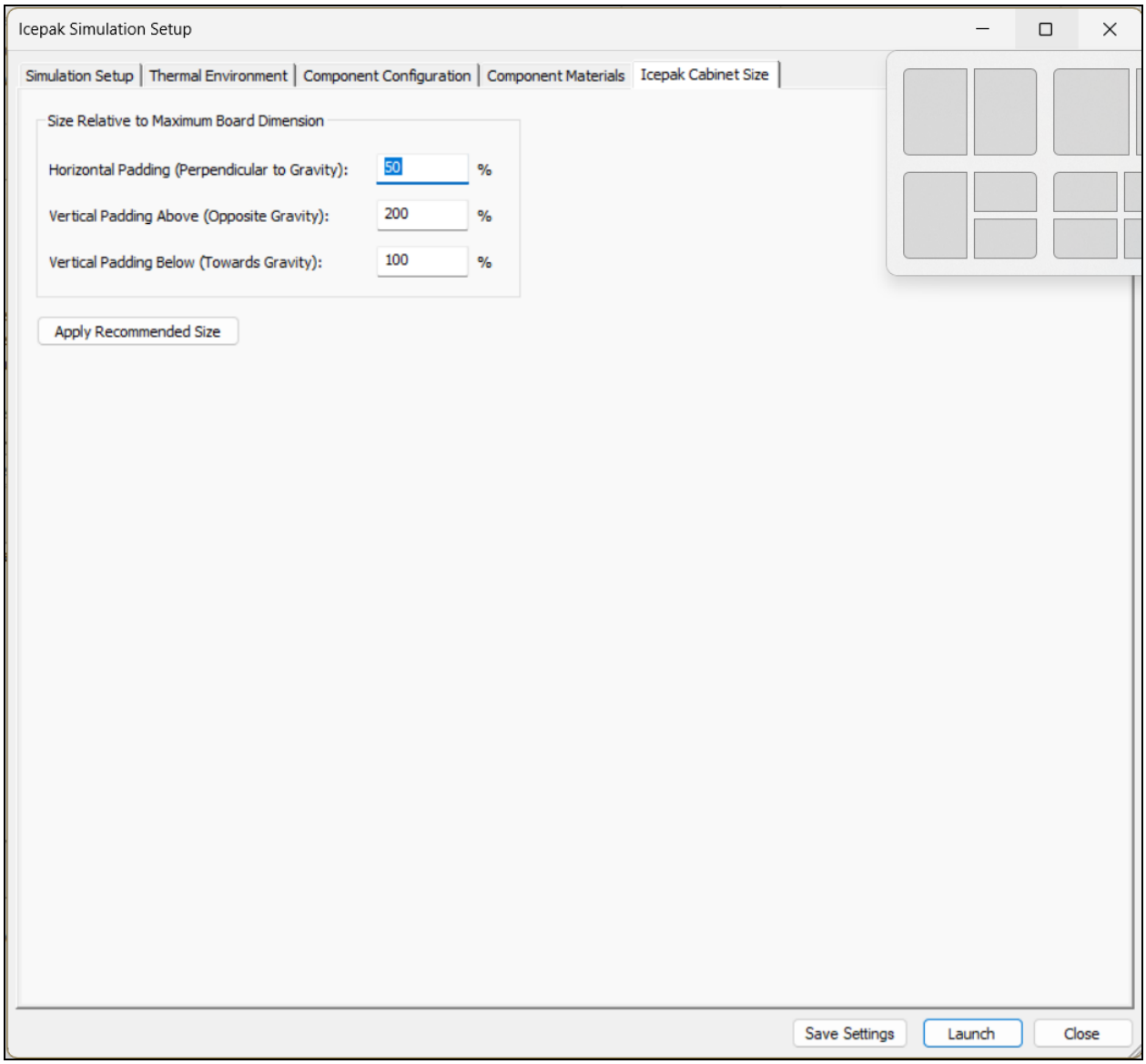

10. From the **Icepak Cabinet Size** tab > **Size Relative to Maximum Board Dimension** area, enter values in the following fields:
    - **Padding Perpendicular to Flow** — The perpendicular expansion factor is calculated relative to the largest dimension of the board, and will be applied along the axes other than the axis of the forced flow (e.g., if the value is 25%, the board spans 20mm in the X direction and 12mm in the Y direction, and the flow is in the -Z direction, then the cabinet will extend 5mm beyond the board in the -X, +X, -Y, and +Y directions).
    - **Leading Padding** — This expansion factor is applied along the axis of the flow vector on the upstream side (e.g., using the configuration from the previous example and a value of

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200%, the cabinet would extend 40mm beyond the board and components in the +Z direction).

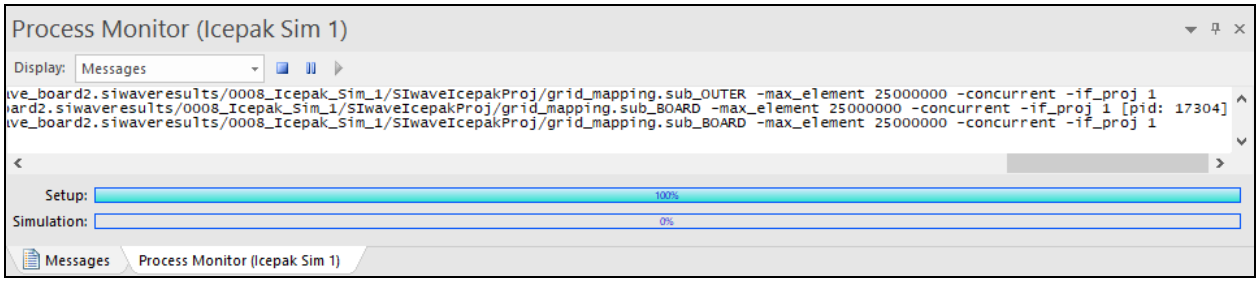
- **Trailing Padding** — This expansion is the same as the previous expansion, but on the downstream side (e.g., using the configuration from the previous examples and a value of 100%, the cabinet would extend 20mm in the -Z direction).

  or

- **Horizontal Padding (Perpendicular to Gravity)** — The horizontal expansion factor is calculated relative to the largest dimension of the board, and will be applied along the axes other than the primary axis of the gravity vector (e.g., if the values is 25%, the board spans 20mm in the X direction and 12mm in the Y direction, and the gravity vector is 0 x + 0 y + -9.8 z, then the cabinet will extend 5mm beyond the board in the -X, +X, -Y, and +Y directions).
- **Vertical Padding Above (Opposite Gravity)** — This vertical expansion factor is applied along the primary axis of the gravity vector in the directory opposite to gravity (e.g., using the configuration from the previous example and a value of 200%, the cabinet would extend 40mm beyond the board and components in the +Z direction).
- **Vertical Padding Below (toward Gravity)** — This vertical expansion is the same as the previous vertical expansion, but in the opposite direction (e.g., using the configuration from the previous examples and a value of 100%, the cabinet would extend 20mm in the -Z direction).

> **Note:**
>
> Alternately, click **Apply Recommended Size** to use the recommended cabinet size. This is largely intended for old projects with out-of-date settings.

11. Click **Launch** to begin the simulation. The **Messages** window updates with a Process Monitor tab that displays the progress.



Viewing Icepak Results

To view the full results of an Icepak simulation, open the project in Icepak. You can launch Icepak directly from SIwave:

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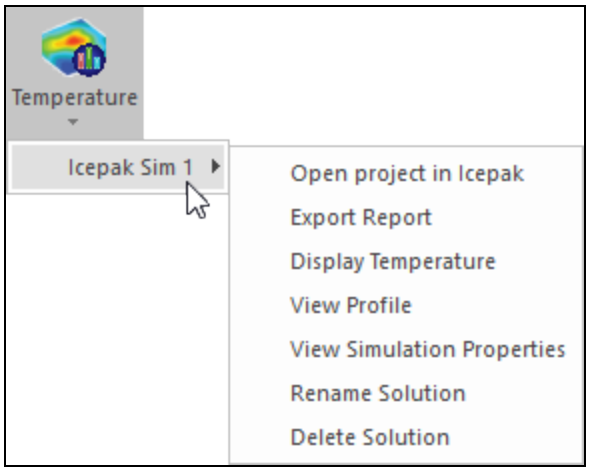
1. Click **Results**.
2. From the Icepak area, select **Temperature** > **[Simulation Name]**.



3. Click **Open Project in Icepak**.

   The simulation opens in Icepak.

To view temperature results in SIwave:

1. Click **Results**.
2. From the Icepak area, select **Temperature > [Simulation Name]**.
3. Click **Display Temperature**.

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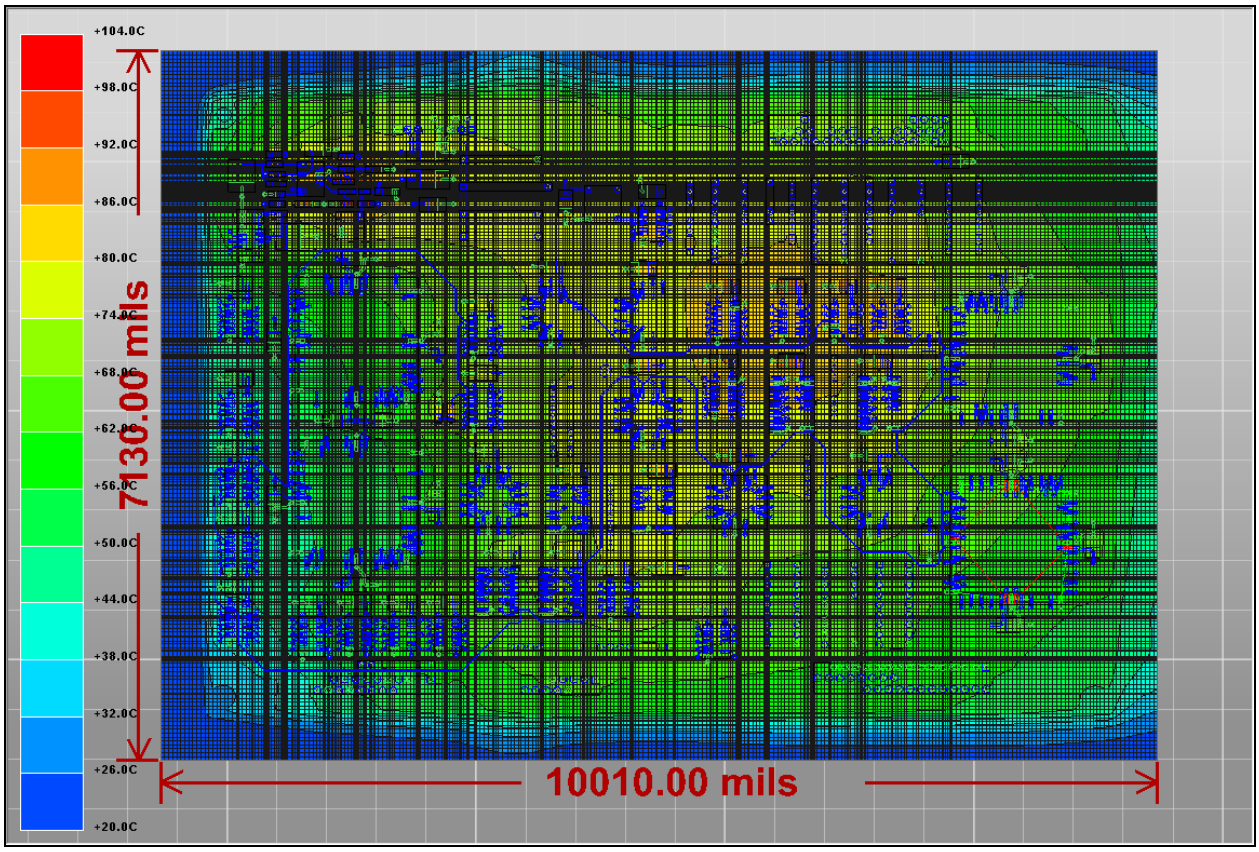
The temperature plot appears in the Modeling workspace.



To change plot settings:

1. Click **View**.
2. From the Show/Hide area, click the **Temperature Plots** icon ( ).

   The **Thermal Data Plots** window appears.

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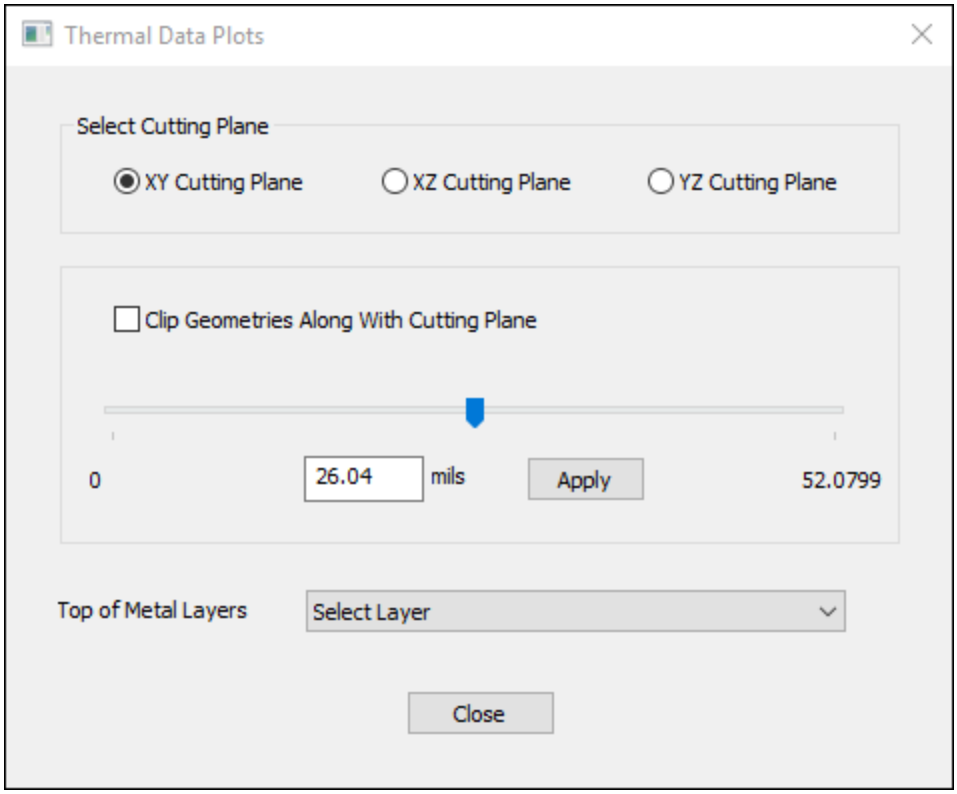

3. From the **Select Cutting Plane** area, use the radio buttons to select **XY**, **XZ**, or **YZ**.
4. Decide whether to **Clip geometries along with cutting plane**. You can use the slider to change the cutting plane size.
5. Use the **Top of Metal Layers** drop-down menu to view a plot of each metal layer's top surface.

From the Icepak results menu, you can also access additional menu options.

Icepak Simulation Results Menu Options

Navigate to the Icepak Results menu:

1. Click **Results**.
2. From the **Icepak** area, select **Temperature** > **[Simulation Name]**.

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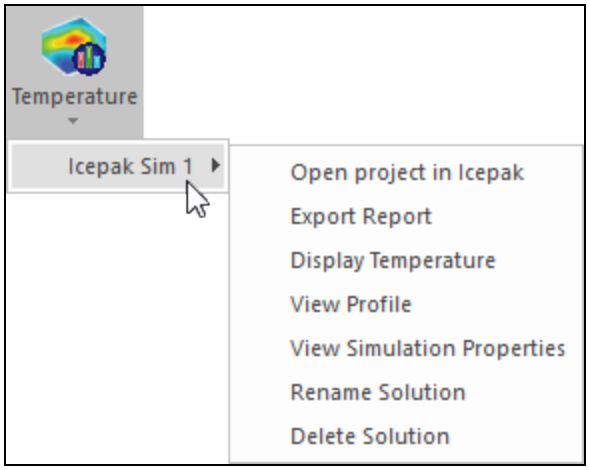

Menu options include:

- **Export Report** — opens an *.html file detailing thermal plots at various elevations.
- **View Profile** — opens the simulation profile.
- **View Simulation Properties** — opens the Simulation Properties window on the Icepak Simulation Setup tab.
- **Rename Solution** — allows you to rename the solution.
- **Delete Solution** — deletes the solution.

Export Report:

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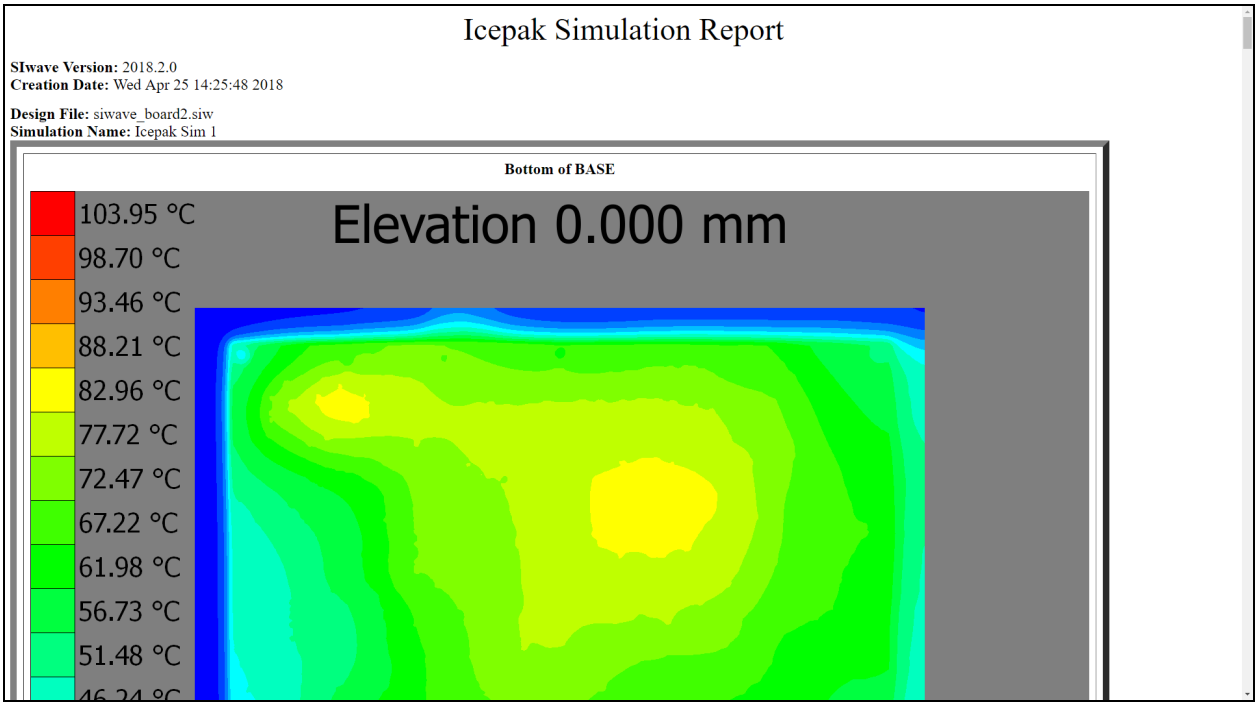

Simulation Profile:

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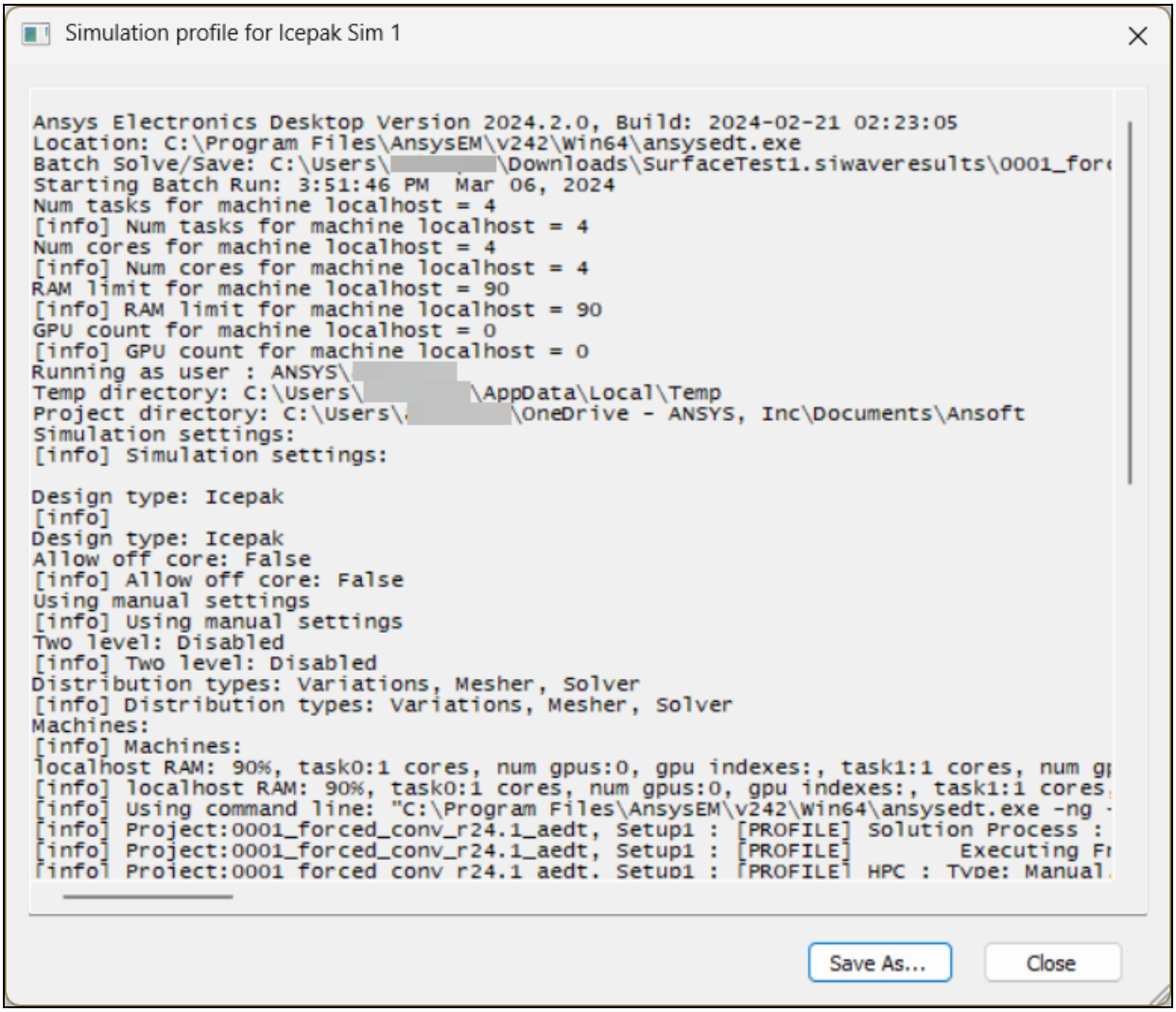

Simulation Properties:

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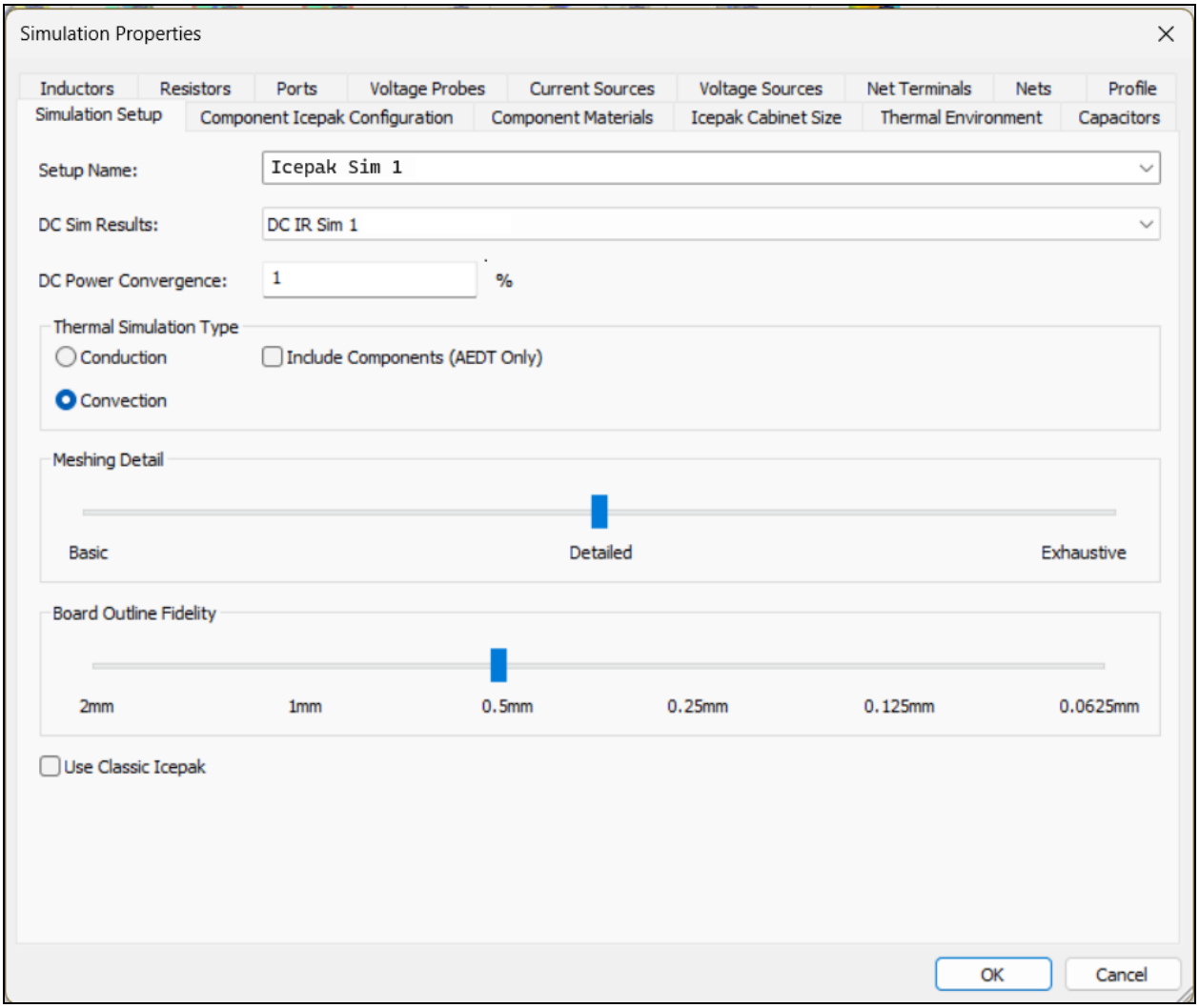

From the Icepak results menu, you can also view Icepak results.

Exporting an Icepak Simulation

Complete these steps to export a model as an Icepak project.

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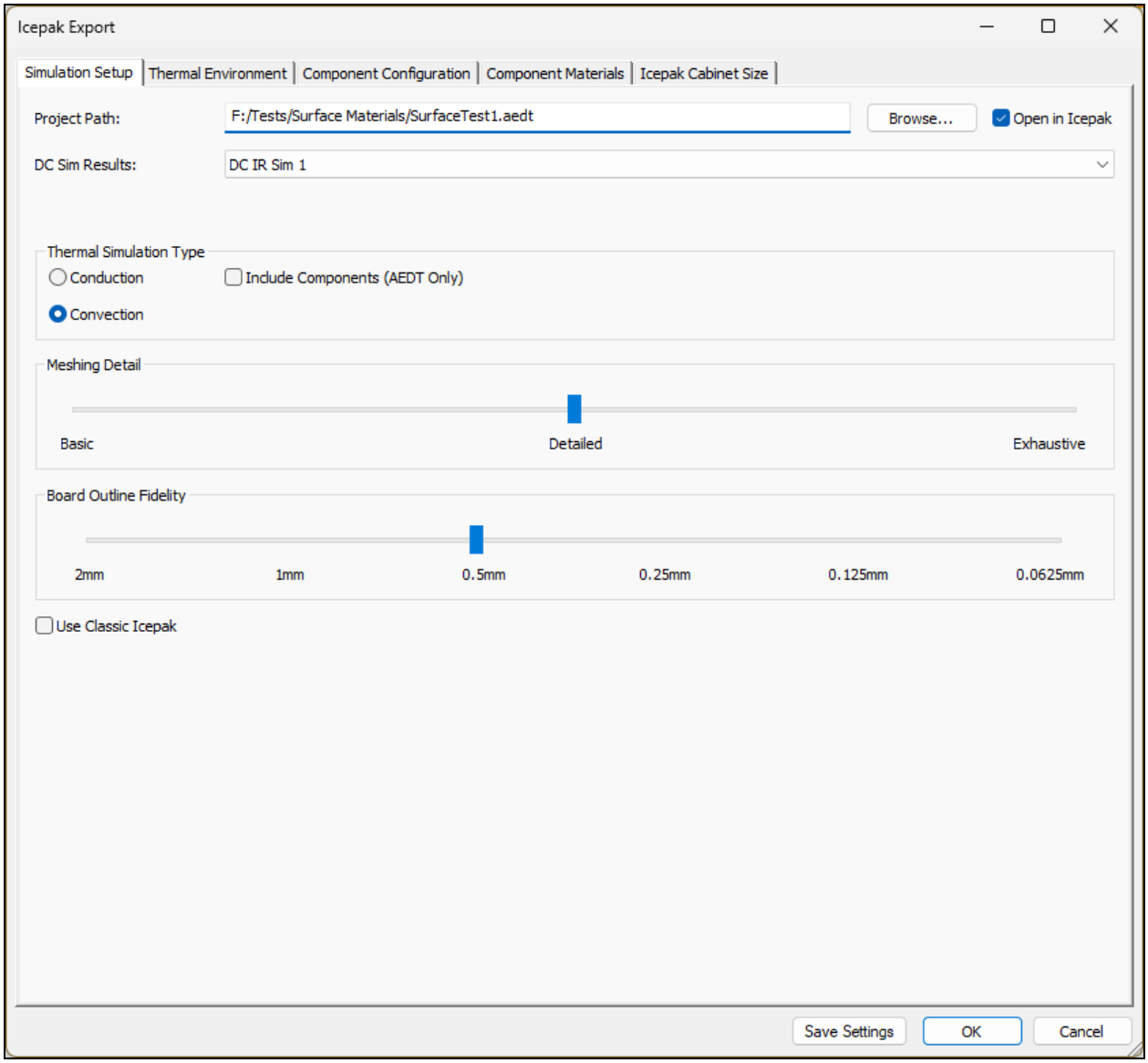
1. From **Export**, select **Icepak** to open the **Icepak Export** window.



2. Specify an appropriate **Project Path** and file name, or click **Browse** to open an explorer window. Then navigate to the appropriate file, double-click it, or select it and click **Save**.
3. To automatically open the project in **Electronics Desktop** after export is complete, check the **Open in Icepak** box.
4. Navigate through the five tabs and make all appropriate selections (i.e., **Simulation Setup**, **Thermal Environment**, **Component Configuration**, **Component Materials**, and **Icepak Cabinet Size**). The tabs are identical to those in the **Icepak Simulation Setup** window. Refer to Computing Icepak Simulations for detailed descriptions of the options available from each tab.

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Note:

Tabs are enabled depending on the selection(s) made in the **Thermal Simulation Type** area of the **Simulation Setup** tab :

- **Conduction** — **Simulation Setup** and **Thermal Environment**
- **Conduction** and **Include Components (AEDT Only)** — **Simulation Setup**, **Thermal Environment**, **Component Configuration**, and **Component Materials**
- **Convection** — **Simulation Setup**, **Thermal Environment**, **Component Configuration**, **Component Materials**, and **Icepak Cabinet Size**

5. Click **OK** to export the simulation to the specified directory. If the **Open in Icepak** box was checked, **Electronics Desktop** automatically opens and displays the file.

Computing SYZ Parameters Using SIwave

The SIwave SYZ solver provides fast and accurate full-wave 2.5D extraction of frequency-dependent parameters. The SIwave solver is the primary solver for signal integrity analyses of packages, PCBs, and PCB systems.

The SIwave field solver employs meshing algorithms to solve both planar objects and 3D objects (e.g., vias and solder balls).

The SIwave SYZ extractor is a high-speed hybrid solver for medium and large-scale analysis of PCBs and packages. SIwave SYZ calculates frequency-dependent scattering S-parameters for signal integrity and EMI investigations, as well as board-level power supply impedance modeling. The SYZ solver uses sources defined in SIwave or via push excitations from Electronics Desktop.

Note:

- Before starting SIwave SYZ extraction, you must define ports at the connection points for the sources and measurements, and identify the power and ground nets in your design. Refer to Simulation Setup.
- SIwave is designed to handle passive S-parameters and cannot compute asymmetrical S-parameters.

Complete these steps to compute S, Y and Z parameters in SIwave.

1. Click **Simulation**.
2. From the **SIwave** area, click **Compute SYZ Parameters** to open the **Compute SYZ-parameters** window.

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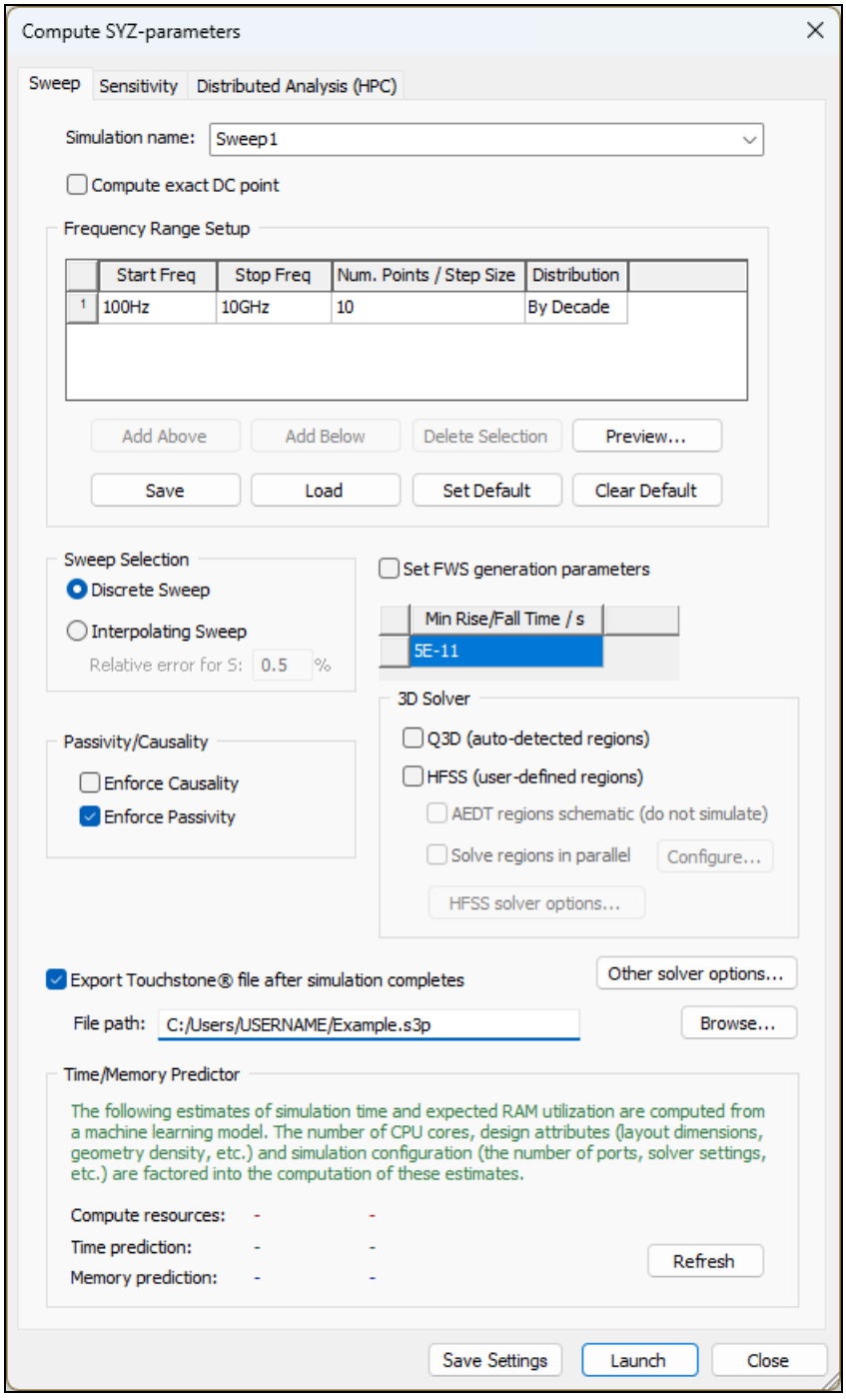

3. From the **Simulation Name** field, enter a name for the solution.
4. If appropriate, check the **Compute exact DC point** check box to combine DC results with the frequency-swept AC results. This provides improved accuracy over the entire simulation bandwidth.

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> **Important:**
>
> The **Compute exact DC point** and **Enforce causality** options are mutually exclusive. Selecting both generates an error.

5. For each frequency point in the **Frequency Range Setup** area, enter values for **Start Freq.** and **Num. Points**.
6. Use the **Distribution** drop-down menu to select a distribution method:
   - **Linear** – the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
   - **By Decade** – distributes the number of points specified logarithmically, over each decade.
7. Enter a value for *either* **Stop Freq.** *or* **Min. Rise/Fall Time**.
   - The **Min. Rise/Fall Time** value represents the time scale that characterizes the rate of change of the input time signal that will be applied in the circuit simulator.

   > **Note:**
   >
   > Entering data in one field automatically sets the other. The maximum frequency is considered to be the knee frequency, f_{knee}, which is related to the rise time T_R by the formula:
   >
   > $f_{knee} = 0.5 / T_R$

8. If appropriate, you can add or remove frequency points using the **Add Above**, **Add Below**, and **Delete Selection** buttons.
9. If appropriate, click **Save** to save frequency point settings as an SIwave Frequency Sweep Distribution File (*.sfsdf). To load previously saved settings from a *.sfsdf file, click **Load**.
10. If appropriate, click **Set Default** to make current settings the default for the simulation type. To return to the original default settings, click **Clear Default**.
11. If appropriate, click **Preview** to open the **Frequency List Preview** window.
12. From the **Sweep Selection** area, use the radio buttons to select either **Discrete** or **Interpolating**.
    - An interpolating sweep estimates a frequency response for an entire frequency range by solving at a relatively small number of frequency points within that range. Between the actual solution frequencies, the frequency response is obtained by rational interpolation. SIwave adaptively chooses the frequency points at which it computes the field solution. After a new frequency point is solved, a new interpolating fit is generated. This is compared to the interpolant from the previous step, and the maximum difference between the two is determined. If the difference exceeds the requested tolerance, then a new

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frequency point is chosen for a solution. The interpolating sweep is complete when the difference between successive interpolants is less than the error tolerance criterion.

- If you choose **Interpolating**, you must also specify the error tolerance.

13. From the **Passivity/Causality** area, use the check boxes to **Enforce Causality** and/or **Enforce Passivity**.

> **Important:**
>
> The **Compute exact DC point** and **Enforce causality** options are mutually exclusive. Selecting both generates an error.

14. If appropriate, check **Set FWS generation parameters** to export the full-wave SPICE subcircuit.

    The Start Frequency value changes to 0Hz. If you have an existing S-parameter solution, you can run an FWS simulation without needing a 0Hz or 1Hz point.

15. If appropriate, check **Q3D (auto-detected regions)** to utilize the Q3D solvers for 3D-type regions such as unreferenced traces, complex via transitions and pad coupling.
16. If appropriate, check **HFSS (user-defined regions)** to use the predefined HFSS regions and launch the HFSS simulation options. Click the **HFSS solver options** button to open the **General** tab in the **Simulation Setup** window, and set the solver options.

    The following guidelines must be followed:

    - You must manually define regions. Regions must contain signal net geometry that is included in the simulation. A region containing only power/ground net geometry or signal net geometry that is not included in the simulation is invalid.
    - Ports must exist either completely inside or completely outside of a region. Simulation configurations consisting of ports that straddle regions are invalid.
    - HFSS regions (which are user defined) and Q3D regions (determined by the solver) can coexist.
    - Power/Ground nets should be properly classified.
    - Signal net geometry in the region, along with power/ground net geometry, is solved using HFSS and the resulting S-parameters are incorporated into the SIwave solve to compute a unified channel response.

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> **Note:**
>
> For both S-Parameter sweep and HFSS Regions simulations, the machines used are those specified in the **Compute SYZ-parameters** > **Distributed Analysis** tab. When multiple regions are present, the regions are solved sequentially, but the adaptive passes and frequency sweep within a given region are distributed.

The **AEDT Regions Schematic** check box allows you to export HFSS regions as a schematic without running a simulation.

The **Solve Regions in Parallel** check box allows you to configure HFSS region simulations in parallel.

17. If appropriate, check **Export Touchstone file after simulation completes** to automatically generate a Touchstone file (*.sNp, *.ts).
18. If appropriate, click **Other solver options** to open the **SIwave Options** window and further customize the simulation.

> **Note:**
>
> If the **Time/Memory Predictor** area does not appear on the Sweep tab, skip to step 20.

19. As explained in the following screenshot, the time/memory predictor estimates the length of time it will take to complete the simulation and the expected RAM use during the simulation, based on an internal Machine Learning (ML) algorithm. The predictor can estimate time and memory utilization of all SYZ simulations, excluding those that include HFSS and/or Q3D regions, or DC point simulations.

> **Note:**
>
> The **Time/Memory Predictor** is a feature available to Ansys AI+ license subscribers, and does not appear otherwise.

From the **Time/Memory Predictor** area, click **Refresh** to populate the table with three rows of pertinent data.

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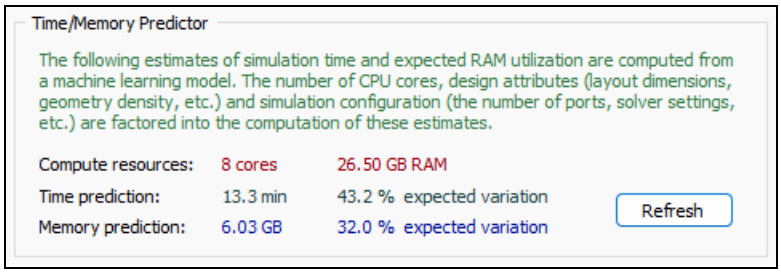
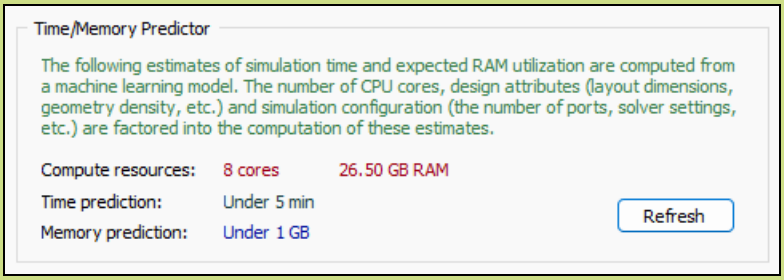


- **Computer resources** – number of cores and memory allocated to the simulation (i.e., user-defined parameters selectable from the **SIwave Options** window > **Multiprocessing** tab).
- **Time prediction** – time (in minutes) for the simulation to complete.
- **Memory prediction** – allocated memory (in gigabytes) required for the simulation to complete.

The second column in the **Time**/**Memory prediction** rows show the average expected variation in the accuracy of the predictions, based on the ML-algorithm.

Note:

If the predictor determines that the time and/or memory allocation falls under the minimum threshold(s), then precise values and expected variation are not shown. Instead, the predictor will show **Under 5 min** and/or **Under 1 GB**, respectively.



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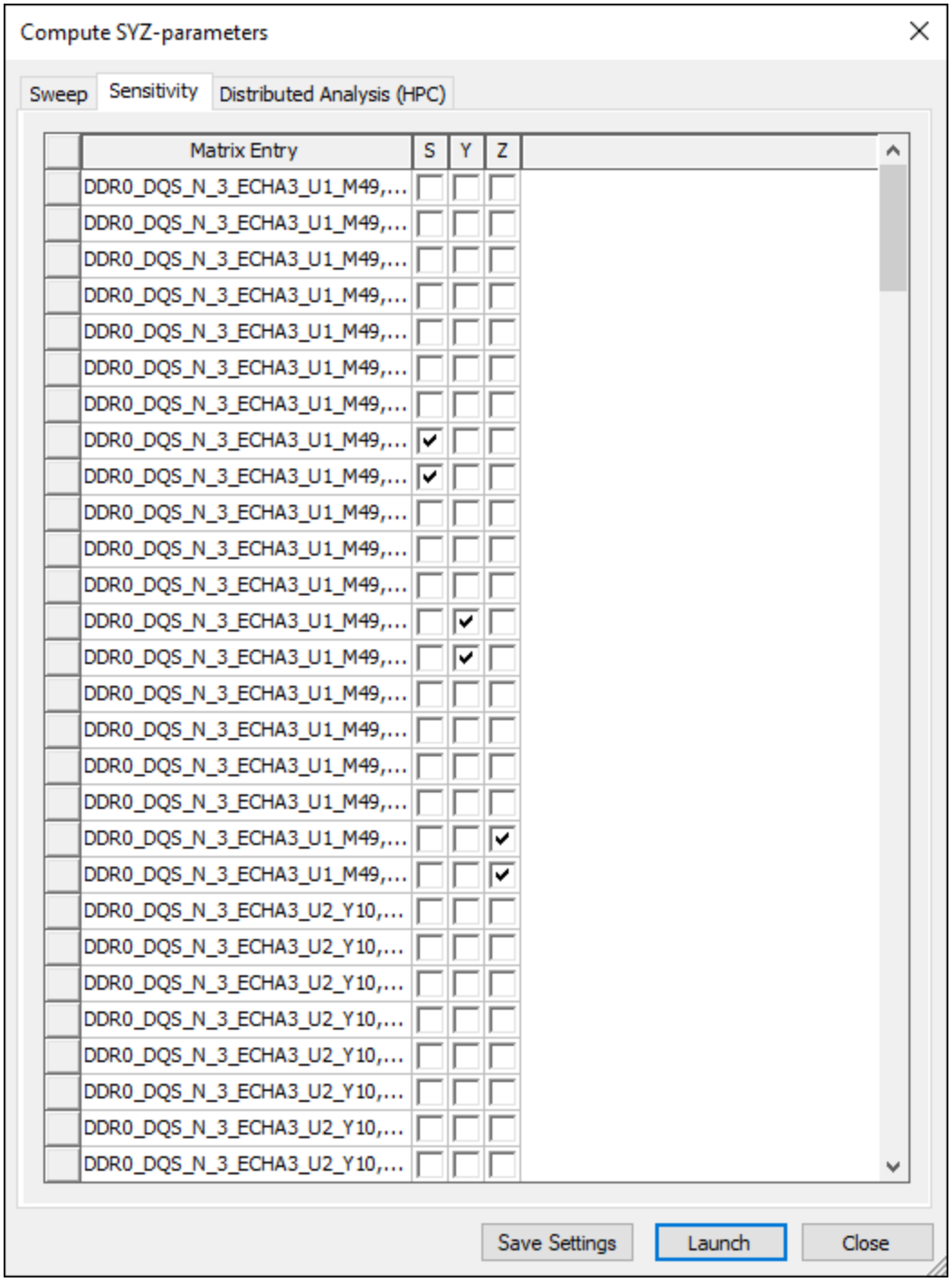
20. Select the **Sensitivity** tab.



21. Select S, Y and Z parameters for the matrices. This computes the partial derivative of an entry of the S, Y or Z-parameter matrix with respect to the impedance of a circuit element.
22. Select the **Distributed Analysis (HPC)** tab to specify a distributed analysis over multiple machines.

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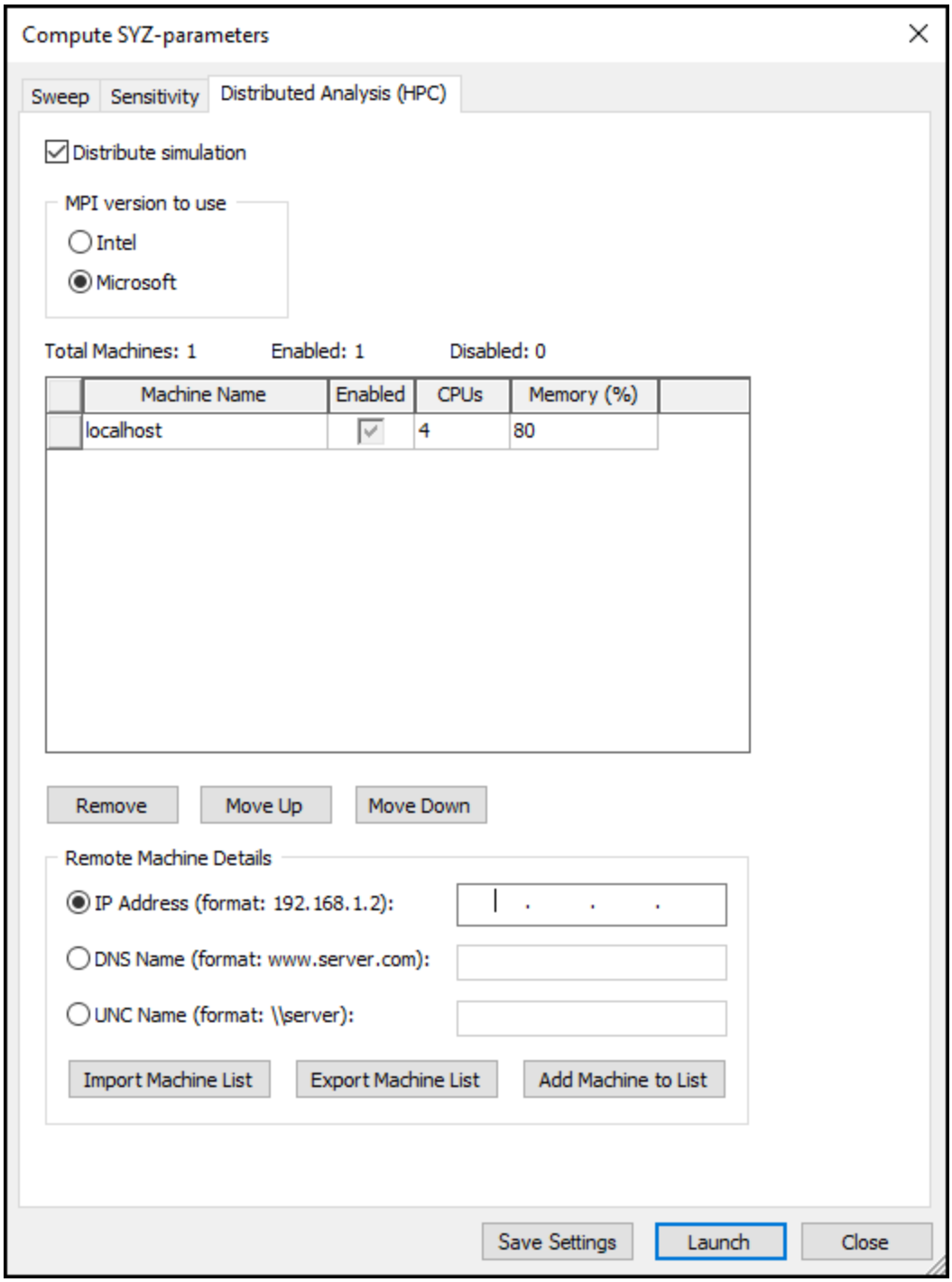

23. To enable distributed analysis, check the **Distribute simulation** check box.
24. From the **MPI version to use** area, use the radio buttons to select either **Intel** or **Microsoft**.
25. The list displays remote machines to be used in the simulation. You can **Remove** machines or rearrange them by clicking **Move Up** and **Move Down**.

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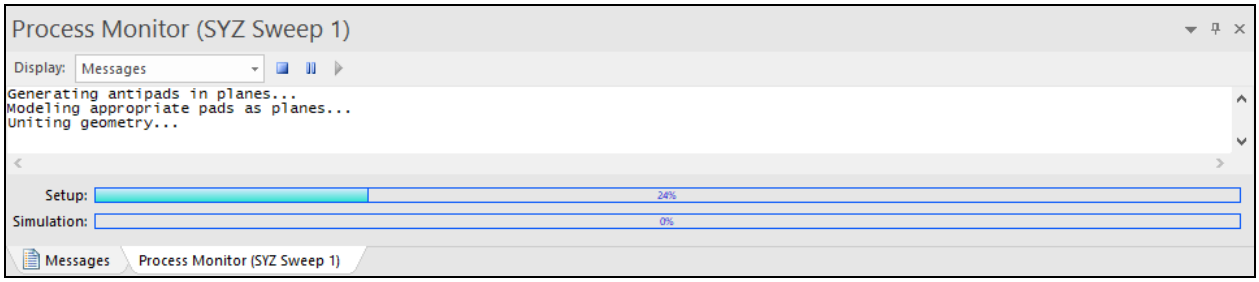
26. To add a machine, enter its information in the **Remote Machine Details** area and click **Add Machine to List**.
27. To export the list as a *.txt file, click **Export Machine List**. Click **Import Machine List** to load a previously saved list.
28. If appropriate, click **Save Settings** to keep your settings for subsequent simulations.
29. Click **Launch** to run the simulation. The **Messages** window updates with a Process Monitor tab that displays the progress.



Viewing SYZ Simulation Results

To view SYZ Sweep results:

1. Click **Results**.
2. From the SIwave area, select **SYZ** > **[Simulation Name]**.

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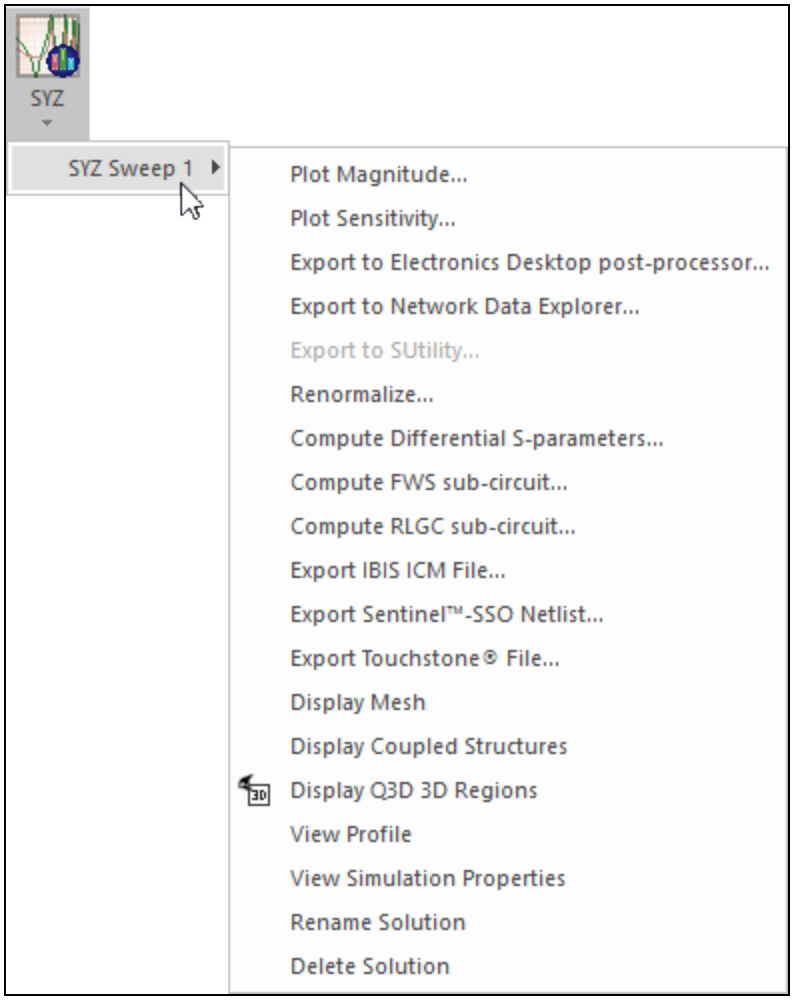

3. Select the type of results you would like to view.

   Result menu options include:

   - **Plot Magnitude** – allows you to view a plot of S-, Y-, and Z- parameters. See: Plotting Magnitude.
   - **Plot Sensitivity** – allows you to view a plot of circuit element sensitivity.
   - **Compute Differential S-Parameters** – allows you to view a differential plot of s-parameters. See: Computing Differential S-parameters.
   - **Compute FWS Sub-Circuit** – allows you to compute and export a Full Wave SPICE (FWS) plot. See: Computing FWS sub-circuit .
   - **Compute RLGC - Sub-Circuit** – allows you to derive RLGC information from the S-parameters. After you compute the RLGC matrices, you can export the RLGC subcircuit. See Computing RLGC Sub-Circuits.

Plot Magnitude:

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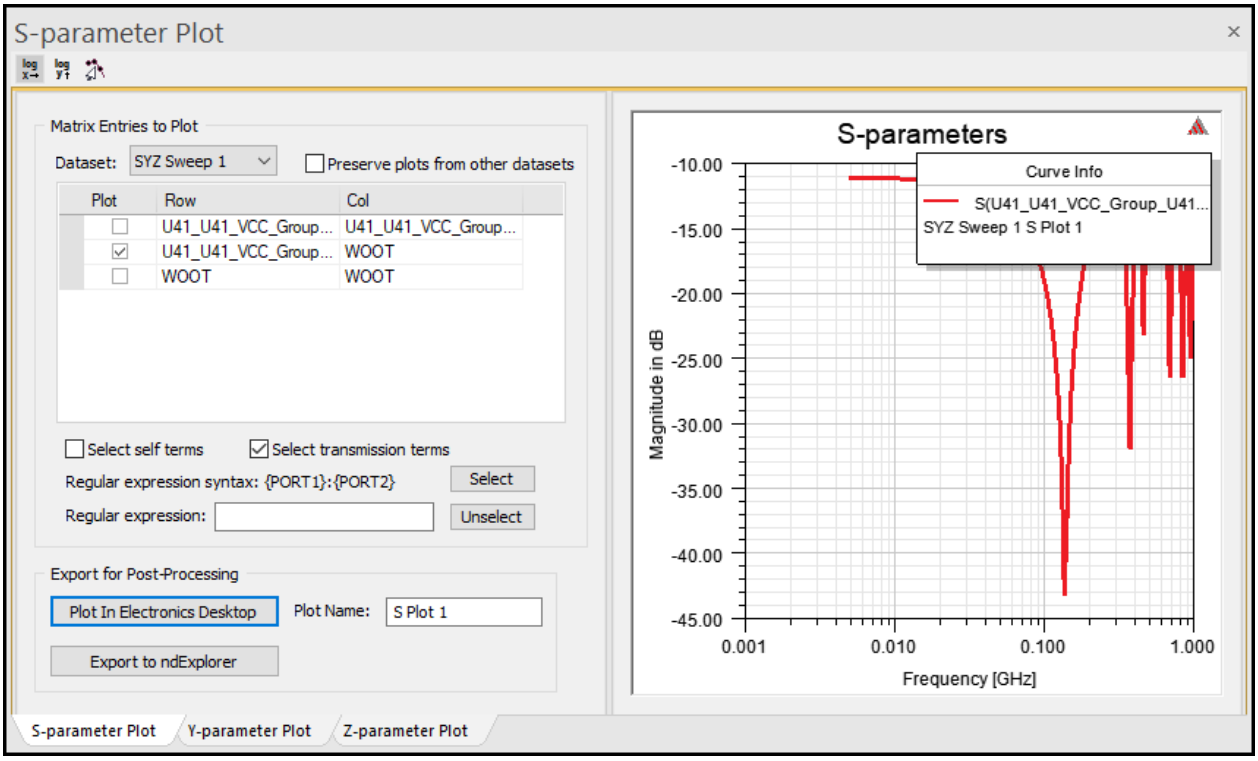

Plot Sensitivity:

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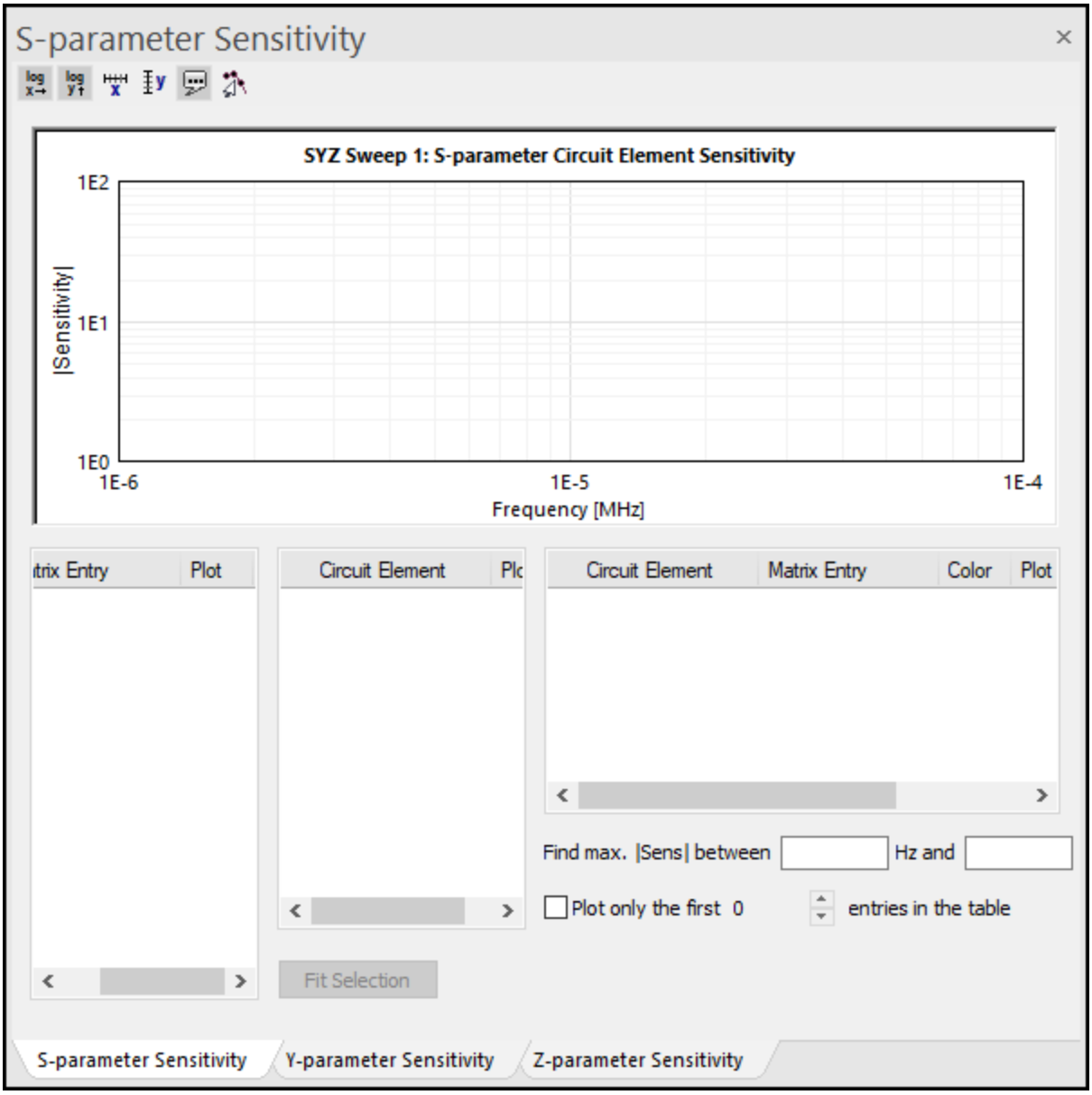

From the SYZ Results menu, you can also access additional menu options and export SYZ simulation information.

SYZ Simulation Results Menu Options

Navigate to the SYZ Results menu:

1. Click **Results**.
2. From the SIwave area, select **SYZ** > **[Simulation Name]**.

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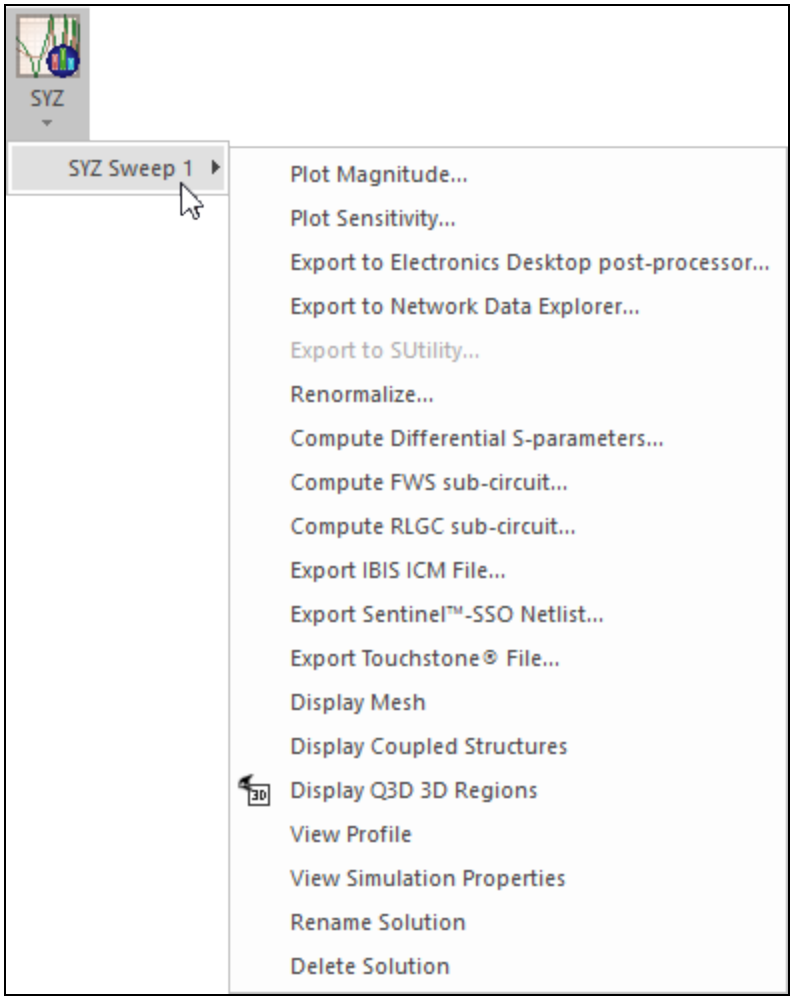

Menu options include:

- **Renormalize** – opens the S- Parameter Renormalization window, where you can modify the reference impedance for one or more ports.
- **Display/Hide Mesh** – displays or hides a mesh in the Modeling workspace. SIwave uses the finite element method to divide the model into thousands of small triangular regions.
- **Display/Hide Coupled Structures** – displays or hides coupled structures in the Modeling workspace.
- **Display/Hide Q3D 3D Regions** – displays or hides 3D regions.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the Sweep tab.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

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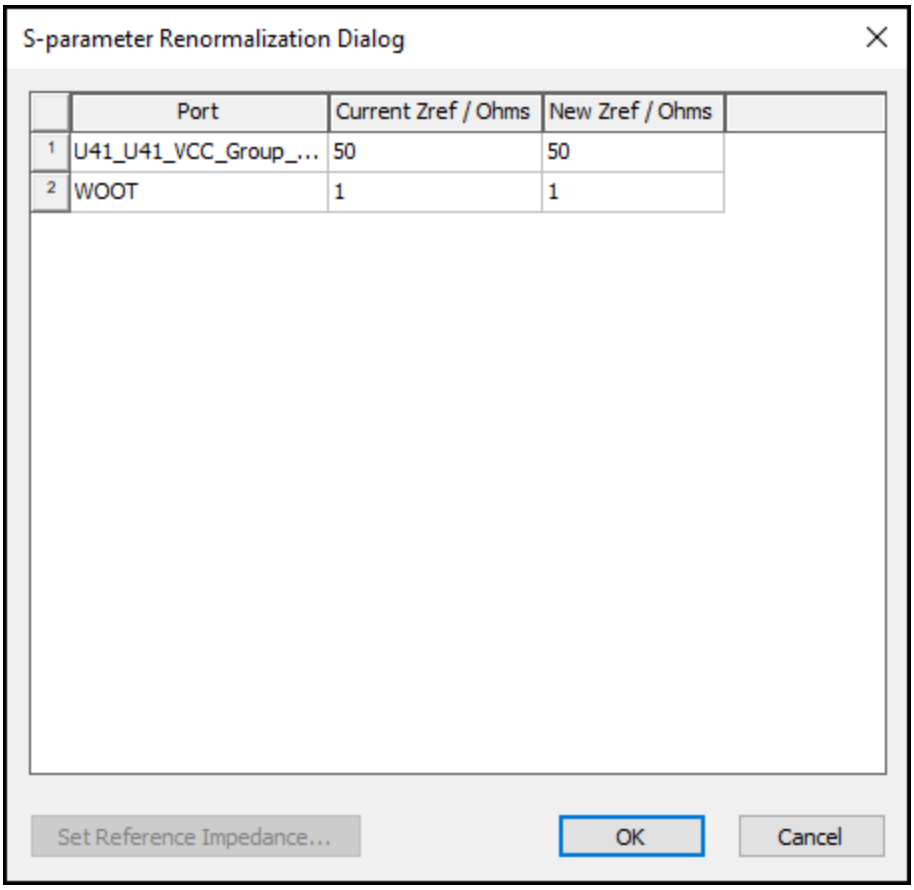
Renormalize:



Simulation Profile:

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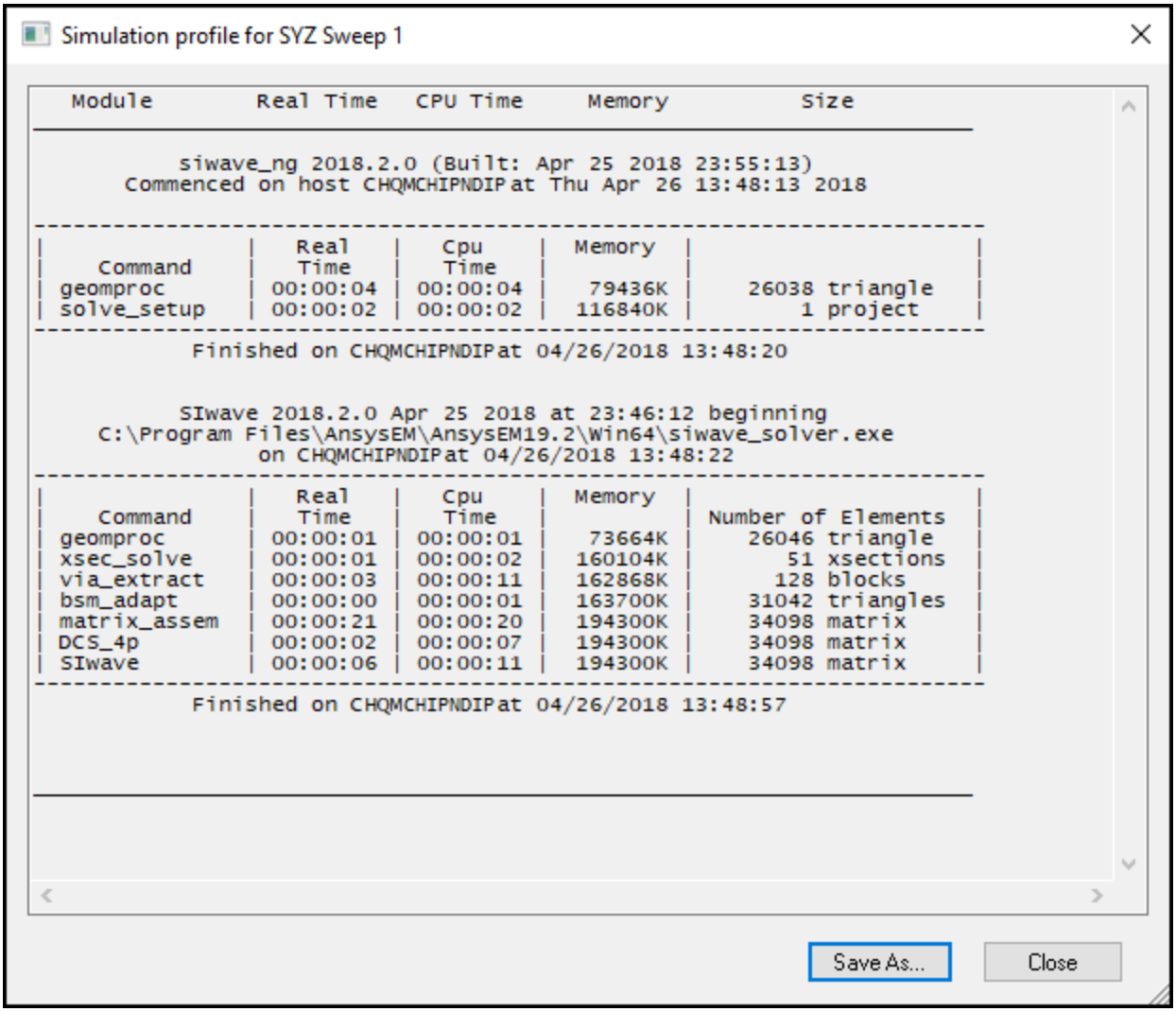

Simulation Properties:

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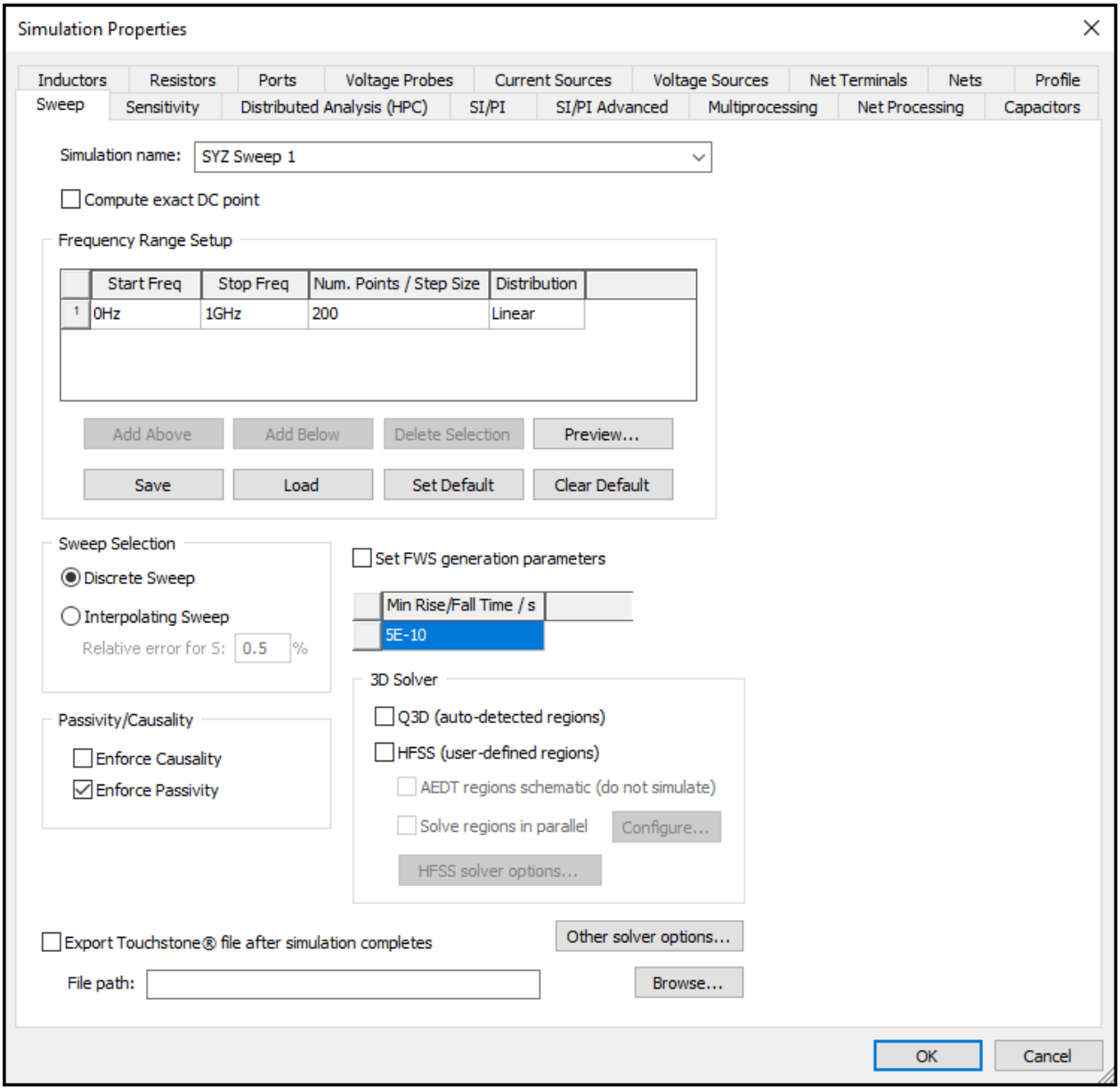

From the SYZ results menu, you can also view SYZ results and export certain information.

Exporting SYZ Information

Navigate to the SYZ Results menu:

1. Click **Results**.
2. From the SIwave area, select **SYZ** > **[Simulation Name]**.

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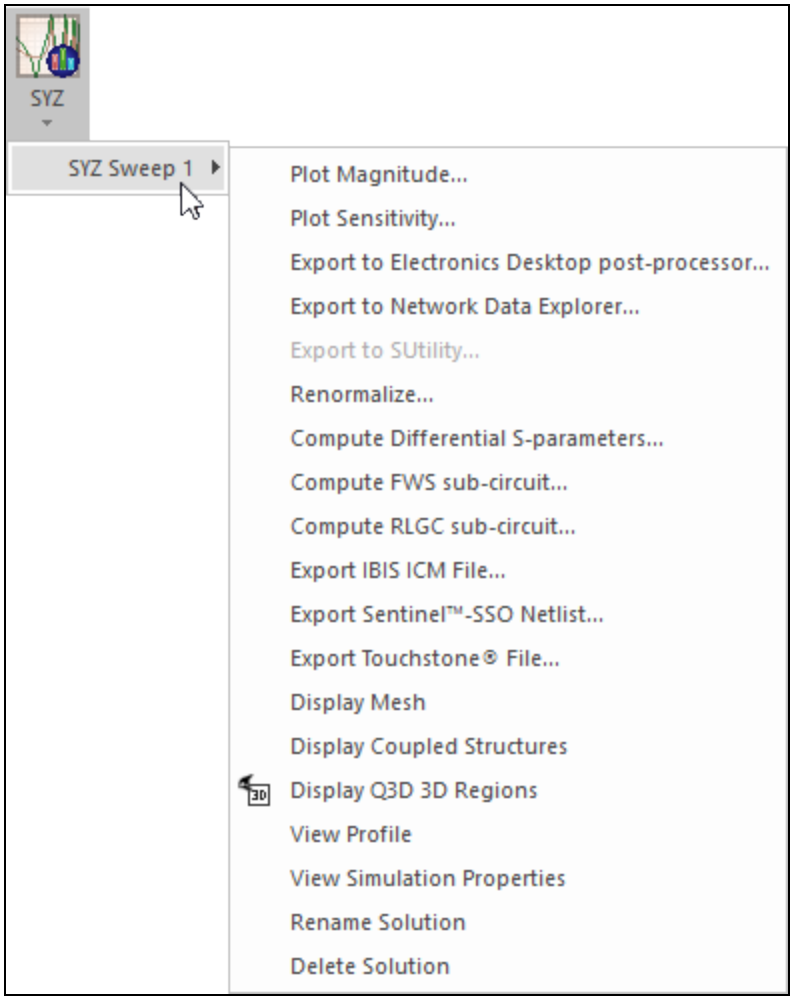

Export menu options include:

- **Export to Electronics Desktop post-processor** – launches Ansys Electronics Desktop and opens the plot.
- **Export to Network Data Explorer** – launches ndExplorer with SYZ data pre-populated.
- **Export to SUtility** – launches SUtility with SYZ data pre-populated.
- **Export IBIS ICM File** – exports files to the IBIS Interconnect Modeling (ICM) standard. See below.
- **Export Sentinel-SSO Netlist** – exports the results of an SIwave SYZ-parameter extraction as a SPICE netlist with a CPP header for Apache Sentinel SSO flow. See below.
- **Export Touchstone File** – exports the SYZ data in an *.sNp file that can be used with third-party tools and opened in any text editor.

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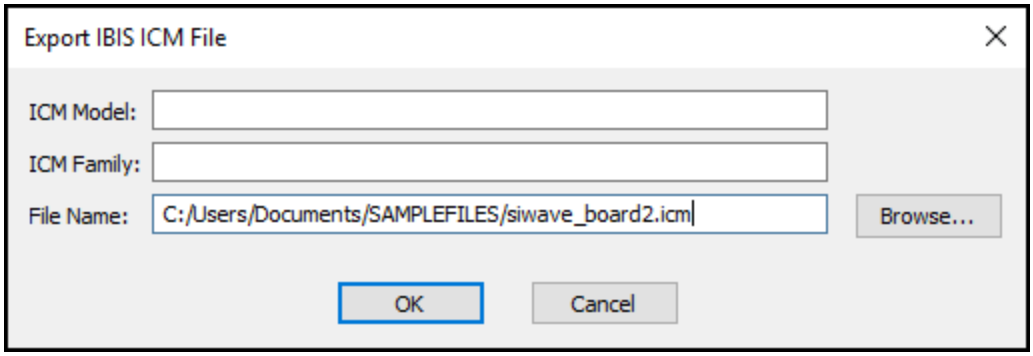
Exporting an IBIS ICM File

The IBIS Interconnect Modeling (ICM) standard specifies a "wrapper" around regular Touchstone files. An .***.icm** file lists original port names and includes a link to a Touchstone (.***.sNp**) file containing the actual SYZ-parameter data.

To export an IBIS ICM file from SIwave:

1. Run an SYZ Sweep.
2. Click **Results**.
3. From the SIwave area, select **SYZ > [Simulation Name] > Export IBIS ICM File**.

   The **Export IBIS ICM File** window appears.



4. Enter the **ICM Model**, **ICM Family**, and appropriate **File Name** and path.
5. Click **OK**.

   The file exports.

> **Note:**
>
> To conform with the ICM (IBIS Interconnect Modeling) standard, only lowercase letters, numbers, underscore and dash ("-") are permitted in the .**sNp** and .**icm** file names.

Exporting a Sentinel-SSO Netlist

To export a Sentinel-SSO Netlist from SIwave:

1. Run an SYZ Sweep.
2. Click **Results**.
3. From the SIwave area, select **SYZ > [Simulation Name] > Export Sentinel-SSO Netlist**.

   The **Export Sentinel-SSO Netlist** window appears.

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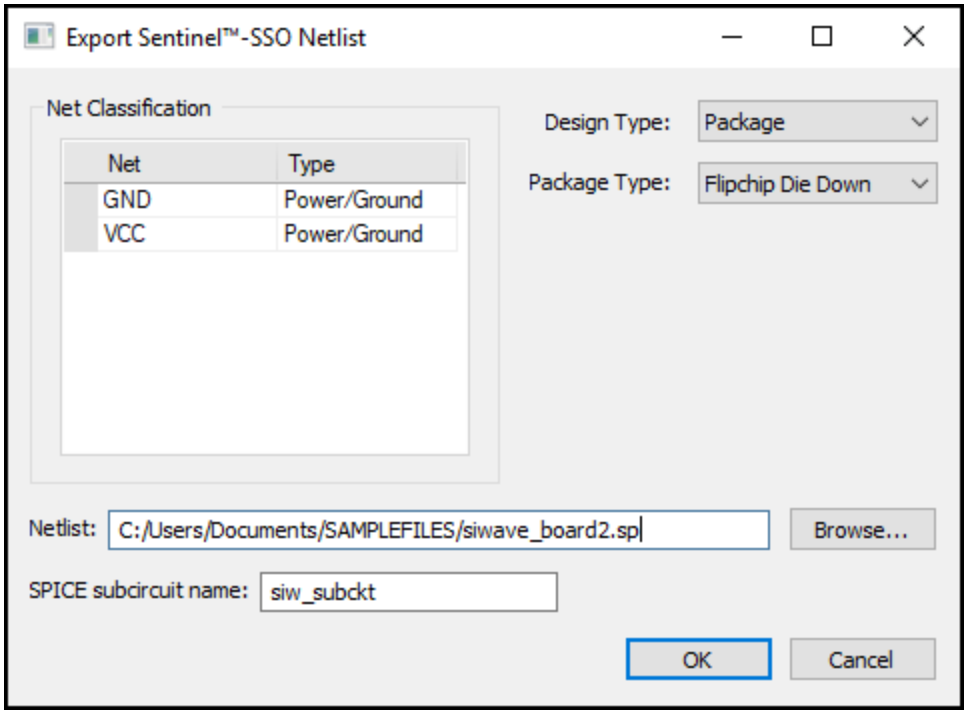

4. From the **Net Classification** area, you can use the **Type** drop-down menus to reclassify nets as **Power/Ground** or **Signal**.
5. Use the **Design Type** drop-down menu to select **Package**, **Board**, or **Die**.
6. If you selected Package, use the **Package Type** drop-down menu to select a package type. This menu is unavailable otherwise.
7. From the **Netlist** field, type a file name and path, or click **Browse** to select these.
8. Specify a **SPICE subcircuit name** for the netlist file, or accept the default (**siw_subckt**).
9. Click **OK** .

   A SPICE netlist file is created in the specified location. A Touchstone file containing the S-parameter data is created in the same directory.

From the SYZ Results menu, you can also view SYZ results or access additional menu options.

Computing Differential S-Parameters

If you have two or more ports defined and have computed the S-parameters for them, you can view the differential and common-mode S-parameters.

To compute the differential S-parameters in SIwave:

1. Click **Results**.
2. From the SIwave area, select **SYZ** > **[Simulation Name]**.
3. Click **Compute Differential S-parameters**.

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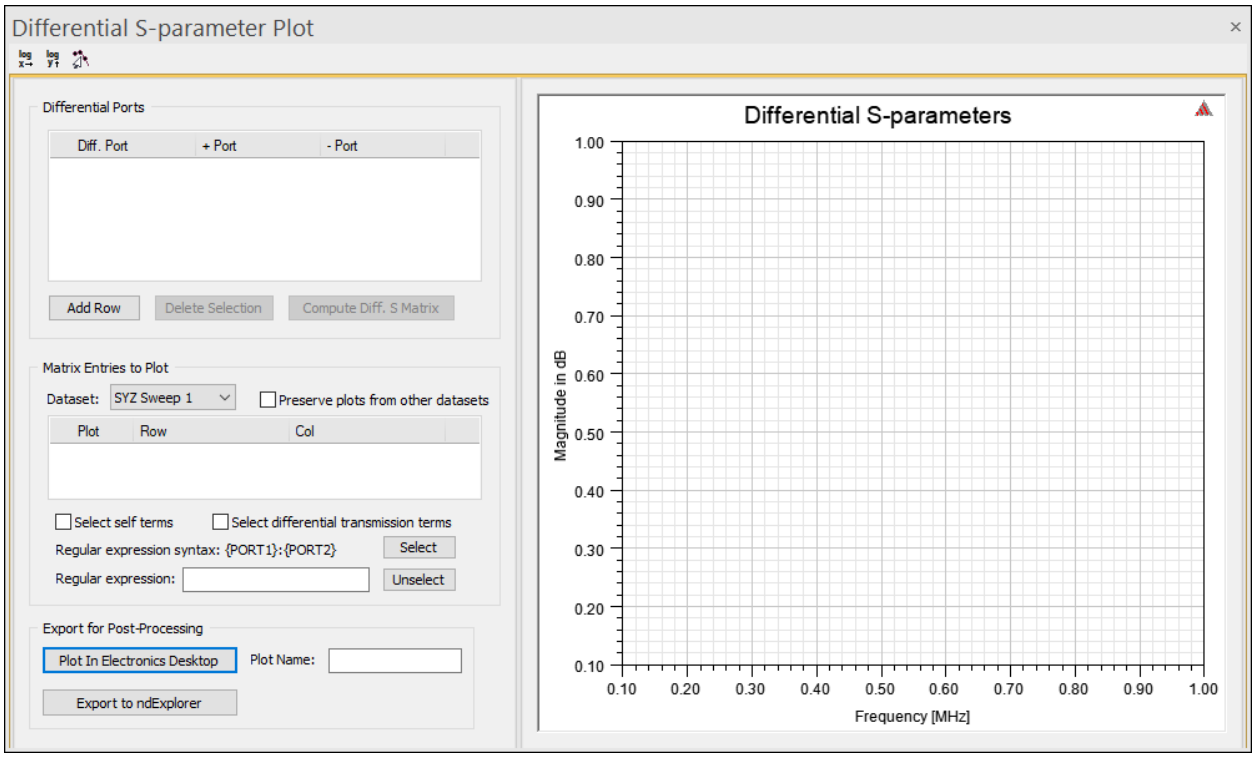
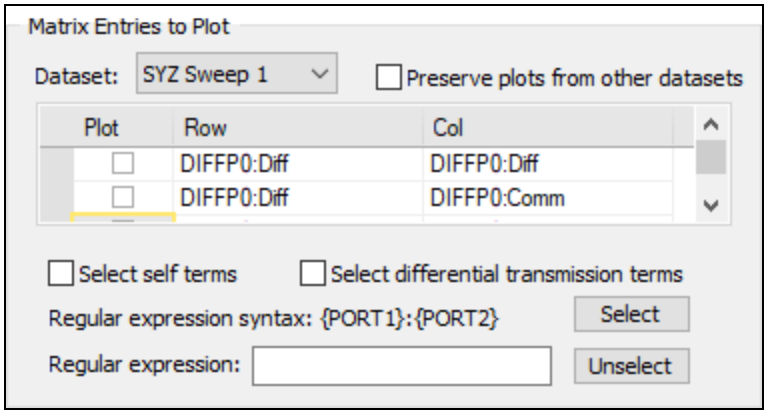
The **Differential S-parameter Plot** window appears.



See Plotting Magnitude for more information about using the plot window.

4. From the **Differential Ports** area, select the **Positive Reference Port** and **Negative Reference Port**.
5. If appropriate, click **Add Row** to add ports.
6. Click **Compute Diff. S Matrix**.

   The **Matrix Entries to Plot** area updates.



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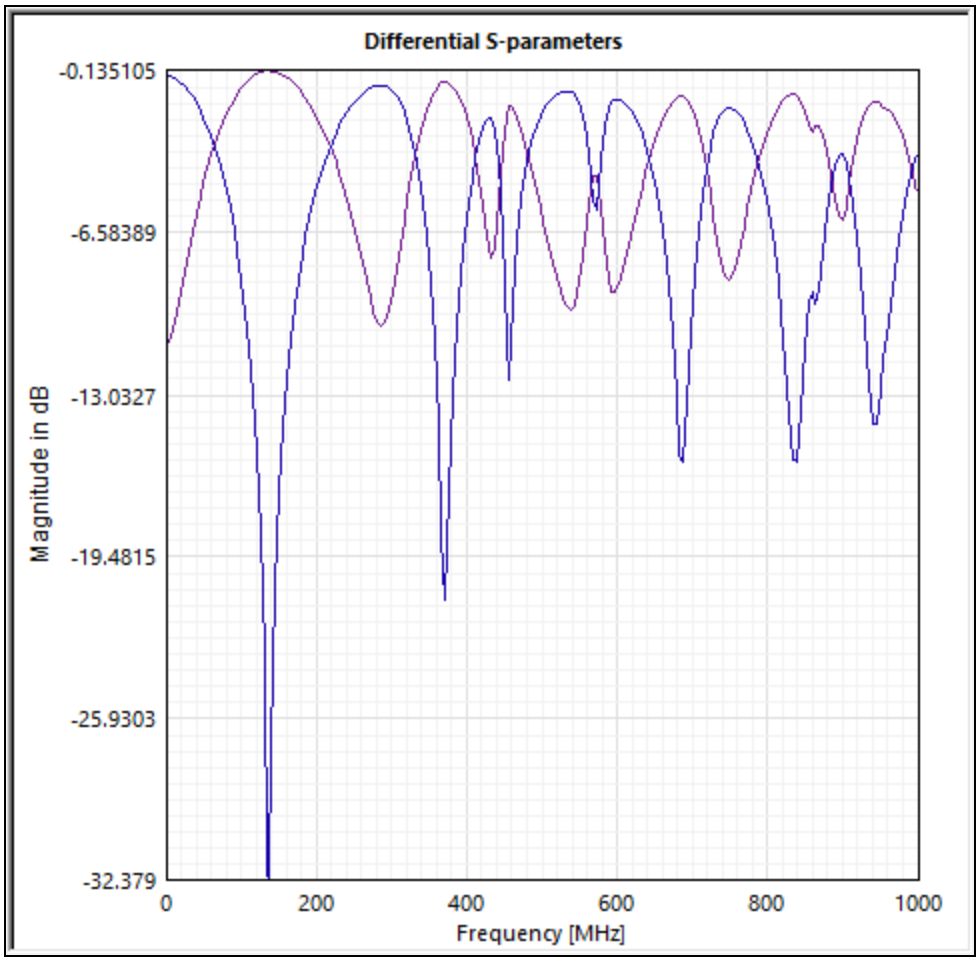
7. Use the check boxes in the **Plot** column to select entries to plot.

   The plot area updates to display the information.



8. To export and view the plot in Ansys Electronics Desktop, enter a name in the **Plot Name** field and click **Plot in Electronics Desktop**.
9. To export and view the plot in ndExplorer, click **Export to ndExplorer**.

Computing RLGC Subcircuits in SIwave

SIwave allows you to derive RLGC information from the S-parameters. After you compute the RLGC matrices, you can export the RLGC subcircuit.

To export a solution into an RLGC subcircuit in SIwave:

1. Click **Results**.
2. From the SIwave area, select **SYZ** > **[Simulation Name]**.
3. Click **Compute RLGC Sub-Circuit**.

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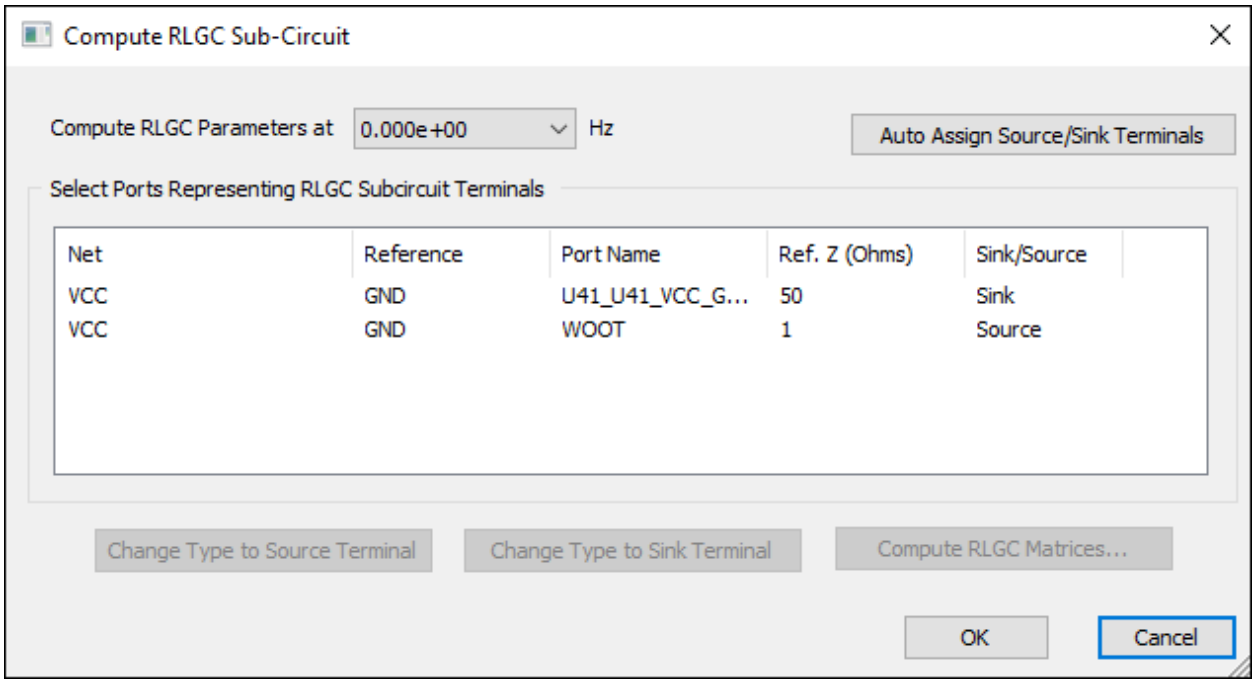
The **Compute RLGC Sub-circuit** window appears.



4. Use the **Compute RLGC Parameters at** drop-down menu to select a frequency.
5. To assign sources and sinks, select a net in the list and use the **Change Type to Source Terminal** and **Change Type to Sink Terminal** buttons. Alternatively, click **Auto Assign Source/Sink Terminals** to have SIwave identify and assign nets for you.

> **Note:**
>
> If you have two conducting objects touching each other, this treats them as one combined object. Nets are auto identified by finding the touching conductors.

6. Click ports in the list to select them. You must select at least one Sink and one Source.
7. Click **Compute RLGC Matrices**.

   The **RLGC Matrices** window appears, on the Resistance tab.

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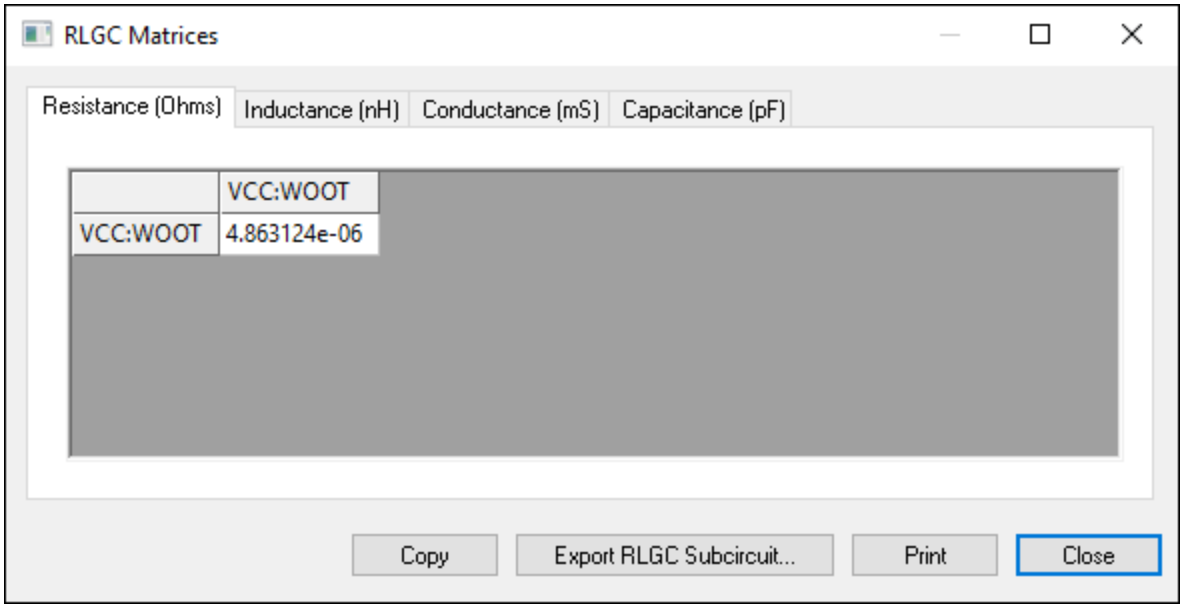
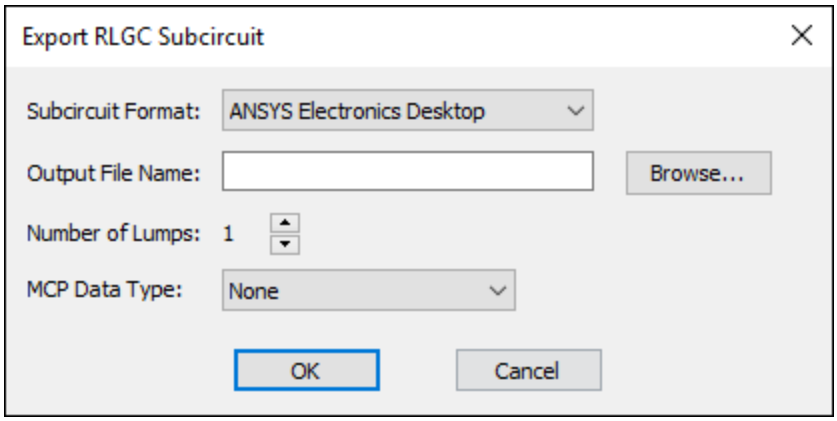


8. Click any tab to view its details (Resistance, Inductance, Conductance, Capacitance).
9. To copy data from a tab, click **Copy**.
10. To print data from a tab, click **Print**.
11. To export the subcircuit, click **Export RLGC Subcircuit**.

    The **Export RLGC Subcircuit** window appears.



12. Use the **Subcircuit Format** drop-down menu to select a format.

    Options include:

    - Ansys Electronics Desktop
    - Berkeley SPICE

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- ESpice DML
- HSPICE
- IBIS Package Model
- Maxwell SPICE
- PSpice
- Twin Builder
- Spectre
- SPEF

13. From the **Output File Name** field, type a file name and path, or click **Browse** to select one.
14. Use the arrow buttons to specify the **Number of Lumps** to be included in the simulation. This can be any discrete value between 1 and 1000.
15. Use the **MCP Data Type** drop-down menu to select **DIE**, **PKG**, or **PCB**.
16. Click **OK** to export the RLGC matrices and return to the **RLGC Matrices** window.
17. Click **Close** to close the **RLGC Matrices** window.
18. Click **OK** to close the **Compute RLGC Sub-Circuit** window.

Computing and Exporting Full-Wave SPICE Subcircuits

The ability to export subcircuits is an important feature of SIwave. Exporting a subcircuit allows you to perform an analysis of the structure in a circuit simulator, together with detailed nonlinear models of the drivers and receivers. You can also simulate systems comprising PCBs and packages by connecting their subcircuits together in SPICE or Spectre.

A full-wave subcircuit analysis includes full-wave effects. Frequency domain information is transferred to circuit simulators that operate in the time domain. Broadband matching of frequency responses is ensured while full-wave solution accuracy is preserved. When S-parameter data is exported to PSpice or HSPICE, an equivalent circuit is created. This circuit consists of frequency controlled voltage and current sources. When terminal S-parameter data is exported to Maxwell Spice software, a new full-wave *N*-port subcircuit is created.

See Full-wave subcircuits for more information on full-wave subcircuit models.

To export a solution into a full-wave SPICE subcircuit from SIwave:

1. Click **Results**.
2. From the SIwave area, select **SYZ** > **[Simulation Name]**.
3. Click **Compute FWS Sub-Circuit**.

   ndExplorer opens, and the **Broadband Export Options** window appears.

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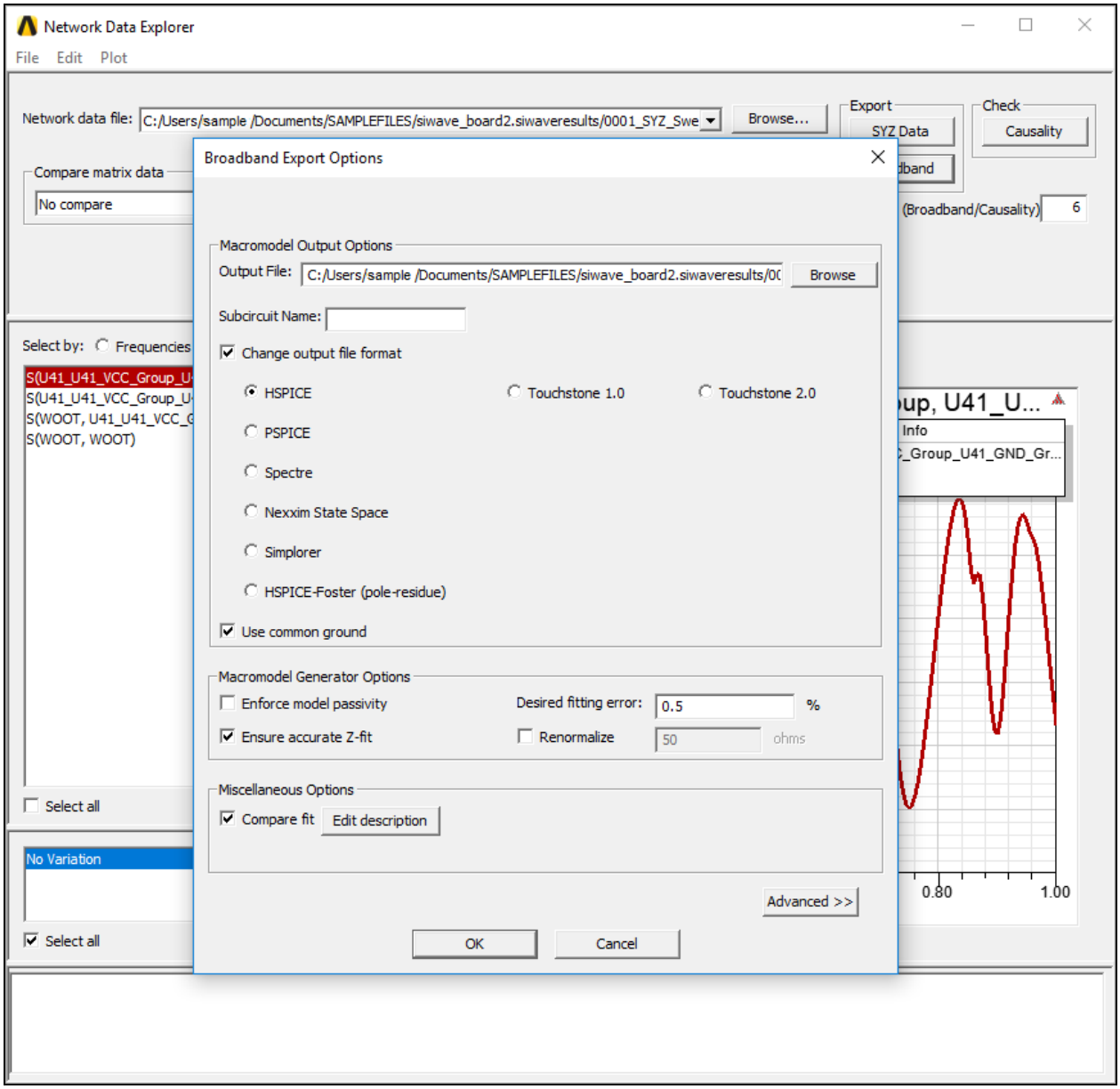

4. From the **Output File** field, enter a name and path for your file, or use the **Browse** button.
5. From the **Subcircuit Name** field, type a name for the subcircuit.
6. Check the **Change output file format** check box. Then use the radio buttons to select your appropriate SPICE file format. The default is HSPICE.
7. If appropriate, select **Use common ground**.
8. Use the check boxes to select your appropriate passivity, Z-fit, and renormalization options. For more information on these options, see Exporting Macro Model.

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9. Click **Advanced>>** to view additional options:
   - Passivity Options
   - Column Fitting Options
   - State Space Fitting Algorithm
   - Enable Relative Error Tolerance
   - Enforce Causality
   - For more information on these options, see Exporting Macro Model.
10. Click **OK**.

    A SPICE file based on the geometry of the planes and added circuit elements exports to the specified location.

For more information, see S-Parameter Technical Notes.

Impedance Scan

The Impedance Scanner can quickly examine trace impedance profiles and identify any violations according to specified criteria. It uses the 2D cross-section solver to extract the impedance of single-ended and differential nets. It considers coupling effects from nearby traces and co-planes.

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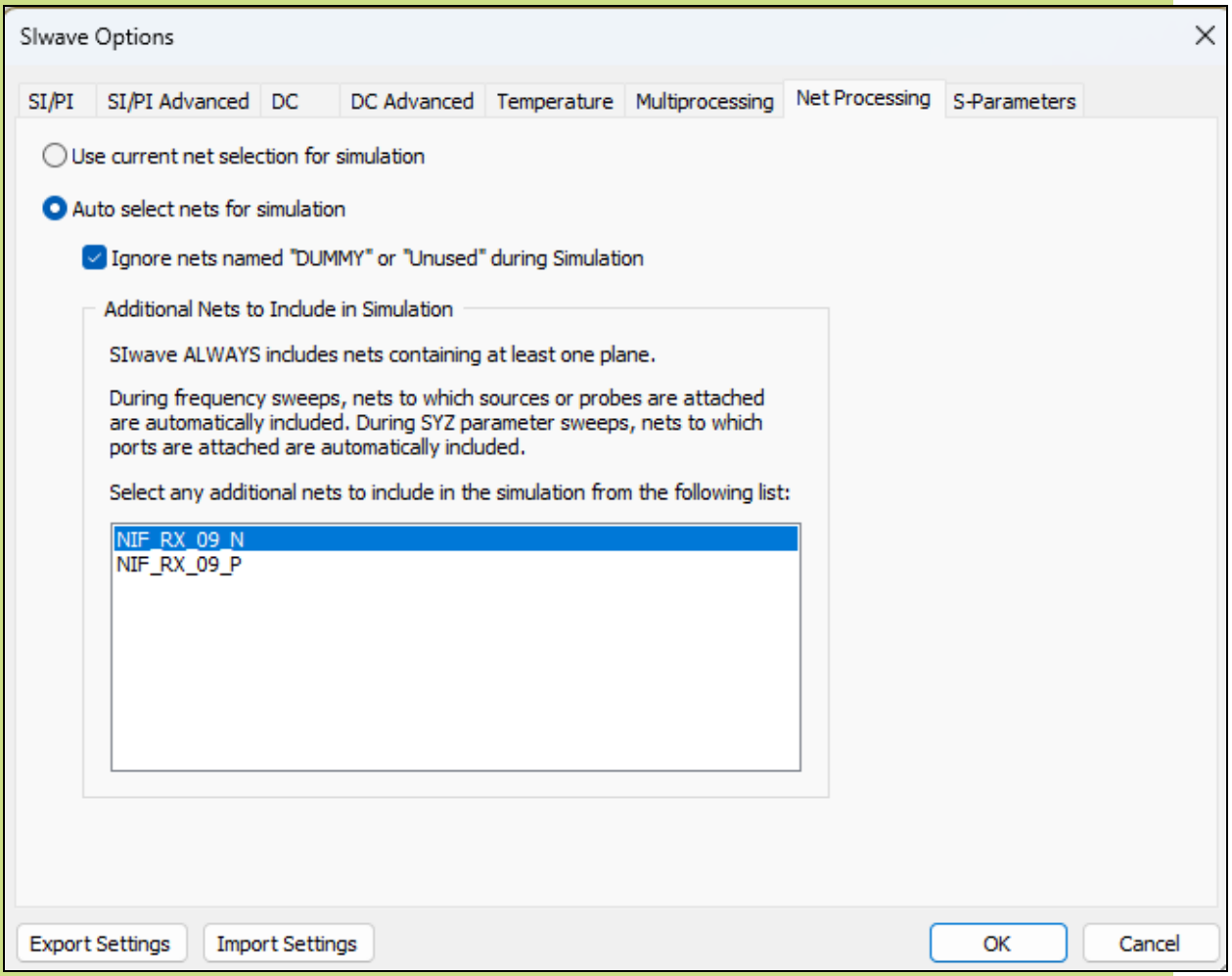
Note:

If the user chooses **Auto select nets for simulation** from the **SIwave Options** window, only user-specified signal nets and Power/Ground nets are included in the simulation. If other nets need to be included, they can either be selected from the **Additional Nets to Include in Simulation** list or identified as Power/Ground prior to scanning.



To run the impedance scan:

1. Click **Simulation** > **Impedance Scan**.

   The **Signal Net Impedance Scan** window appears.

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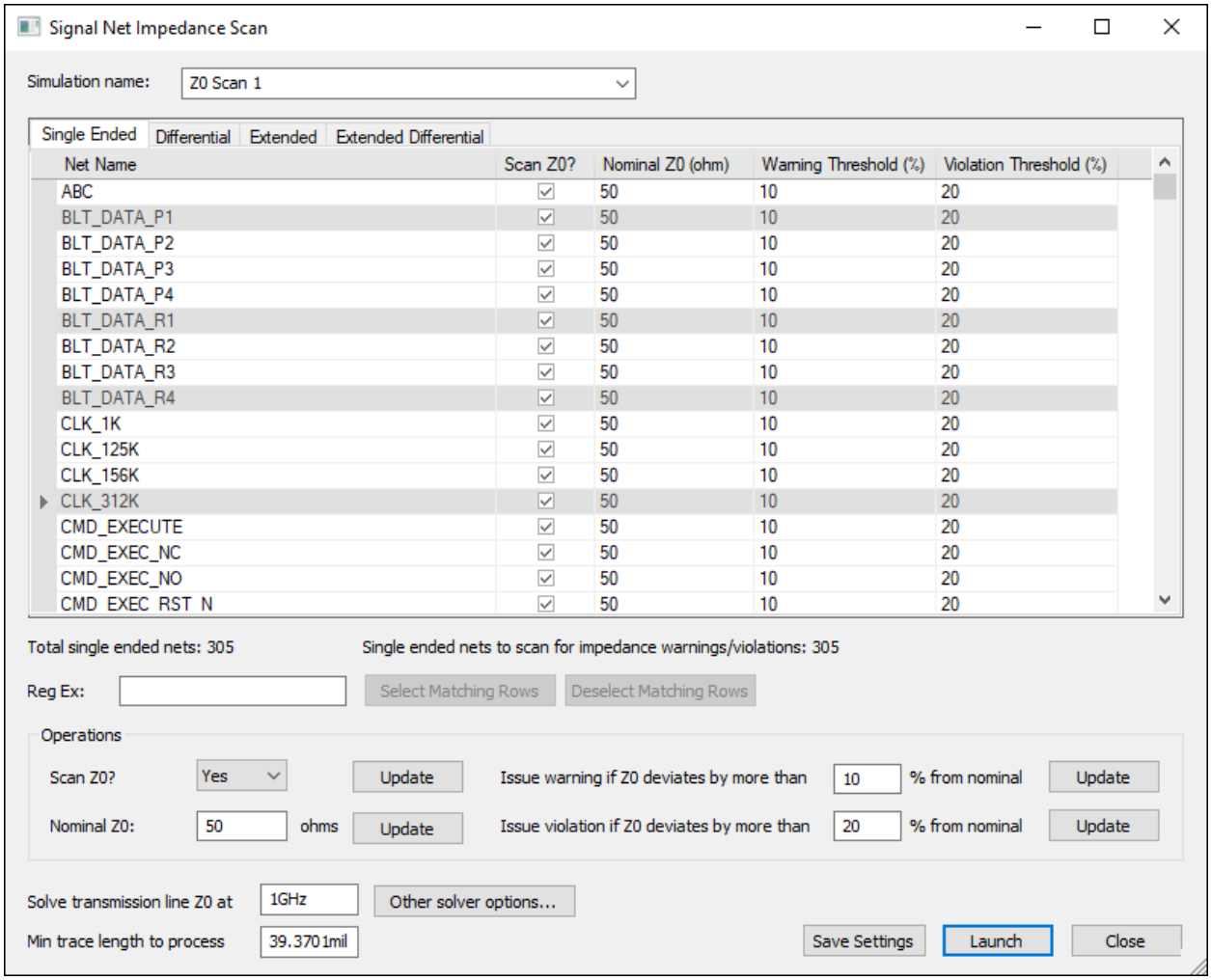

2. From the **Simulation Name** field, enter a name for the simulation or leave the default.
3. Use the **Single Ended**, **Differential**, **Extended**, and **Extended Differential** tabs to select nets for scanning. Select a row by clicking the gray column adjacent to the row, or use Regular Expressions to select and deselect rows.
4. The **Operations** area of the window is unavailable until you select one or more rows. Use the fields there to set options for the selected row(s). You can also directly edit information in the net list.
5. Enter the frequency at which to run the solver.
6. Enter the minimum trace length. This threshold applies to all net types.
7. If appropriate, click **Other Solver Options** to set additional options.
8. If appropriate, click **Save Settings** to retain your settings.
9. Click **Launch** to run the simulation.

   The **Messages** window updates with a Process Monitor tab that displays the progress.

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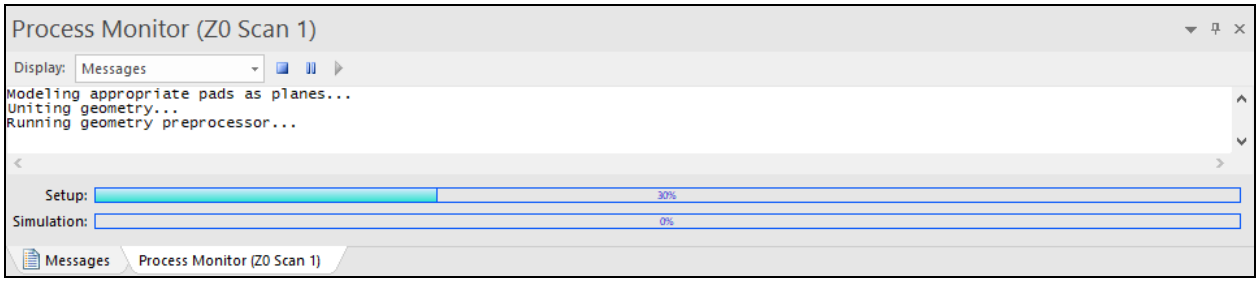
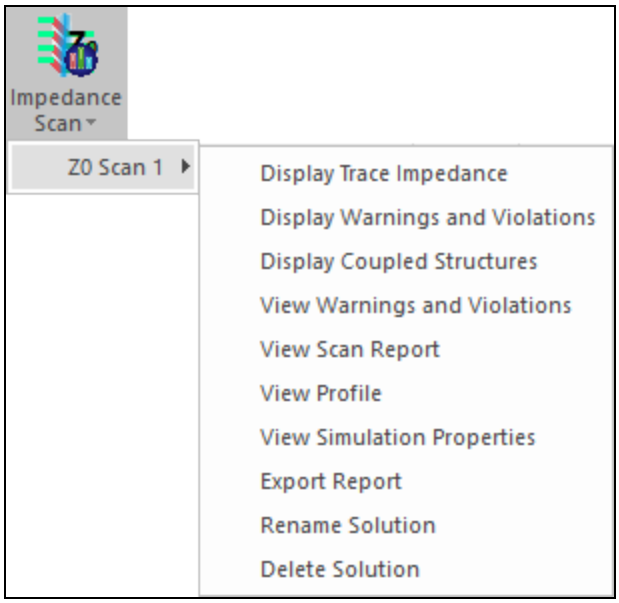


Viewing Impedance Scan Results

To view Impedance Scan results:

1. Click **Results**.
2. From the SIwave area, select **Impedance Scan** > **[Simulation Name]**.



3. Select the type of results you would like to view.

   Result menu options include:

   - **Display/Hide Trace Impedance** – toggles an impedance color legend and highlights traces according to that legend. The Trace Impedance window allows you to select specific layers for which to view information.
   - **Display/Hide Warnings and Violations** – allows you to toggle highlights for warnings/violations. When selected, traces within threshold are highlighted green, those with warnings are highlighted orange, those with violations are highlighted red. Traces belonging to differential nets that are not coupled are highlighted in gray.

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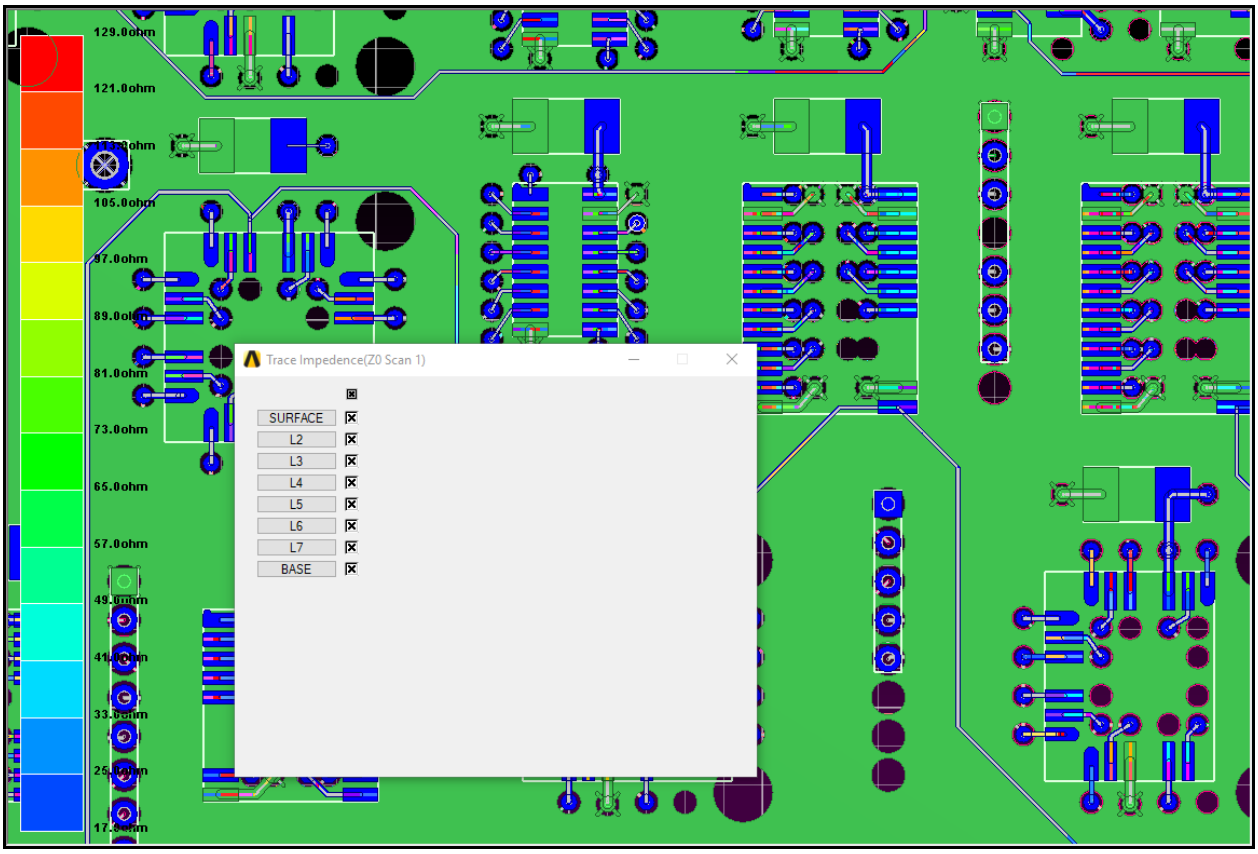
- **Display/Hide Coupled Structures** – toggles display of coupled structures in the Modeling workspace.
- **View Warnings and Violations** – displays a table of warnings and violations that can be exported. You can adjust the nominal impedance and violation/warning thresholds from this window.
- **View Scan Report** – opens an HTML report listing nets in violation (red), nets with warnings (orange), and nets within thresholds (green). You can save this report.

Display Trace Impedance:



Display Warnings and Violations:

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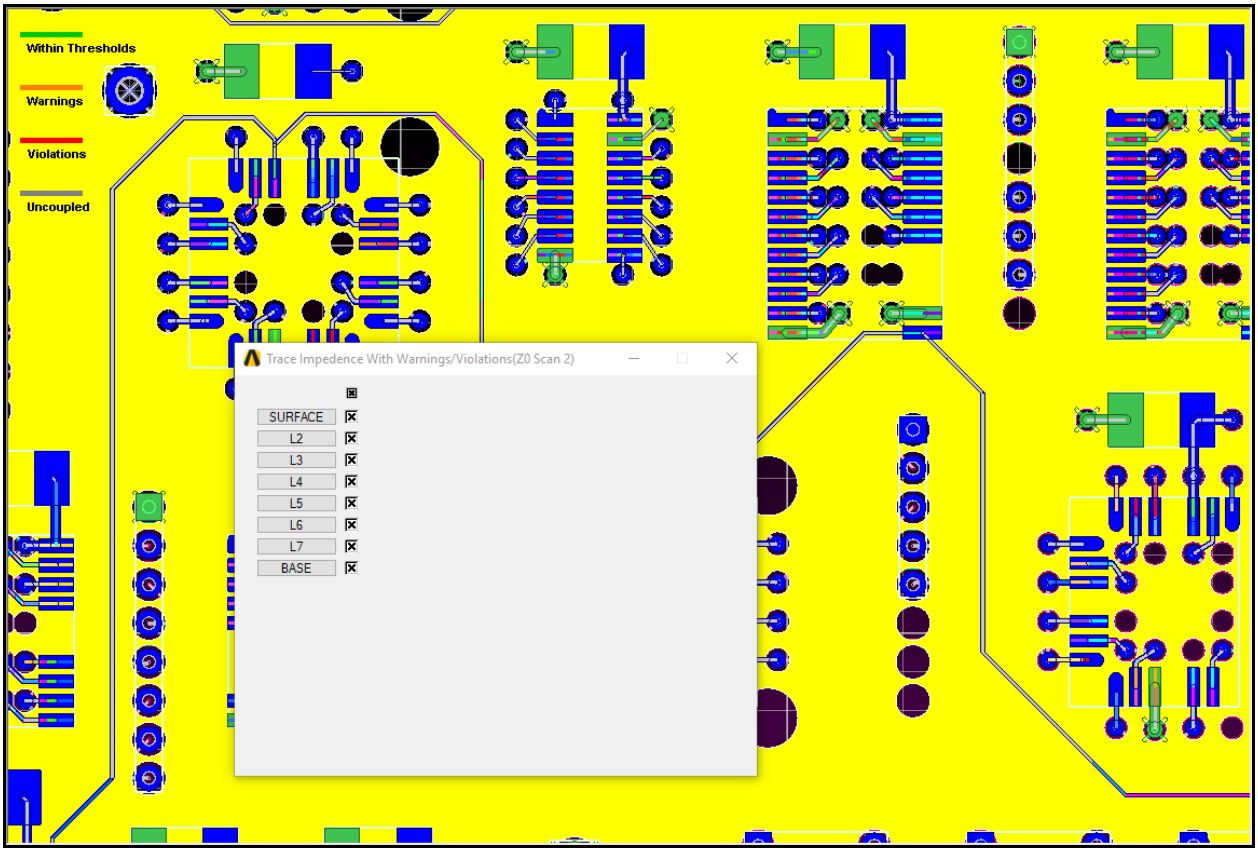

View Violations and Warnings:

For every net:

- A line segment shows neither a warning nor a violation when its impedance is within the warning threshold percentage of nominal impedance (either above or below).
- A line segment shows a warning when its impedance is greater than or less than the warning threshold, but within the violation threshold percentage of nominal impedance.
- A line segment shows a violation when its impedance is greater than or less than the violation threshold percentage of nominal impedance.

For example, given a nominal impedance of 50 ohms, a 10% warning threshold, and a 20% violation threshold:

- Impedance of 45-55 ohms = no warning or violation
- Impedance of 40-44 ohms = warning
- Impedance of 56-60 ohms = warning
- Impedance of 0-39 ohms = violation
- Impedance of 61+ ohms = violation

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This window allows you to **Show All** violations and warnings, or display **Only Violations** or **Only warnings**.

- Click **Edit Nominal Impedance and Thresholds** to change violation and warning thresholds.
- Edit the **Min Length to Display** and click **Update** to change which line segments display.
- Click **Export Table** to export the information in CSV format.

View Scan Report:

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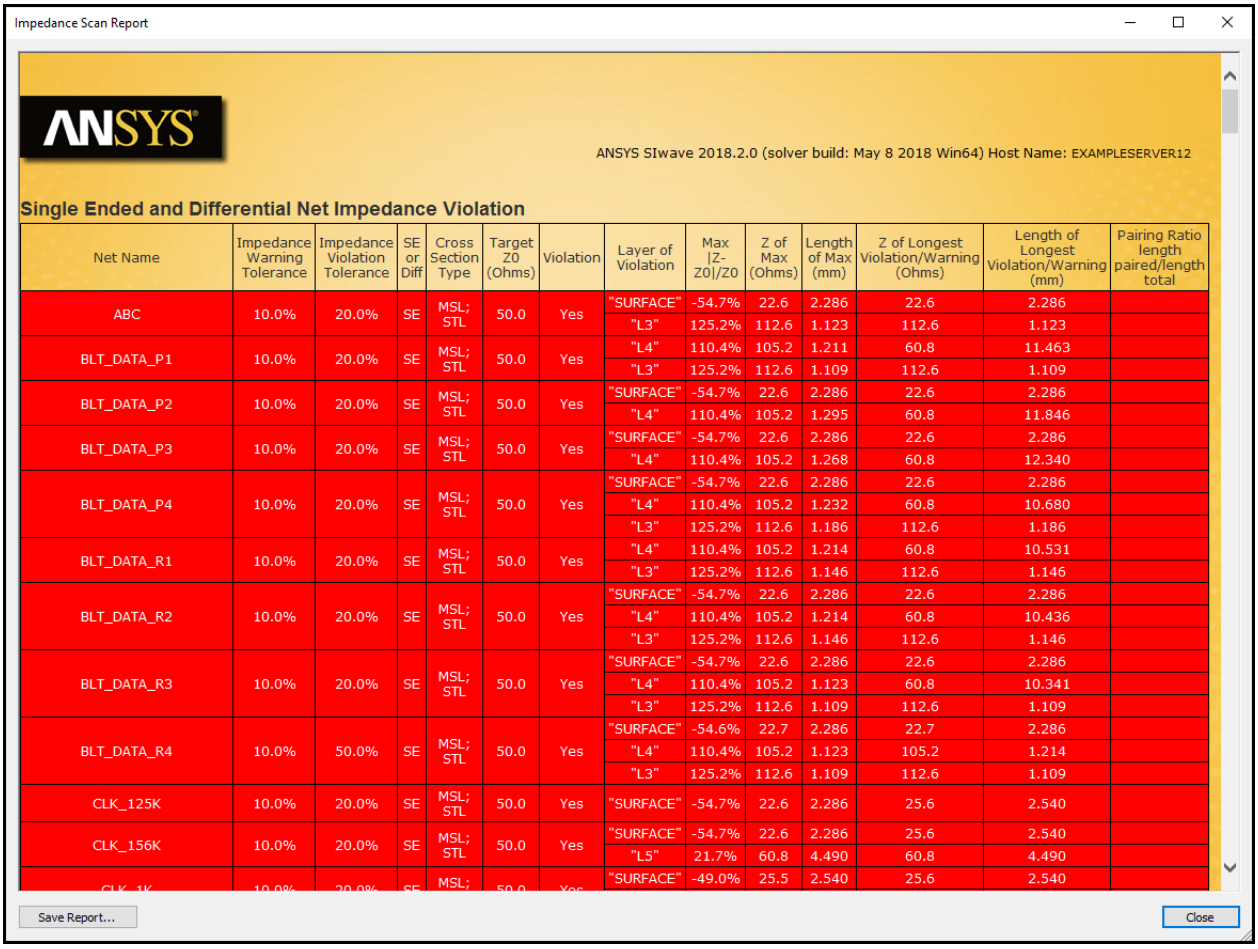

Net Name	Impedance Warning Tolerance	Impedance Violation Tolerance	SE or Diff	Cross Section Type	Target Z0 (Ohms)	Violation	Layer of Violation	Max |Z-Z0|/Z0	Z of Max (Ohms)	Length of Max (mm)	Z of Longest Violation/Warning (Ohms)	Length of Longest Violation/Warning (mm)	Pairing Ratio length paired/length total
ABC	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	22.6	2.286	
							"L3"	125.2%	112.6	1.123	112.6	1.123	
BLT_DATA_P1	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"L4"	110.4%	105.2	1.211	60.8	11.463	
							"L3"	125.2%	112.6	1.109	112.6	1.109	
BLT_DATA_P2	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	22.6	2.286	
							"L4"	110.4%	105.2	1.295	60.8	11.846	
BLT_DATA_P3	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	22.6	2.286	
							"L4"	110.4%	105.2	1.268	60.8	12.340	
BLT_DATA_P4	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	22.6	2.286	
							"L4"	110.4%	105.2	1.232	60.8	10.680	
							"L3"	125.2%	112.6	1.186	112.6	1.186	
BLT_DATA_R1	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"L4"	110.4%	105.2	1.214	60.8	10.531	
							"L3"	125.2%	112.6	1.146	112.6	1.146	
BLT_DATA_R2	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	22.6	2.286	
							"L4"	110.4%	105.2	1.214	60.8	10.436	
							"L3"	125.2%	112.6	1.146	112.6	1.146	
BLT_DATA_R3	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	22.6	2.286	
							"L4"	110.4%	105.2	1.123	60.8	10.341	
							"L3"	125.2%	112.6	1.109	112.6	1.109	
BLT_DATA_R4	10.0%	50.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.6%	22.7	2.286	22.7	2.286	
							"L4"	110.4%	105.2	1.123	105.2	1.214	
							"L3"	125.2%	112.6	1.109	112.6	1.109	
CLK_125K	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	25.6	2.540	
CLK_156K	10.0%	20.0%	SE	MSL; STL	50.0	Yes	"SURFACE"	-54.7%	22.6	2.286	25.6	2.540	
							"L5"	21.7%	60.8	4.490	60.8	4.490	
CLK_1K	10.0%	20.0%	SE	MSL;	50.0	Yes	"SURFACE"	-49.0%	25.5	2.540	25.6	2.540	

From the Impedance Scan Results menu, you can also export results or access additional menu options.

Impedance Scan Results Menu Options

Navigate to the Impedance Scan results menu:

1. Click **Results**.
2. From the SIwave area, select **Impedance Scan** > **[Simulation Name]**.

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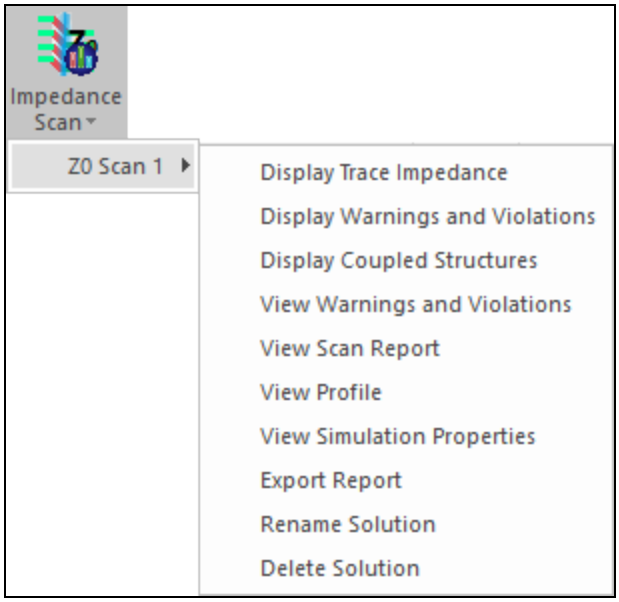

Menu options include:

- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the SI/PI tab.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Simulation Profile:

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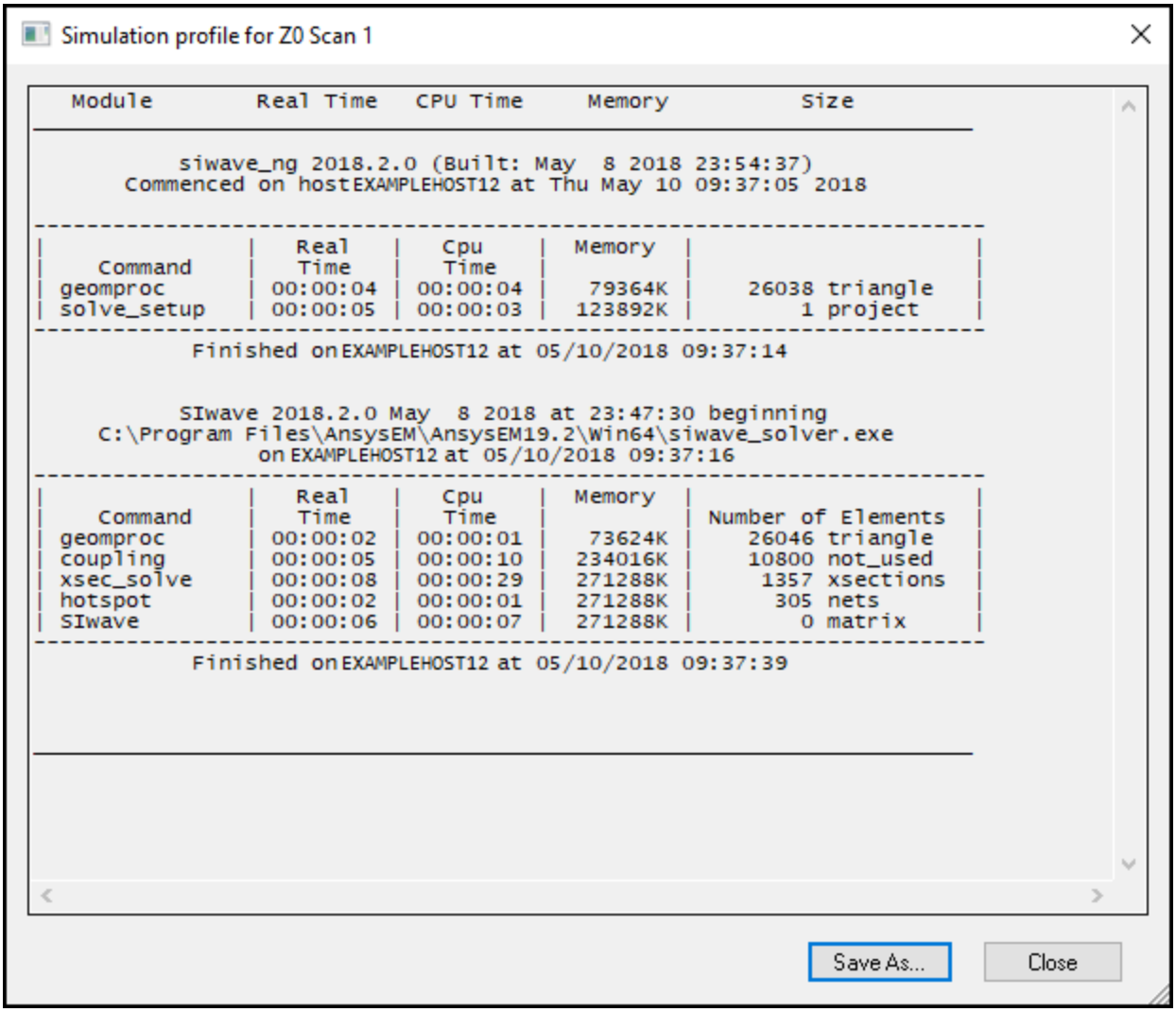

Simulation Properties:

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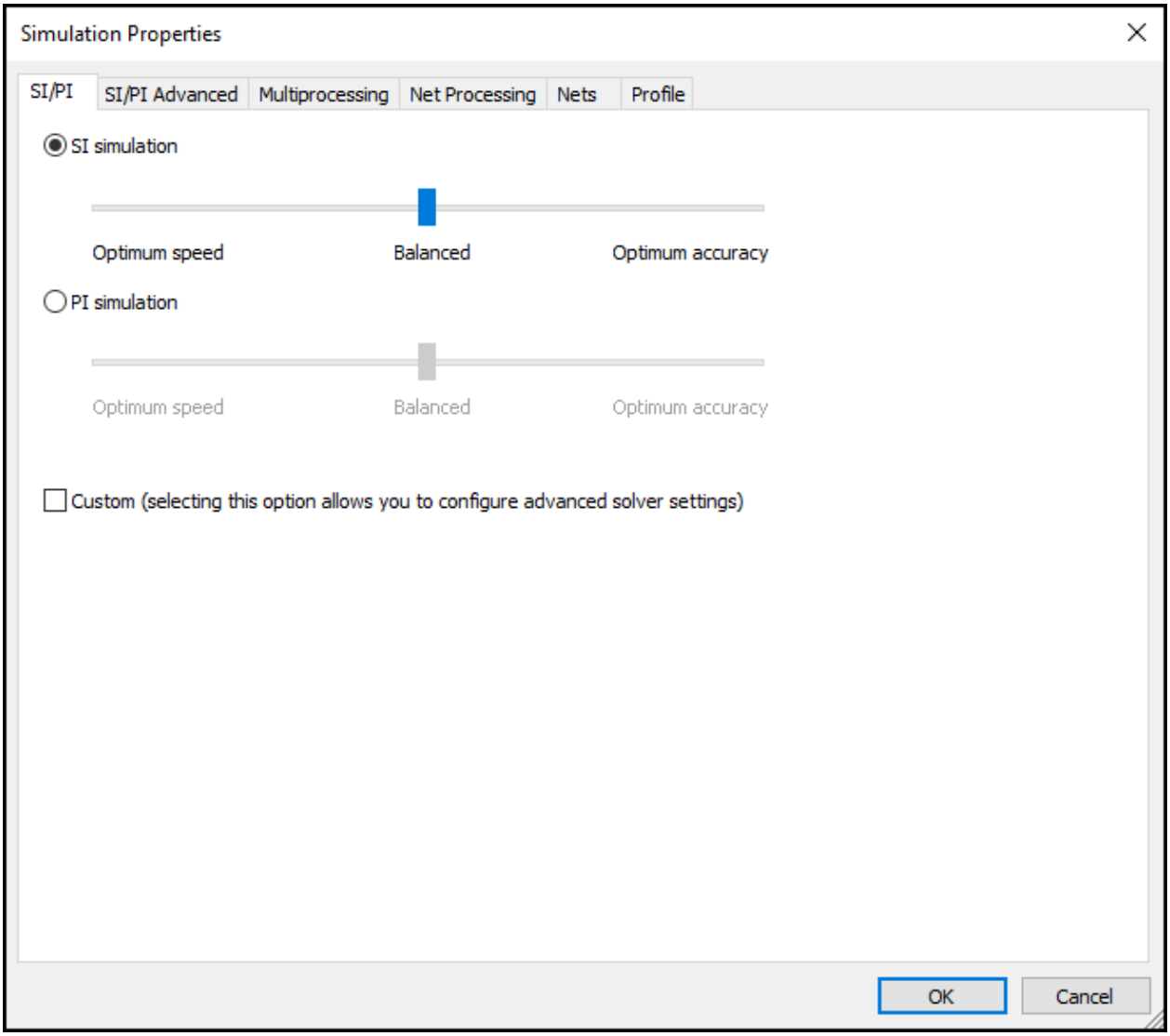

From the Impedance Scan Results menu, you can also view Impedance Scan results and export the Impedance Scan.

Exporting an Impedance Scan Report

SIwave can generate an HTML report that contains the impedance plot image for every layer with the color scale in ohms. The file can also display tables showing impedance deviation thresholds, warnings, and violations.

For every net:

- A line segment shows neither a warning nor a violation when its impedance is within the warning threshold percentage of nominal impedance (either above or below).

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- A line segment shows a warning when its impedance is greater than or less than the warning threshold, but within the violation threshold percentage of nominal impedance.
- A line segment shows a violation when its impedance is greater than or less than the violation threshold percentage of nominal impedance.

For example, given a nominal impedance of 50 ohms, a 10% warning threshold, and a 20% violation threshold:

- Impedance of 45-55 ohms = no warning or violation
- Impedance of 40-44 ohms = warning
- Impedance of 56-60 ohms = warning
- Impedance of 0-39 ohms = violation
- Impedance of 61+ ohms = violation

To export an impedance scan report in HTML format:

1. Click **Results** > **Impedance Scan** > **[Scan Name]** > **Export Report**.

   A **Save As** window appears.

2. From the **Project Directory** field, type your appropriate file name and path, or click **Browse** to select it.
3. Click **Save**.

   The HTML file is exported to your chosen directory.

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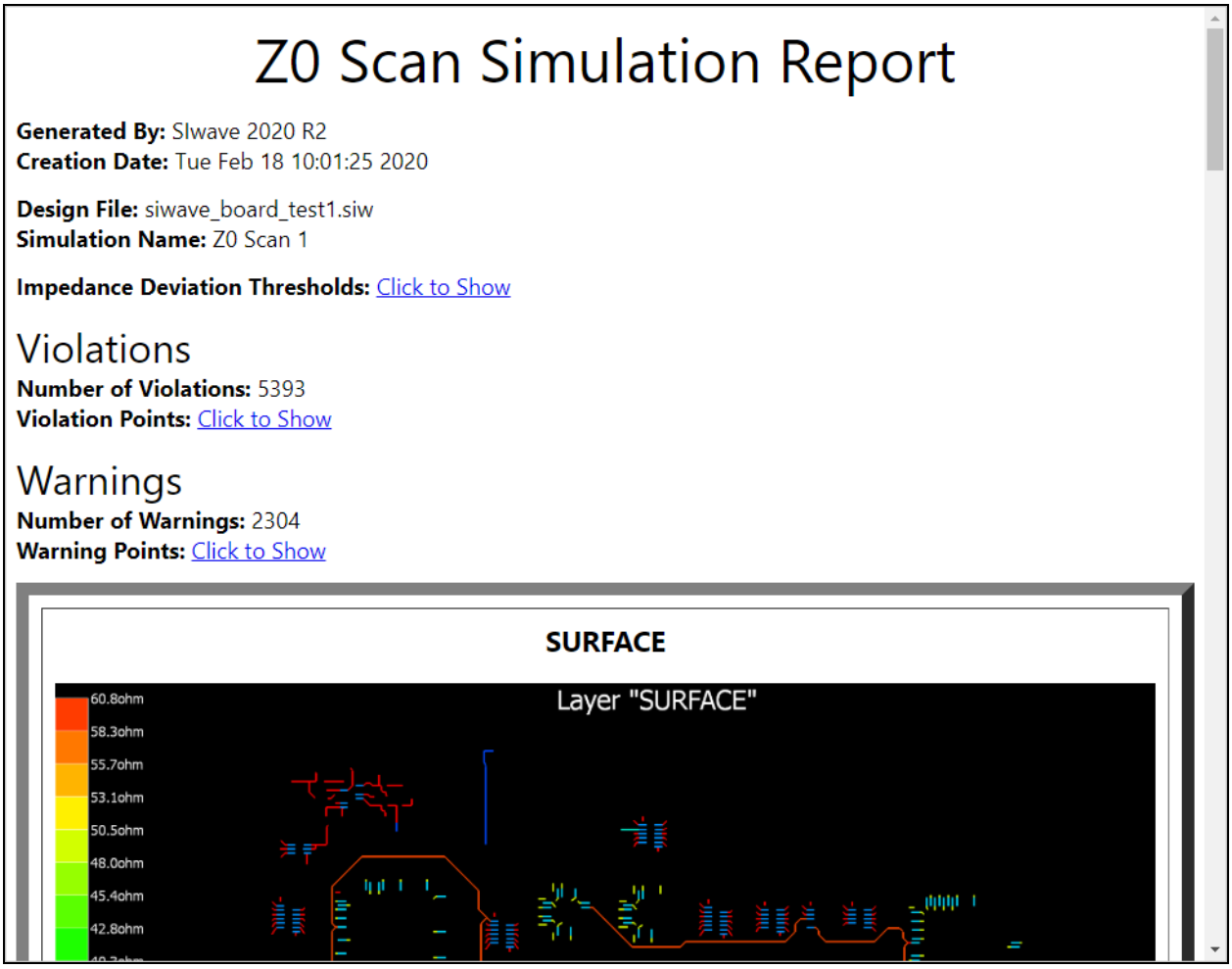
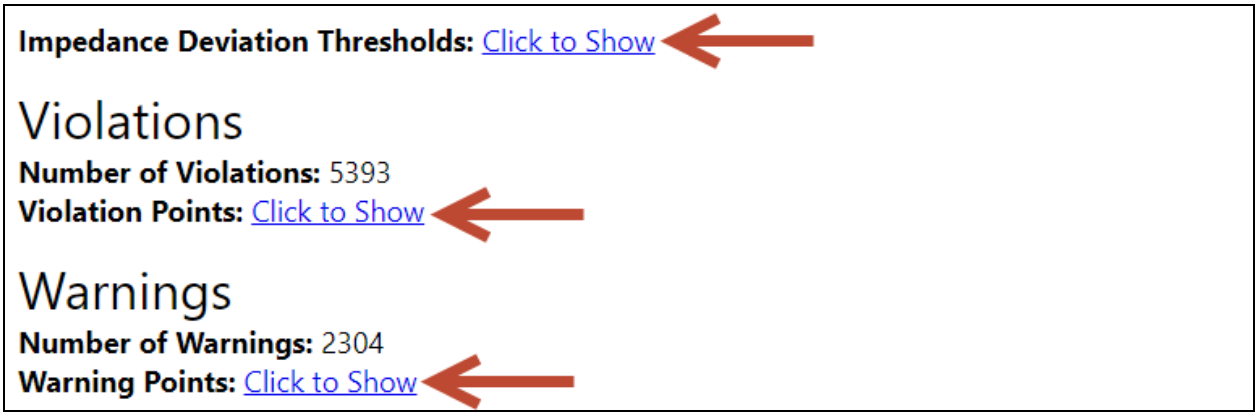


The **Click to Show** and **Click to Hide** buttons toggle tables listing impedance deviation thresholds, violation points, and warnings.



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Impedance Deviation Thresholds: Click to Hide

Net	Nominal Impedance(ohms)	Deviation % for Warning	Deviation % for Violation
ABC	50	10	20
BLT_DATA_P1	50	10	20
BLT_DATA_P2	50	10	20
BLT_DATA_P3	50	10	20
BLT_DATA_P4	50	10	20
BLT_DATA_R1	50	10	20
BLT_DATA_R2	50	10	20
BLT_DATA_R3	50	10	20
BLT_DATA_R4	50	10	20
CLK_1K	50	10	20
CLK_125K	50	10	20
CLK_156K	50	10	20
CLK_312K	50	10	20
CMD_EXECUTE	50	10	20
CMD_EXEC_NC	50	10	20
CMD_EXEC_NO	50	10	20
CMD_EXEC_RST_N	50	10	20
COMPARATOR_VCC	50	10	20
CSCP_N	50	10	20
CSCR_N	50	10	20
CSDP_N	50	10	20
CSDR_N	50	10	20
CSEP_N	50	10	20

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Violations

Number of Violations: 5393
Violation Points: Click to Hide

Table sorted by: Impedance Deviation Percentage
(Switch to sort by Net)
(Switch to sort by Length)

Net	Layer	Start Point (mils)	End Point (mils)	Length (mils)	Impedance (ohms)	Impedance Deviation (%)
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4250.000000)	(2375.000000, 4257.183837)	7.183837	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4257.183837)	(2375.000000, 4297.795291)	40.611454	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4297.795291)	(2375.000000, 4427.204709)	129.409418	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4427.204709)	(2375.000000, 4467.816163)	40.611454	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4467.816163)	(2375.000000, 4475.000000)	7.183837	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4475.000000)	(2375.000000, 4482.183837)	7.183837	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4482.183837)	(2375.000000, 4522.795291)	40.611454	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4522.795291)	(2375.000000, 4702.204709)	179.409418	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4702.204709)	(2375.000000, 4742.816163)	40.611454	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4742.816163)	(2375.000000, 4750.000000)	7.183837	17.1366	65.7269
UN2CAPACITOR218PA0	SURFACE	(2375.000000, 4750.000000)	(2375.000000, 4757.183837)	7.183837	17.1366	65.7269

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Warnings

Number of Warnings: 2304
Warning Points: Click to Hide

Table sorted by: Impedance Deviation Percentage
(Switch to sort by Net)
(Switch to sort by Length)

Net	Layer	Start Point (mils)	End Point (mils)	Length (mils)	Impedance (ohms)	Impedance Deviation (%)
UN17ACT257243PY10	L5	(5420.000000, 2770.000000)	(5580.317632, 2770.000000)	160.317632	59.9876	19.9751
UN17ACT257243PY10	L5	(5583.202522, 2770.000000)	(5630.207040, 2770.000000)	47.004518	59.9876	19.9751
UN17ACT257243PY10	L5	(5630.207040, 2770.000000)	(5633.191724, 2770.000000)	2.984684	59.9876	19.9751
UN17ACT257243PY10	L5	(5633.191724, 2770.000000)	(5720.316769, 2770.000000)	87.125045	59.9876	19.9751
UN17ACT257243PY10	L5	(5720.316769, 2770.000000)	(5723.201659, 2770.000000)	2.884891	59.9876	19.9751
UN17ACT257243PY10	L5	(5723.201659, 2770.000000)	(5770.000000, 2770.000000)	46.798341	59.9876	19.9751
UN17ACT257243PY10	L5	(5775.000000, 2770.000000)	(5915.000000, 2770.000000)	140.000000	59.9876	19.9751
WMHF__MTHF_N	L5	(2560.000000, 3670.000000)	(2927.500000, 3670.000000)	367.500000	59.9876	19.9751
UN17ACT257243PY10	L5	(5581.040787, 2770.000000)	(5583.202522, 2770.000000)	2.161736	59.9875	19.975

The **Table sorted by** field describes how Violations and Warnings are sorted. By default, both are sorted by deviation percentage. Use the **Switch to sort...** links to change this to sort by Net, Length, or back to Deviation.

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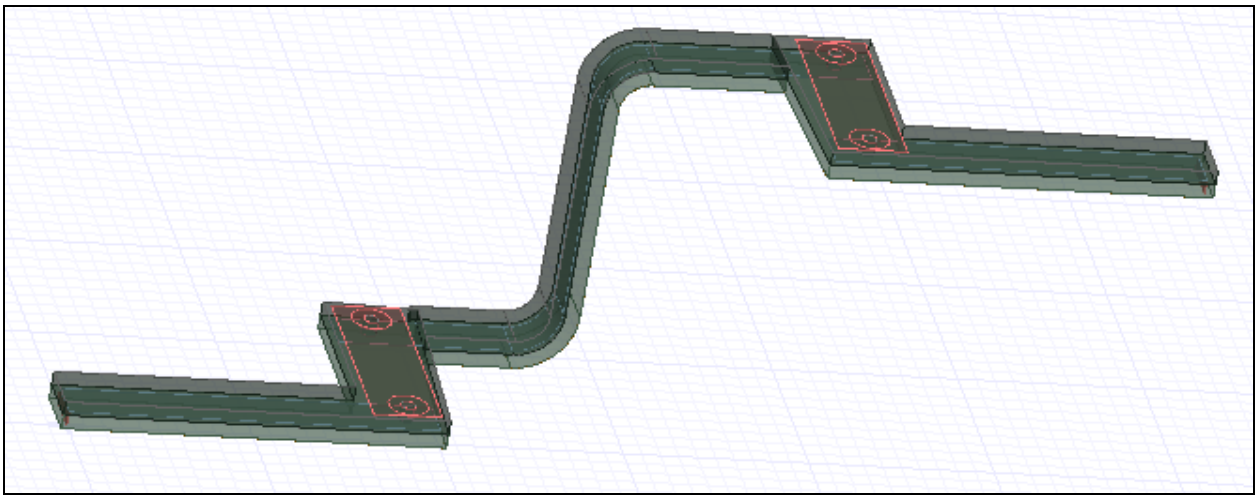
Computing Designs With Rigid-Flex Bends

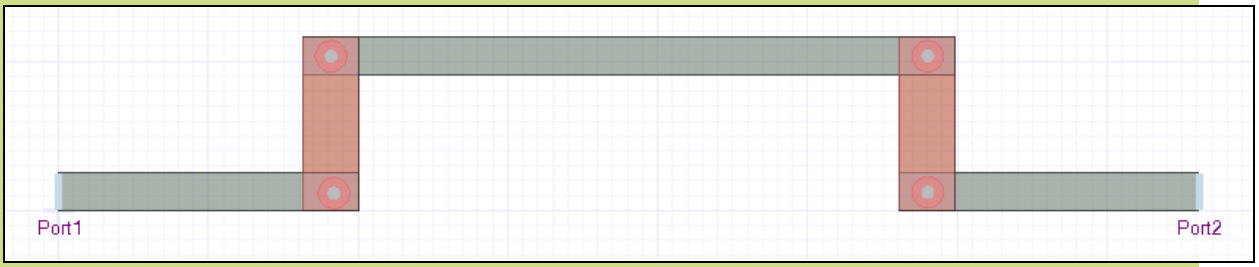


PCB Designs created with rigid-flex bends can be imported and simulated in SIwave with the following caveats:

- Attempting to simulate a design with overlapping metal layers will result in an error. Refer to the HFSS 3D Layout Help topic about Defining Zones.
- Dielectric layers that overlap across zones need to be subdivided into layers of matching thickness. Refer to the HFSS 3D Layout Help topic about Editing Zones.
- Zone boundaries and stackups can **not** be modified within individual zones. However, layer materials and thicknesses can be edited in bulk using the **Layer Stackup Editor**. Refer to Editing Layer Properties.
- Currently, support for rigid-flex bends does **not** extend to CPA or PSI simulations.

Note:

SIwave is **not** a 3D solver. Designs with rigid-flex bends are simulated in their flat state.



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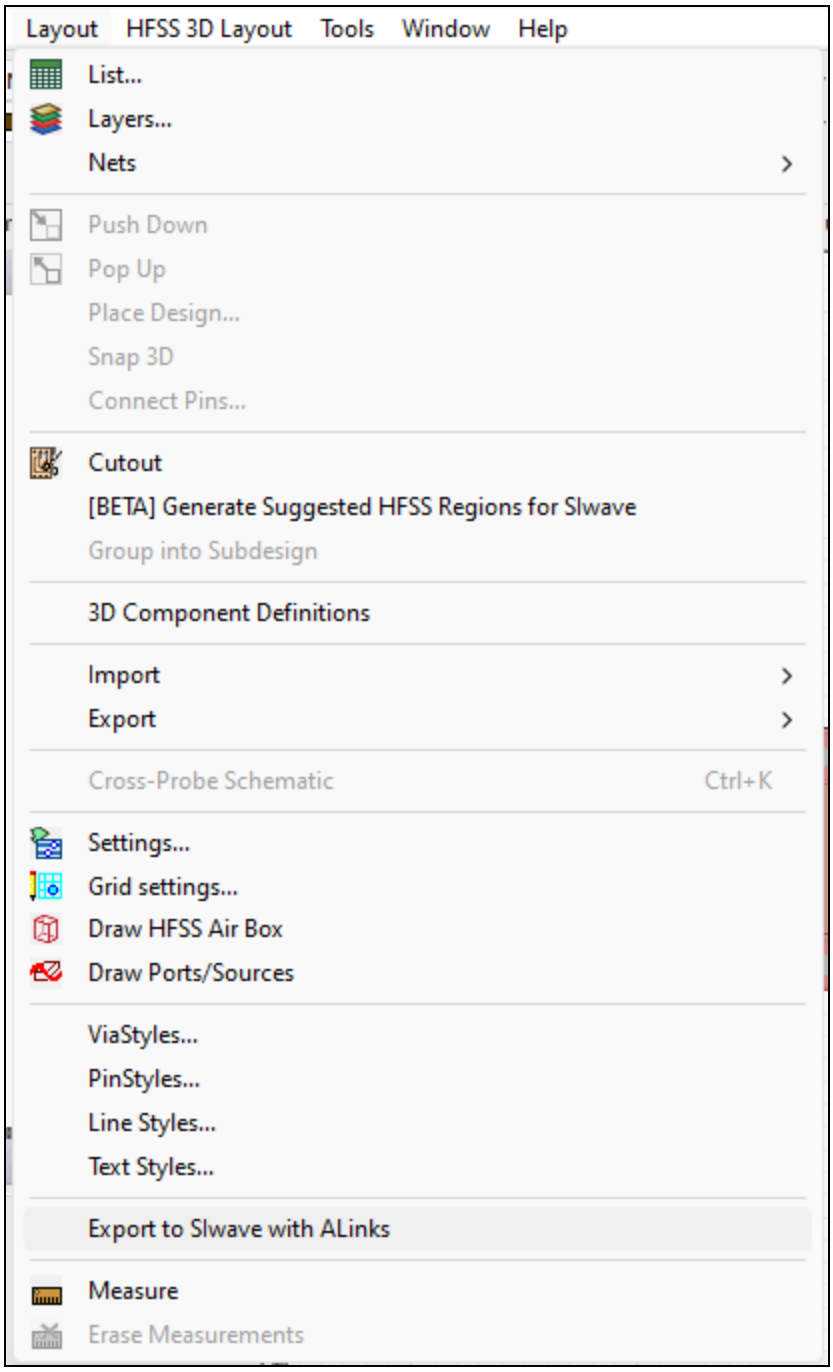
Importing a Design With Rigid-Flex Bends

Complete the following steps to import a PCB design with rigid-flex bends from HFSS 3D Layout.

1. From **Electronics Desktop**, navigate to **Layout** and select **Export to SIwave with ALinks**.



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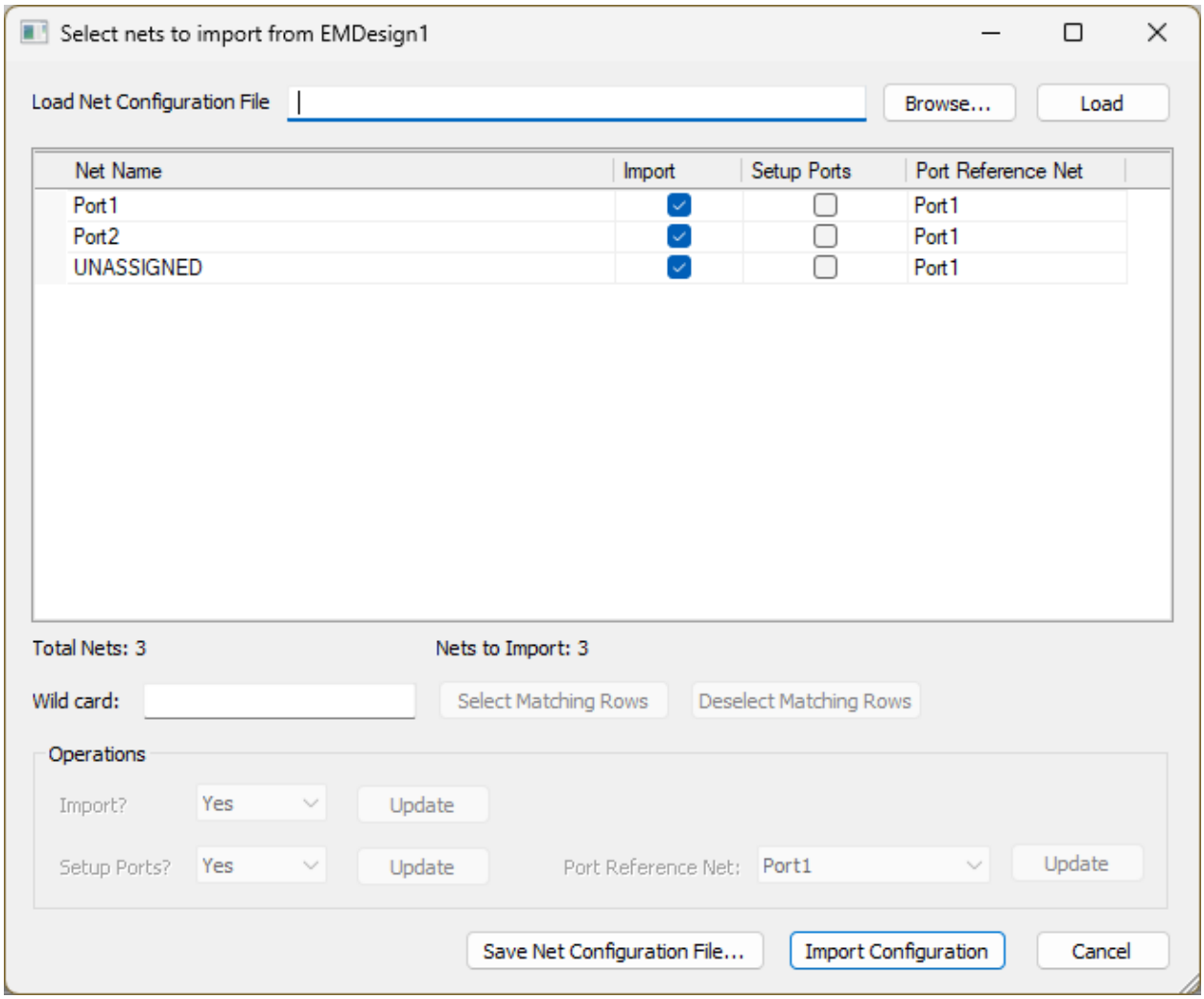
The **SIwave** splash screen will open. Wait for the new instance of **SIwave** to load.

When SIwave opens, the **Select nets to import from EMDesign*N*** window will also open.



2. If appropriate, load a net configuration file by doing the following:
   a. Click **Browse**, adjacent to **Load Net Configuration File** to open an explorer window.
   b. Navigate to an SIwave net configuration file.
   c. Select the file and click Open to return to the **Select nets to import from EMDesign*N*** window.
   d. Click **Load**.
3. Check/uncheck boxes in the **Import** column to select which nets to import. All nets are imported by default.

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4. If appropriate, enter characters for a **Wild card** search in the adjacent field. Then click **Select Matching Rows**/**Deselect Matching Rows**, as required.
5. Click **Save Net Configuration File** to open an explorer window. Navigate to an appropriate directory and **Save** the net configuration file in ***.ncf** format.
6. Click **Import Configuration**.

Running the PI Advisor

The primary goal of the SIwave PI Advisor is to find a set of decoupling capacitor assignments that satisfy the impedance mask specified by users at minimum cost. With the PI Advisor, the user can impose various constraints on the optimization problem (e.g., the total number of capacitors, types of caps, and total dollar cost). Typical constraints imposed during simulation include capacitor price, total number of capacitors, appropriate network impedance, types of capacitors and capacitor placement. Constraints are incorporated into the overall cost function as a weighted penalty.

The PI Advisor performs an analysis on the design geometry along with any capacitors selected for optimization, producing several solutions or schemes, each of which seeks to optimize the trade-off between capacitor cost and design performance. Solutions are listed by quality, price, the total number of capacitors, and the number of different types of capacitors used to achieve the designated impedance profile. The PI Advisor is also able to compute and display the loop inductance associated with the mounting locations of each of the capacitors selected for optimization.

With the PI Advisor, users can perform two sets of analysis. A simple lumped analysis functions as a pre-layout simulation, providing users with a quick calculation for determining capacitor values and placement within user-defined regions. Based on the user-defined impedance mask, the analysis determines the lumped circuit equivalent of all the capacitors on a board or package and can be used to develop the best candidate capacitors for a design. The analysis automatically determines the best type and number of capacitors given a frequency-dependent impedance mask. The built-in capacitor library browser provides an intuitive interface for selecting and analyzing various capacitors in the vendor-provided library. All capacitor models have been provided by the manufacturer and are represented as touchstone models.

The most accurate simulation involves the presence of a printed circuit board or package, and utilizes accurate frequency dependent capacitor models (i.e., the touchstone models) in a post-layout simulation. The impact of the capacitor's physical location and mounting technique are captured by the full-wave SIwave extraction engine. Multiple bill of materials (i.e., BOM) schemes are available and can be applied to a final PCB or package design. PI Advisor can perform loop inductance analyses and plot 3-D bar graphs representing loop inductance values per each capacitor in a user-defined region, giving an immediate, intuitive understanding of each capacitor's effectiveness.

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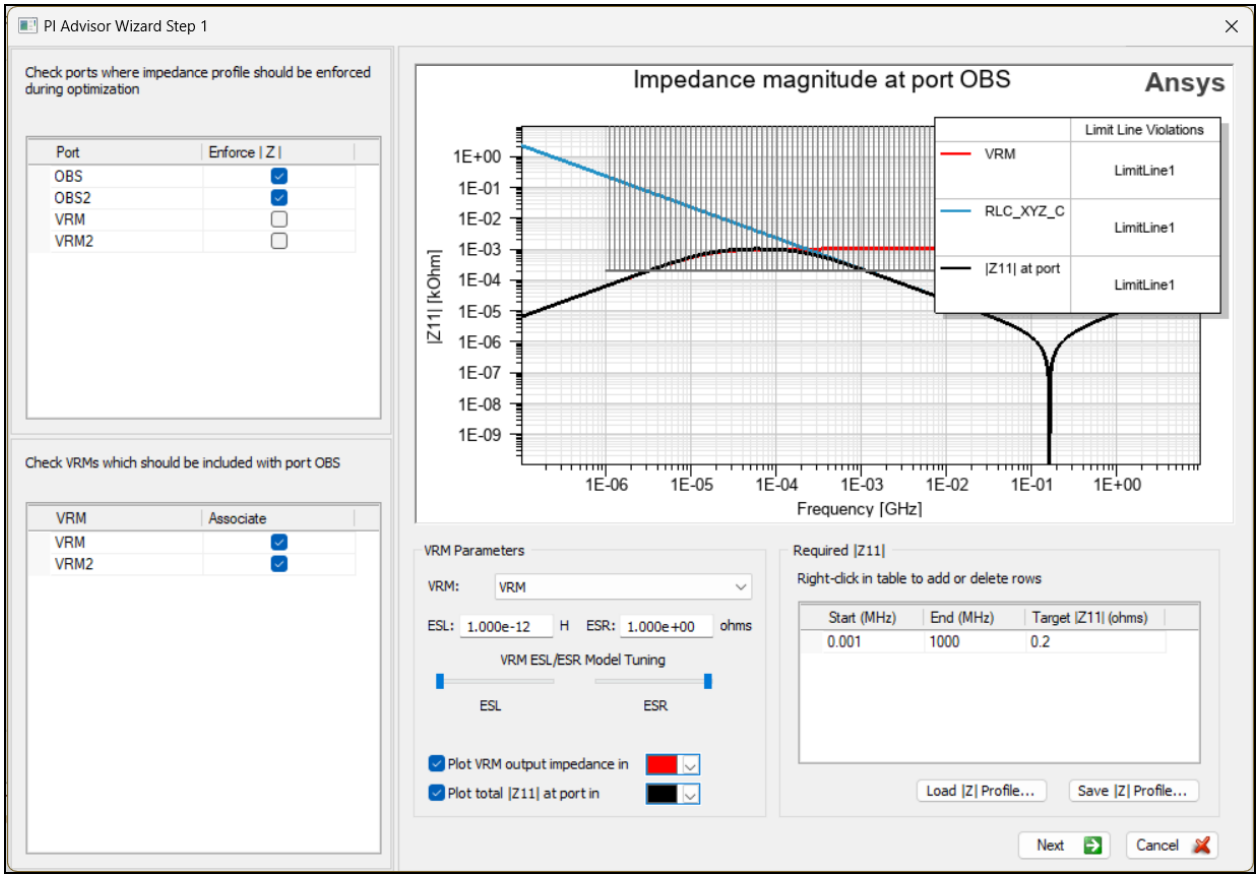
Note:

A new AnsPlot plotting tool is running in PI Advisor-related graphs, as well as in the Capacitor/Inductor Library Browser. The previous plotting tool (i.e., pre-2024 R2) ensured only specific curves could trigger a visual indication of a violation. The new tool does not allow individual curves to be excluded from indicating violations. However, selecting a curve on the legend or in the graph now provides a visual representation of any violations the curve is responsible for. To use the previous plotting tool, create a `USE_ANSPLOT_FOR_PI_ADVISOR` environment variable set to **0** and restart SIwave.

Complete these steps to run the PI Advisor wizard.

1. Navigate to the **Simulation** tab and click **PI Advisor** to open the **PI Advisor Wizard Step 1** window.



2. From the top-left table, check the boxes adjacent to any/all **Ports** to **Enforce** an impedance profile. The impedance curves and mask present in the impedance magnitude graph will change accordingly.

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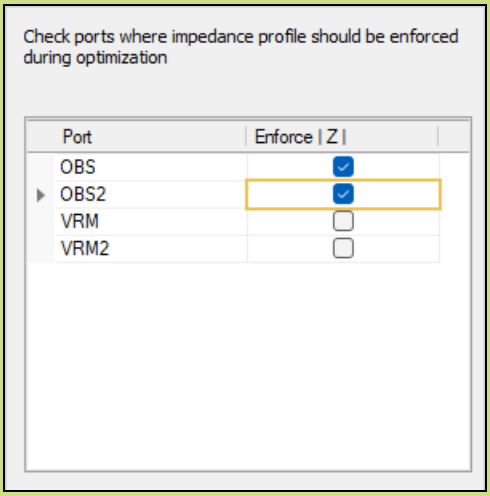
Note:

Variables changed in steps **3-7** will affect the currently selected port (i.e., the port with a yellow square wrapping the checkbox field). Different selections may be made for different ports



3. After selecting one or more ports (e.g., **OBS** and **OBS2**), use the bottom-left table to check any VRM box(es) that should be included with the port(s) (e.g., **VRM** and **VRM2**).
4. From the **VRM Parameters** area, select a port from the drop-down menu (e.g., **VRM**) and define its ESL/ESR parameters by either entering values or moving the sliders.
5. Hide/show the curves shown in the graph or change their color by checking **Plot VRM output impedance in** and/or **Plot total |Z11| at port in** and selecting new colors from the drop-down menus.
6. From the **Required |Z11|** area, complete these steps to create an impedance profile and change the impedance mask:
   a. **Load** or **Save** a |Z| profile.
   b. Right-click within the table, then click **Add Row**.

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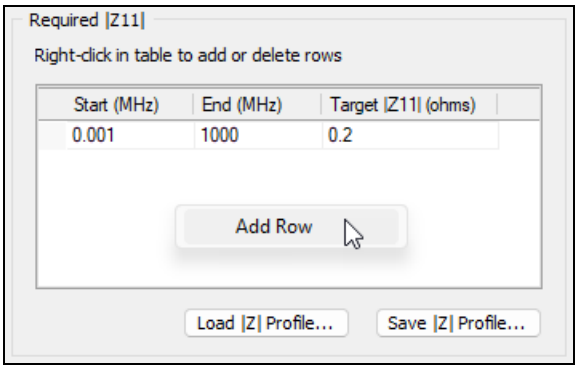

c. Enter new values in the **Start**, **End**, and **Target** fields.

d. Repeat steps **b-c**, as necessary. The impedance magnitude graph updates each time a field is modified.

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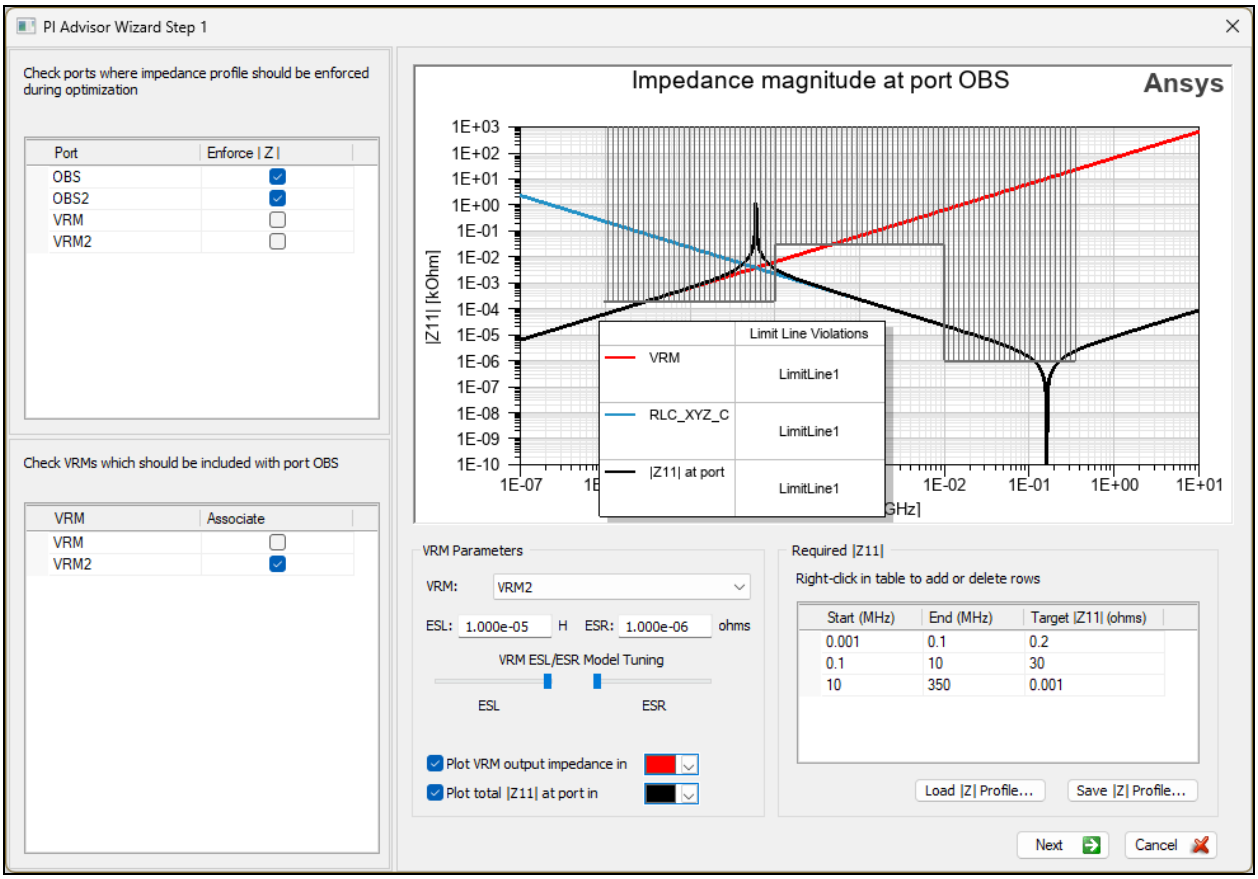

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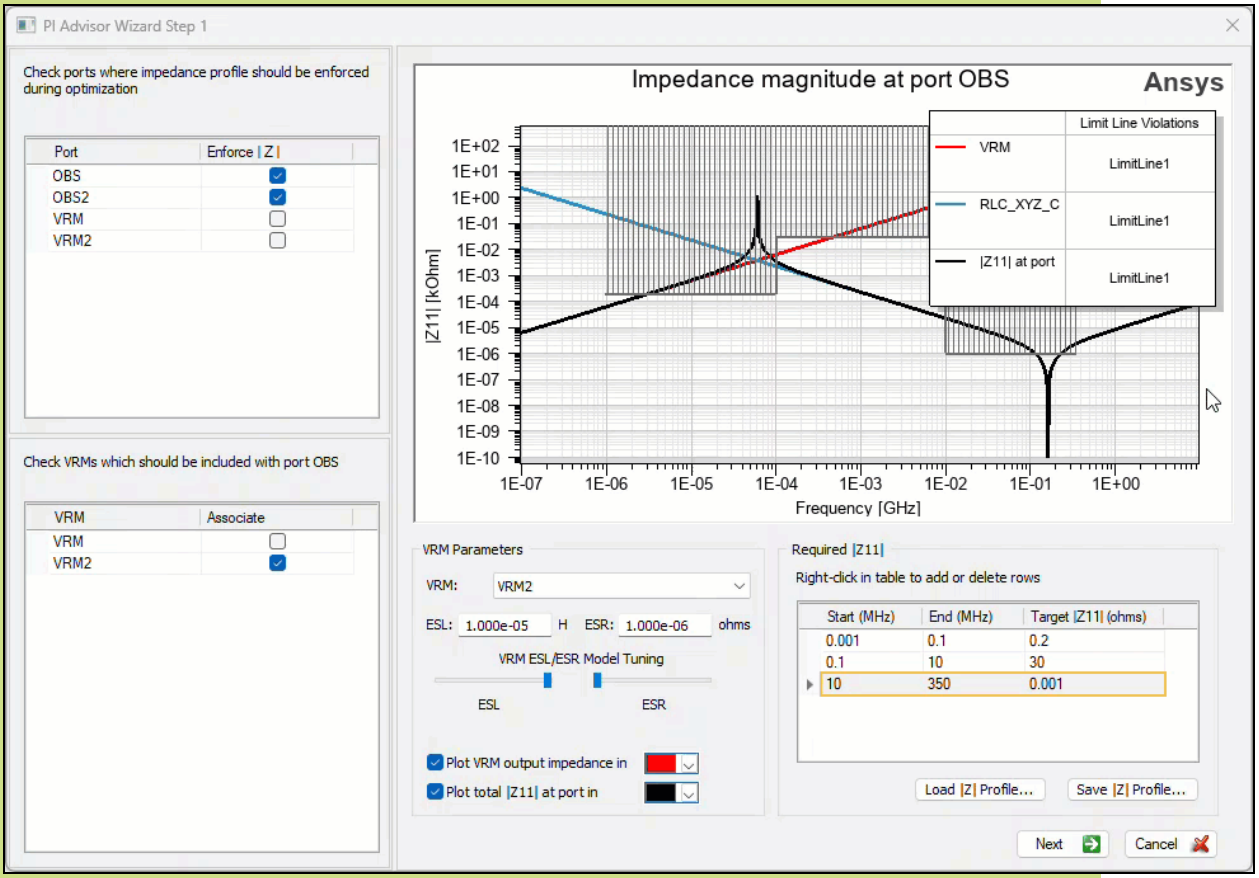
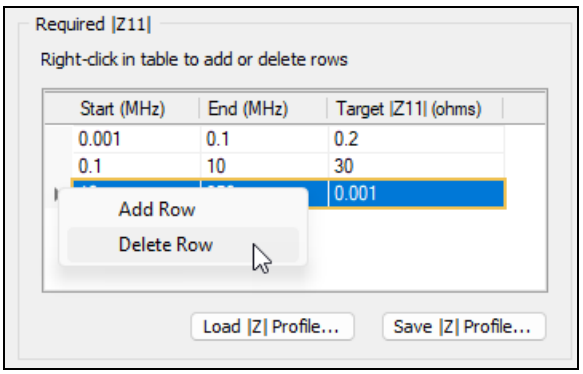
Note:

Click+drag the legend within the impedance magnitude table to move it to a more convenient location.



e. To delete a row, right-click in the blank cell left of the row and select **Delete Row**.



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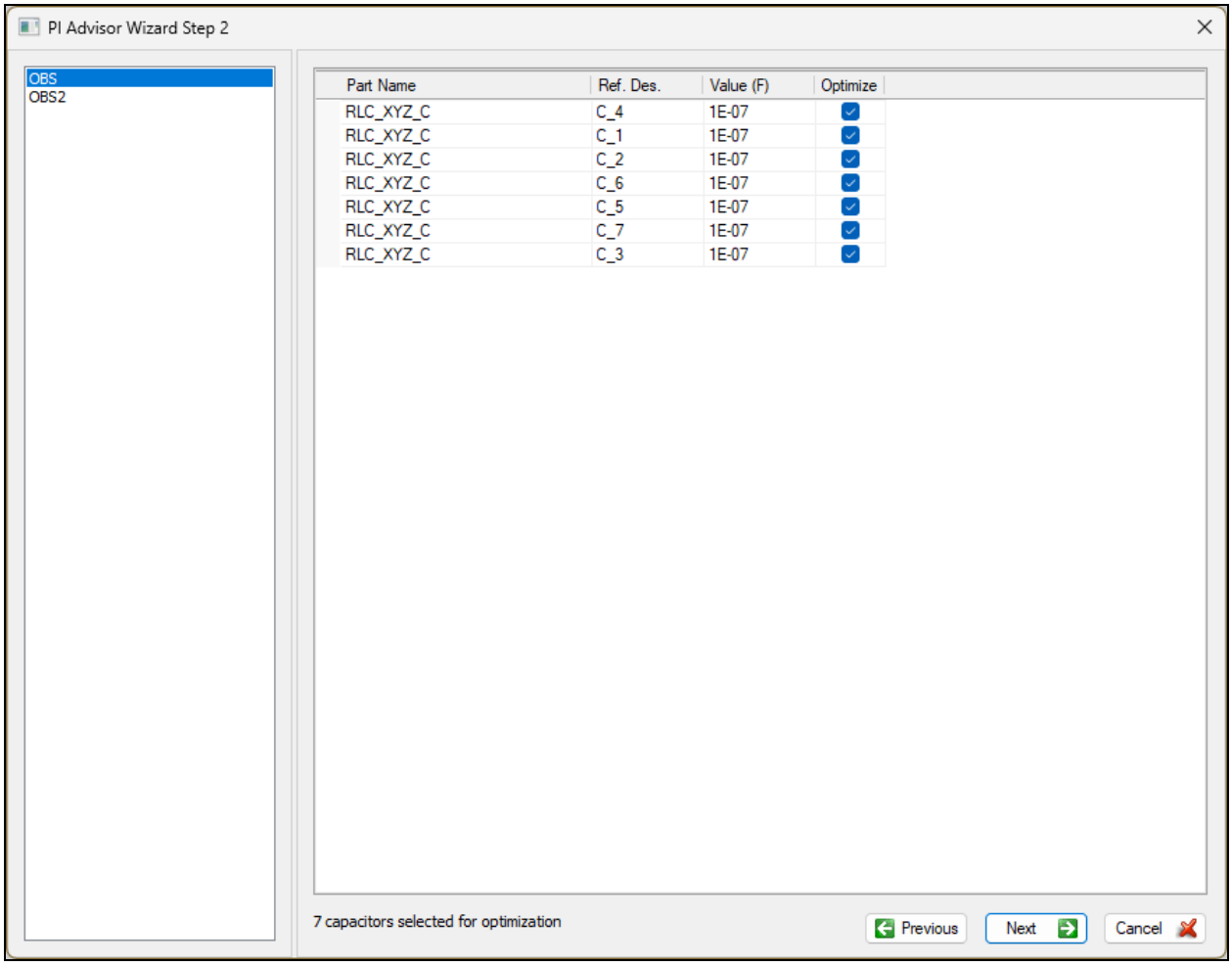
7. Click **Next** to open the **PI Advisor Wizard Step 2** window.



8. Check the boxes adjacent to one or more capacitors to select them for optimization.

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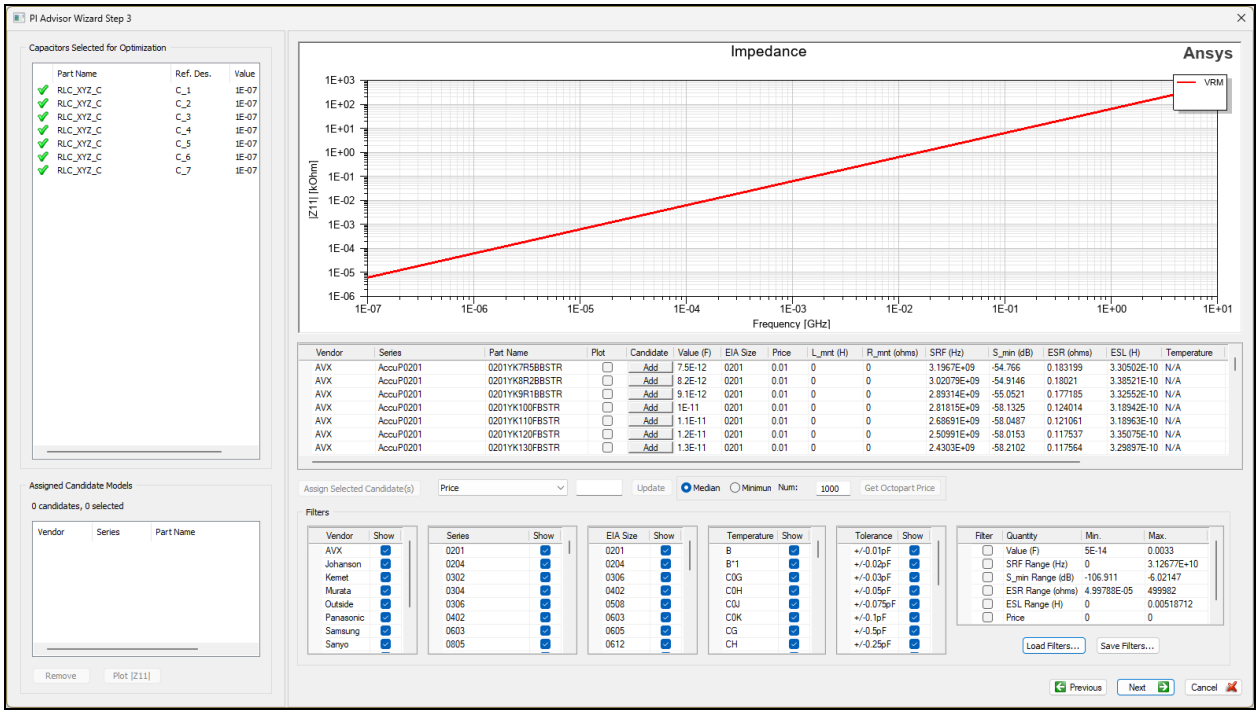
9. Click **Next** to open the **PI Advisor Wizard Step 3** window.



10. From the **Capacitors Selected for Optimization** area, select from among the capacitors chosen in step 8.
11. **Plot** and **Add** candidate capacitor models for each capacitor selected from the **Capacitors Selected for Optimization** area, based on value (e.g., capacitance, self resonant frequency, ESL and/or ESR) and price. Filter the lists, as necessary. Refer to Using the Capacitor Library Browser for similar usage instructions.

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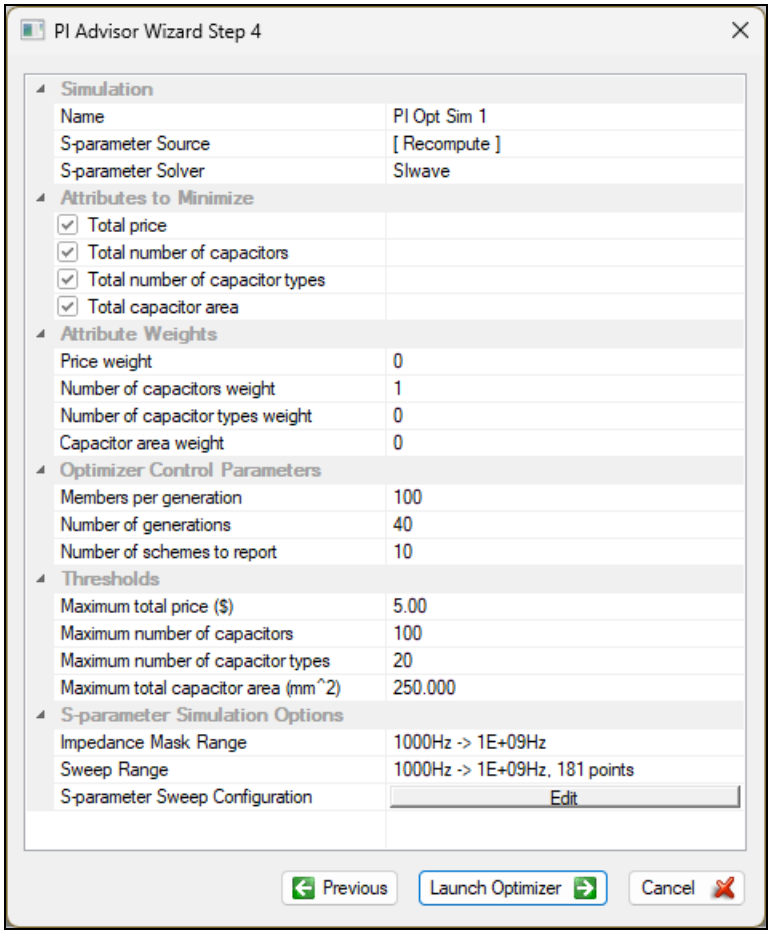
12. Click **Next** to open the **PI Advisor Wizard Step 4** window.



13. From the **Simulation** area, select either **PSI** or **SIwave** from the **S-parameter Solver** drop-down menu.

> **Note:**
>
> The PSI solver is a more accurate solver, but the simulation is slower, while the SIwave solver is faster. Refer to Running Simulations for more information.

14. From the **Attributes to Mininimize** area, check **Total price**, **Total number of capacitors**, **Total number of capacitor types**, and/or **Total capacitor area**.
15. From the **Optimizer Control Parameters** area, update the associated values, as appropriate. The PI Advisor optimizer generates a population of trial designs with the given number of members. Initially, only **1** decoupling capacitor is assigned, but through a series of generations (i.e., schemes), more capacitors are added. The optimizer tracks the quality of the members based on the optimization goals and impedance targets. When all generations are completed, the optimizer returns the best member designs.

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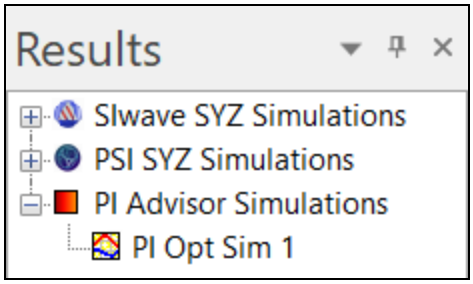
Members per generation — the number of different designs (i.e., members) the optimizer simultaneously generates, from one scheme to the next. Increasing this number may improve the quality of the final result at the expense of computation time, since there will be a larger population of designs to choose from.

Number of generations — how many schemes are run. The optimized designs will contain a maximum number of capacitors equal to this set value. Optimized designs may have fewer capacitors, if the optimizer concludes additional capacitors will not help meet goals.

Number of schemes to report — how many schemes are finally returned.

> **Note:**
>
> A quality metric of **1** is the ideal final outcome. **1** indicates all goals are met. An integer less than **1** indicates some violations of the impedance goals remain. Having more members and schemes helps explore a larger potential design space, usually leading to a better final result, but at the expense of longer run time.

16. From the **Thresholds** area, update the values in the **Maximum total price**, **Maximum number of capacitors**, **Maximum number of capacitor types**, and/or **Maximum total capacitor area** fields.
17. Click **Launch Optimizer** and wait for optimization to complete.
18. From the **Results** window, expand **PI Advisor Simulations** and double-click the new simulation results (e.g., **PI Opt Sim 1**) to open the **Optimization Results** window.



19. From the **Optimization Results** window, select one or more schemes from the **Scheme** area, then click **Apply Scheme to Design**. Each scheme contains information about the capacitors selected for the scheme, such as the number of capacitor types used and the total cost. An impedance plot will appear for each port based on the capacitors used.

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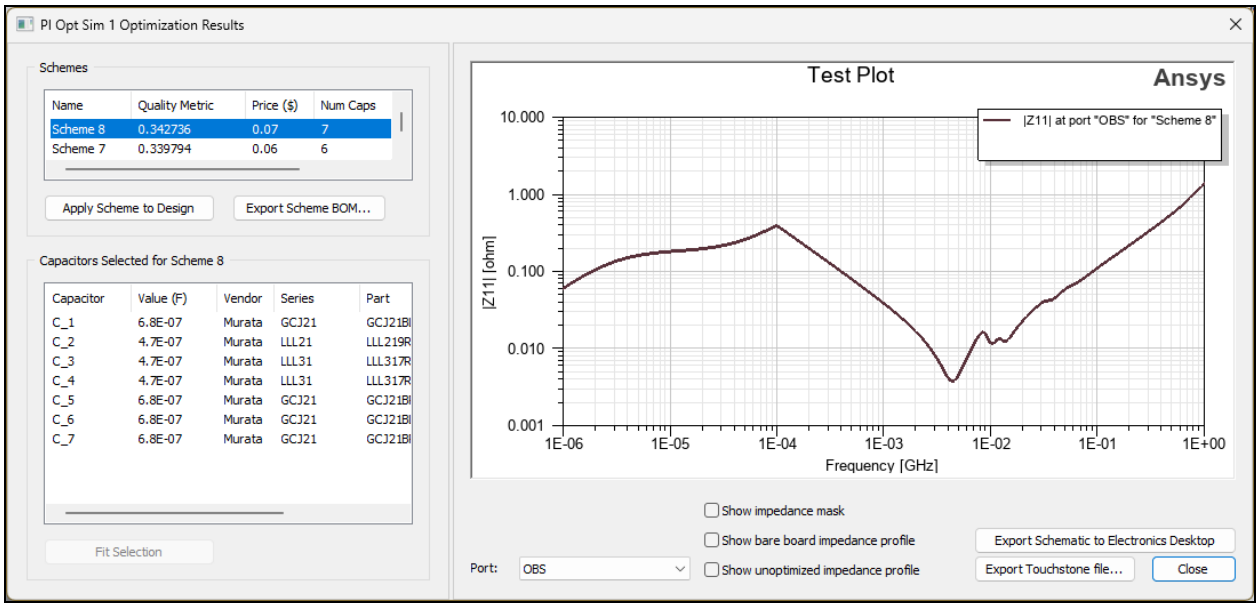

20. Select another **Port** from the drop-down menu to view to view its associated plot.
21. If necessary, check any/all of the following boxes:
    - **Show impedance mask** — displays an impedance mask overlaying the plot
    - **Show bare board impedance profile** — displays the bare board (i.e., all capacitors removed) impedance profile
    - **Show unoptimized impedance profile** — displays an unoptimized (i.e., the board with the default capacitor assignment) impedance profile
22. If necessary, click **Export Schematic to Electronics Desktop**. Refer to Exporting a Scheme as a Schematic.
23. If necessary, click **Export Touchstone file** to open an explorer window. Navigate to an

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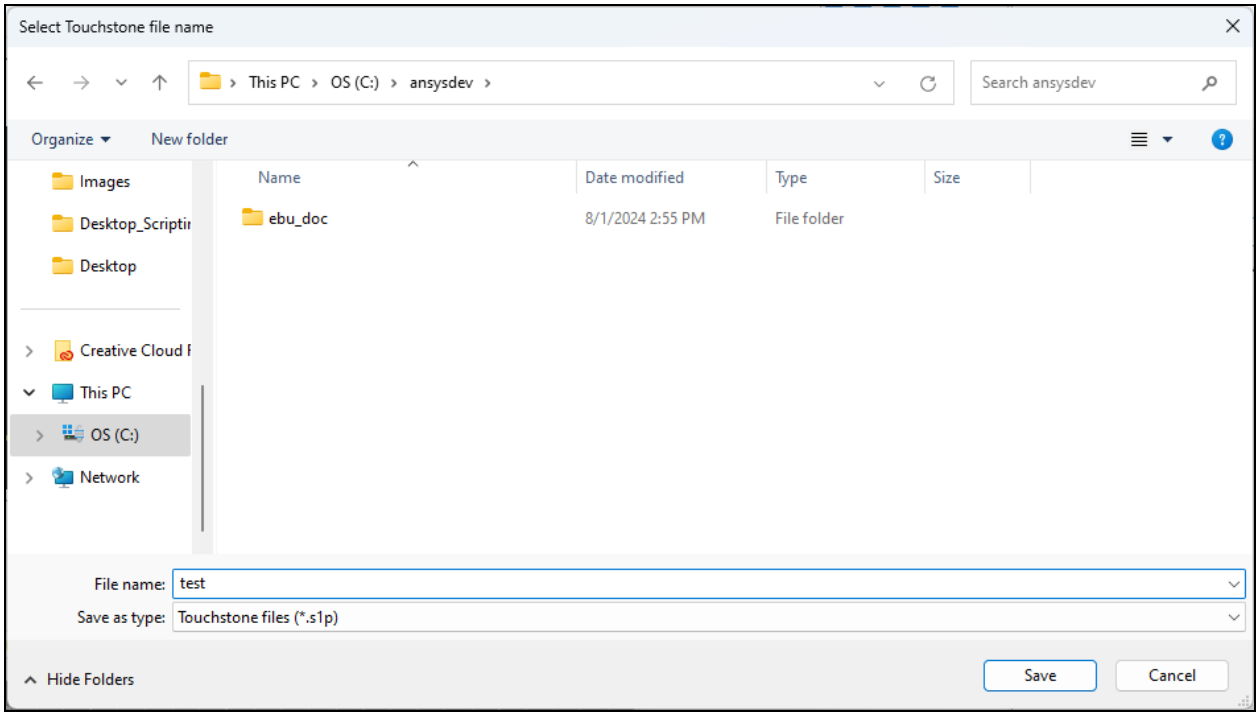
appropriate directory, then enter a **File name** and **Save** the new file.



24. To view the loop inductance between each port/capacitor, from the **Results** window, right-click **PI Opt Sim 1** and select **Export Loop Inductance Table**.

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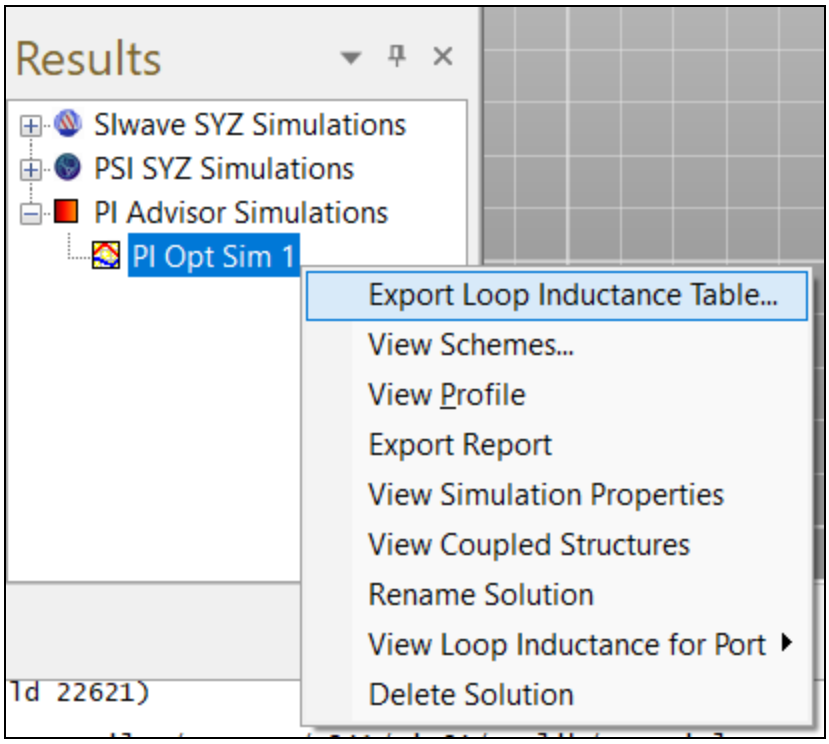

Exporting a PI Advisor Simulation Report

Users can export an HTML report containing the simulation results, including schemes, impedance plots, and loop inductance. Complete these steps to view a **PI Advisor Simulation Report**.

1. From the **Results** window, right-click the simulation results and select **Export Report** to open an explorer window.

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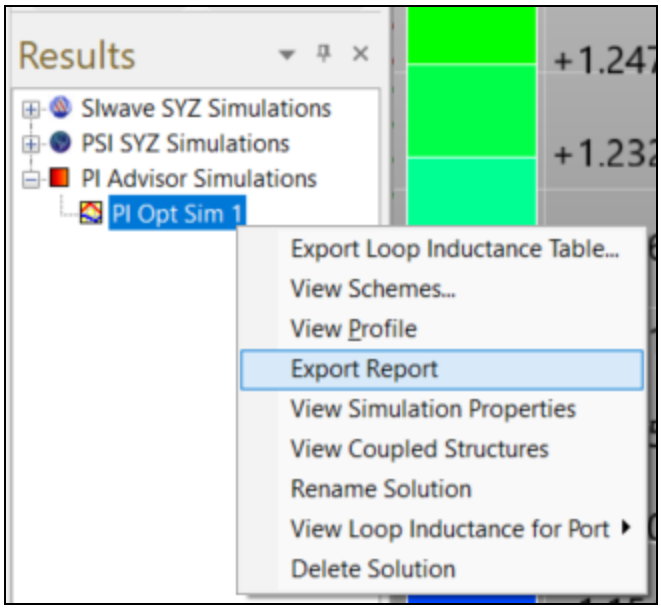
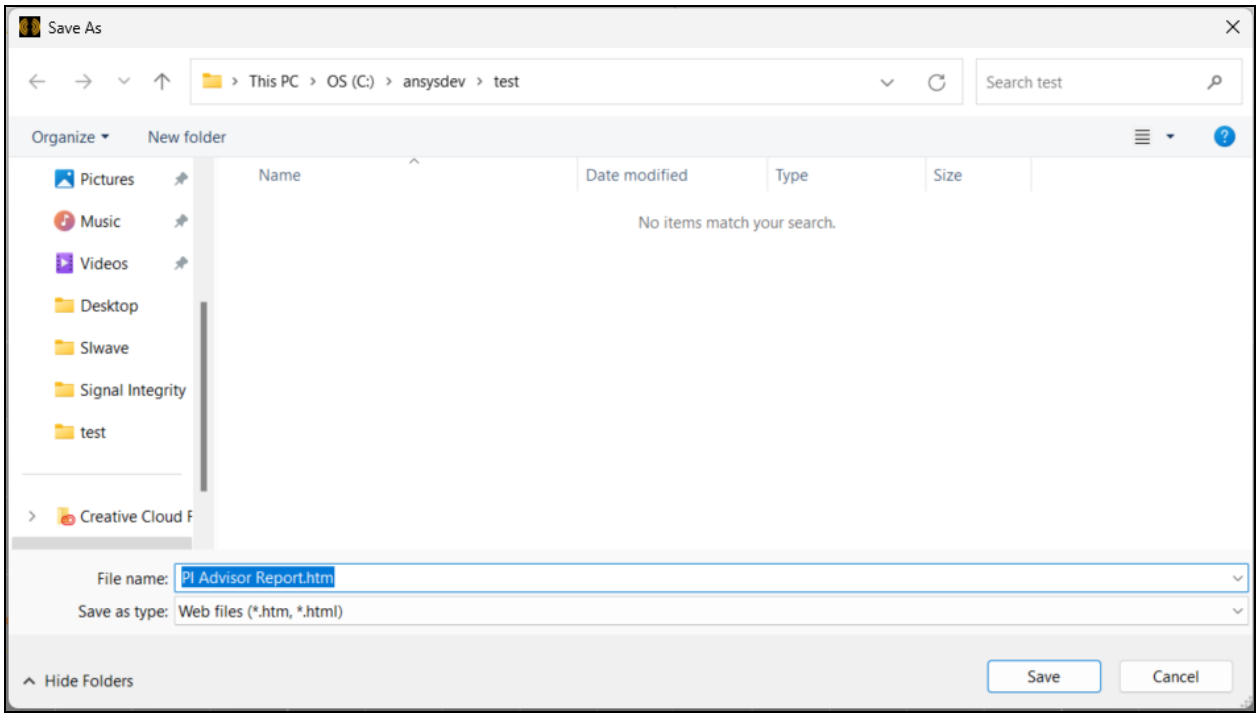


2. From the explorer window, navigate to an appropriate directory to save the report *.htm file. Then give the report a **File name** and click **Save**.



The report opens in the system's default browser. The report contains the software version, date of its creation, file and simulation names, and a summary of schemes, which contains names, quality metrics, prices, the number of capacitors, and capacitor types.

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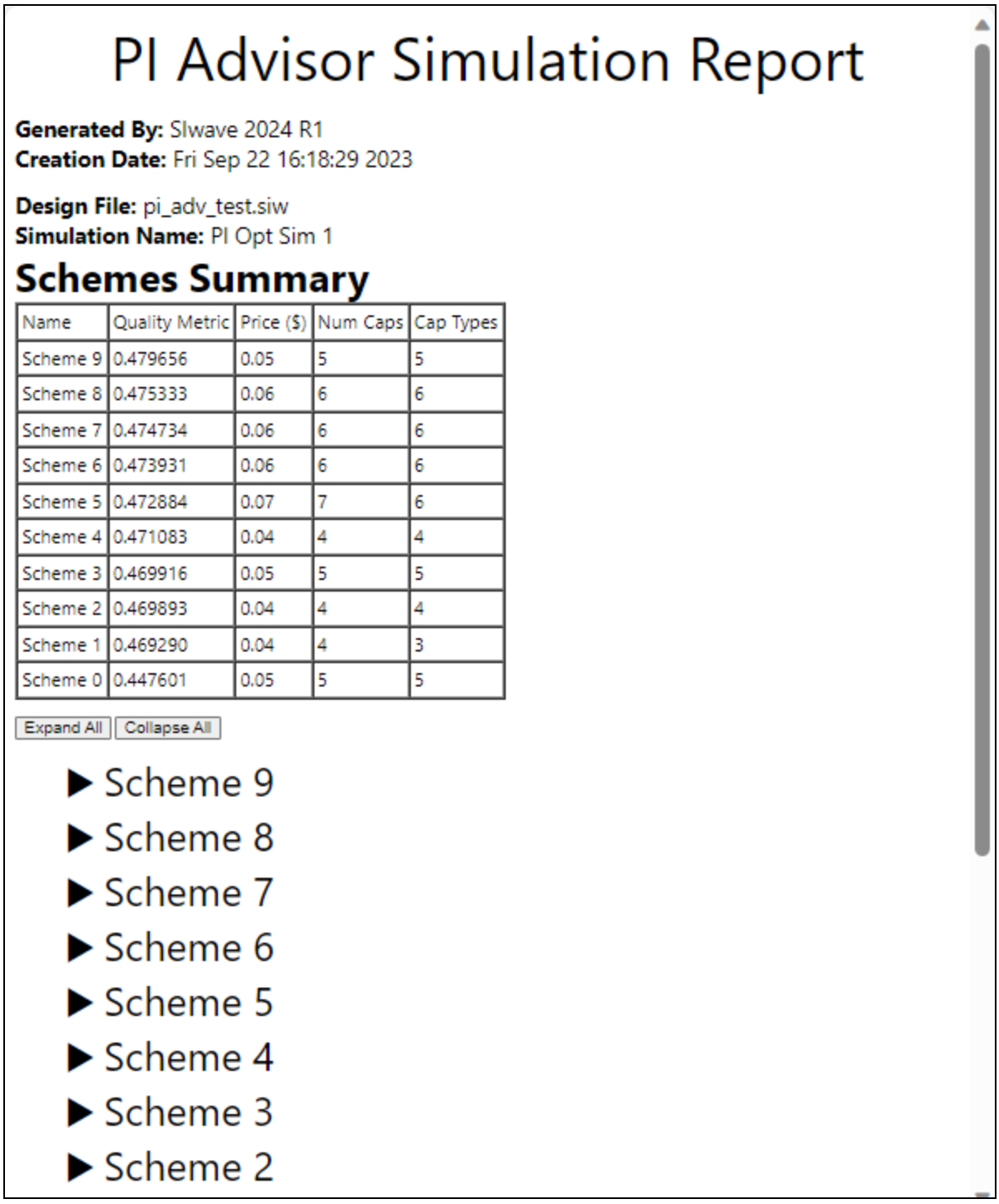

PI Advisor Simulation Report

Generated By: SIwave 2024 R1
Creation Date: Fri Sep 22 16:18:29 2023

Design File: pi_adv_test.siw
Simulation Name: PI Opt Sim 1

Schemes Summary

Name	Quality Metric	Price ($)	Num Caps	Cap Types
Scheme 9	0.479656	0.05	5	5
Scheme 8	0.475333	0.06	6	6
Scheme 7	0.474734	0.06	6	6
Scheme 6	0.473931	0.06	6	6
Scheme 5	0.472884	0.07	7	6
Scheme 4	0.471083	0.04	4	4
Scheme 3	0.469916	0.05	5	5
Scheme 2	0.469893	0.04	4	4
Scheme 1	0.469290	0.04	4	3
Scheme 0	0.447601	0.05	5	5

Expand All | Collapse All

▶ Scheme 9
▶ Scheme 8
▶ Scheme 7
▶ Scheme 6
▶ Scheme 5
▶ Scheme 4
▶ Scheme 3
▶ Scheme 2

3. Expand each scheme to view its precise tabulated breakdown table, including specific vendor and part information, and the plotted results.

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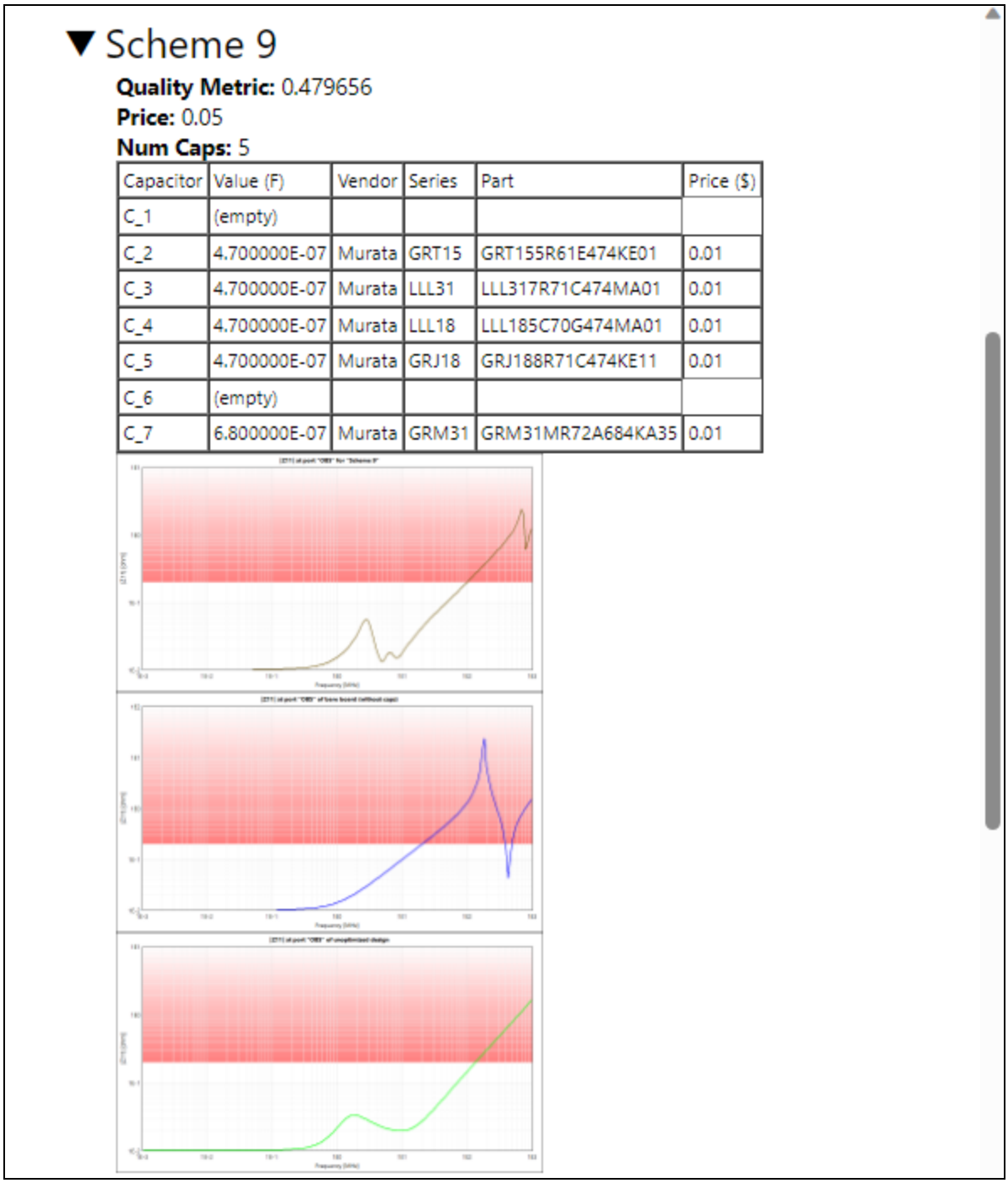

Capacitor	Value (F)	Vendor	Series	Part	Price ($)
C_1	(empty)				
C_2	4.700000E-07	Murata	GRT15	GRT155R61E474KE01	0.01
C_3	4.700000E-07	Murata	LLL31	LLL317R71C474MA01	0.01
C_4	4.700000E-07	Murata	LLL18	LLL185C70G474MA01	0.01
C_5	4.700000E-07	Murata	GRJ18	GRJ188R71C474KE11	0.01
C_6	(empty)				
C_7	6.800000E-07	Murata	GRM31	GRM31MR72A684KA35	0.01

Exporting a Scheme as a Schematic

Schemes found by the SIwave PI Advisor can be exported into **Electronics Desktop** as Circuit design schematics. During generation, an N-port component is created, with all designated ports, selected capacitors, and correct wiring, automating the process of creating a schematic

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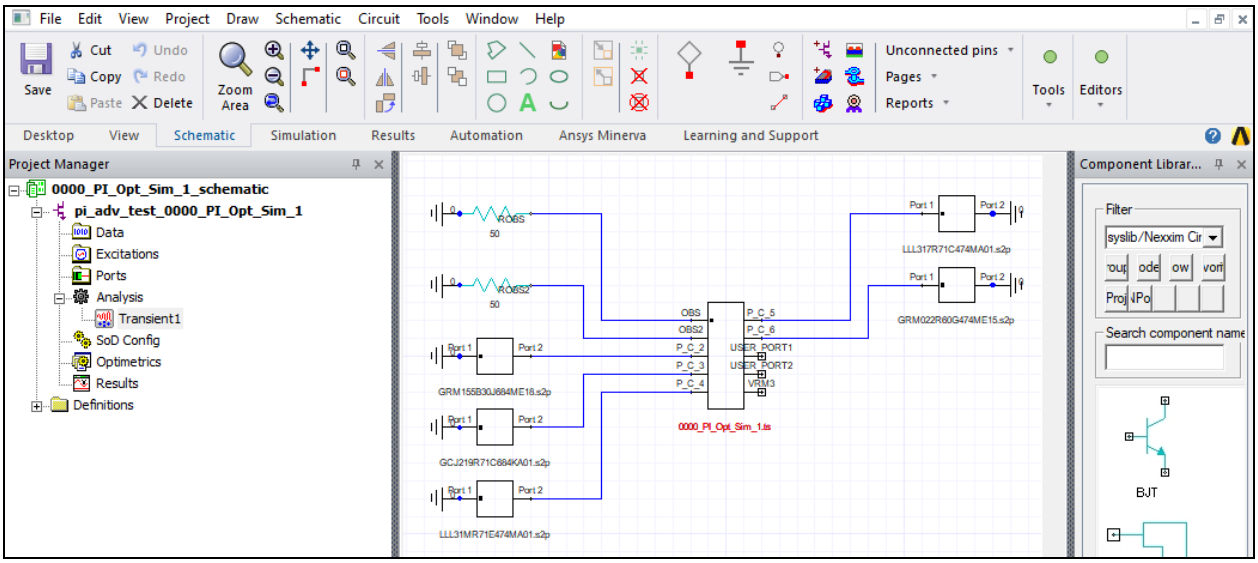
manually. To export a scheme as a schematic, click **Export Schematic to Electronics Desktop** to begin generating a schematic. **Electronics Desktop** will automatically open the schematic in the **Schematic Editor** with its components and parameters populated in the **Project Manager** window.



Keep in mind the following:

- Only one scheme can be exported at a time. If more than one scheme is selected, an error message will appear.
- The central N-port will have a port for each port in the SIwave design, as well as ports with names such as `P_<capacitor name>`, except for ports included as VRMs associated with measurement ports (i.e., observation ports) during PI Advisor setup.
- Ports associated with capacitors will be given 2-port N-ports with S-parameter models corresponding to the capacitors.
- Measurement ports and unpopulated capacitors will be connected to 50ohm resistors and grounded.
- All other port types will be left open.
- A transient analysis setup will be present in the **Project Manager** window.

Refer to the Circuit Help for more information.

Changing Port Properties

Complete these steps to estimate |Z11| at a port and view impedance curves and masks directly from the **Modeling Workspace**.

1. From the **Modeling Workspace**, click in the center of a port to populate the **Properties Workspace**.

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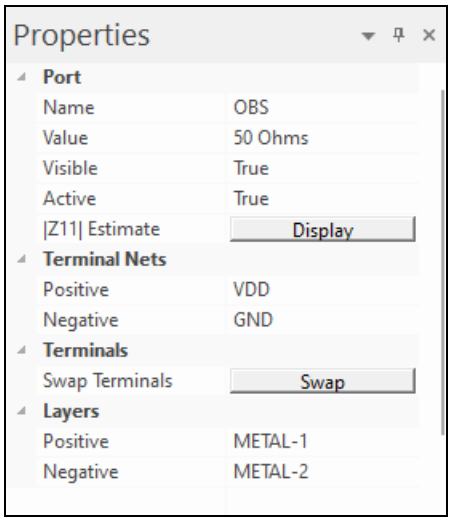

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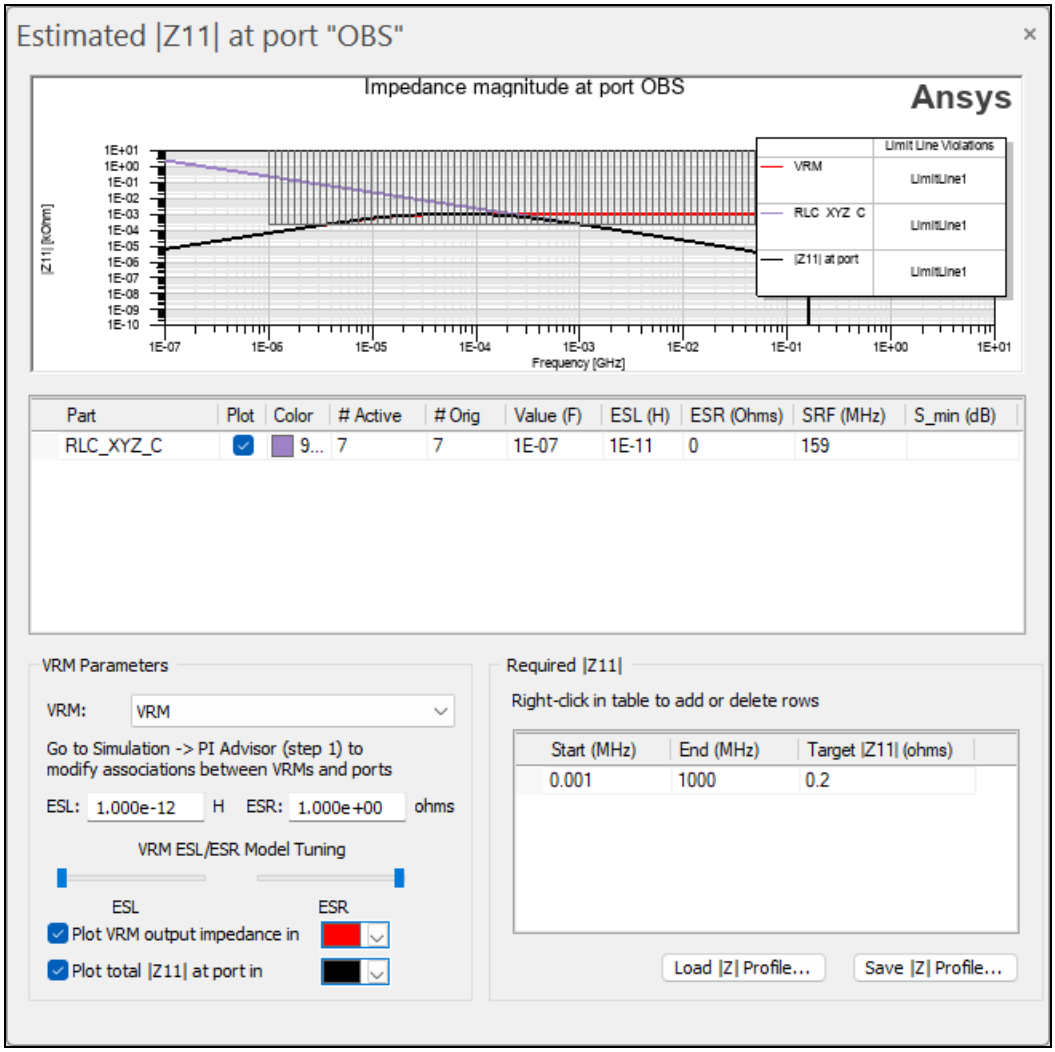
2. Next to **|Z11| Estimate**, click **Display** to open the **Estimated |Z11| at port** window.



3. The **Estimated |Z11| at port** window is functionally similar to options available at the PI Advisor Wizard - Step 1 window. Refer to steps 3-7.

PSI Simulations

The PSI solver provides fast 3D power integrity analyses, especially for packages. The PSI field solver employs meshing algorithms to solve both planar objects and 3D objects, such as vias and solderballs.

In this section, you will learn about:

- Selecting PSI Simulation Options
- Computing AC Simulations
- Computing S-,Y-, Z- Parameters

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PDN Channel Builder and PI Advisor simulations can use either the SIwave solver or the PSI solver:

- PDN Channel Builder Simulation
- PI Advisor Simulation

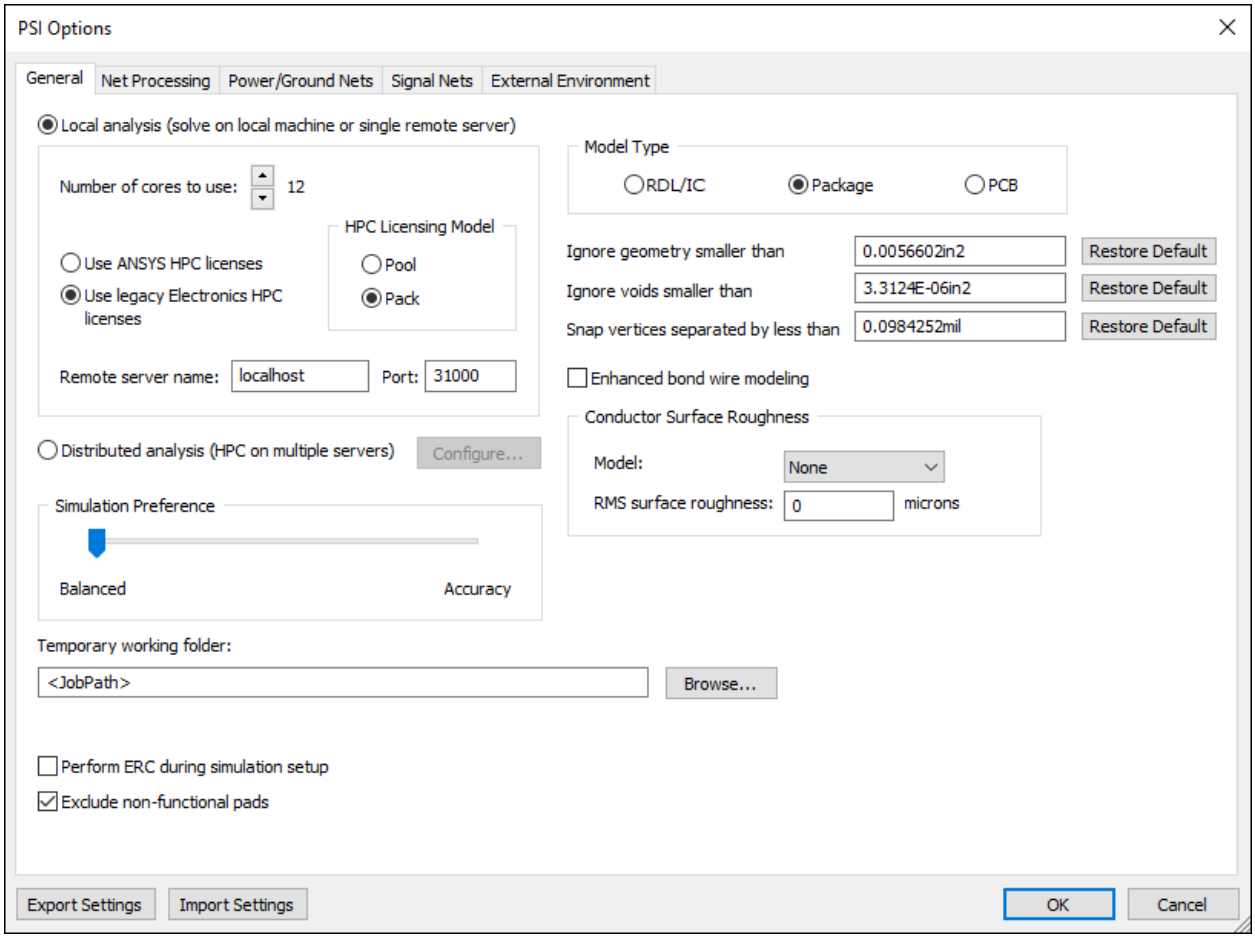
Selecting PSI Simulation Options

Some PSI parameters can be set globally for all simulation types. These global parameters include geometry options, solver settings, and mesh refinement settings.

To define the global PSI options in SIwave:

1. Click **Simulation**.
2. From the **PSI** area, click **Options**.

   The **PSI Options** window appears, on the **General** tab.



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3. Use the radio buttons to select either **Local analysis** or **Distributed analysis**. Options will gray out or become visible accordingly.

> **Note:**
>
> The option to choose a license type (either Ansys HPC or Electronics HPC) is not available when SIwave is running in Pro/Premium/Enterprise licensing mode.

   - For **Local analysis**, set the number of cores to use, licensing options, and remote server preferences.
   - For **Distributed analysis**, click **Configure** to set licensing and remote server

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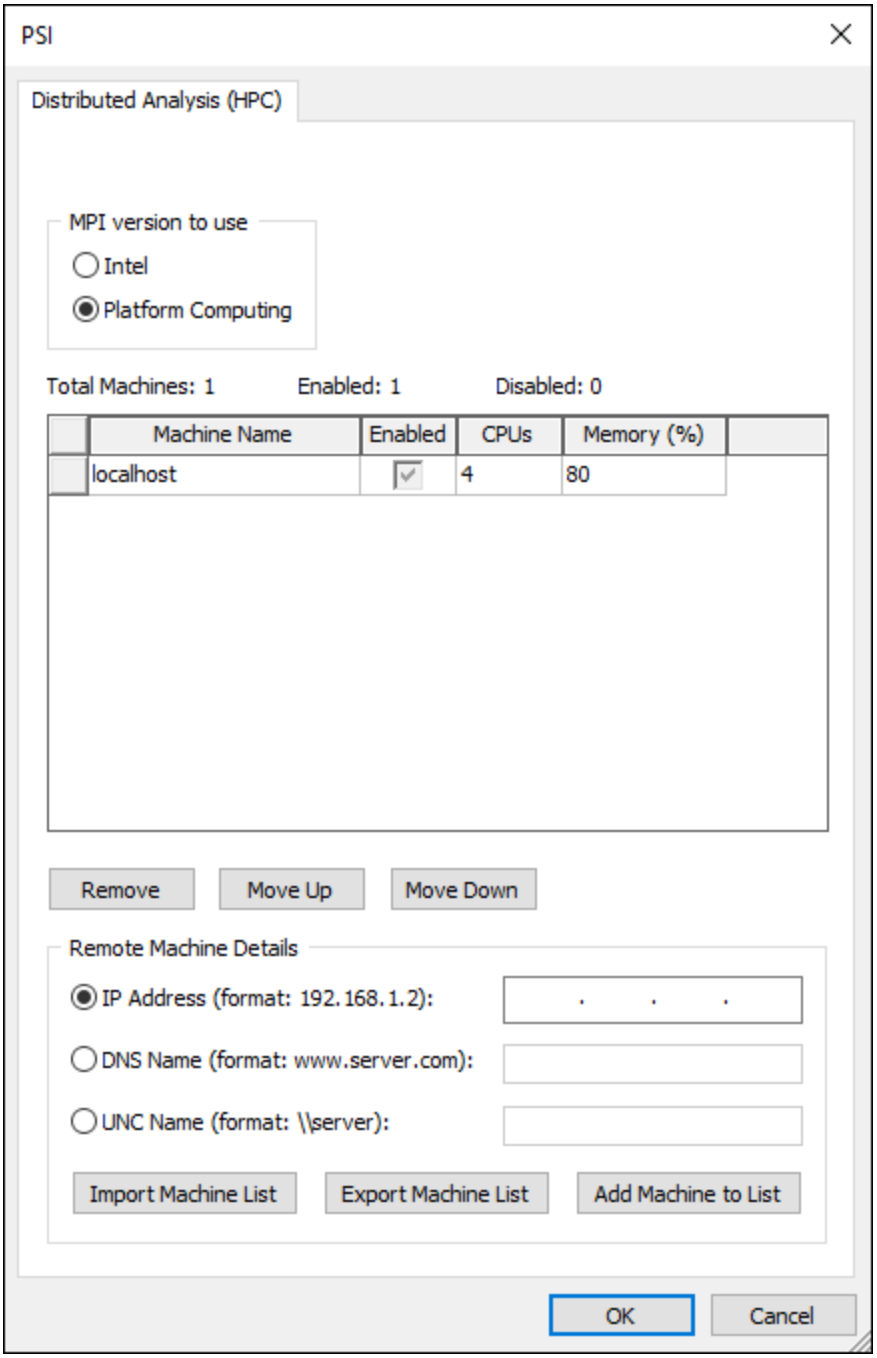
preferences:



4. Use the **Simulation Preference** slider to balance the simulation toward accuracy or speed.
5. From the **Model Type** area, use the radio buttons to select **RDL/IC**, **Package**, or **PCB**. Based on your selection, simulation parameters, such as meshing and polygon defeaturing, are automatically tuned for optimal robustness and performance.

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6. Specify the location of the **Temporary Working Folder**. To specify a temporary working folder other than the default job path, click **<JobPath>**, and enter the location, or click **Browse**.

   Temporary working files are created during analysis. These are later deleted after the analysis completes. If the job path points to the local computer, but the analysis was run on a separate server computer, then the temporary working files would transfer across the network to the local computer, thereby slowing down the simulation. Therefore, to improve the simulation run time, ensure that the analysis stores these temporary files on the computer running the application and not over the network.

7. If appropriate, check the boxes for additional options:
   - **Ignore geometry smaller than** – geometry whose area (after being combined with any overlapping geometry) falls below this specified threshold is ignored during simulation.
   - **Ignore voids smaller than** – voids whose area (after being combined with any overlapping geometry) falls below this specified threshold is ignored during simulation.

     > **Note:**
     >
     > Ansys recommends using the default settings. Refer to Advanced Geometry Processing Options.

   - **Snap vertices separated by less than** – entities (e.g., vias) and vertices that are separated by less than the distance specified in this box may be snapped together during solver pre-processing.
   - **Enhanced bond wire modeling** – models wire bonds with greater definition (this also increases run time and memory requirements).
   - **Ignore nets named "DUMMY" or "Unused" during Simulation** – uncheck this to include dummy/unused nets in the simulations. By default, all such nets are ignored.
   - **Perform ERC during simulation setup** – use to turn error checking on or off while generating the solver input file.

     In some designs, the same net may be divided into multiple nets with separate names - these nets are connected at a star point. To simulate these nets, the error checking for DC shorts needs to be turned off, and all overlapping nets are internally united during simulation.

   - **Exclude non-functional pads** – remove non-functional pads. All layers in which a via does not make an electrical connection to any other geometry do not contain a pad. By default, non-functional pads are not included in the simulation. Typically non-functional pads are removed when a PCB is manufactured.
8. Specify the **Conductor Surface Roughness** options for a better-refined conductivity calculation. See RMS Surface Roughness and Conductivity Technical Notes.

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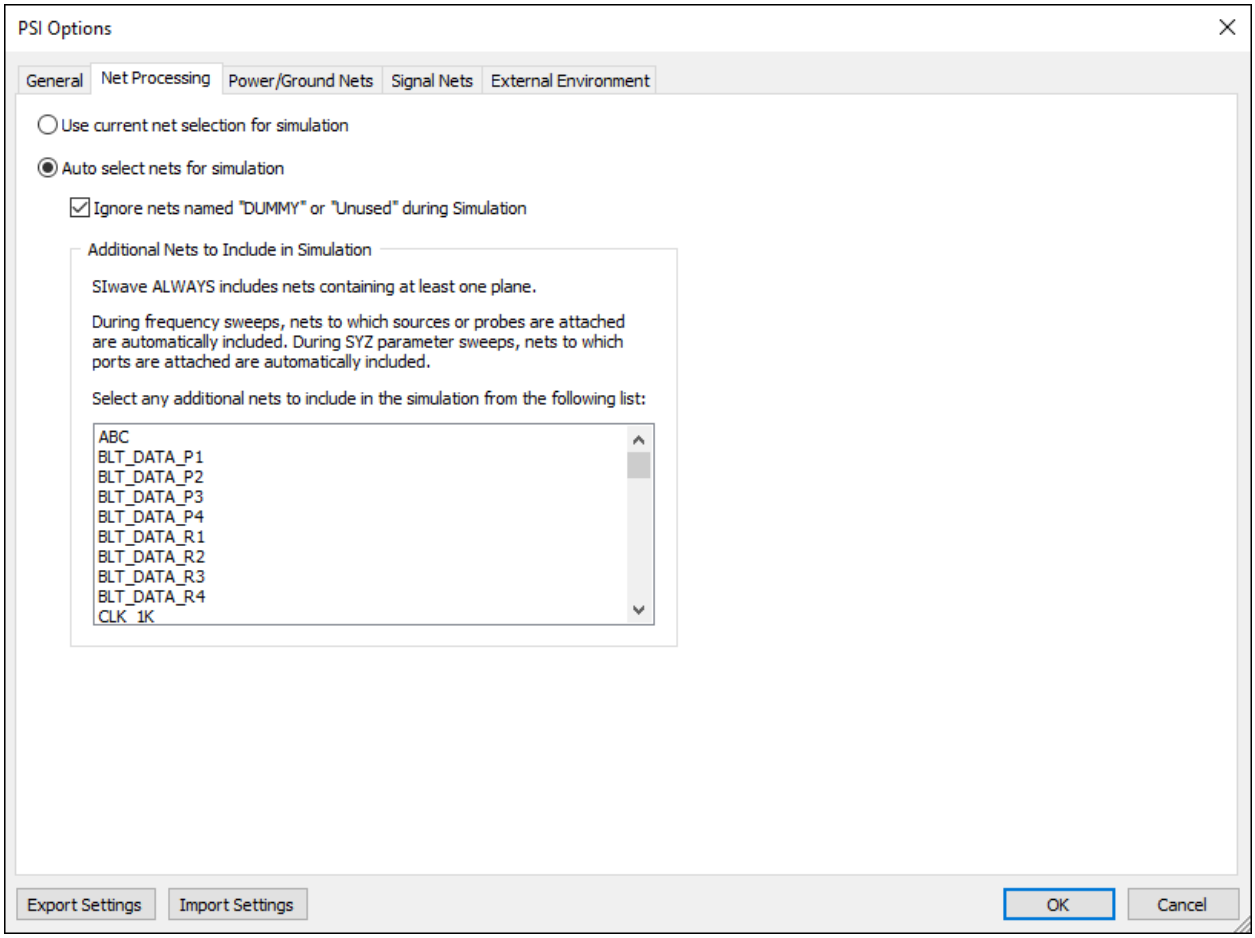
> **Note:**
>
> This option applies only when **Conductor modeling** is set to **Impedance boundary** in the **Signal Nets** tab of the **Simulation Control** window. In this case, the surface boundary condition is used and a finite-element mesh is not generated inside the metal conductor. Using the boundary condition models causes the frequency sweep to converge more slowly and increases run time.

9. Select the **Net Processing** tab.

   The **Net Processing** tab displays.



10. Use the radio buttons and list to select nets to include in your simulation.
11. Select the **Power/Ground Nets** tab.

    The **Power/Ground Nets** tab displays.

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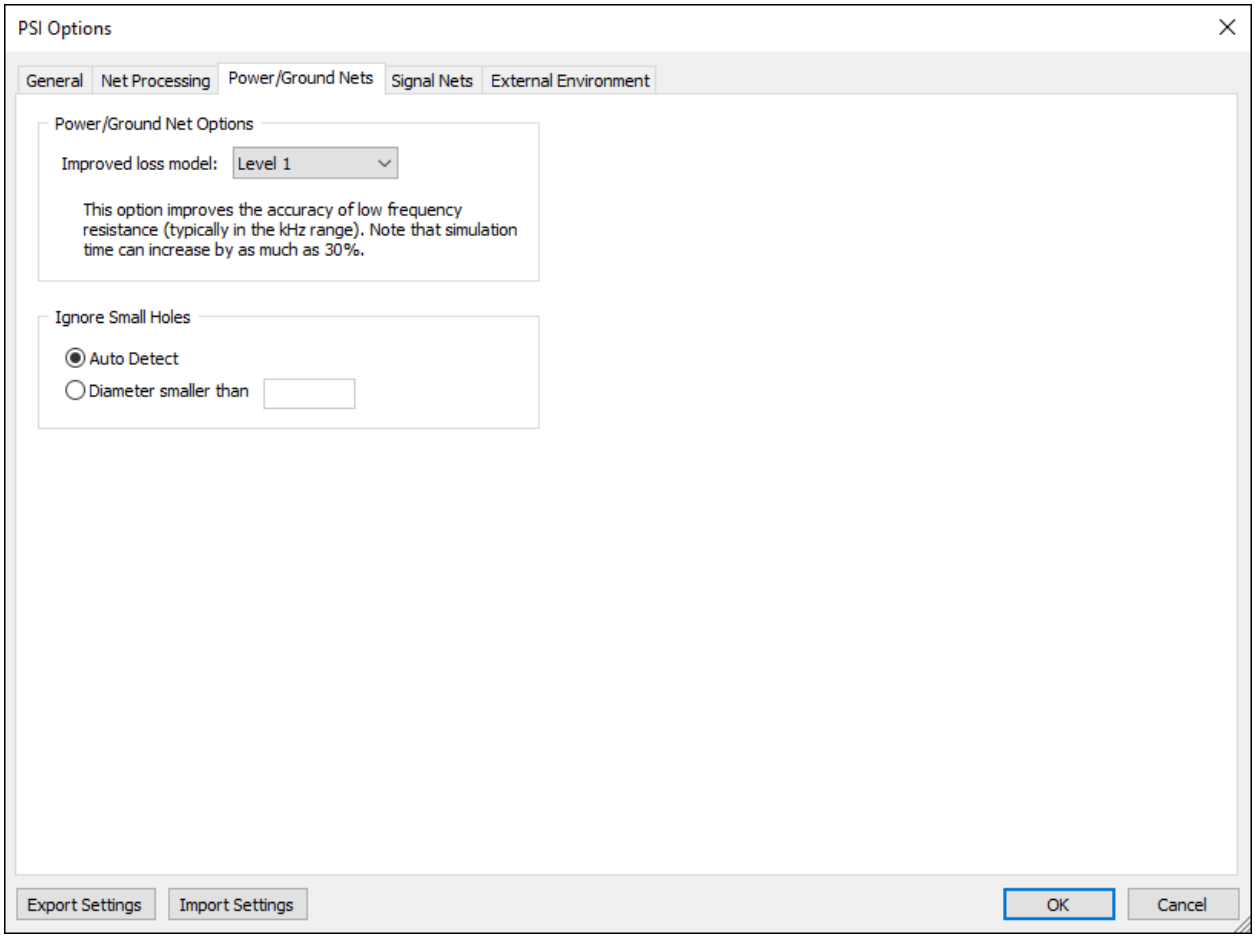

12. Use the **Improved loss model** drop-down menu to select a model.

    To measure metal loss in power and ground nets with greater accuracy at low frequency, typically in the kHz range, you can apply additional levels of complexity in the loss model. Ansys recommends using **Level 1**because the higher-order loss models substantially increase run time. For signal simulations that need higher accuracy, **Level 2** should suffice.

13. From the **Ignore Small Holes** area, use the radio buttons to either automatically detect small holes or specify the diameter that constitutes "small." Anything below that value will be ignored.
14. Select the **Signal Nets** tab.

    The **Signal Nets** tab displays.

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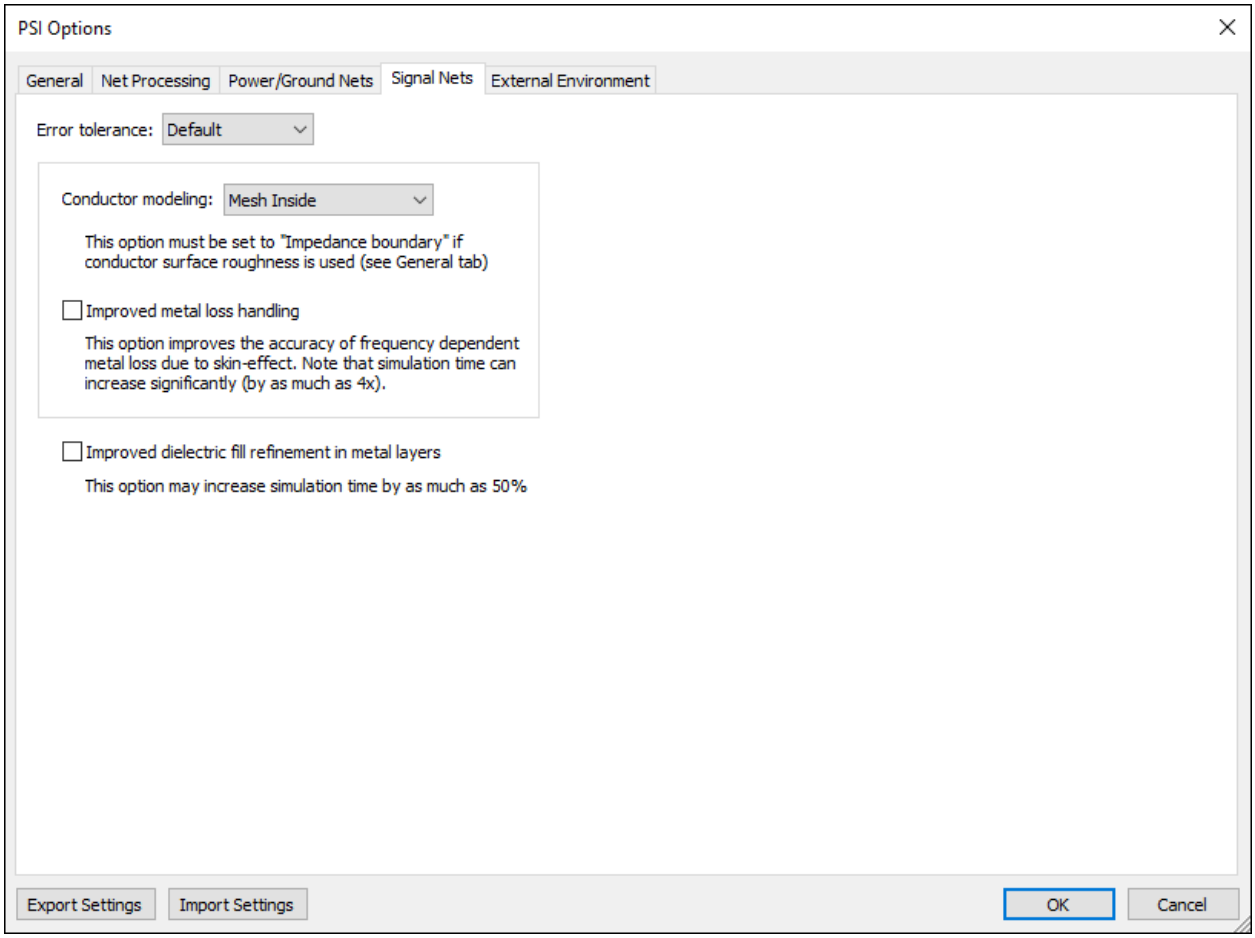

15. Use the **Error tolerance** drop-down menu to specify a value. This value is normalized to one for performing the dynamic analysis computations. The smaller the error tolerance value, the more accurate (and longer) the computation. By default, the error tolerance setting is tied to the speed-balance-accuracy slide setting: A value of 0.02 is tied to **Accuracy**, and 0.04 is tied to **Balanced**.
16. Use the **Conductor modeling** drop-down menu to select either **Mesh inside** or **Impedance boundary**.

> **Note:**
>
> If you selected one of the conductor surface models in the **General** tab, you must use the **Impedance boundary** option.

17. Check the **Improved metal loss handling** check box to improve the accuracy of frequency dependent metal loss due to skin-effect.

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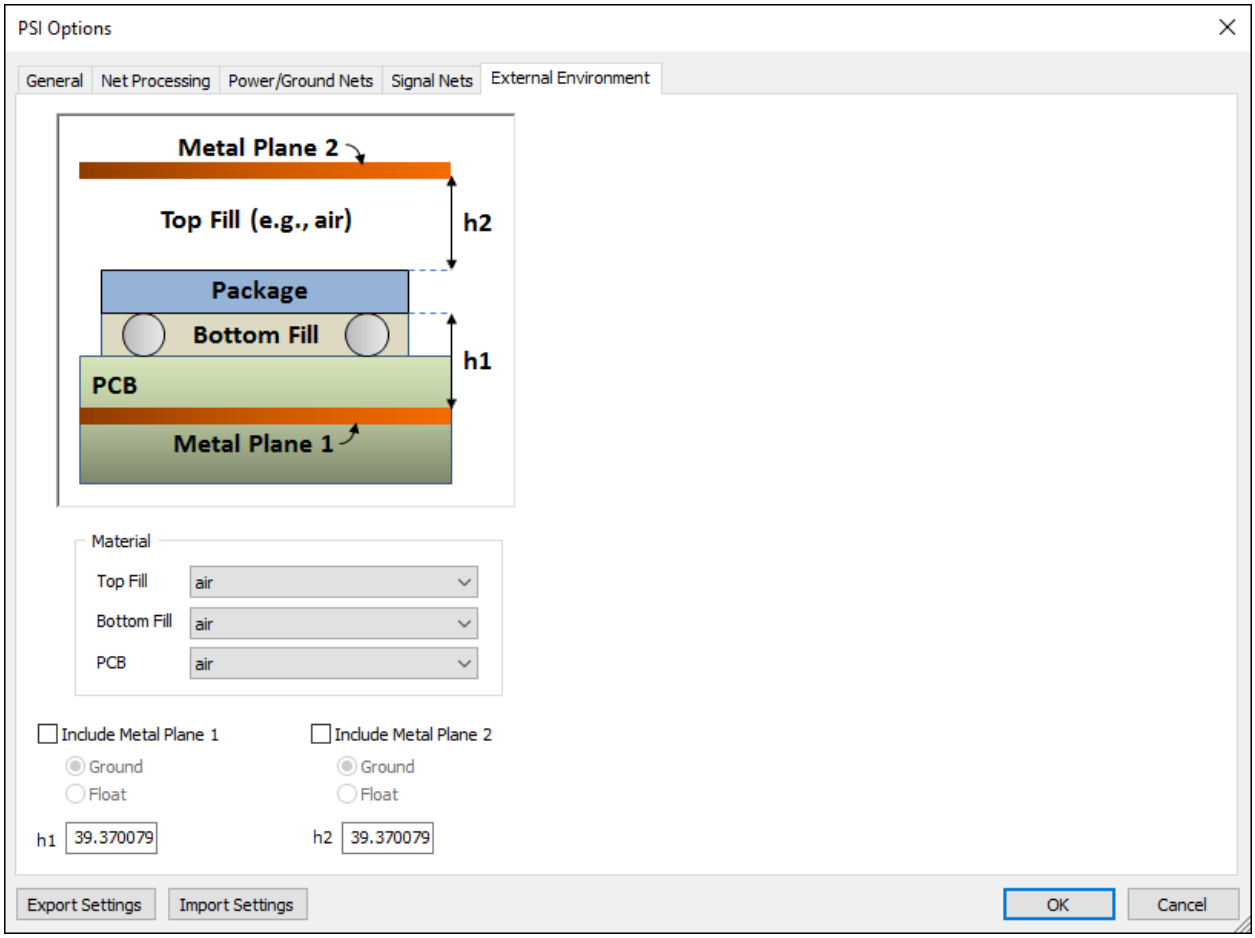
18. Check the **Improved dielectric fill refinement in metal layers** check box to control accuracy. However, increasing the accuracy also substantially increases the simulation time by as much as 50%. Ansys recommends leaving this option unchecked because the default setting provides sufficiently good accuracy and faster simulation.
19. Select the **External Environment** tab.

    The **External Environment** tab displays.



20. From the **Material** area, use the **Top Fill**, **Bottom Fill**, and **PCB** drop-down menus to select materials.
21. Check **Include Metal Plane 1** and **Include Metal Plane 2** to add up to two metal planes to the model. **Metal Plane 1** represents the upper PCB Ground or VDD plane. **Metal Plane 2** can represent a metal cover, a heat sink, or any other metal plane located above the package. This metal plane behaves similarly to **Metal Plane 1**.
22. For each selected metal plane, select either **Ground** or **Float**.

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- Select **Ground** to use the metal plane as part of the return path. This configuration affects the inductance and capacitance of the package nets.
- Select **Float** to leave the metal plane floating. This configuration affects only the capacitance of the package nets.

23. For each selected metal plane, enter a value for height:
    - **h1** represents the distance from the bottom layer of the package stackup to the top of **Metal Plane 1**. The solder balls included in this space add to the inductance and capacitance effects on the package nets.
    - **h2** represents the distance from the top layer of the package stackup to the bottom of **Metal Plane 2**.
24. Optionally, use the **Export Settings** button to save your settings as an SIwave Sim Settings File (*.sws). Click **Import Settings** to browse and select an *.sws file for import.
25. Click **OK** to apply all settings.

Computing AC Simulations

The PSI AC current/voltage solver uses the given source configuration to compute the current flow within each element of a PCB model, including discrete components, vias, traces, planes, bondwires, and sources.

To compute an AC simulation in SIwave:

1. Click **Simulation**.
2. From the PSI area, click **Compute AC Currents**.

   The **Compute AC currents using PSI** window appears.

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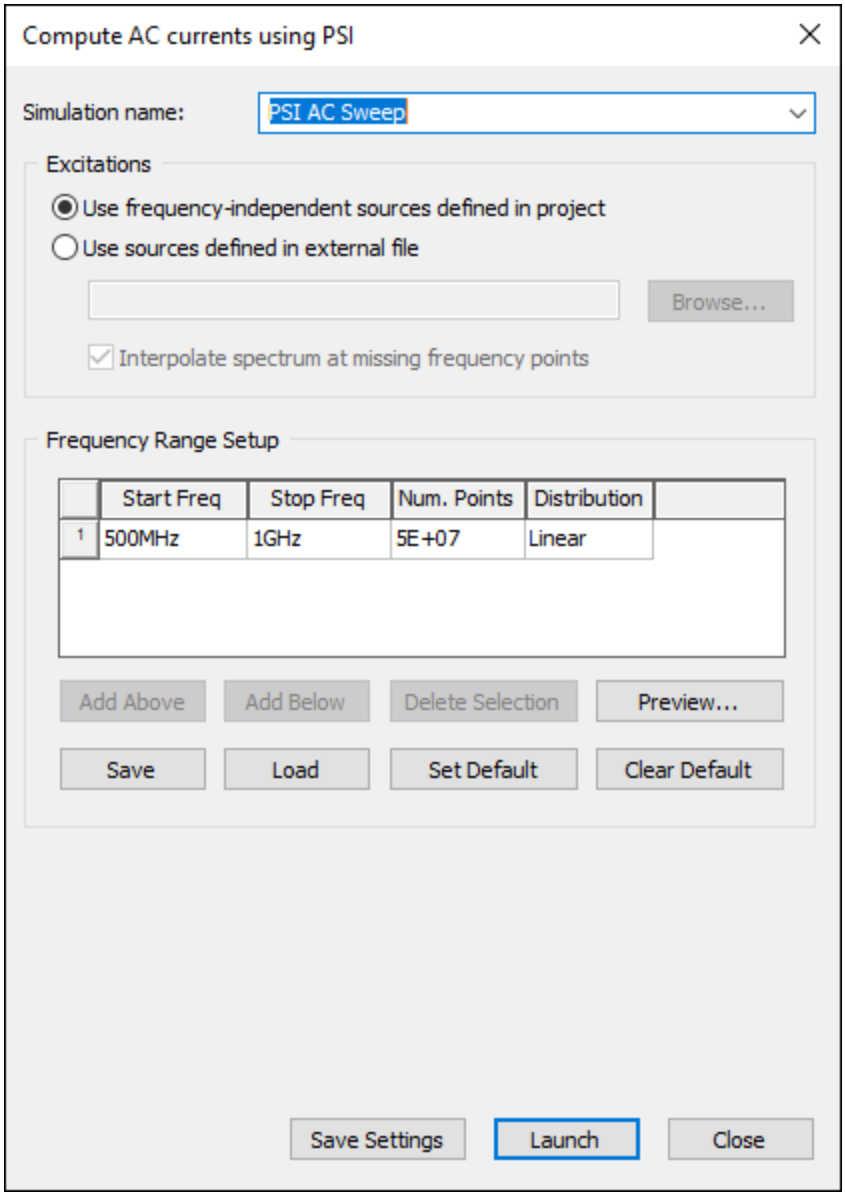

3. From the **Simulation name** field, enter a name for the simulation or leave the default.
4. From the **Excitations** area:
   - **Use frequency-independent sources defined in project** – by default, excitations are defined by the current project.
   - **Use sources defined in external file** – allows you to browse and select an external excitations file.
   - When using an external excitations file, you can select the option to **Interpolate spectrum at missing frequency points**.

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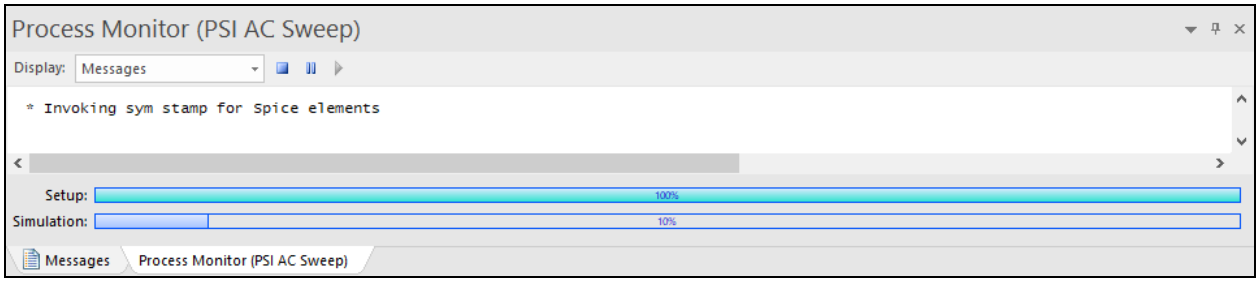
Note:

- PSI only understands frequency-independent current and voltage sources and time-domain piecewise linear current sources (*not* frequency-domain sources).
- If you push excitations from Ansys Electronics Desktop, the external file option is automatically selected and the file field populated.

5. From the **Frequency Range Setup** table:
   a. From the **Start Freq** text box, enter the starting frequency of the frequency sweep.

      SIwave solves the solution beginning with the frequency entered in the Start box and ending with the frequency entered in the Stop box.
   b. From the **Stop Freq** text box, enter the ending frequency of the frequency sweep.
   c. From the **Num Points** box, enter the number of points.
   d. Use the **Distribution** drop-down menu to select either **Linear** or **By Decade**.
      - **Linear** – the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
      - **By Decade** – distributes the number of points specified logarithmically, over each decade.
   e. You can add and remove rows at your appropriate locations using the **Add Above**, **Add Below**, and **Delete Selection** buttons.
   f. Click **Preview** to see the frequency range in the **Frequency List Preview** window.
   g. Click **Save** to save the grid values to a SIwave Frequency Sweep Distribution File (*.sfsdf). You can also load a previously saved *.sfsdf file.
   h. Click the **Set Default** button to set the current grid settings as a default value for that simulation type.
   i. Click the **Clear Default** button to remove the default setting and return the population of the grid to its normal behavior.
6. If appropriate, click **Save Settings** to keep the simulation settings.
7. Click **Launch** to begin the simulation.

   The **Messages** window updates with a Process Monitor tab that displays the progress.



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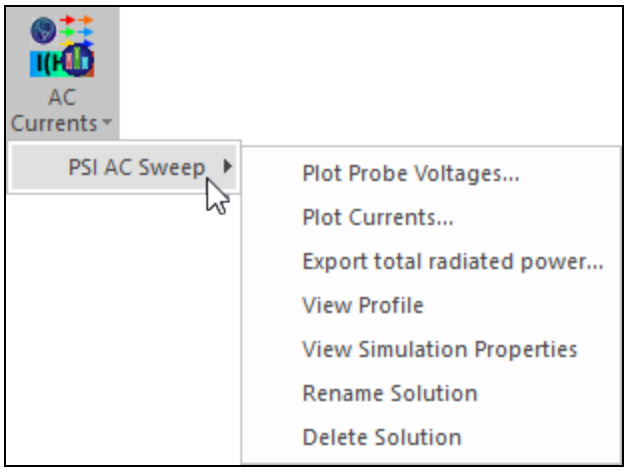
Viewing AC Simulation Results

To view AC simulation results in SIwave:

1. Click **Results**.
2. From the PSI area, select **AC Currents** > **[Simulation Name]**.



Result options include:

- Plot Probe Voltages
- Plot Currents

Plotting Probe Voltages

From the AC Sweep Results menu:

1. Click **Plot Probe Voltages**.

   The **Voltage Probe Plot Generation** window appears.

2. Select an appropriate options.
3. Click **Create Plot**.

Plotting Currents

From the AC Sweep Results menu:

1. Click **Plot Currents**.

   The **PSI AC Current Simulation Results** window appears, and the Modeling workspace updates to display AC currents.

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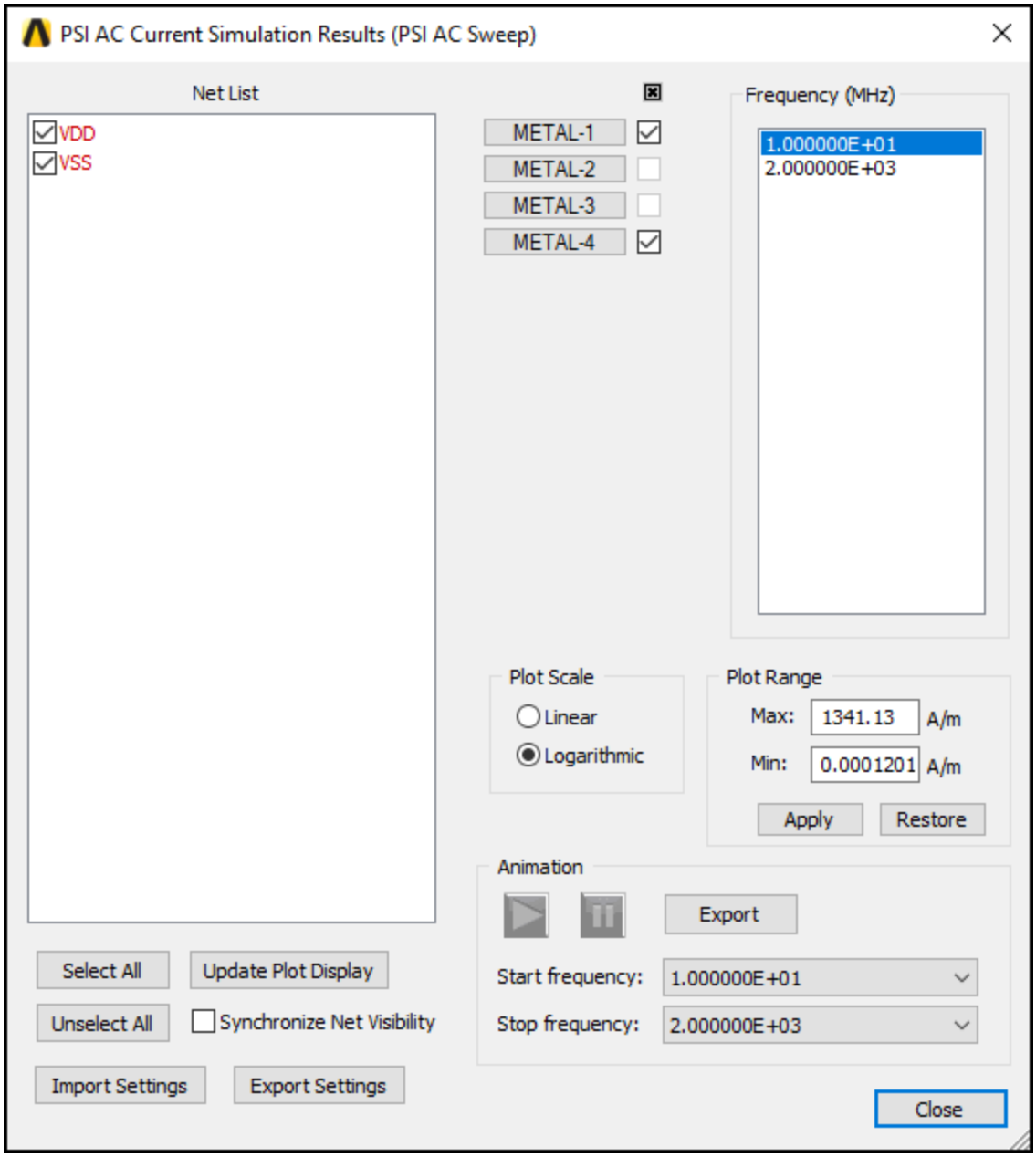

2. Use the **Net List** to select net visibility.
3. Use the layer check boxes to select layer visibility.
4. Use the **Frequency** list to select a frequency. The Modeling workspace updates to show that frequency's current information.
5. Select your appropriate **Plot Scale** and **Plot Range** options.

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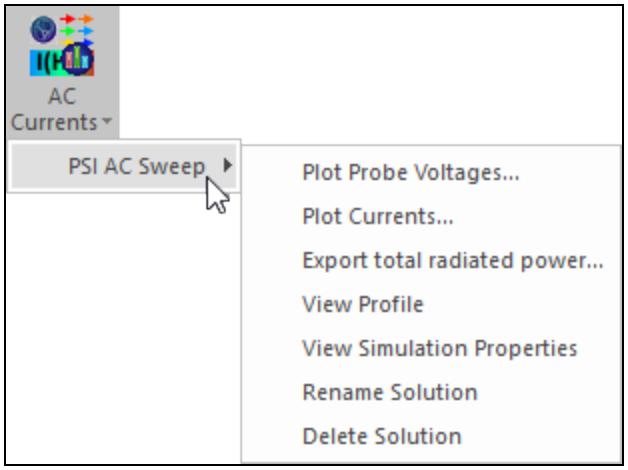
6. To view the currents as an animation:
   a. Use the drop-down menus to select a **Start Frequency** and **Stop Frequency**.
   b. Click the **Play** and **Pause** button to control the animation.
   c. Click **Export** to save the animation as either an *.avi or *.gif file.
7. If appropriate, you can **Import Settings** or **Export Settings** for net visibility, plot scaling and plot range. These settings are saved in XML format.

From the AC Sweep Results menu, you can also access additional menu options.

AC Sweep Results Menu Options

Navigate to the AC Sweep Results menu:

1. Click **Results**.
2. From the PSI area, select **AC Currents** > **[Simulation Name]**.



Menu options include:

- **Export total radiated power...** – exports power information in Comma Separated Value (*.csv) format.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the Sweep tab.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Total Radiated Power CSV file:

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Freq [Hz]	RadiatedPower [W]
5E+08	0.056471
5.5E+08	0.039166
6E+08	0.334561
6.5E+08	0.046567
7E+08	0.166308
7.5E+08	0.143375
8E+08	0.26196
8.5E+08	0.100521
9E+08	0.234894
9.5E+08	0.07746
1E+09	0.058901

Simulation Profile:

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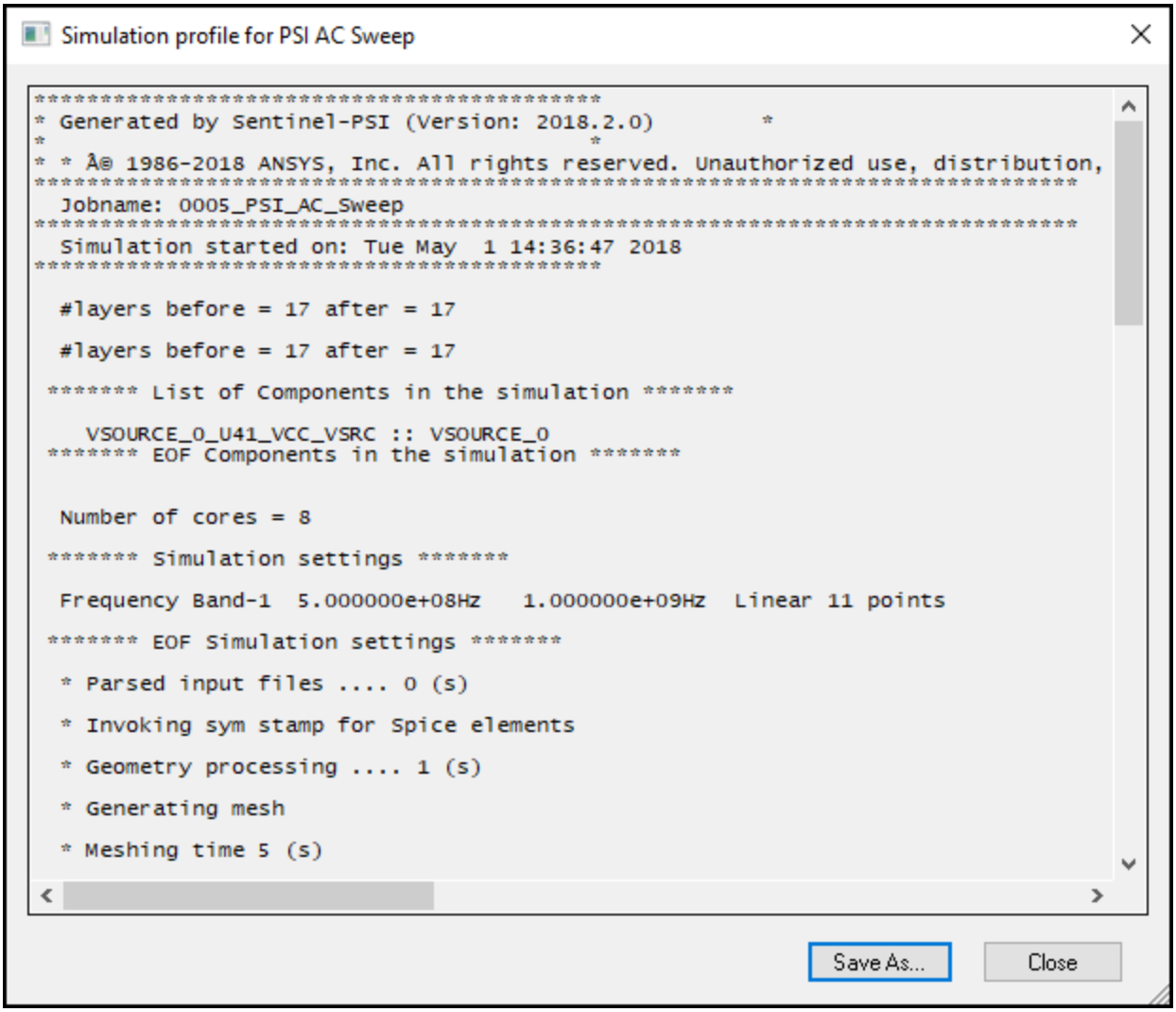

Simulation Properties:

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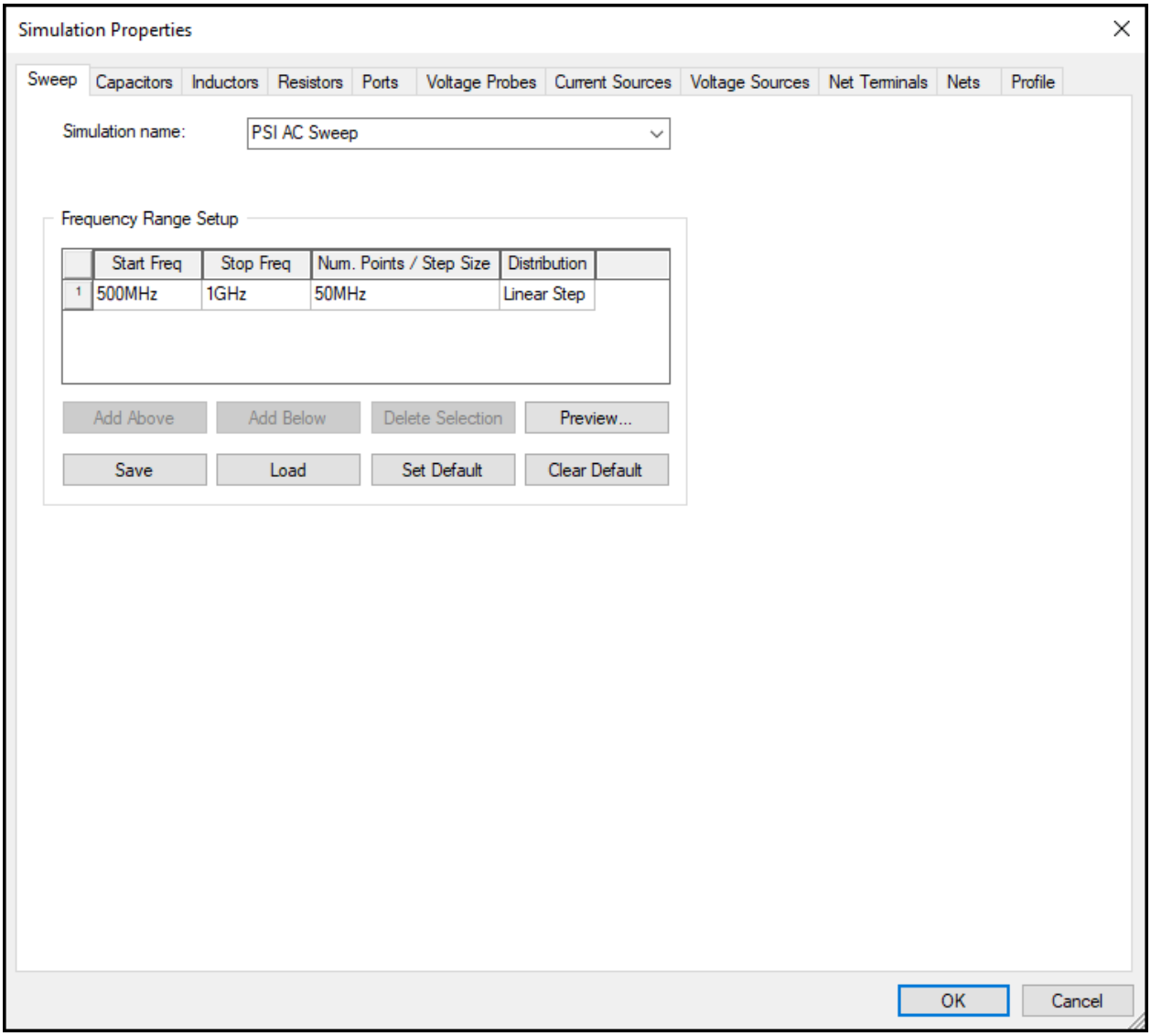

From the AC Sweep Results menu, you can also plot probe voltages and currents.

Computing SYZ Parameters Using PSI

PSI meshes the selected nets and extracts the SYZ-parameters at and between defined ports, with high-speed Finite Element Meshing (FEM) using prism elements. PSI SYZ is optimized for power integrity and signal integrity analyses of packages. The extraction generates a FWS SPICE file that can be exported for post-processing (see SSO export.).

Complete these steps to compute the S-,Y-, and Z-parameters using PSI:

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1. Click **Simulation**.
2. From the PSI area, click **Compute SYZ Parameters**.

> **Note:**
>
> There are two Compute SYZ Parameters icons on the Simulation tab. Do not use the one in the SIwave area.

The **Compute SYZ-parameters using PSI** window appears.

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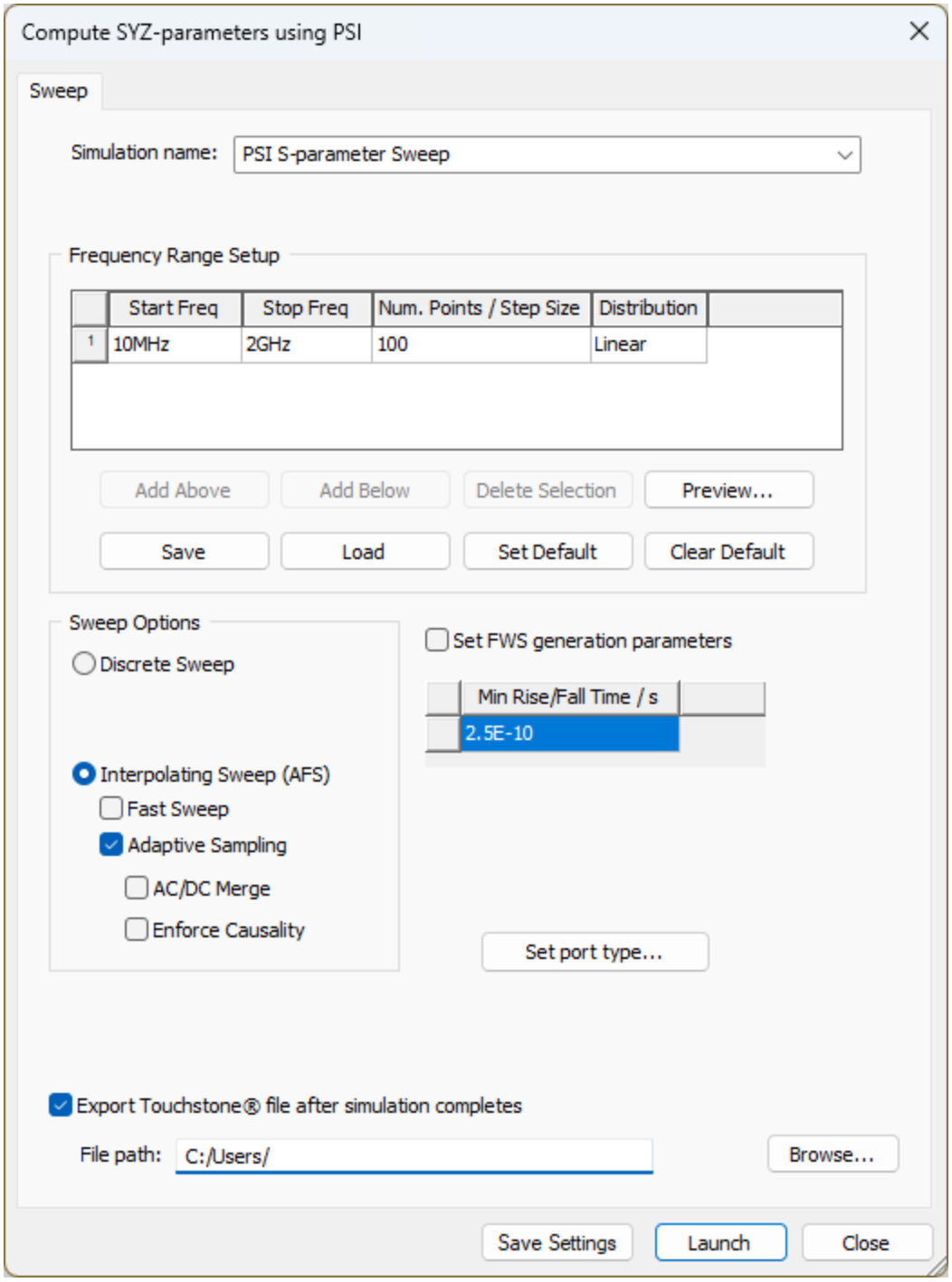

3. From the **Simulation Name** field, enter a name or leave the default.
4. From the **Frequency Range Setup** area, enter values for **Start Freq**, and **Num. Points**.
5. Use the **Distribution** drop-down menu to select a distribution method:

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- **Linear** – the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
- **By Decade** – distributes the number of points specified logarithmically, over each decade.

6. Enter a value for *either* **Stop Freq** *or* **Min. Rise/Fall Time**.

   The **Min. Rise/Fall Time** value represents the time scale that characterizes the rate of change of the input time signal that will be applied in the circuit simulator.

   > **Note:**
   >
   > Entering data in one field automatically sets the other. The maximum frequency is considered to be the knee frequency, f_{knee}, which is related to the rise time T_R by the formula:
   >
   > $f_{knee} = 0.5 / T_R$

7. If appropriate, you can add or remove frequency points using the **Add Above**, **Add Below**, and **Delete Selection** buttons.
8. If appropriate, click **Save** to save frequency point settings as an SIwave Frequency Sweep Distribution File (*.sfsdf). To load previously saved settings from a *.sfsdf file, click **Load**.
9. If appropriate, click **Set Default** to make current settings the default for the simulation type. To return to the original default settings, click **Clear Default**.
10. If appropriate, click **Preview** to open the Frequency List Preview.
11. From the **Sweep Options** area, use the radio buttons to select either **Discrete** or **Interpolating**.
    - An interpolating sweep estimates a frequency response for an entire frequency range by solving at a relatively small number of frequency points within that range. Between the actual solution frequencies, the frequency response is obtained by rational interpolation.PSI adaptively chooses the frequency points at which it computes the field solution. After a new frequency point is solved, a new interpolating fit is generated. This is compared to the interpolant from the previous step, and the maximum difference between the two is determined. If the difference exceeds the requested tolerance, then a new frequency point is chosen for a solution. The interpolating sweep is complete when the difference between successive interpolants is less than the error tolerance criterion.
    - If you choose **Interpolating**, you can also specify whether to use **Fast Sweep** and/or **Adaptive Sampling**. The Fast Sweep algorithm improves runtime by requiring fewer samples to simulate, but uses more memory. Adaptive Sampling determines the number of sample frequency points from the response over the frequency band, adding more points around rapidly changing responses such as resonance peaks.

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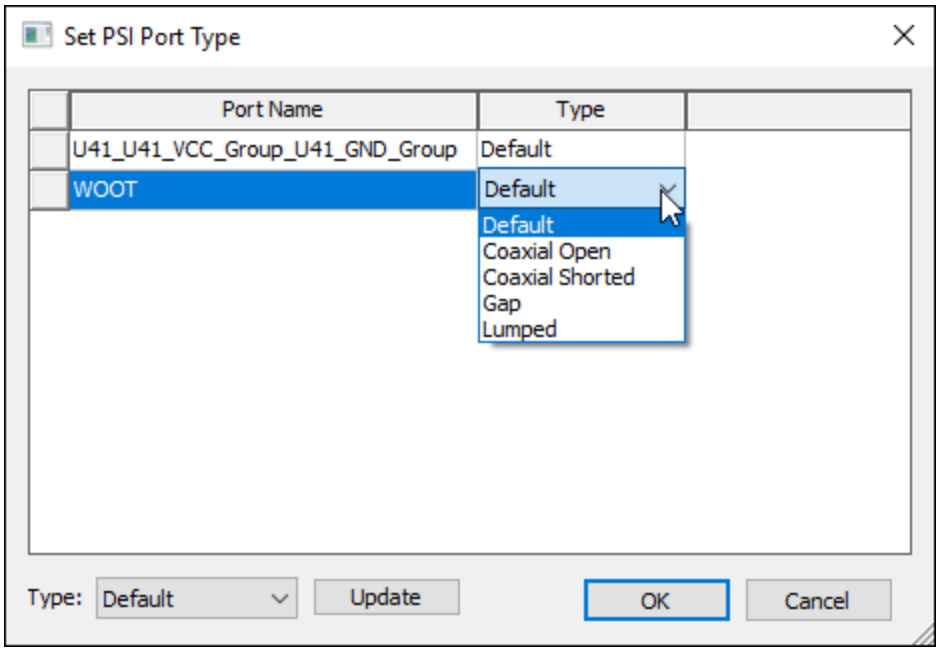
- To generate S-parameters at the DC point, check **AC/DC Merge**.
- To enforce causality, check **Enforce Causality**.

12. If appropriate, check **Set FWS generation parameters** to export the full-wave SPICE subcircuit.

    The Start Frequency value changes to 0Hz. If you have an existing S-parameter solution, you can run an FWS simulation without needing a 0Hz or 1Hz point.

13. If appropriate, check **Export Touchstone file after simulation completes** to automatically generate a Touchstone file (*.sNp, *.ts) after the SYZ sweep completes.
14. If appropriate, click **Set port type** to change port types. For more information, see PSI Solver Port Setup. You can also edit Touchstone Port properties.

    The **Set PSI Port Type** window appears.



15. Click **OK** to exit the Set PSI Port Type window.
16. Click **Launch** to run the simulation.

    The **Messages** window updates with a Process Monitor tab that displays the progress.

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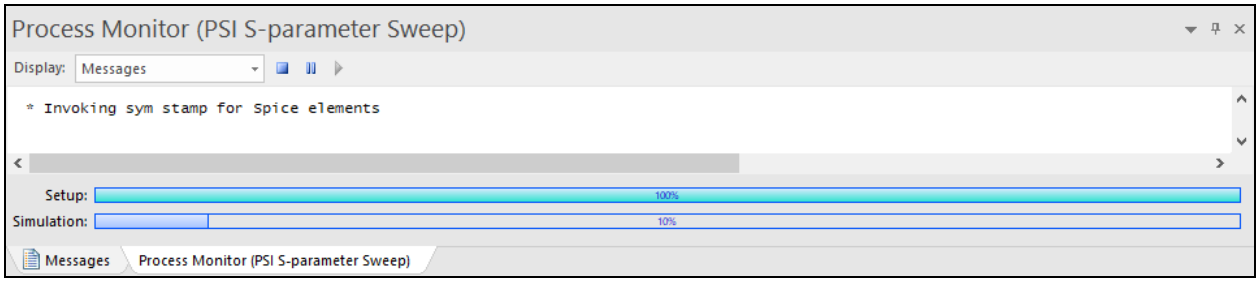
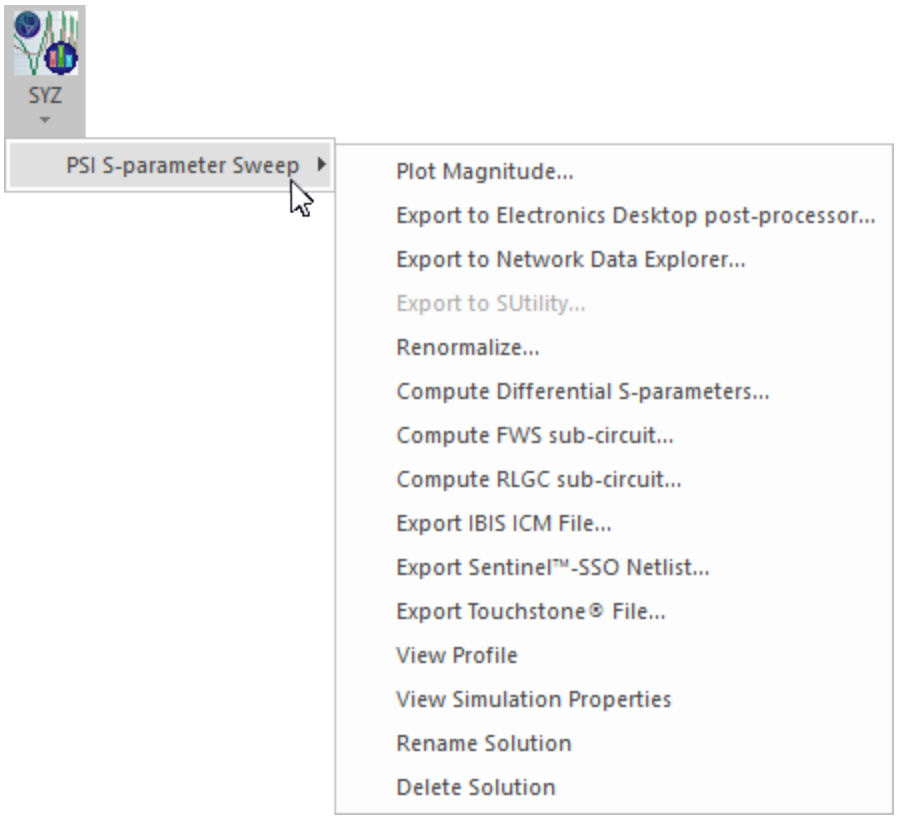


Viewing PSI SYZ Results

To view PSI SYZ results in SIwave:

1. Click **Results**.
2. From the PSI area, select **SYZ** > **[Simulation Name]**.



3. Select the type of results you would like to view.

   Result menu options include:

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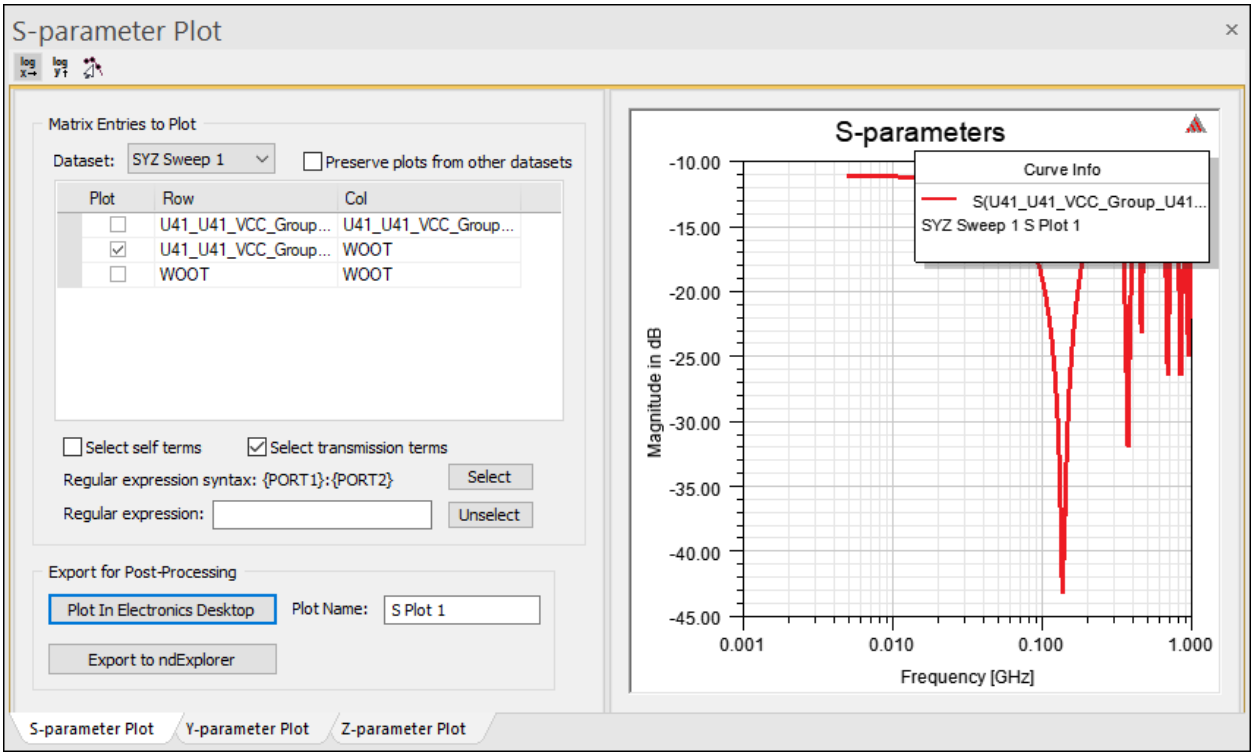
- **Plot Magnitude** – allows you to view a plot of S-, Y-, and Z- parameters. See Plotting Magnitude.
- **Compute Differential S-Parameters** – allows you to view a differential plot of s-parameters. See Computing Differential S-parameters.
- **Compute FWS Sub-Circuit** – allows you to compute and export a Full Wave SPICE (FWS) plot. See Computing FWS sub-circuit .
- **Compute RLGC - Sub-Circuit** – allows you to derive RLGC information from the S-parameters. After you compute the RLGC matrices, you can export the RLGC subcircuit. See Computing RLGC Sub-Circuits.

Plot Magnitude:



From the SYZ Results menu, you can also access additional menu options and export simulation information.

PSI SYZ Results Menu Options

Navigate to the PSI SYZ Results menu:

1. Click **Results**.
2. From the PSI area, select **SYZ** > **[Simulation Name]**.

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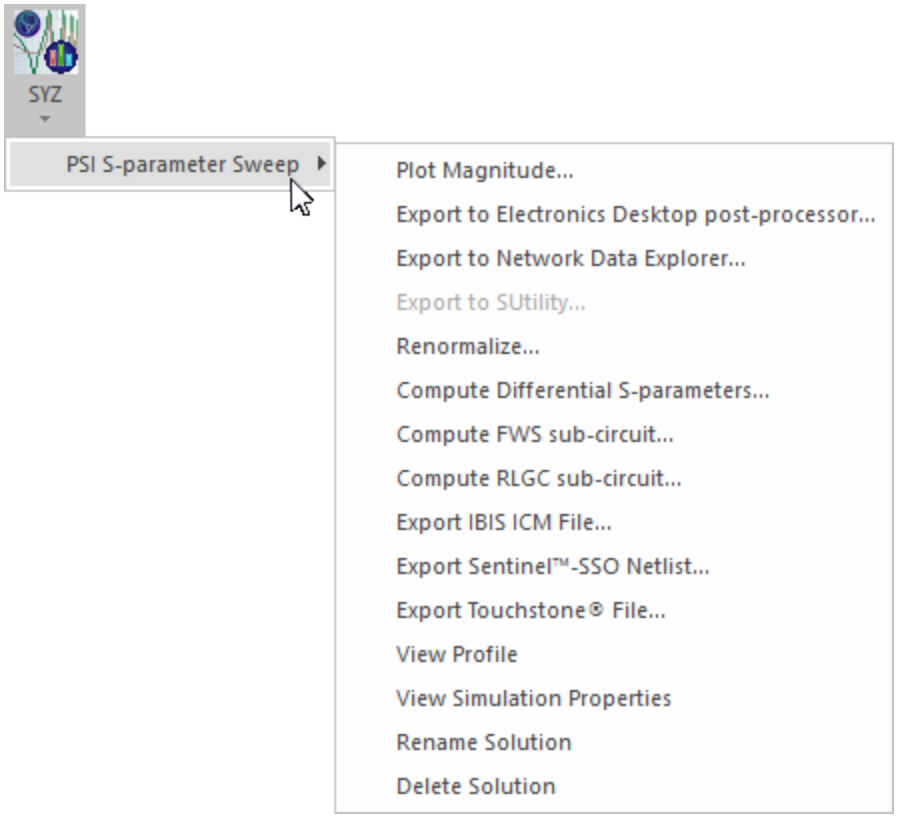

Menu options include:

- **Renormalize** – opens the S- Parameter Renormalization window, where you can modify the reference impedance for one or more ports.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the Sweep tab.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.

Renormalize:

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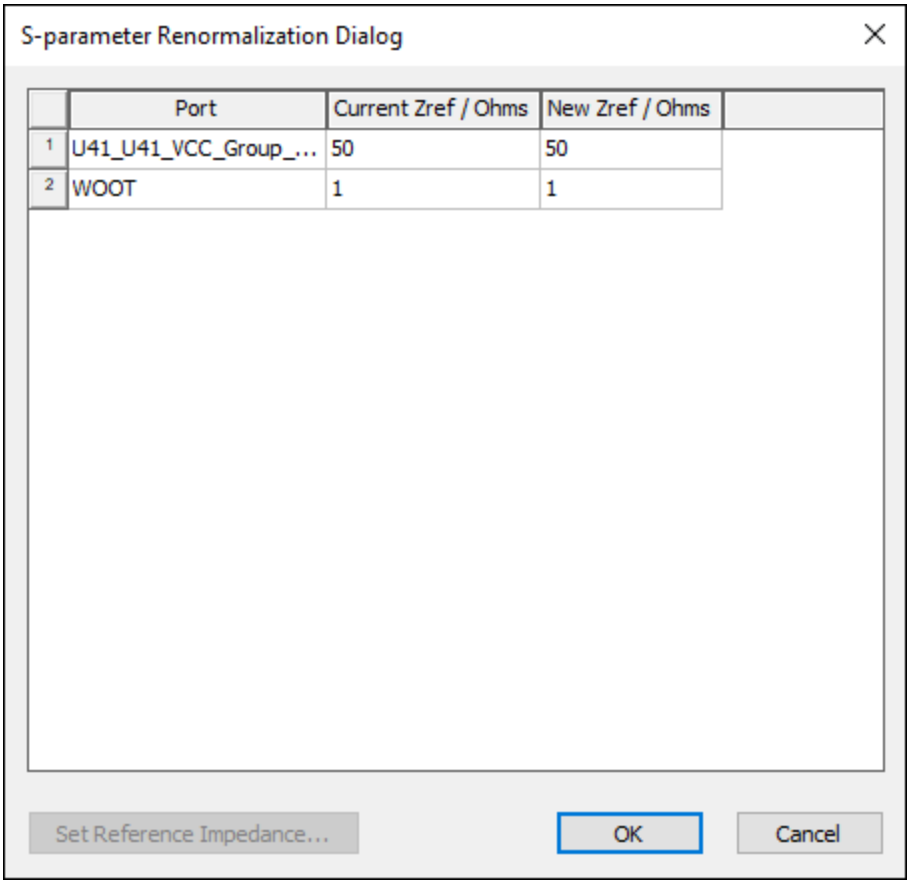

Simulation Profile:

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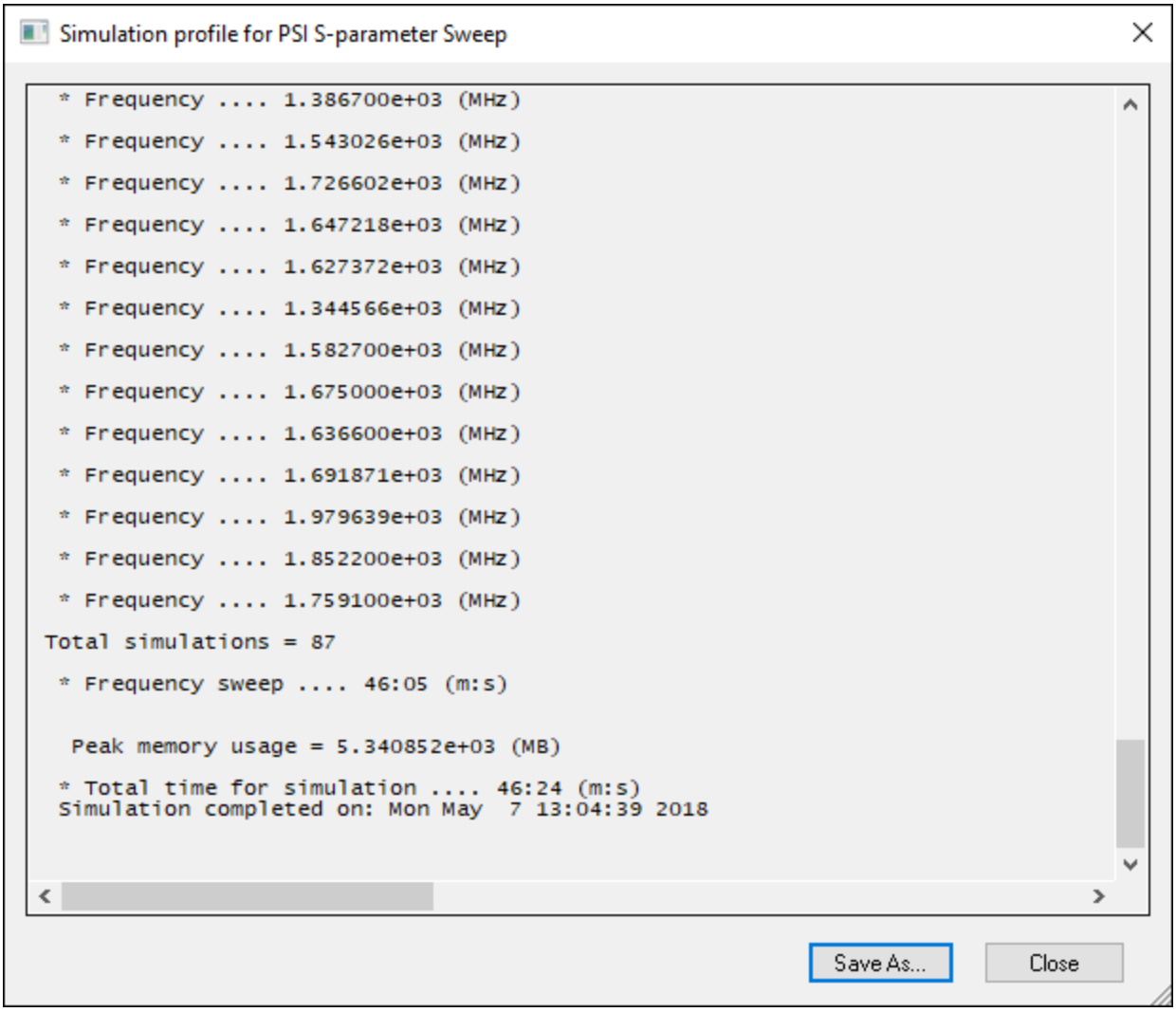

Simulation Properties:

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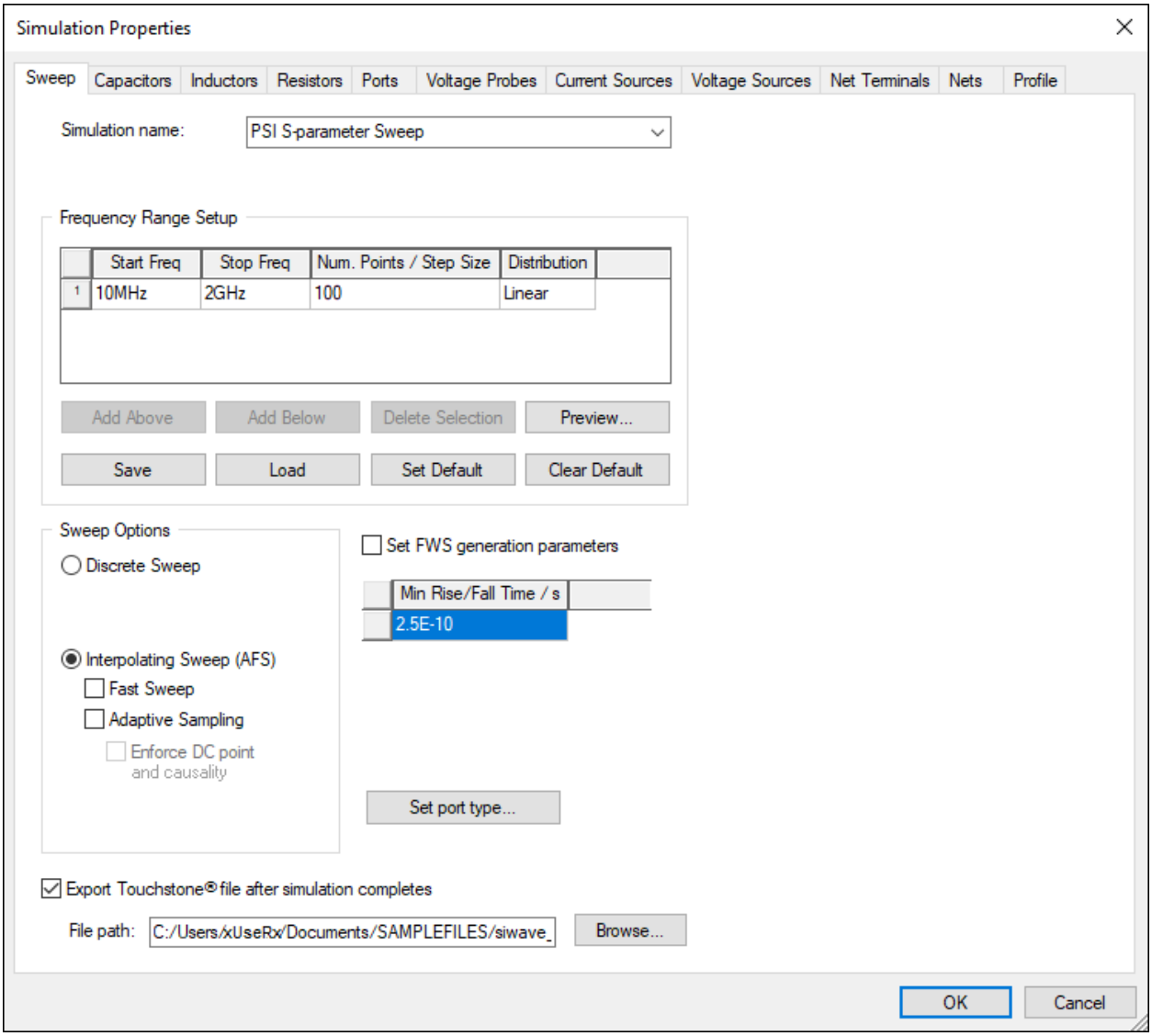

From the SYZ results menu, you can also view PSI SYZ results and export certain information.

Exporting PSI SYZ Information

Navigate to the PSI SYZ Results menu:

1. Click **Results**.
2. From the PSI area, select **SYZ** > **[Simulation Name]**.

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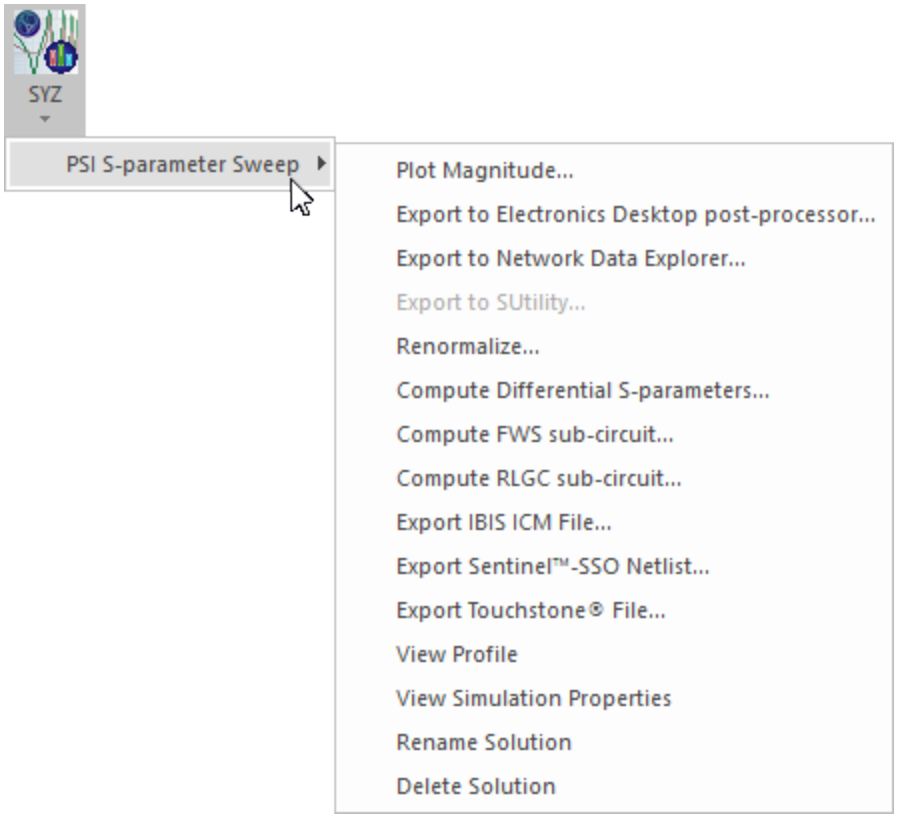

Export menu options include:

- **Export to Electronics Desktop post-processor** – launches Ansys Electronics Desktop and opens the plot.
- **Export to Network Data Explorer** – launches ndExplorer with SYZ data pre-populated.
- **Export to SUtility** – launches SUtility with SYZ data pre-populated.
- **Export IBIS ICM File** – exports files to the IBIS Interconnect Modeling (ICM) standard. See below.
- **Export Sentinel-SSO Netlist** – exports the results of a PSI SYZ-parameter extraction as a SPICE netlist with a CPP header for Apache Sentinel SSO flow. See below.
- **Export Touchstone File** – exports the SYZ data in an *.sNp file that can be used with third-party tools and opened in any text editor.

Exporting an IBIS ICM File

The IBIS Interconnect Modeling (ICM) standard specifies a "wrapper" around regular Touchstone files. An .***.icm** file lists original port names and includes a link to a Touchstone (.***.sNp**) file containing the actual SYZ-parameter data.

To export an IBIS ICM file from PSI:

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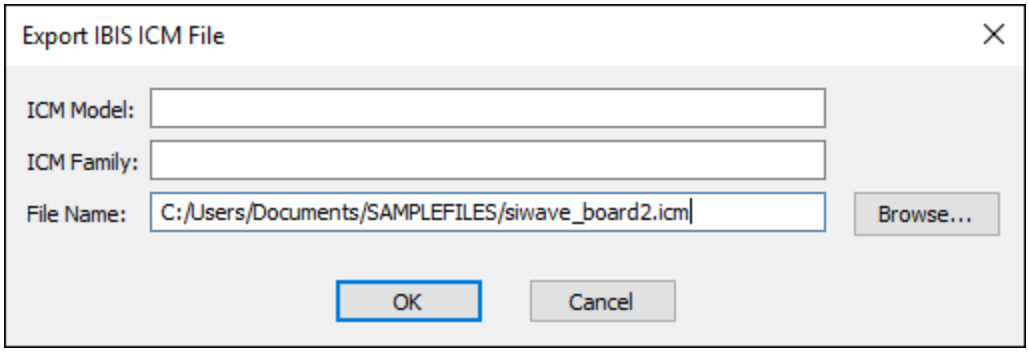
1. Run an SYZ Sweep.
2. Click **Results**.
3. From the PSI area, select **SYZ > [Simulation Name] > Export IBIS ICM File**.

   The **Export IBIS ICM File** window appears.



4. Enter the **ICM Model**, **ICM Family**, and appropriate **File Name** and path.
5. Click **OK**.

   The file exports.

> **Note:**
>
> To conform with the ICM (IBIS Interconnect Modeling) standard, only lowercase letters, numbers, underscore and dash ("-") are permitted in the .**sNp** and .**icm** file names.

Exporting a Sentinel-SSO Netlist

To export a Sentinel-SSO Netlist from PSI:

1. Run an SYZ Sweep.
2. Click **Results**.
3. From the PSI area, select **SYZ > [Simulation Name] > Export Sentinel-SSO Netlist**.

   The **Export Sentinel-SSO Netlist** window appears.

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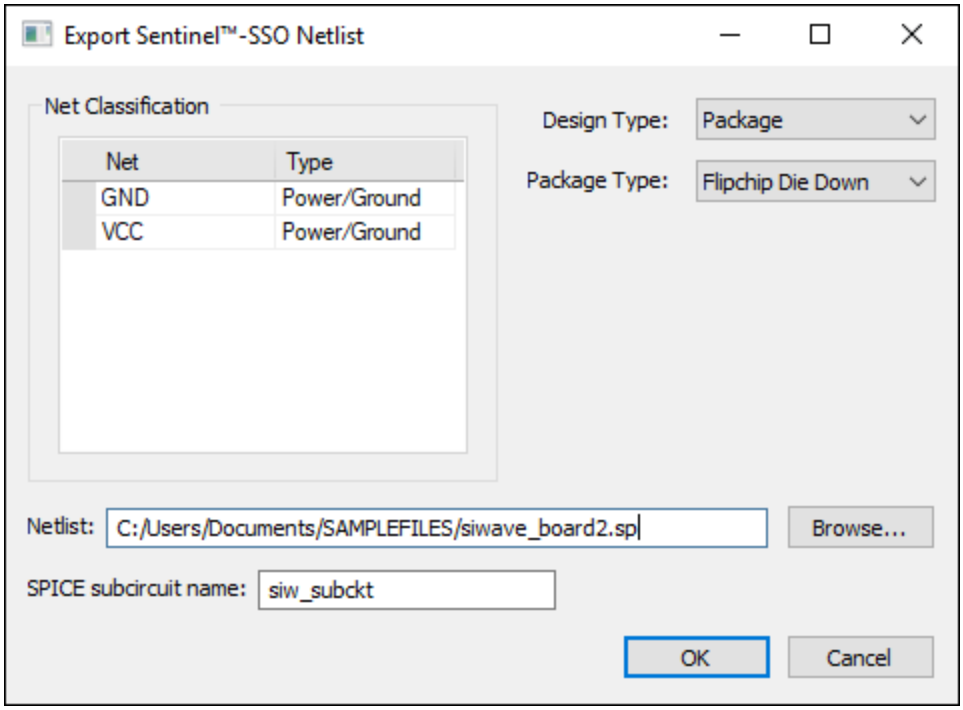

4. From the **Net Classification** area, you can use the **Type** drop-down menus to reclassify nets as **Power/Ground** or **Signal**.
5. Use the **Design Type** drop-down menu to select **Package**, **Board**, or **Die**.
6. If you selected Package, use the **Package Type** drop-down menu to select a package type. This menu is unavailable otherwise.
7. From the **Netlist** field, type a file name and path, or click **Browse** to select these.
8. Specify a **SPICE subcircuit name** for the netlist file, or accept the default (**siw_subckt**).
9. Click **OK**.

   A SPICE netlist file is created in the specified location. A Touchstone file containing the S-parameter data is created in the same directory.

From the PSI SYZ Results menu, you can also view SYZ results or view and change SYZ properties.

Computing Differential S-Parameters

If you have two or more ports defined and have computed the S-parameters for them, you can view the differential and common-mode S-parameters.

To compute differential S-parameters from PSI:

1. Click **Results**.
2. From the PSI area, select **SYZ** > **[Simulation Name]**.

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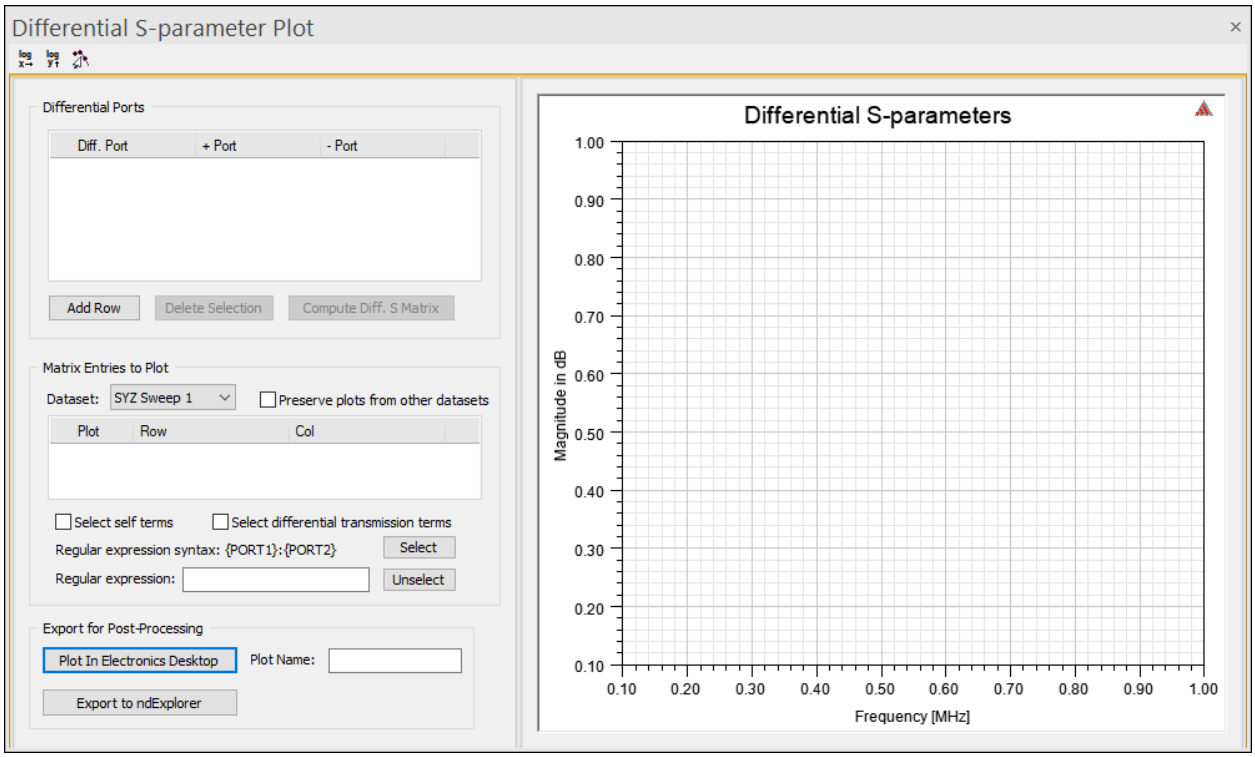
3. Click **Compute Differential S-parameters**.

   The **Differential S-parameter Plot** window appears.



   See Plotting Magnitude for more information about using the plot window.

4. From the **Differential Ports** area, select the **Positive Reference Port** and **Negative Reference Port**.
5. If appropriate, click **Add Row** to add ports.
6. Click **Compute Diff. S Matrix**.

   The **Matrix Entries to Plot** area updates.

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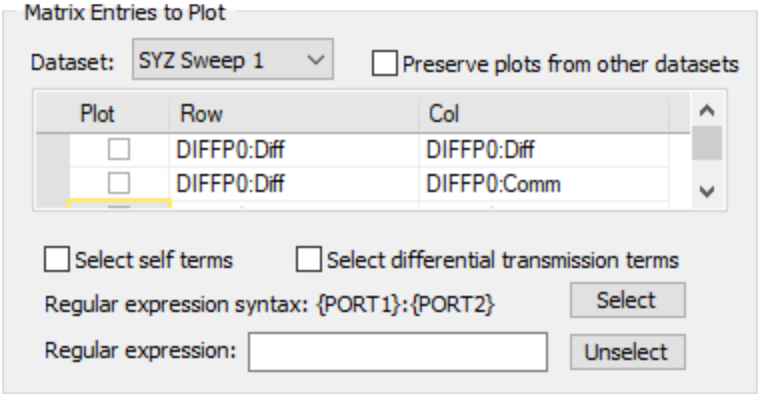
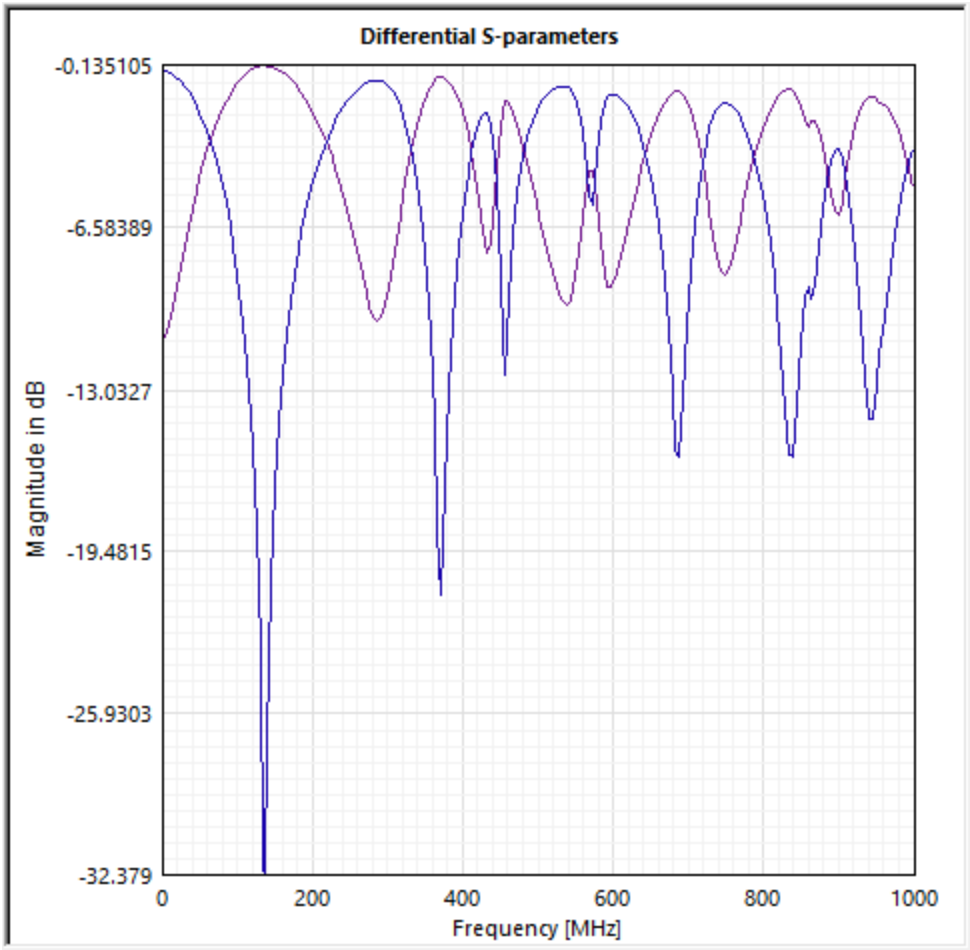


7. Use the check boxes in the **Plot** column to select entries to plot.

   The plot area updates to display the information.



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8. To export and view the plot in Ansys Electronics Desktop, enter a name in the **Plot Name** field and click **Plot in Electronics Desktop**.
9. To export and view the plot in ndExplorer, click **Export to ndExplorer**.

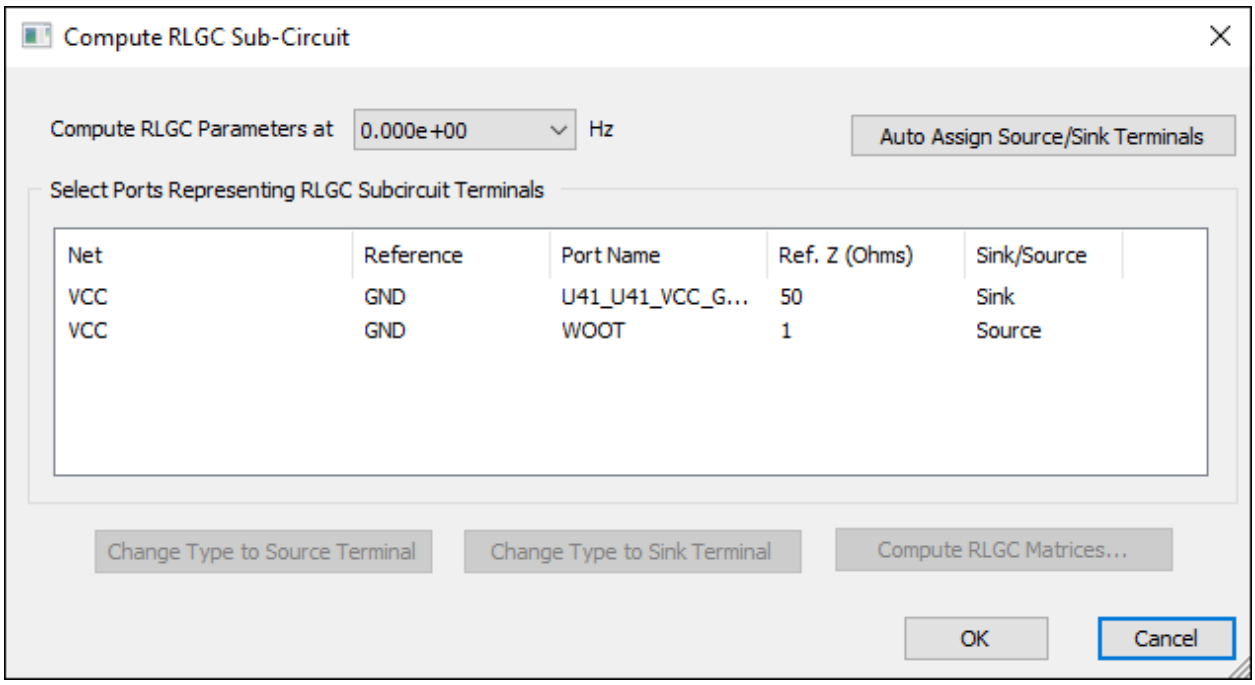
Computing PSI RLGC Subcircuits

SIwave allows you to derive RLGC information from the S-parameters. After you compute the RLGC matrices, you can export the RLGC subcircuit.

To export a solution into an RLGC subcircuit from PSI:

1. Click **Results**.
2. From the PSI area, select **SYZ** > **[Simulation Name]**.
3. Click **Compute RLGC Sub-Circuit**.

   The **Compute RLGC Sub-circuit** window appears.



4. Use the **Compute RLGC Parameters at** drop-down menu to select a frequency.
5. To assign sources and sinks, select a net in the list and use the **Change Type to Source Terminal** and **Change Type to Sink Terminal** buttons. Alternatively, click **Auto Assign Source/Sink Terminals** to have SIwave identify and assign nets for you.

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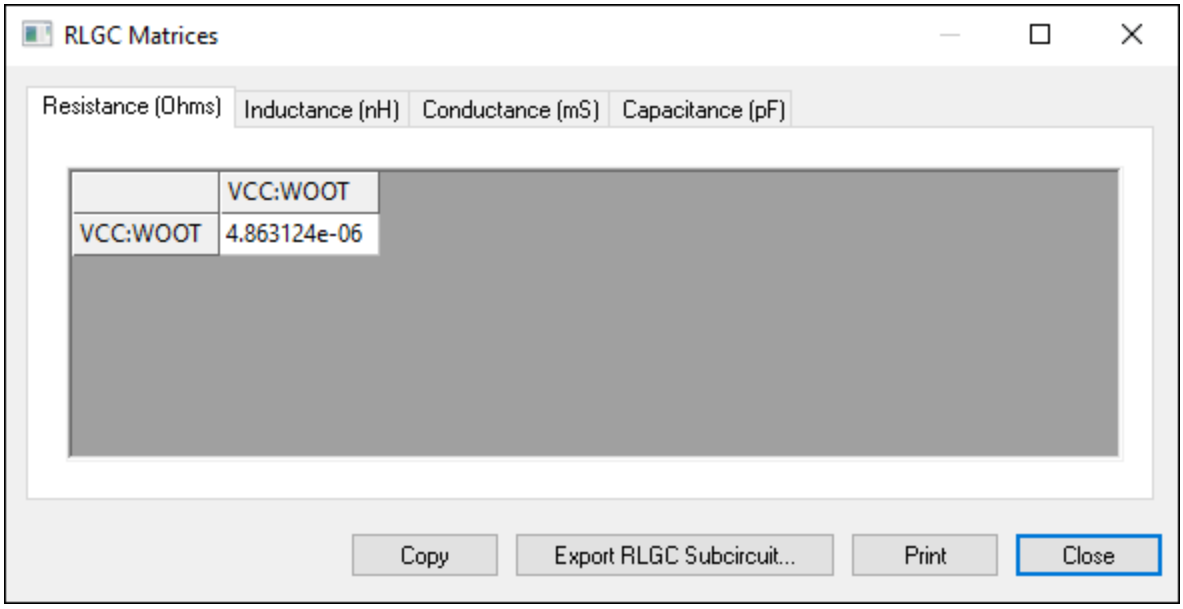
> **Note:**
>
> If two conducting objects touch, SIwave treats them as one combined object. Nets are auto identified by finding the touching conductors.

6. Click ports in the list to select them. You must select at least one Sink and one Source.
7. Click **Compute RLGC Matrices**.

   The **RLGC Matrices** window appears, on the Resistance tab.



8. Click any tab to view its details (Resistance, Inductance, Conductance, Capacitance).
9. To copy data from a tab, click **Copy**.
10. To print data from a tab, click **Print**.
11. To export the subcircuit, click **Export RLGC Subcircuit**.

    The **Export RLGC Subcircuit** window appears.

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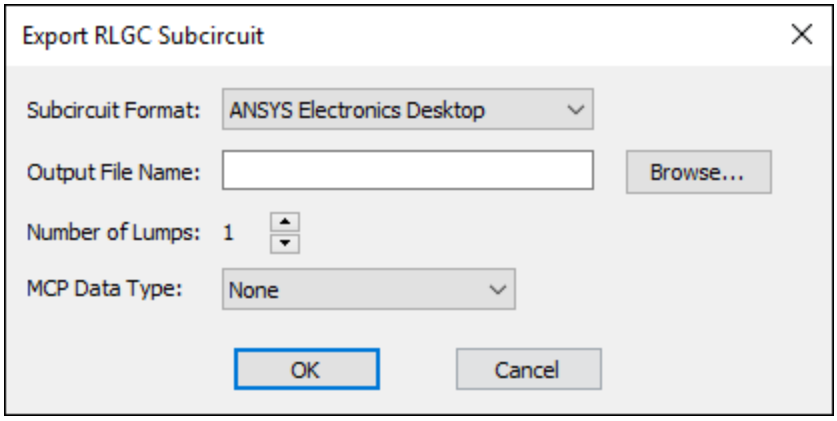

12. Use the **Subcircuit Format** drop-down menu to select a format.

    Options include:

    - Ansys Electronics Desktop
    - Berkeley SPICE
    - ESpice DML
    - HSPICE
    - IBIS Package Model
    - Maxwell SPICE
    - PSpice
    - Simplorer
    - Spectre
    - SPEF

13. From the **Output File Name** field, type a file name and path, or click **Browse** to select one.
14. Use the arrow buttons to specify the **Number of Lumps** to be included in the simulation. This can be any discrete value between 1 and 1000.
15. Use the **MCP Data Type** drop-down menu to select **DIE**, **PKG**, or **PCB**.
16. Click **OK** to export the RLGC matrices and return to the **RLGC Matrices** window.
17. Click **Close** to close the **RLGC Matrices** window.
18. Click **OK** to close the **Compute RLGC Sub-Circuit** window.

Computing and Exporting Full-Wave SPICE Subcircuits

The ability to export subcircuits is an important feature of SIwave. Exporting a subcircuit allows you to perform an analysis of the structure in a circuit simulator, together with detailed nonlinear models of the drivers and receivers. You can also simulate systems comprising PCBs and packages by connecting their subcircuits together in SPICE or Spectre.

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A full-wave subcircuit analysis includes full-wave effects. Frequency domain information is transferred to circuit simulators that operate in the time domain. Broadband matching of frequency responses is ensured while full-wave solution accuracy is preserved. When S-parameter data is exported to PSpice or HSPICE, an equivalent circuit is created. This circuit consists of frequency controlled voltage and current sources. When terminal S-parameter data is exported to Maxwell Spice software, a new full-wave *N*-port subcircuit is created.

See Full-wave subcircuits for more information on full-wave subcircuit models.

To export a solution into a full-wave SPICE subcircuit from PSI:

1. Click **Results**.
2. From the PSI area, select **SYZ** > **[Simulation Name]**.
3. Click **Compute FWS Sub-Circuit**.

   ndExplorer opens, and the **Broadband Export Options** window appears.

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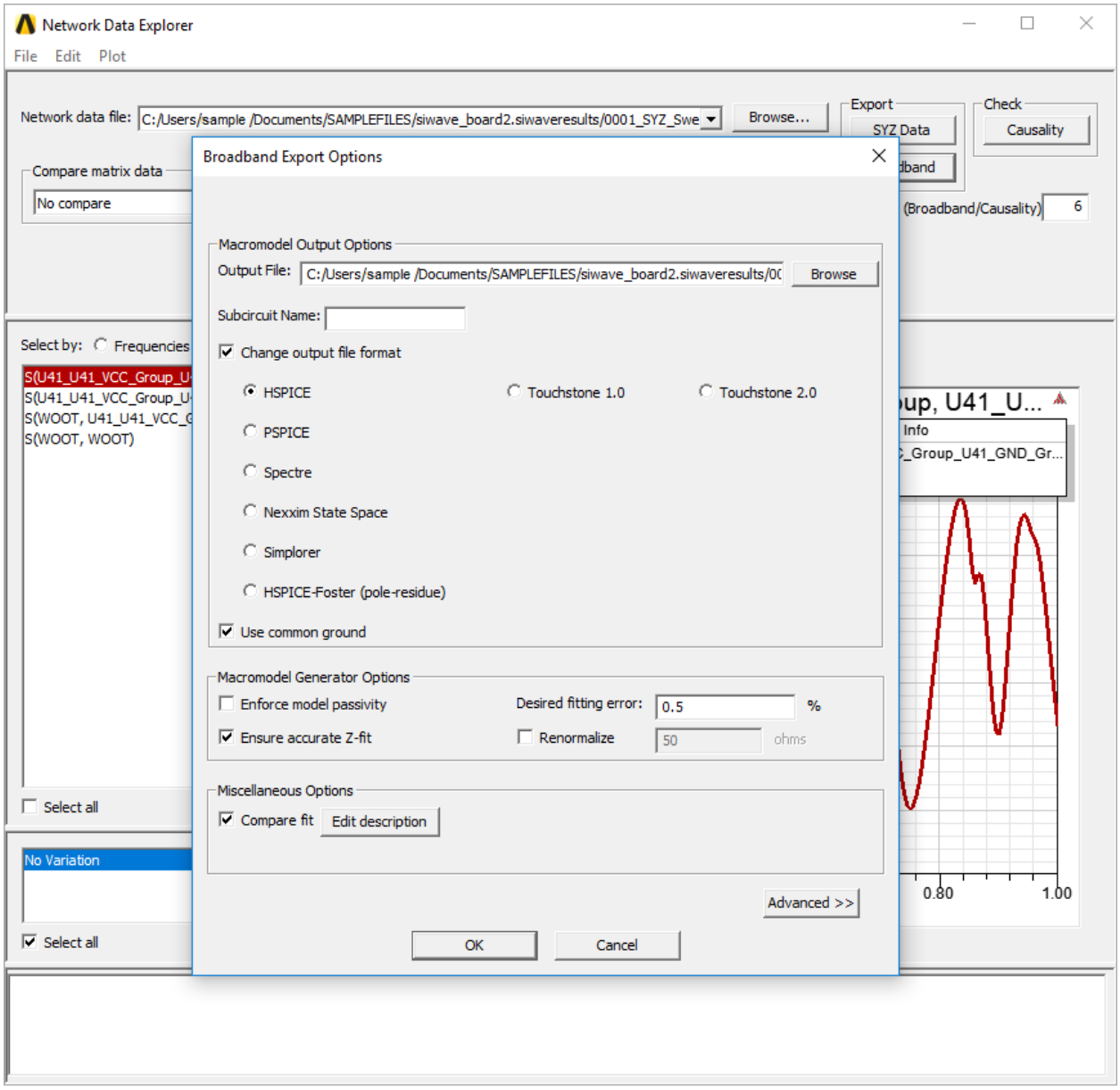

4. From the **Output File** field, enter a name and path for your file, or use the **Browse** button.
5. From the **Subcircuit Name** field, type a name for the subcircuit.
6. Check the **Change output file format** check box. Then use the radio buttons to select your appropriate SPICE file format. The default is HSPICE.
7. If appropriate, select **Use common ground**.
8. Use the check boxes to select your appropriate passivity, Z-fit, and renormalization options. For more information on these options, see Exporting Macro Model.

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9. Click **Advanced>>** to view additional options:
   - Passivity Options
   - Column Fitting Options
   - State Space Fitting Algorithm
   - Enable Relative Error Tolerance
   - Enforce Causality
   - For more information on these options, see Exporting Macro Model.
10. Click **OK**.

    A SPICE file based on the geometry of the planes and added circuit elements exports to the specified location.

For more information, see S-Parameter Technical Notes.

PDN Channel Builder

PDN Channel Builder extracts a power delivery network (PDN) model using either SIwave or PSI. It generates a power channel model of a combined die and package. The model includes the Power and Ground nets in the die and the voltage regulator module (VRM).

As a preliminary step, you should create an IC Die Network.

To invoke the PDN Channel Builder simulation in SIwave:

1. Click **Simulation**.
2. Click **PDN Channel Builder**.

   The **PDN Channel Builder** window opens with the **Die Configuration** tab selected.

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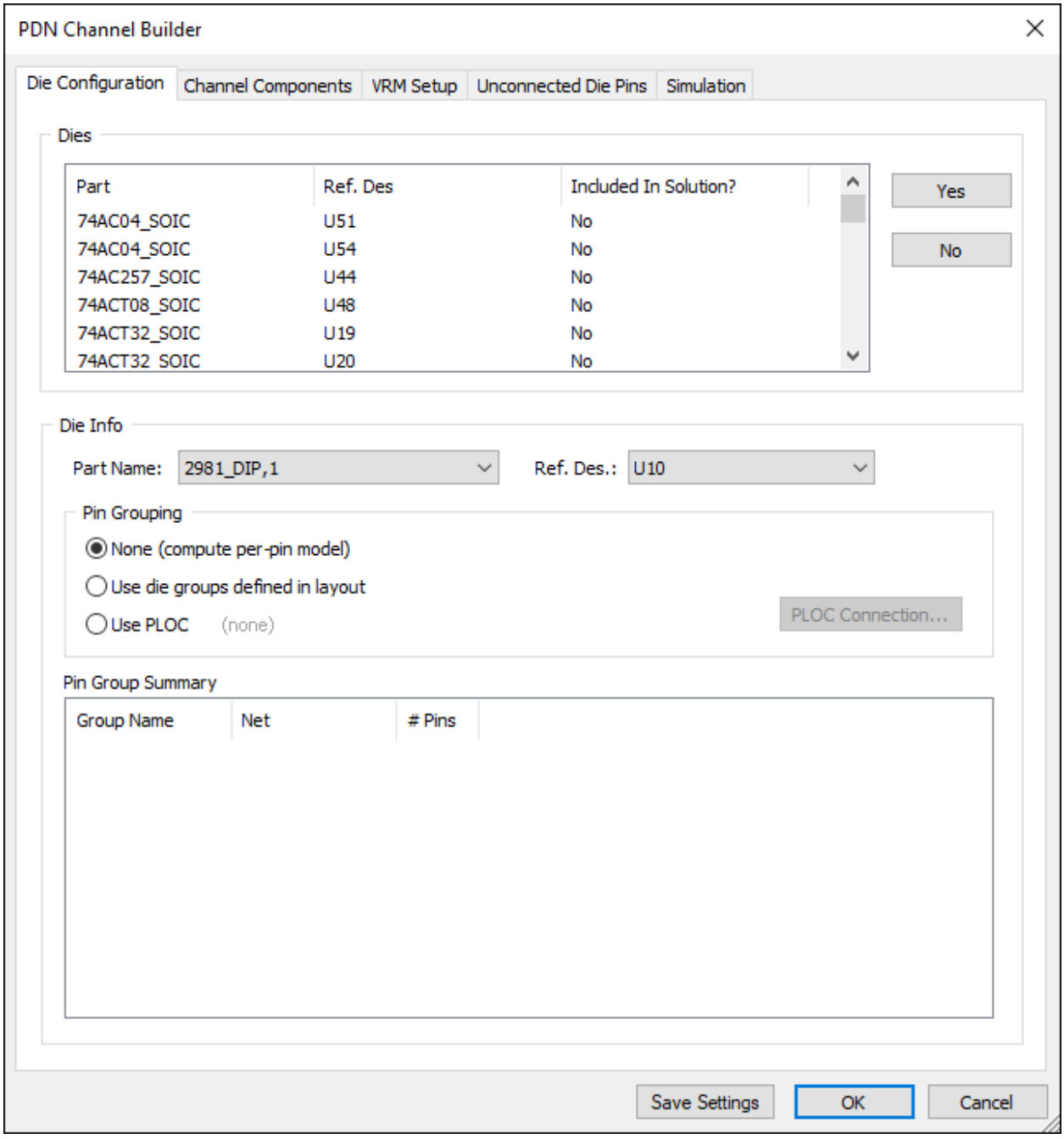

On the **Die Configuration** tab:

- The **Dies** list allows you to select which dies are included in a simulation using the **Yes** and **No** buttons.

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> **Important:**
>
> SIwave allows selection of multiple dies.
>
> When two or more are selected, their **Pin Grouping** must be set to either **Use die groups defined in layout** or **Use PLOC**.

- The **Die Info** area allows you to set pin grouping models, per die.
- The **Pin Group Summary** area lists existing pin groups.

3. Select a **Part Name** and **Ref. Des.** from the drop-down menus.
4. From the **Pin Grouping** area, use the radio buttons to select **None**, **Use die groups**, or **Use PLOC**.
5. If you selected **Use PLOC**, click **PLOC Connection** to adjust additional settings. Otherwise, proceed to Step 13.

   The **CPM/PLOC/Voltus Import** window appears.

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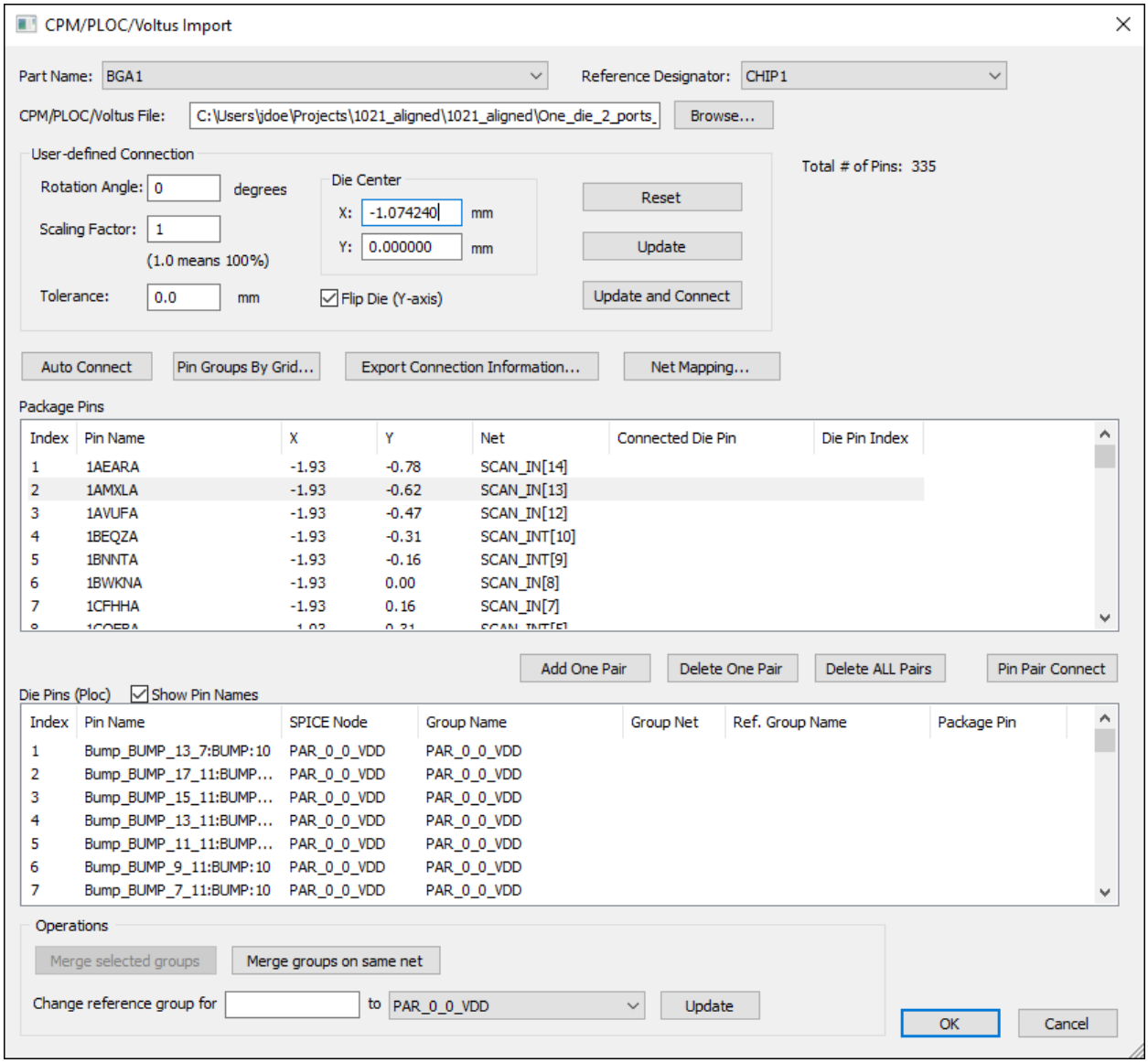

The **Package Pins** area lists the package pins.

6. From the **IC Die Information** panel, use the **Browse** button to locate and select the CPM, PLOC, or Voltus file you want to import.

   The list of **Die Pins** populates. Values for **Rotation**and **Location of die center on package** are read from the file and displayed. The **Flip Die** check box setting is determined automatically from data in the CPM file.

7. Click **Auto Connect** .

   The lists of **Package Pins** and **Die Pins** are updated to show the connections. The upper-right area of the window displays the number of **Pins mapped** and the number of **Pins**

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unmapped. For a successful auto-connect, all of the pins will be mapped and no pins will be unmapped.

8. If appropriate, you can **Create Pin Groups** in the Package and Die Pins
9. If appropriate, you can **Export Connection Information** to a text file.
10. The **Operations** area contains buttons to **Merge selected groups** or **Merge groups on same net**. You can change the reference group for a specified pin to a pin group selected from the drop-down menu. Click **Update** to update the reference group.
11. Click **OK** to close the**Apache CPM/PLOC Import** window and return to the **PDN Channel Builder** window, **PLOC Connection** tab.

    From the **Die** panel, the **Pin Group Summary** and **Port Summary** fields are populated with information from the PLOC file.

    - The **Pin Group Summary** area lists any pin groups in the PLOC component when it is connected.
    - The **Port Summary** area lists any ports in the PLOC component when it is connected.
    - The **VRM** area specifies the components and pins that supply voltage and ground to the die.
12. From the **VRM** area, select the **Part** and **Reference Designator**.

    For each **Part/Ref Des** row in the **VRM** panel, select a **Power Net** and **Ground Net** to be extracted, and specify the **Supply Voltage**. Use the **Add Rows** and **Delete Rows** buttons to specify multiple parts or multiple sources.
13. If appropriate, click **Save Settings** to preserve the parameters for the **PLOC** connections.
14. Select the **Channel Components** tab.

    The **Channel Components** tab displays.

    Review the Channel components. These are passive components mounted on the package (other than the Die and BGA). If any passive component has a capacitor models specified, those component pins are automatically extracted and exposed in the Spice netlist. This helps in studying subsequent what-if scenarios without having to go through the extraction again. If a component contains simple R and L elements, these components are absorbed into the extraction and not exposed at the Spice netlist level.
15. Select the **VRM Setup** tab.

    The **VRM Setup** tab displays.

    Specify BGA components and pins that supply voltage and ground to the die. To select parts, use the **Part** and **Ref. Des** drop-down menus, or click the gray area adjacent to a row. You can select multiple rows using Ctrl+click.

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- Select a **Power Net** and **Ground Net** to be extracted, and specify the **Supply Voltage**. Use the **Add Rows** and **Delete Rows** buttons to add and remove parts as appropriate. You can also **Restore Recommended VRM Assignments**.
- The net with the largest number of BGA component pins is designated as the Reference (Ground) net. Other nets are routed to BGA component, and are terminated with a DC supply voltage of 1.5V by default. This value can be edited independently for each net, and the voltage level can be modified even after the extraction. If a suitable PCB model is available, it can replace the VRM model after the extraction is done.
- The pin groups defined on the BGA component are extracted and VRM supply voltages are distributed to these groups. If no pin groups are defined, all the pins for each net are grouped automatically, and the supply voltages are connected on net-by-net basis.

16. Select the **Unconnected Die Pins** tab.

    The **Unconnected Die Pins** tab displays.

    If you previously selected PLOC connections, this tab allows you to specify Supply Voltage values for any unconnected PLOC nets. To update a voltage value, select a net, enter a value in the **Supply Voltage** field, and click **Update**.

    If you did not select any PLOC connections, the options on this tab will be disabled.

17. Select the **Simulation** tab.

    The **Simulation** tab displays.

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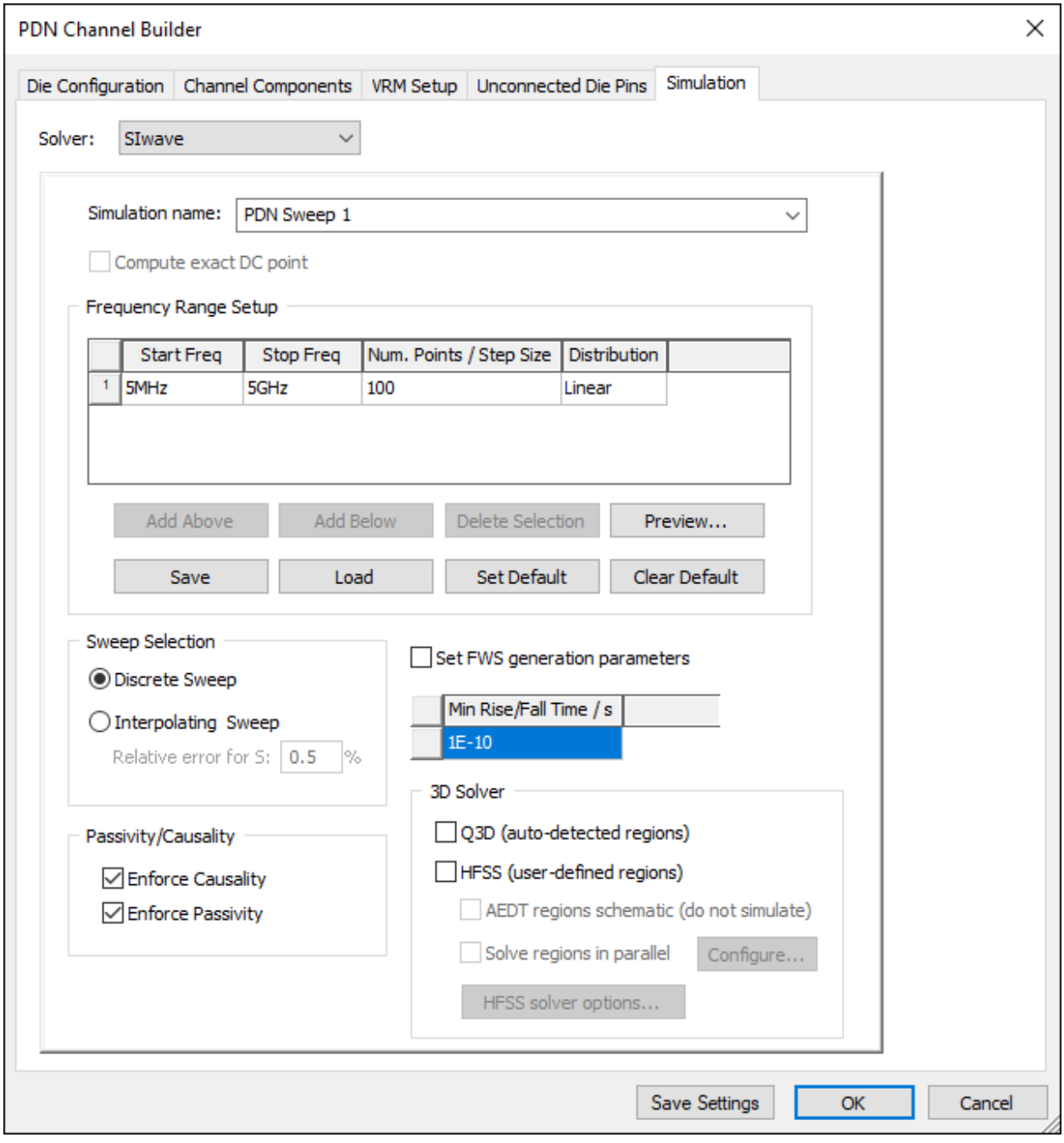

18. Use the **Solver** drop-down menu to select either **SIwave** or **PSI**.
19. From the **Simulation Name** field, enter a name or accept the default.
20. From the **Frequency Range Setup** area, add and delete rows as appropriate using the **Add Above**, **Add Below**, and **Delete Selection** buttons.
21. Click the cells and enter new values to change the **Start Freq.**, **Stop Freq.**, **Num. Points/Step Size**, and **Distribution**.

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22. From the **Sweep Selection** area, use the radio buttons to select either **Discrete Sweep** or **Interpolating Sweep**.

    If you choose an **Interpolating Sweep**, you must enter the **Relative Error** percentage. Additionally, the **Compute exact DC point** option becomes available.

23. If appropriate, check the **FWS generation parameters** check box
24. Click the cell and enter a value to set the **Min. Rise/Fall Time**.
25. From the **3D Solver** area, you can use the check boxes to select **Q3D** or **HFSS**. Q3D automatically detects regions for inclusion, while HFSS requires you to click and set **HFSS solver options**.
26. If appropriate, click **Other solver options** to change general solver settings.
27. If appropriate, click **Save Settings** to preserve simulation settings.
28. Click **OK** to start the simulation.

Signal Net Analyzer

The Signal Net Analyzer gives you the ability to get a quick idea of characteristic impedance and to rapidly generate transient voltage waveforms of pin-to-pin signal propagation. The Signal Net Analyzer generates an impedance delay plot for each trace path selected.

Traces comprising propagation paths are modeled as frequency dependent W-element transmission lines. Source/sink pins can (optionally) have IBIS driver/receiver models. When a trace passes over a cutout or void, the trace is split and the sections before and after the split may have different Z_0 values since they see different references. The Signal Net Analyzer's 2D Method of Moments (MoM) solver allows you to investigate the cross-section of the transmission line—Z_0 will be higher in the void regions. The MoM solver generates a frequency-dependent W-element for each trace segment, and a lumped RCG (no L) model for each via. You can plot the transient response using time-domain Ansys Nexxim or HSPICE.

> **Note:**
>
> Before running the Signal Net Analyzer, two preliminary steps are recommended:
>
> 1. Set the frequencies for the Signal Net Analyzer to employ in its analysis. See: Changing Signal Net Analyzer Options.
> 2. Define IBIS buffer models for any pins to be analyzed. See: Defining IBIS Models for Pins .

To use the Signal Net Analyzer in SIwave:

1. Click **Simulation**.
2. Use the **Signal Net Analyzer** drop-down menu to select **Signal Net Analyzer**.

   The **Signal Net Analyzer** window appears.

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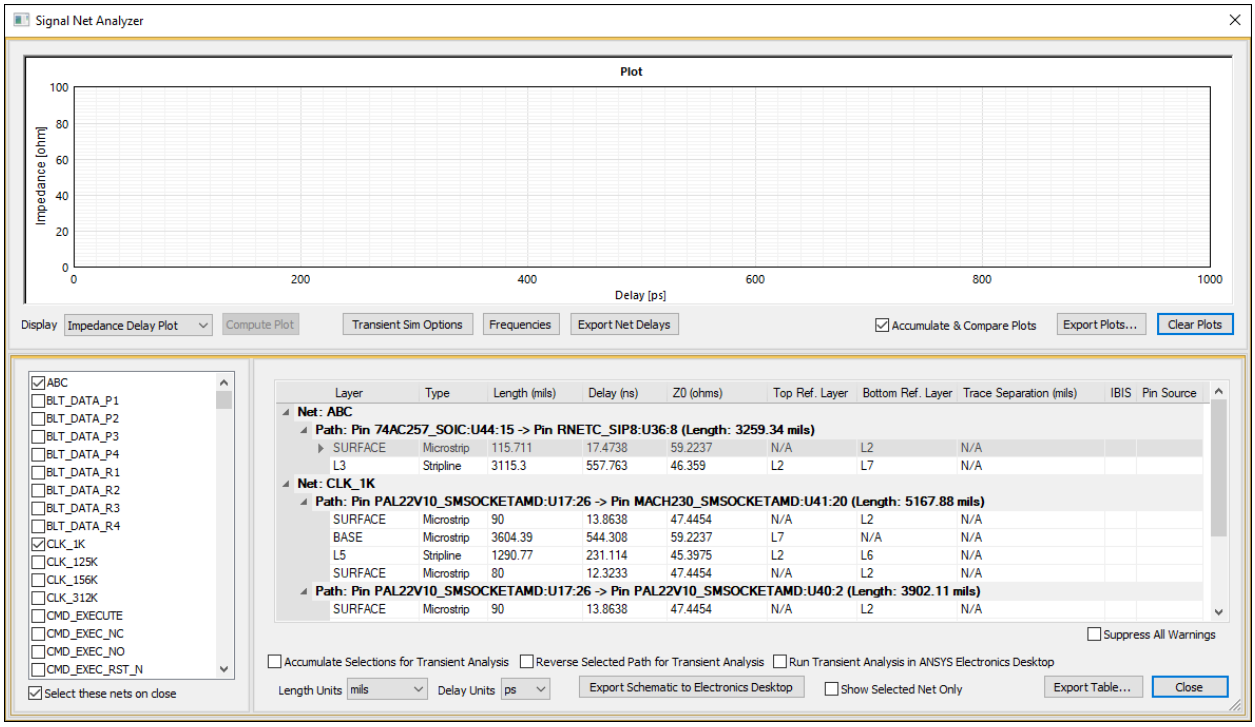

The Signal Net Analyzer window contains three panes:

- **Net Selection Pane** – located to the bottom-left, this pane allows you to select nets for analysis.

  > **Note:**
  >
  > - You must make a selection in this pane before the functionality of the Plot and Options panes will be enabled.
  > - You can also select nets by clicking objects belonging to the net in the Modeling workspace.
  > - Selecting power/ground nets will result in a warning message. You can suppress these messages from the Options pane.

- **Plot Pane** – located at the top of the window, this pane displays offers plotting options.

  From here, you can:

  - View the selected plot. Use the **Display** drop-down menu to select the type of plot you want to see (impedance vs. delay plot or transient response plot), then click **Compute Plot** to view the plot.
  - Enable or disable **Accumulate & Compare Plots**. By default, this is enabled, which allows the pane to display multiple plots. Deselect to view a single plot.

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- Reset the plot area by clicking **Clear Plots**.
- Click **Export Plots** to save the data as a *.CSV or *.TXT file.
- Click **Export Net Delays** to export a net delay report.

- **Options Pane** – located to the bottom-right, this pane allows you to view additional details about the selected net(s) and change analysis options. While nets are loading, a green progress bar in this pane shows the loading status.

  From here, you can:

  - Select units of measure for display using the drop-down menus.
  - Click **Suppress All Warnings** to ignore any warning messages.
  - Export a Circuit schematic to Electronics Desktop. Use the check boxes to select Transient analysis options, then click **Export Schematic to Electronics Desktop**. For more information on these options, consult the Circuit help.
  - Click **Export Table** to export the table of selected nets in either *.CSV or *.TXT format.

Changing Signal Net Analyzer Options

You can change the Signal Net Analyzer frequency range and coupling distance settings.

To modify these settings from SIwave:

1. Click **Simulation**.
2. Use the **Signal Net Analyzer** drop-down menu to select **Signal Net Analyzer Options**.

   The **Signal Net Analyzer Options** window appears.

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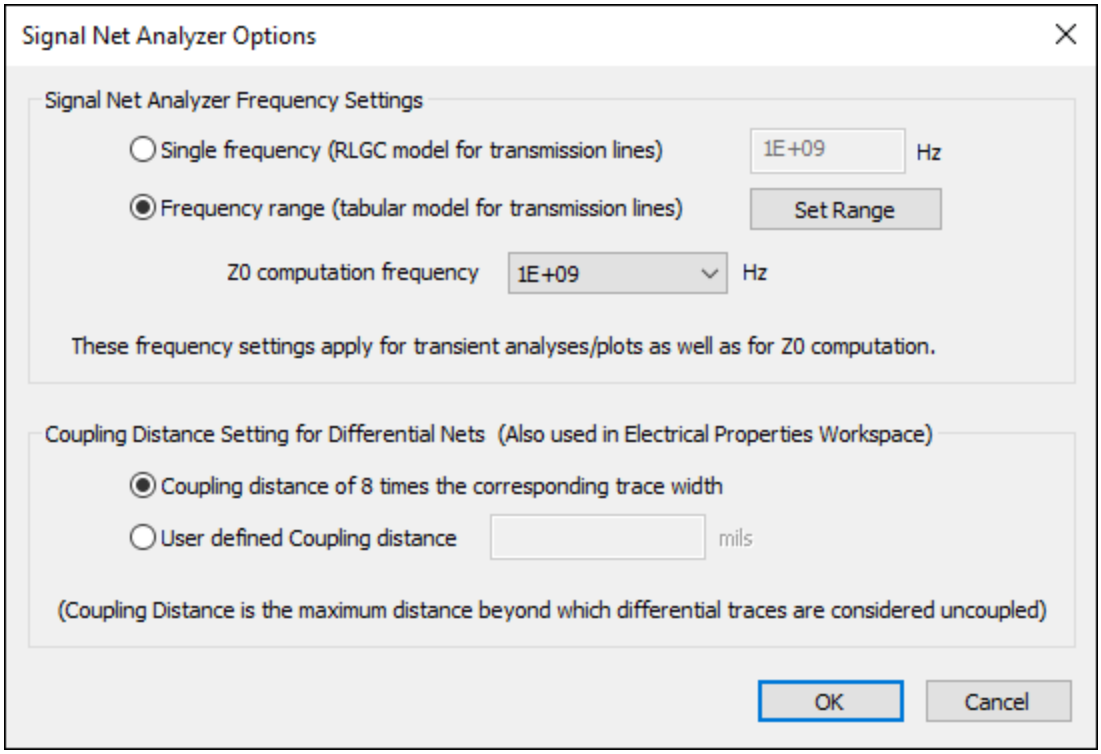

3. Use the radio buttons to select either a **Single frequency** or a **Frequency range**.
4. If you selected a range, click **Set Range**. Otherwise, proceed to Step 12.

   The **Signal Net Analyzer Frequency Set Range** window appears.

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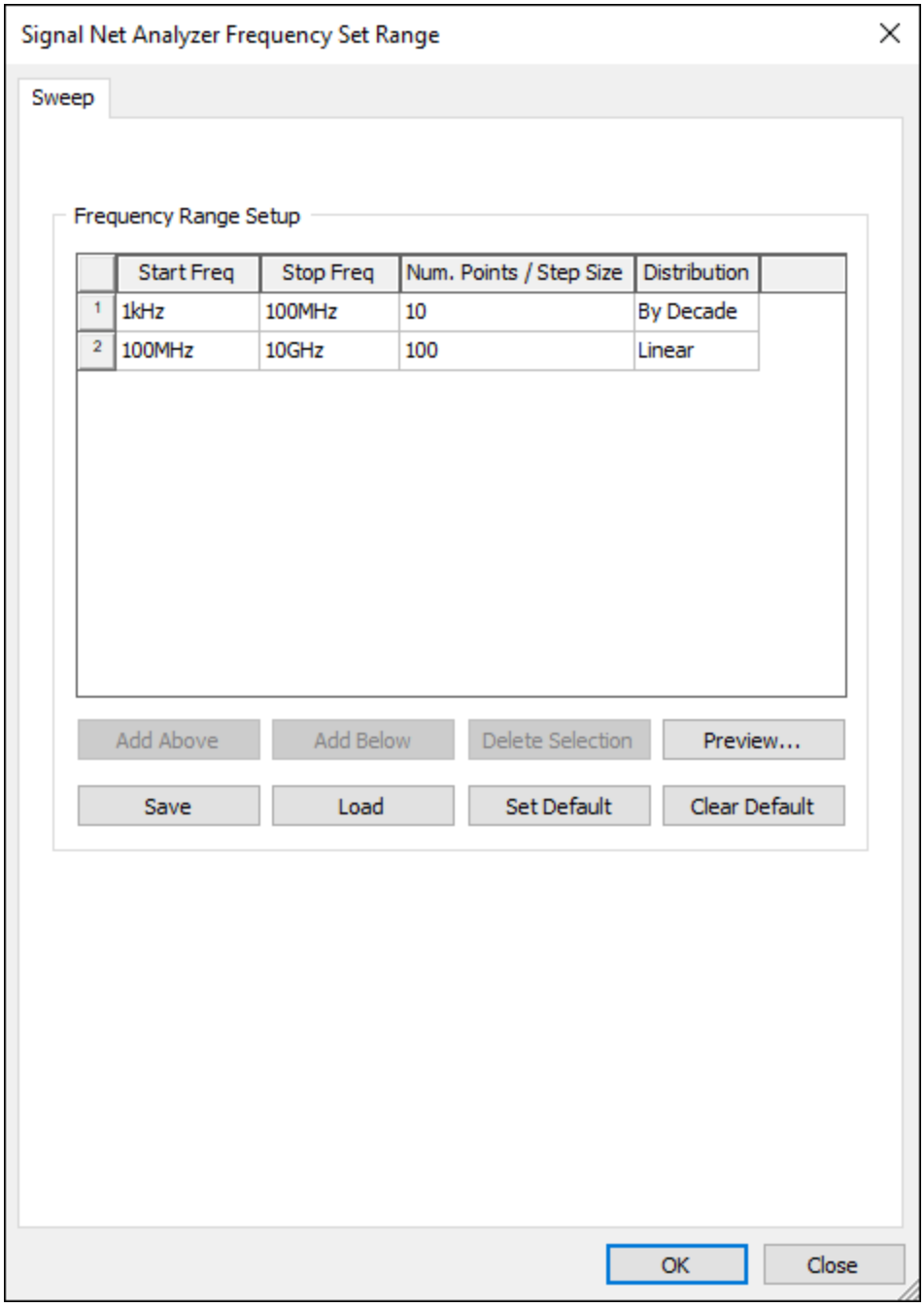

5. Enter a value for **Start Frequency**.
6. Enter a value for **Stop Frequency**.
7. Specify the **Number of Solution Points**.
8. Use the **Distribution** drop-down menu to select the method for distributing points. You can select either:

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- **Linear** – the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
- **By Decade** – distributes the number of points specified logarithmically, over each decade.

9. If appropriate, add and remove rows using the **Add Above**, **Add Below**, and **Delete Selection** buttons. You can also **Save** your settings as an SIwave Frequency Sweep Distribution File (*.sfsdf) or **Load** a previously saved file.
10. If appropriate, click **Preview** to view the frequency list.
11. Click **OK** to return to the **Signal Net Analyzer Options** window.
12. Use the **Z0 Computation Frequency** drop-down menu to select a frequency.
13. Specify the coupling distance used to locate coupling between traces during load of the SNA main grid, and during impedance plot & transient plot. The default setting is **Coupling distance of 8 times the corresponding trace width**. Change this by selecting **User defined Coupling distance** and entering a value, in mils.
14. Click **OK** to save your settings.

Viewing Impedance vs. Delay Plot

To view the characteristic Impedance vs. Delay plot:

1. Open the Signal Net Analyzer.
2. Use the Display drop-down menu to select **Impedance Delay Plot**.
3. Use the **Ctrl** or **Shift** keys to click on a path in the plot area.

> **Note:**
>
> The Impedance Delay Plot is not a Time-Domain Reflectometer (TDR), so the delay in the plot is the one-way delay (not the 2x delay you would see with a TDR). With SNA, you get an accurate characteristic impedance Z_0 for each segment without multiple reflection.

4. To view the plotted frequencies, click **Frequencies**.

   The **Frequencies** window appears showing the frequency range. If needed, you can modify

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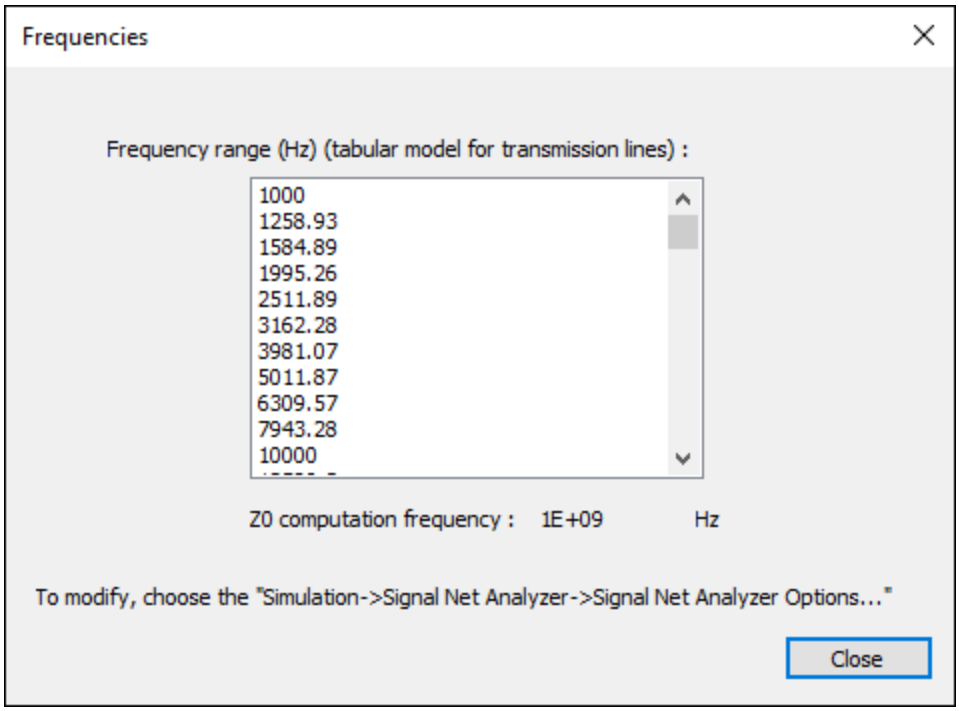
these frequencies, but you must exit the Signal Net Analyzer to do so.



Viewing Transient Response Plot

1. Open the Signal Net Analyzer.
2. Use the **Display** drop-down menu to select **Transient Response Plot**.
3. Use the **Ctrl** or **Shift** keys to click a path in the plot area.
4. Click **Transient Simulation Options**.

   The **Transient Simulation Options** window appears.

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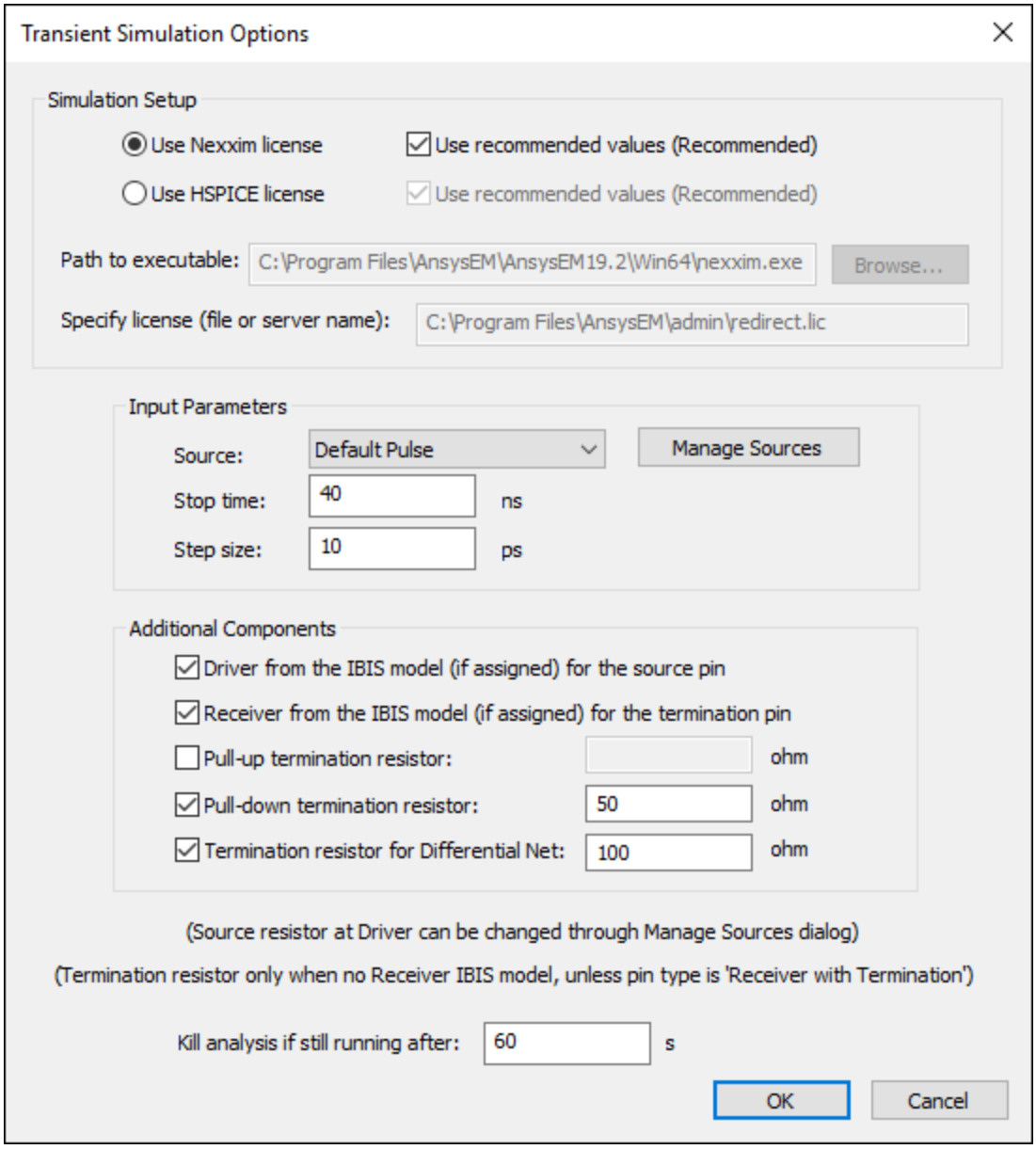

5. Configure the settings as appropriate.
   - Select either **Nexxim** or **HSPICE**, and the paths to both the executable file and license.
   - From the **Input Parameters** area, select an input source. Click **Manage Sources** to add or delete sources.
   - Enter a **Stop time** and **Step size**.
   - From the **Additional Components** area, check all appropriate options. Specify ohm values if appropriate.
   - From the **Kill Analysis if still running after** field, specify the maximum time you want to try to run the analysis. The analysis will abort after the time specified.

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6. Click **OK**.
7. Click **Compute Plot**.
8. To perform transient analysis in bulk (superimpose and compare plots), check the **Accumulate Selections for Transient Analysis** check box.
9. To manually reverse a net path, check the **Reverse Selected Path for Transient Analysis** check box.
10. To run the analysis in Ansys Electronics Desktop, check the **Run Transient Analysis in Ansys Electronics Desktop** check box. SIwave displays the netlist for the W-element, and Ansys Electronics Desktop opens to run the transient analysis and display the resulting time domain plots.

Exporting Net Delay Report

1. Open the Signal Net Analyzer.
2. From the plot pane, click **Export Net Delays**.

   The **Export Net Delay Report** window appears.

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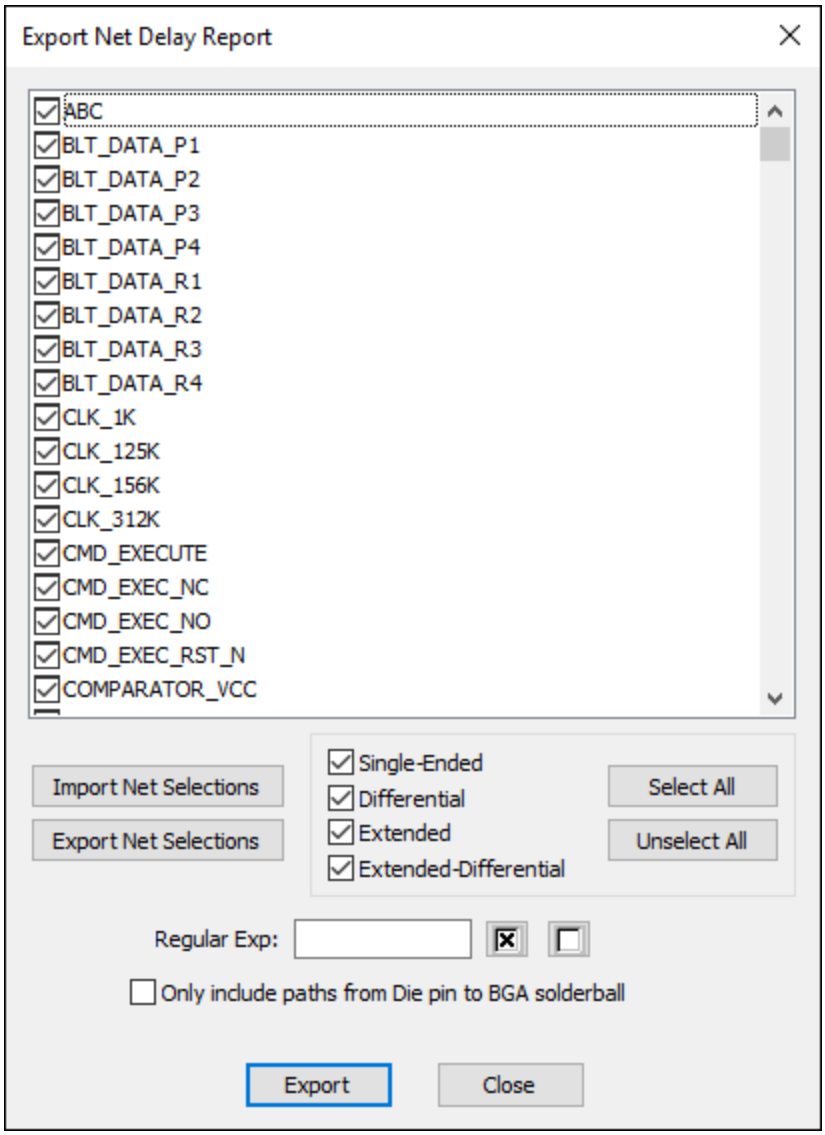

3. Select/deselect nets for the report one of several ways:
   - Select/deselect individual nets using the list.
   - Select/deselect nets by type (single-ended, differential, extended, extended-differential).
   - Select/deselect nets using regular expressions.
   - **Select All** or **Unselect All** nets.
   - Click **Import Net Selections** to import a net selections file (*.netsel).
4. If appropriate, click **Export Net Selections** to save a net selections file (*.netsel) for later import.
5. If appropriate, select **Only include paths from Die pin to BGA solderball**. When this option is enabled, only paths along nets that have a die pin on one end and a solderball on the other end will appear in the report.

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The report will note that this filter has been applied:

Report Filter: Only showing net paths that go from a Die pin to a BGA Solderball

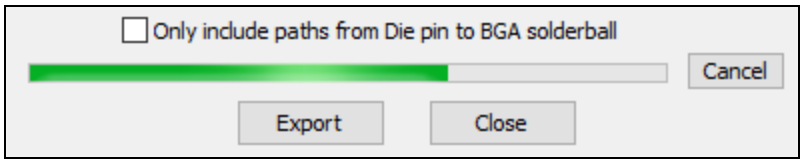
If there are no pins with a solderball applied, SIwave will warn you that the report will be empty.

6. Click **Export**.

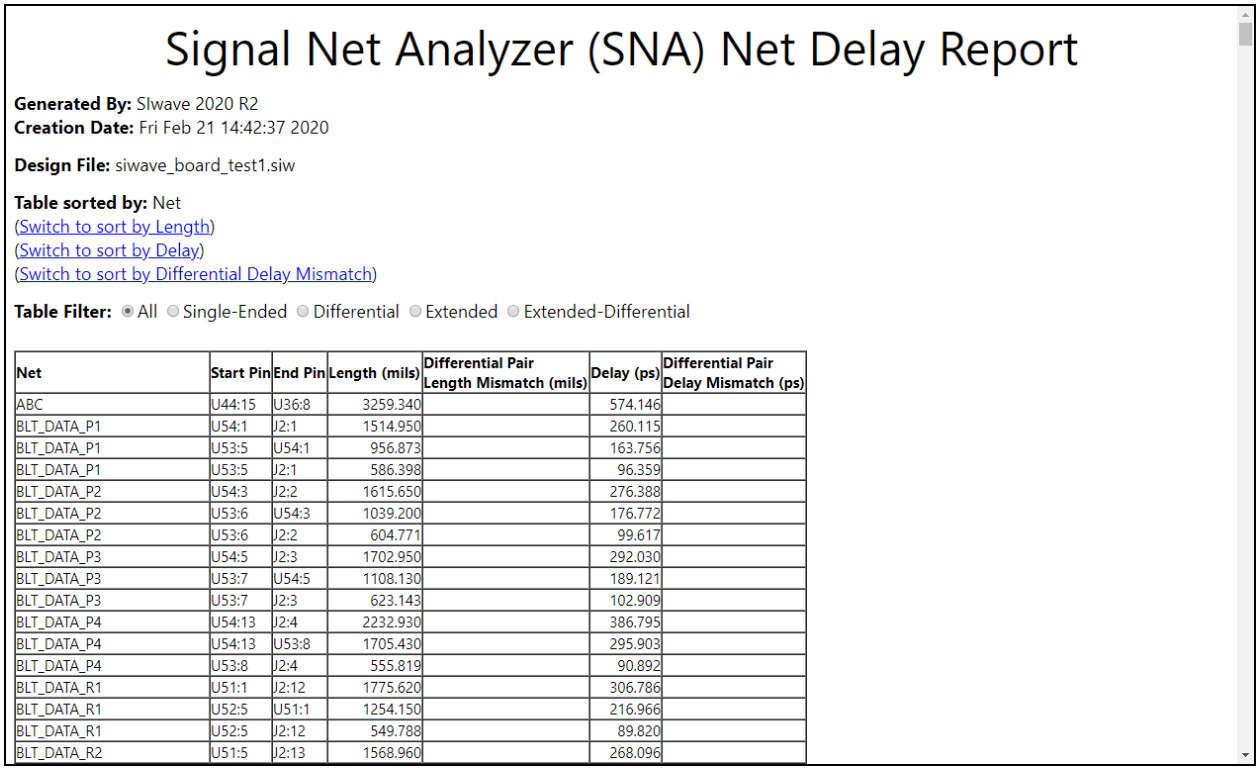
   A file browser appears.

7. Specify a file name and directory to save the report, then click **Save**.

   A progress bar appears:



When finished, the report saves to the specified location, and opens in your default HTML file viewer.



Signal Net Analyzer (SNA) Net Delay Report

Generated By: SIwave 2020 R2
Creation Date: Fri Feb 21 14:42:37 2020

Design File: siwave_board_test1.siw

Table sorted by: Net
(Switch to sort by Length)
(Switch to sort by Delay)
(Switch to sort by Differential Delay Mismatch)

Table Filter: ◉ All ○ Single-Ended ○ Differential ○ Extended ○ Extended-Differential

Net	Start Pin	End Pin	Length (mils)	Differential Pair Length Mismatch (mils)	Delay (ps)	Differential Pair Delay Mismatch (ps)
ABC	U44:15	U36:8	3259.340		574.146	
BLT_DATA_P1	U54:1	J2:1	1514.950		260.115	
BLT_DATA_P1	U53:5	U54:1	956.873		163.756	
BLT_DATA_P1	U53:5	J2:1	586.398		96.359	
BLT_DATA_P2	U54:3	J2:2	1615.650		276.388	
BLT_DATA_P2	U53:6	U54:3	1039.200		176.772	
BLT_DATA_P2	U53:6	J2:2	604.771		99.617	
BLT_DATA_P3	U54:5	J2:3	1702.950		292.030	
BLT_DATA_P3	U53:7	U54:5	1108.130		189.121	
BLT_DATA_P3	U53:7	J2:3	623.143		102.909	
BLT_DATA_P4	U54:13	J2:4	2232.930		386.795	
BLT_DATA_P4	U54:13	U53:8	1705.430		295.903	
BLT_DATA_P4	U53:8	J2:4	555.819		90.892	
BLT_DATA_R1	U51:1	J2:12	1775.620		306.786	
BLT_DATA_R1	U52:5	U51:1	1254.150		216.966	
BLT_DATA_R1	U52:5	J2:12	549.788		89.820	
BLT_DATA_R2	U51:5	J2:13	1568.960		268.096	

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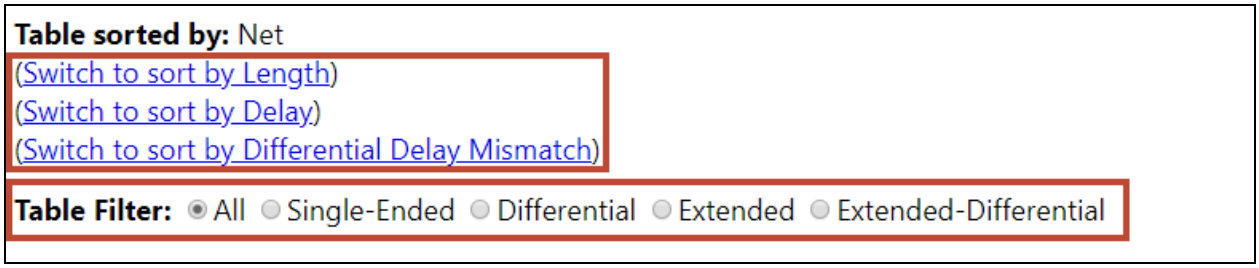
8. Use the **Switch to sort...** links and the **Table Filter** radio buttons to display your appropriate information.



Exporting Output Report

The Signal Net Analyzer output report duplicates the nets table from the Signal Net Analyzer window in either TXT or CSV format.

> **Note:**
>
> Using a script, you can also export the table in HTML format. See: ScrExportSNAReport.

To export the table from the UI:

1. Open the Signal Net Analyzer.
2. From the options pane, select nets to view them in the table.
3. From the options pane, click **Export Table**.

   The **Export Table** window appears.
4. Use the drop-down menu to select the type of file you would like to save (TXT or CSV).
5. Enter a name for the file and click **Save**.
6. When finished, the report saves to the specified location.

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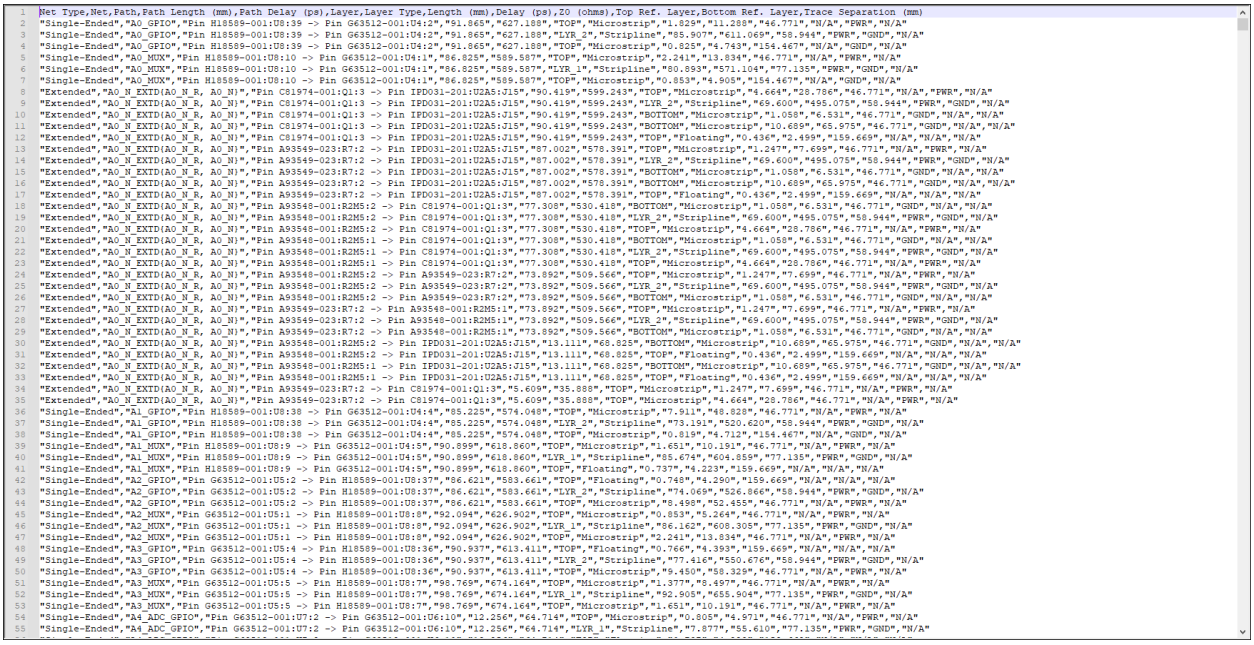
CSV Report:



```
Net Type,Net,Path,Path Length (mm),Path Delay (ps),Layer,Layer Type,Length (mm),Delay (ps),Z0 (ohms),Top Ref. Layer,Bottom Ref. Layer,Trace Separation (mm)
"Single-Ended","A0_GPIO","Pin H18589-001:U8:39 -> Pin G63512-001:U4:2","91.865","627.188","TOP","Microstrip","1.829","11.288","46.771","N/A","PWR","N/A"
"Single-Ended","A0_GPIO","Pin H18589-001:U8:39 -> Pin G63512-001:U4:2","91.865","627.188","LYR_2","Stripline","85.907","611.069","58.944","PWR","GND","N/A"
"Single-Ended","A0_GPIO","Pin H18589-001:U8:39 -> Pin G63512-001:U4:2","91.865","627.188","TOP","Microstrip","0.825","4.743","154.467","N/A","GND","N/A"
"Single-Ended","A0_MUX","Pin H18589-001:U8:10 -> Pin G63512-001:U4:1","86.825","589.587","TOP","Microstrip","2.241","13.834","46.771","N/A","PWR","N/A"
"Single-Ended","A0_MUX","Pin H18589-001:U8:10 -> Pin G63512-001:U4:1","86.825","589.587","LYR_1","Stripline","80.893","571.104","77.135","PWR","GND","N/A"
"Single-Ended","A0_MUX","Pin H18589-001:U8:10 -> Pin G63512-001:U4:1","86.825","589.587","TOP","Microstrip","0.853","4.905","154.467","N/A","GND","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin C81974-001:Q1:3 -> Pin IPD031-201:U2A5:J15","90.419","599.243","TOP","Microstrip","4.664","28.786","46.771","N/A","PWR","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin C81974-001:Q1:3 -> Pin IPD031-201:U2A5:J15","90.419","599.243","LYR_2","Stripline","69.600","495.075","58.944","PWR","GND","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin C81974-001:Q1:3 -> Pin IPD031-201:U2A5:J15","90.419","599.243","BOTTOM","Microstrip","1.058","6.531","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin C81974-001:Q1:3 -> Pin IPD031-201:U2A5:J15","90.419","599.243","BOTTOM","Microstrip","10.689","65.975","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin C81974-001:Q1:3 -> Pin IPD031-201:U2A5:J15","90.419","599.243","TOP","Floating","0.436","2.499","159.669","N/A","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin IPD031-201:U2A5:J15","87.002","578.391","TOP","Microstrip","1.247","7.699","46.771","N/A","PWR","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin IPD031-201:U2A5:J15","87.002","578.391","LYR_2","Stripline","69.600","495.075","58.944","PWR","GND","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin IPD031-201:U2A5:J15","87.002","578.391","BOTTOM","Microstrip","1.058","6.531","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin IPD031-201:U2A5:J15","87.002","578.391","BOTTOM","Microstrip","10.689","65.975","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin IPD031-201:U2A5:J15","87.002","578.391","TOP","Floating","0.436","2.499","159.669","N/A","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin C81974-001:Q1:3","77.308","530.418","BOTTOM","Microstrip","1.058","6.531","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin C81974-001:Q1:3","77.308","530.418","LYR_2","Stripline","69.600","495.075","58.944","PWR","GND","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin C81974-001:Q1:3","77.308","530.418","TOP","Microstrip","4.664","28.786","46.771","N/A","PWR","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:1 -> Pin C81974-001:Q1:3","77.308","530.418","BOTTOM","Microstrip","1.058","6.531","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:1 -> Pin C81974-001:Q1:3","77.308","530.418","LYR_2","Stripline","69.600","495.075","58.944","PWR","GND","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:1 -> Pin C81974-001:Q1:3","77.308","530.418","TOP","Microstrip","4.664","28.786","46.771","N/A","PWR","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin A93549-023:R7:2","73.892","509.566","TOP","Microstrip","1.247","7.699","46.771","N/A","PWR","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin A93549-023:R7:2","73.892","509.566","LYR_2","Stripline","69.600","495.075","58.944","PWR","GND","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin A93549-023:R7:2","73.892","509.566","BOTTOM","Microstrip","1.058","6.531","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin A93548-001:R2M5:1","73.892","509.566","TOP","Microstrip","1.247","7.699","46.771","N/A","PWR","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin A93548-001:R2M5:1","73.892","509.566","LYR_2","Stripline","69.600","495.075","58.944","PWR","GND","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin A93548-001:R2M5:1","73.892","509.566","BOTTOM","Microstrip","1.058","6.531","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin IPD031-201:U2A5:J15","13.111","68.825","BOTTOM","Microstrip","10.689","65.975","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:2 -> Pin IPD031-201:U2A5:J15","13.111","68.825","TOP","Floating","0.436","2.499","159.669","N/A","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:1 -> Pin IPD031-201:U2A5:J15","13.111","68.825","BOTTOM","Microstrip","10.689","65.975","46.771","GND","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93548-001:R2M5:1 -> Pin IPD031-201:U2A5:J15","13.111","68.825","TOP","Floating","0.436","2.499","159.669","N/A","N/A","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin C81974-001:Q1:3","5.609","35.888","TOP","Microstrip","1.247","7.699","46.771","N/A","PWR","N/A"
"Extended","A0_N_EXTD(A0_N_R, A0_N)","Pin A93549-023:R7:2 -> Pin C81974-001:Q1:3","5.609","35.888","TOP","Microstrip","4.664","28.786","46.771","N/A","PWR","N/A"
"Single-Ended","A1_GPIO","Pin H18589-001:U8:38 -> Pin G63512-001:U4:4","85.225","574.048","TOP","Microstrip","7.911","48.828","46.771","N/A","PWR","N/A"
"Single-Ended","A1_GPIO","Pin H18589-001:U8:38 -> Pin G63512-001:U4:4","85.225","574.048","LYR_2","Stripline","73.191","520.620","58.944","PWR","GND","N/A"
"Single-Ended","A1_GPIO","Pin H18589-001:U8:38 -> Pin G63512-001:U4:4","85.225","574.048","TOP","Microstrip","0.819","4.712","154.467","N/A","GND","N/A"
"Single-Ended","A1_MUX","Pin H18589-001:U8:9 -> Pin G63512-001:U4:5","90.899","618.860","TOP","Microstrip","1.651","10.191","46.771","N/A","PWR","N/A"
"Single-Ended","A1_MUX","Pin H18589-001:U8:9 -> Pin G63512-001:U4:5","90.899","618.860","LYR_1","Stripline","85.674","604.859","77.135","PWR","GND","N/A"
"Single-Ended","A1_MUX","Pin H18589-001:U8:9 -> Pin G63512-001:U4:5","90.899","618.860","TOP","Floating","0.737","4.223","159.669","N/A","N/A","N/A"
"Single-Ended","A2_GPIO","Pin G63512-001:U5:2 -> Pin H18589-001:U8:37","86.621","583.661","TOP","Floating","0.748","4.290","159.669","N/A","N/A","N/A"
"Single-Ended","A2_GPIO","Pin G63512-001:U5:2 -> Pin H18589-001:U8:37","86.621","583.661","LYR_2","Stripline","74.069","526.866","58.944","PWR","GND","N/A"
"Single-Ended","A2_GPIO","Pin G63512-001:U5:2 -> Pin H18589-001:U8:37","86.621","583.661","TOP","Microstrip","5.498","52.455","46.771","N/A","PWR","N/A"
"Single-Ended","A2_MUX","Pin G63512-001:U5:1 -> Pin H18589-001:U8:8","92.094","626.902","TOP","Microstrip","0.853","5.264","46.771","N/A","PWR","N/A"
"Single-Ended","A2_MUX","Pin G63512-001:U5:1 -> Pin H18589-001:U8:8","92.094","626.902","LYR_1","Stripline","86.162","608.305","77.135","PWR","GND","N/A"
"Single-Ended","A2_MUX","Pin G63512-001:U5:1 -> Pin H18589-001:U8:8","92.094","626.902","TOP","Microstrip","2.241","13.834","46.771","N/A","PWR","N/A"
"Single-Ended","A3_GPIO","Pin G63512-001:U5:4 -> Pin H18589-001:U8:36","90.937","613.411","TOP","Floating","0.766","4.393","159.669","N/A","N/A","N/A"
"Single-Ended","A3_GPIO","Pin G63512-001:U5:4 -> Pin H18589-001:U8:36","90.937","613.411","LYR_2","Stripline","77.416","550.676","58.944","PWR","GND","N/A"
"Single-Ended","A3_GPIO","Pin G63512-001:U5:4 -> Pin H18589-001:U8:36","90.937","613.411","TOP","Microstrip","5.450","58.329","46.771","N/A","PWR","N/A"
"Single-Ended","A3_MUX","Pin G63512-001:U5:5 -> Pin H18589-001:U8:7","98.769","674.164","TOP","Microstrip","1.377","8.497","46.771","N/A","PWR","N/A"
"Single-Ended","A3_MUX","Pin G63512-001:U5:5 -> Pin H18589-001:U8:7","98.769","674.164","LYR_1","Stripline","92.905","655.904","77.135","PWR","GND","N/A"
"Single-Ended","A3_MUX","Pin G63512-001:U5:5 -> Pin H18589-001:U8:7","98.769","674.164","TOP","Microstrip","1.651","10.191","46.771","N/A","PWR","N/A"
"Single-Ended","A4_ADC_GPIO","Pin G63512-001:U7:2 -> Pin G63512-001:U6:10","12.256","64.714","TOP","Microstrip","0.805","4.971","46.771","N/A","PWR","N/A"
"Single-Ended","A4_ADC_GPIO","Pin G63512-001:U7:2 -> Pin G63512-001:U6:10","12.256","64.714","LYR_1","Stripline","7.877","55.610","77.135","PWR","GND","N/A"
```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	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1	Net Type	Net	Path	Path Leng	Path Dela	Layer	Layer Typ	Length (m	Delay (ps)	Z0 (ohms)	Top Ref. L	Bottom Re	Trace Separation (mm)		
2	Single-Ended	A0_GPIO	Pin H1858	91.865	627.188	TOP	Microstrip	1.829	11.288	46.771	N/A	PWR	N/A		
3	Single-Ended	A0_GPIO	Pin H1858	91.865	627.188	LYR_2	Stripline	85.907	611.069	58.944	PWR	GND	N/A		
4	Single-Ended	A0_GPIO	Pin H1858	91.865	627.188	TOP	Microstrip	0.825	4.743	154.467	N/A	GND	N/A		
5	Single-Ended	A0_MUX	Pin H1858	86.825	589.587	TOP	Microstrip	2.241	13.834	46.771	N/A	PWR	N/A		
6	Single-Ended	A0_MUX	Pin H1858	86.825	589.587	LYR_1	Stripline	80.893	571.104	77.135	PWR	GND	N/A		
7	Single-Ended	A0_MUX	Pin H1858	86.825	589.587	TOP	Microstrip	0.853	4.905	154.467	N/A	GND	N/A		
8	Extended	A0_N_EXT	Pin C8197	90.419	599.243	TOP	Microstrip	4.664	28.786	46.771	N/A	PWR	N/A		
9	Extended	A0_N_EXT	Pin C8197	90.419	599.243	LYR_2	Stripline	69.6	495.075	58.944	PWR	GND	N/A		
10	Extended	A0_N_EXT	Pin C8197	90.419	599.243	BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A		
11	Extended	A0_N_EXT	Pin C8197	90.419	599.243	BOTTOM	Microstrip	10.689	65.975	46.771	GND	N/A	N/A		
12	Extended	A0_N_EXT	Pin C8197	90.419	599.243	TOP	Floating	0.436	2.499	159.669	N/A	N/A	N/A		
13	Extended	A0_N_EXT	Pin A9354	87.002	578.391	TOP	Microstrip	1.247	7.699	46.771	N/A	PWR	N/A		
14	Extended	A0_N_EXT	Pin A9354	87.002	578.391	LYR_2	Stripline	69.6	495.075	58.944	PWR	GND	N/A		
15	Extended	A0_N_EXT	Pin A9354	87.002	578.391	BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A		
16	Extended	A0_N_EXT	Pin A9354	87.002	578.391	BOTTOM	Microstrip	10.689	65.975	46.771	GND	N/A	N/A		
17	Extended	A0_N_EXT	Pin A9354	87.002	578.391	TOP	Floating	0.436	2.499	159.669	N/A	N/A	N/A		
18	Extended	A0_N_EXT	Pin A9354	77.308	530.418	BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A		
19	Extended	A0_N_EXT	Pin A9354	77.308	530.418	LYR_2	Stripline	69.6	495.075	58.944	PWR	GND	N/A		
20	Extended	A0_N_EXT	Pin A9354	77.308	530.418	TOP	Microstrip	4.664	28.786	46.771	N/A	PWR	N/A		
21	Extended	A0_N_EXT	Pin A9354	77.308	530.418	BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A		
22	Extended	A0_N_EXT	Pin A9354	77.308	530.418	LYR_2	Stripline	69.6	495.075	58.944	PWR	GND	N/A		
23	Extended	A0_N_EXT	Pin A9354	77.308	530.418	TOP	Microstrip	4.664	28.786	46.771	N/A	PWR	N/A		
24	Extended	A0_N_EXT	Pin A9354	73.892	509.566	TOP	Microstrip	1.247	7.699	46.771	N/A	PWR	N/A		
25	Extended	A0_N_EXT	Pin A9354	73.892	509.566	LYR_2	Stripline	69.6	495.075	58.944	PWR	GND	N/A		
26	Extended	A0_N_EXT	Pin A9354	73.892	509.566	BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A		
27	Extended	A0_N_EXT	Pin A9354	73.892	509.566	TOP	Microstrip	1.247	7.699	46.771	N/A	PWR	N/A		
28	Extended	A0_N_EXT	Pin A9354	73.892	509.566	LYR_2	Stripline	69.6	495.075	58.944	PWR	GND	N/A		
29	Extended	A0_N_EXT	Pin A9354	73.892	509.566	BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A		
30	Extended	A0_N_EXT	Pin A9354	13.111	68.825	BOTTOM	Microstrip	10.689	65.975	46.771	GND	N/A	N/A		
31	Extended	A0_N_EXT	Pin A9354	13.111	68.825	TOP	Floating	0.436	2.499	159.669	N/A	N/A	N/A		
32	Extended	A0_N_EXT	Pin A9354	13.111	68.825	BOTTOM	Microstrip	10.689	65.975	46.771	GND	N/A	N/A		
33	Extended	A0_N_EXT	Pin A9354	13.111	68.825	TOP	Floating	0.436	2.499	159.669	N/A	N/A	N/A		
34	Extended	A0_N_EXT	Pin A9354	5.609	35.888	TOP	Microstrip	1.247	7.699	46.771	N/A	PWR	N/A		
35	Extended	A0_N_EXT	Pin A9354	5.609	35.888	TOP	Microstrip	4.664	28.786	46.771	N/A	PWR	N/A		
36	Single-Ended	A1_GPIO	Pin H1858	85.225	574.048	TOP	Microstrip	7.911	48.828	46.771	N/A	PWR	N/A		
37	Single-Ended	A1_GPIO	Pin H1858	85.225	574.048	LYR_2	Stripline	73.191	520.62	58.944	PWR	GND	N/A		
38	Single-Ended	A1_GPIO	Pin H1858	85.225	574.048	TOP	Microstrip	0.819	4.712	154.467	N/A	GND	N/A		
39	Single-Ended	A1_MUX	Pin H1858	90.899	618.86	TOP	Microstrip	1.651	10.191	46.771	N/A	PWR	N/A		
40	Single-Ended	A1_MUX	Pin H1858	90.899	618.86	LYR_1	Stripline	85.674	604.859	77.135	PWR	GND	N/A		

- Open as raw, comma-separated data or in the program of your choice. The file is displayed in Microsoft Excel.

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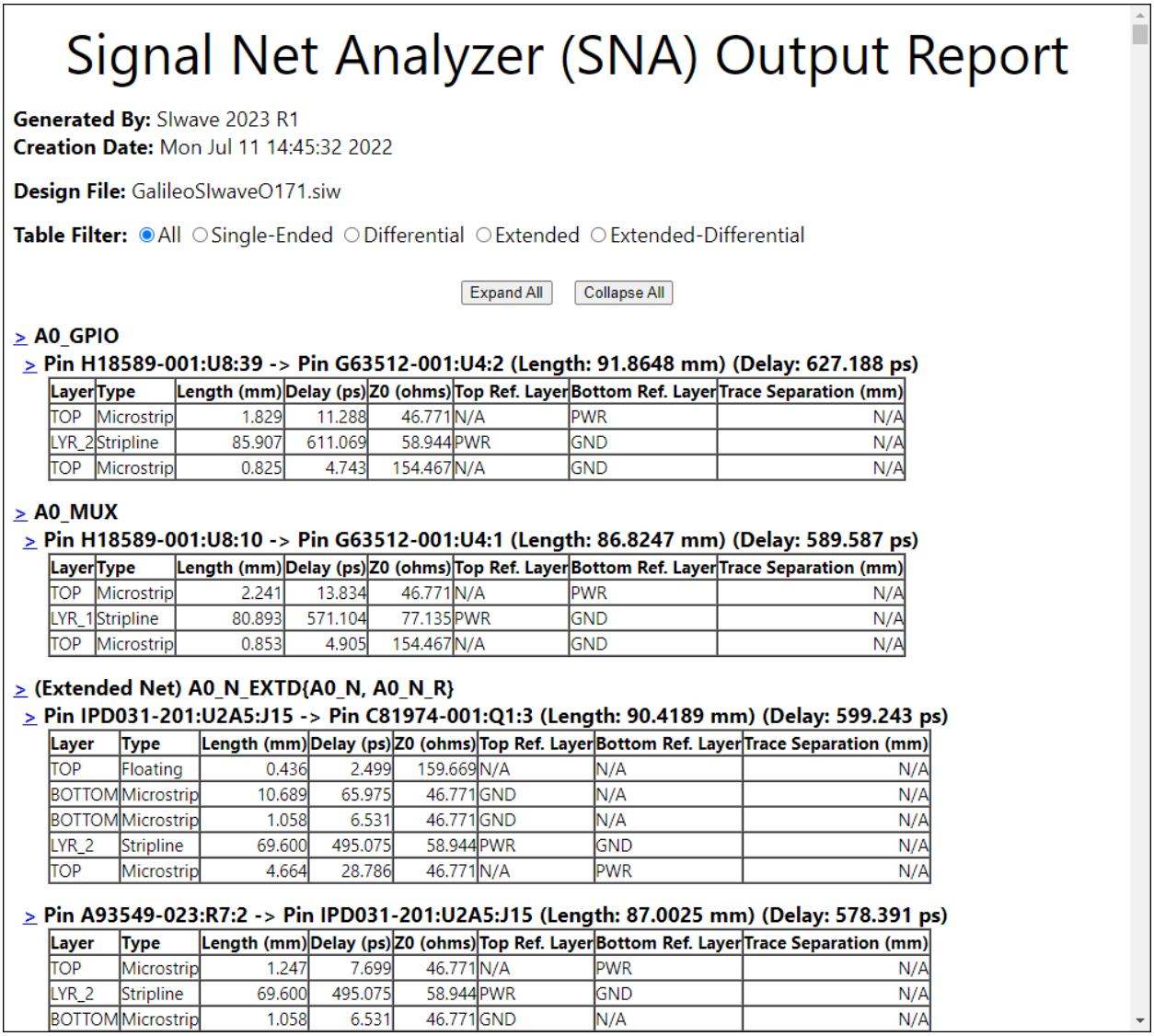
HTML Report (Exported using ScrExportSNAReport):



Signal Net Analyzer (SNA) Output Report

Generated By: SIwave 2023 R1
Creation Date: Mon Jul 11 14:45:32 2022

Design File: GalileoSIwaveO171.siw

Table Filter: ◉ All ○ Single-Ended ○ Differential ○ Extended ○ Extended-Differential

Expand All Collapse All

> **A0_GPIO**

> **Pin H18589-001:U8:39 -> Pin G63512-001:U4:2 (Length: 91.8648 mm) (Delay: 627.188 ps)**

Layer	Type	Length (mm)	Delay (ps)	Z0 (ohms)	Top Ref. Layer	Bottom Ref. Layer	Trace Separation (mm)
TOP	Microstrip	1.829	11.288	46.771	N/A	PWR	N/A
LYR_2	Stripline	85.907	611.069	58.944	PWR	GND	N/A
TOP	Microstrip	0.825	4.743	154.467	N/A	GND	N/A

> **A0_MUX**

> **Pin H18589-001:U8:10 -> Pin G63512-001:U4:1 (Length: 86.8247 mm) (Delay: 589.587 ps)**

Layer	Type	Length (mm)	Delay (ps)	Z0 (ohms)	Top Ref. Layer	Bottom Ref. Layer	Trace Separation (mm)
TOP	Microstrip	2.241	13.834	46.771	N/A	PWR	N/A
LYR_1	Stripline	80.893	571.104	77.135	PWR	GND	N/A
TOP	Microstrip	0.853	4.905	154.467	N/A	GND	N/A

> **(Extended Net) A0_N_EXTD{A0_N, A0_N_R}**

> **Pin IPD031-201:U2A5:J15 -> Pin C81974-001:Q1:3 (Length: 90.4189 mm) (Delay: 599.243 ps)**

Layer	Type	Length (mm)	Delay (ps)	Z0 (ohms)	Top Ref. Layer	Bottom Ref. Layer	Trace Separation (mm)
TOP	Floating	0.436	2.499	159.669	N/A	N/A	N/A
BOTTOM	Microstrip	10.689	65.975	46.771	GND	N/A	N/A
BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A
LYR_2	Stripline	69.600	495.075	58.944	PWR	GND	N/A
TOP	Microstrip	4.664	28.786	46.771	N/A	PWR	N/A

> **Pin A93549-023:R7:2 -> Pin IPD031-201:U2A5:J15 (Length: 87.0025 mm) (Delay: 578.391 ps)**

Layer	Type	Length (mm)	Delay (ps)	Z0 (ohms)	Top Ref. Layer	Bottom Ref. Layer	Trace Separation (mm)
TOP	Microstrip	1.247	7.699	46.771	N/A	PWR	N/A
LYR_2	Stripline	69.600	495.075	58.944	PWR	GND	N/A
BOTTOM	Microstrip	1.058	6.531	46.771	GND	N/A	N/A

- Open in your preferred internet browser.
- Use the **Table Filter** radio buttons to display an appropriate net type(s).
- Expand and hide nets and pins using the **>** links.

Computing HFSS 3D Layout Simulations

The HFSS 3D Layout feature can be utilized to perform highly accurate 3D, full-wave simulations of signal and power delivery nets in PCBs and IC packages using Ansys HFSS solver technology. This flow is optimized for planar geometry and will, by default, include any

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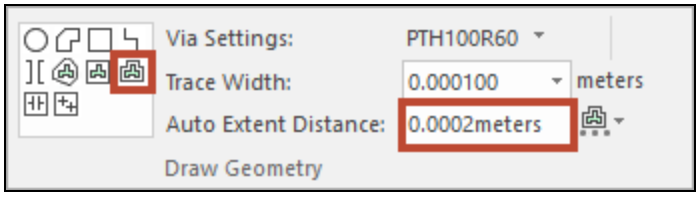
capacitors, inductors and resistors attached to the subset of geometry selected for simulation. Most port configurations considered legal for SIwave/PSI simulations are automatically converted into port configurations understood by the HFSS solver (which makes running different solvers on the same project setup trivial).

Running a simulation with HFSS 3D Layout typically involves the following steps:

1. Identify power/ground nets.
2. Select power/ground nets for analysis.
3. Enter a value for the plane extent in the **Auto Extent Distance** field, and click the **Automatically Draw Region Extent** icon just to the left of the numeric entry field to apply the extent to the selected signal nets.



   The geometric shape of the extent is outlined on the design.
4. Define HFSS 3D Layout options and launch the SYZ solver.
5. View HFSS 3D Layout results using **Results** > **HFSS 3D Layout** > **SYZ**.

You can also:

- Create reports, such as magnitude plots.
- Utilize HFSS Regions schematics.
- Run SYZ analyses in HFSS 3D Layout to bypass hierarchical restrictions.
- Configure parallel HFSS simulations.

HFSS 3D Layout Simulation Options

To define HFSS 3D Layout simulation options:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, on the **General** tab.

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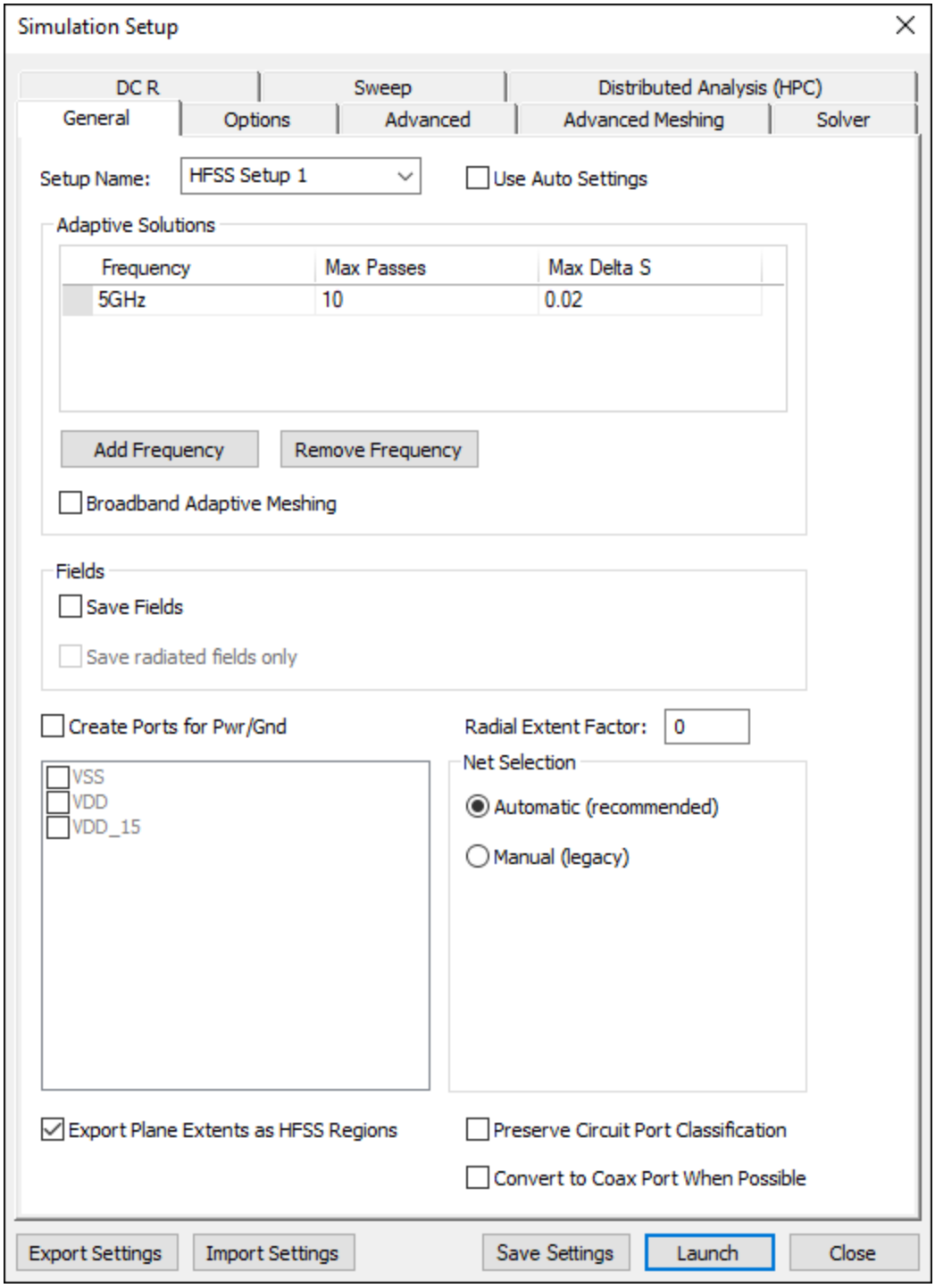

From any tab, you can click **Export Settings** to save the settings as an HFSS 3D Layout Settings File (*.dss), or click **Import Settings** to load settings from a previously saved file.

2. Select any tab to specify solver settings:

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- **General** Options
- Meshing **Options**
- **Advanced** Options
- **Advanced Meshing** Options
- **Solver** Options
- **Sweep** Options
- **DC R** Options
- **Distributed Analysis (HPC)** Options

Defining HFSS 3D Layout General Options

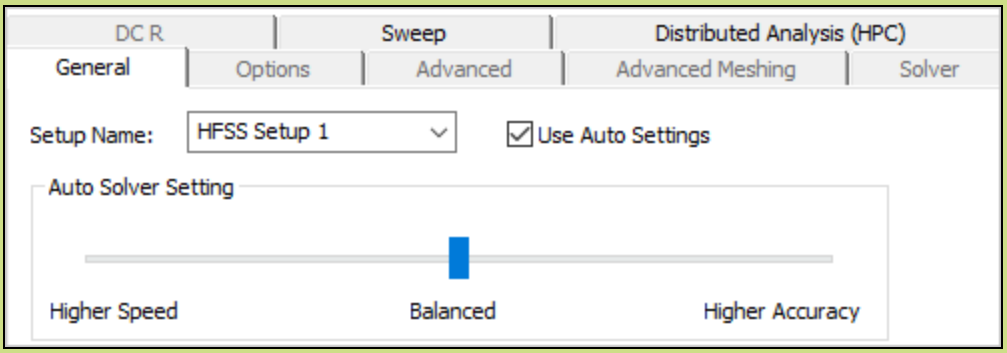
To define HFSS 3D Layout options for simulation:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

   Note:

   Selecting **Use Auto Settings** disables the Options, Advanced, Advanced Meshing, Solver, and DC R tabs. It also removes the Adaptive Solutions and Fields areas in favor of an **Auto Solver Setting** slider. Use this to select **Higher Speed**, **Balanced**, or **Higher Accuracy**.

   Specify the **General** options:

   a. Enter the **Setup Name**. This must be unique.

   b. From the **Adaptive Solutions** area:

      - Specify the solution **Frequency** and units at which to generate the solution. If a frequency sweep is solved, an adaptive analysis is performed only at the solution frequency.

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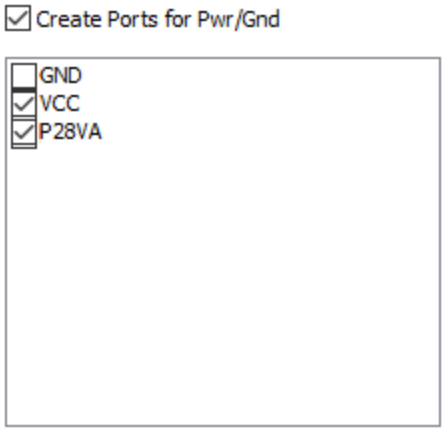
- Enter the **Max Passes** that you would like HFSS to perform. This value is a stopping criterion for the adaptive solution; if the maximum number of passes has been completed, the adaptive analysis stops. If the maximum number of passes has not been completed, the adaptive analysis will continue unless the convergence criteria are reached.
- Enter a value for the **Maximum Delta S** to specify the magnitude of the change of the S-parameters between two consecutive adaptive passes. The Maximum Delta S is a stopping criterion for the adaptive solution. If the magnitude of the change of all S-parameters are less than this value from one iteration to the next, the adaptive analysis stops. Otherwise, it continues until the requested number of passes is completed.
- If appropriate, use the check box to enable **Broadband Adaptive Meshing**.

c. From the **Fields** area:
   - Select **Save Fields** to save the calculated 3D field solutions associated with all port modes at the chosen frequencies. You can also select **Save radiated fields only**.

d. Select the **Create Ports for Pwr/Gnd** check box to add ports to the designated nets. Then select the nets from the list.



e. Specify the **Radial Extent Factor** (sizing parameter for port radius).

f. From the **Net Selection** area, select how nets in the project will be exported:
   - **Automatic** – method selects nets based on the same criteria algorithm used for determining nets to include in an SIwave SYZ simulation (any nets where we will automatically generate coaxial ports are also included).
   - **Manual** – selects nets using the same criteria used in release 2015 (uses the same logic as the MCAD exports).

g. Make optional selections:
   - **Export Plane Extents as HFSS Regions** – export the design's plane extents as HFSS regions in the HFSS 3D Layout project

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- **Preserve Circuit Port Classification** – all ports are exported as circuit ports, ignoring other selected options (e.g., **Convert to Coax Port When Possible**)
- **Convert to Coax Port When Possible** – circuit ports with a positive terminal connected to a pin and a negative terminal connected to a pin group on the same component are exported as coaxial ports

> **Note:**
>
> Consult the HFSS 3D Layout help for additional information on extents, circuit ports, and coax ports in 3D Layout simulations.

h. Click **Launch** to start the SYZ extraction.

The procedure is complete.

Defining HFSS 3D Layout Advanced Options

To define HFSS 3D Layout options for simulation:

1. **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

2. Select the **Advanced** tab.

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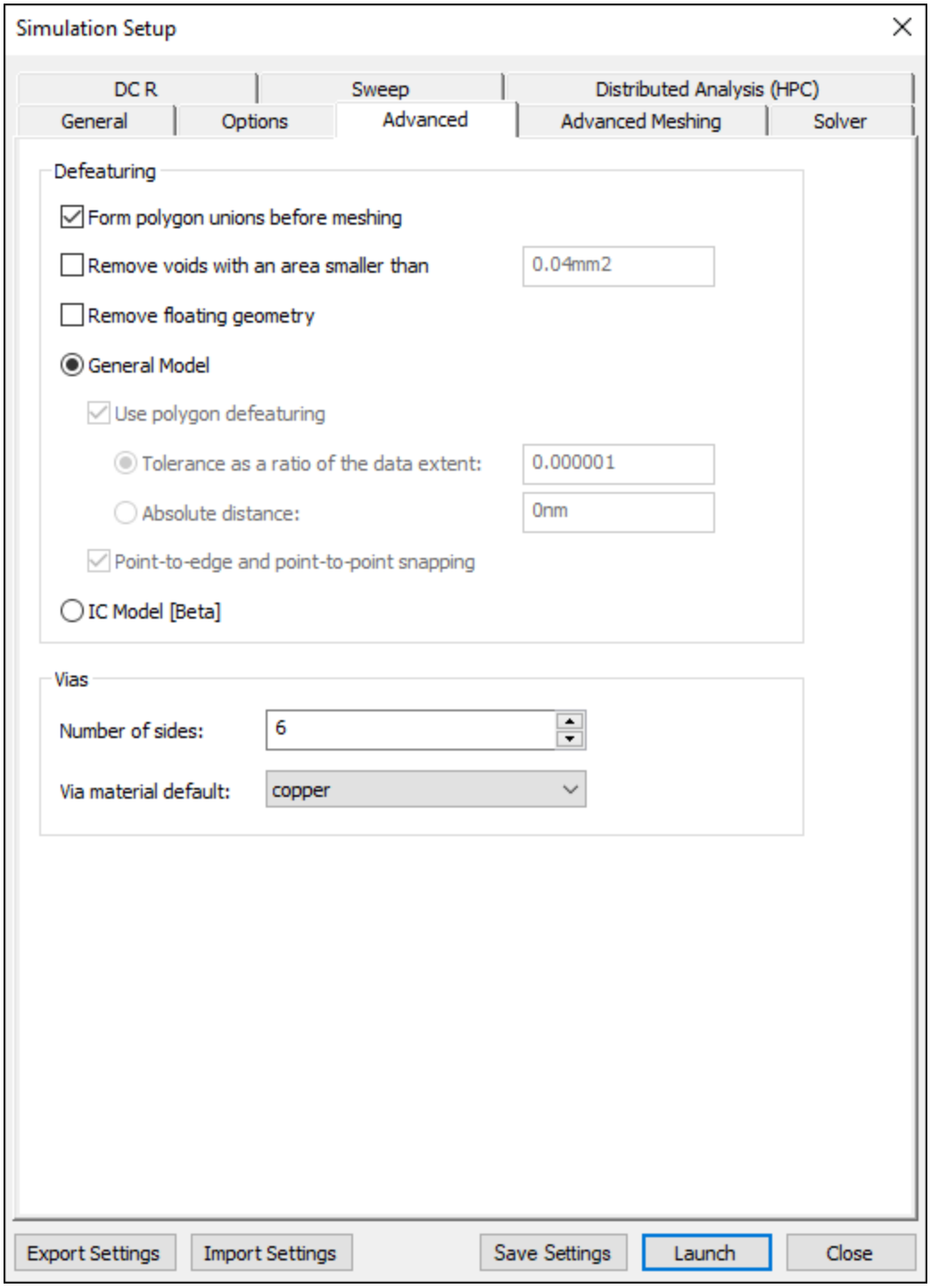

3. If appropriate, enable the **Form polygon unions before meshing** check box to specify whether all objects are combined or "unioned" before meshing takes place. This can simplify the mesh; it can, however, also remove internal boundaries that may be desirable. "Unioning" is a complex operation and sensitive to almost coincident edges; it some

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instances, a union may produce undesirable results. Inspecting the mesh is a simple way to verify the operation.

4. If appropriate, enable the **Remove voids with an area smaller than** check box and enter a value.
5. If appropriate, enable the **Remove floating geometry** check box.
6. Select either the **General Model** or **IC Model (Beta)**.
7. If applicable, specify the **General Model** options:
   a. Select the **Use polygon defeaturing** check box to remove very close points, points that don't contribute to the geometry of an edge (e.g. collinear), and very thin intrusions. When used with "unioning", it can be helpful in healing geometry that isn't snapped together.
   b. Enter a value for the **Tolerance as a ratio of the data extent**. This is specified as a ratio of the overall data extent; this value must necessarily be very small.
   c. Enter a value for the **Absolute distance** for polygon defeaturing.
   d. If appropriate, enable **Point-to-edge and Point-to-point snapping**.
8. Select the **Number of sides** to use when creating the 3D representation of vias; if less than 3, the via is modeled as a flat ribbon. Vias may be modeled as a simple 'wirebond' or as a 3D ribbon or solid. The values specified in the analysis setup only apply to vias that do not have specific property overrides; all properties explicitly specified for a via take precedence over these values.
9. Select the **Via material default**. When a material has not been specified in the padstack definition and there is no override in the properties for a via, then this material will be associated with the via mesh.
10. Click **OK**.

Defining HFSS 3D Layout Meshing Options

To define HFSS 3D Layout meshing options for simulation:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

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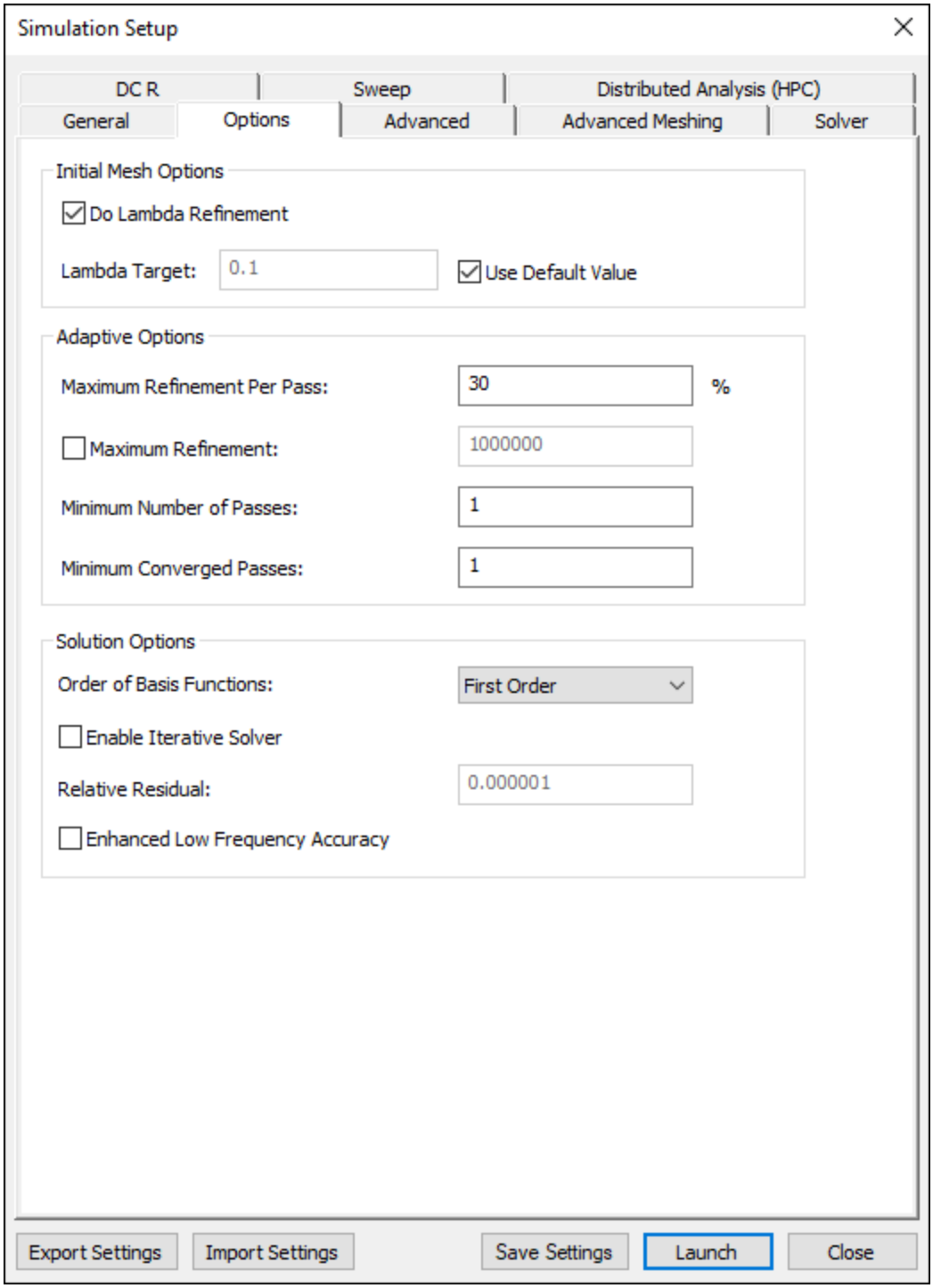
2. Select the **Options** tab.



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> **Note:**
>
> If you selected **Use Auto Settings** on the **General** tab, the **Options** tab will be unavailable.

3. Specify the **Initial Mesh Options** that define the initial mesh:
   a. Select **Do Lambda Refinement** to refine the initial mesh based on the material-dependent wavelength.
   b. Enter a value for the **Lambda Target**. This represents the fraction of the wavelength that determines the refined tetrahedra edge length, e.g. if the value is 0.1, then an edge length of 0.1*lambda is used as the refinement target.
   c. Click **Use Defaults** to use the default settings. The Target defaults depend on the **Order of Basis Function** selections (e.g., for driven solutions and a first order basis function, the default target is 0.3333; HFSS will refine the mesh until most element lengths are approximately one-third wavelength).
4. Specify the **Adaptive Options**.
   a. Enter a value for the **Maximum Refinement Per Pass**. This determines how many tetrahedra are added at each iteration of the adaptive refinement process. The tetrahedra with the highest error will be refined. The value is a percentage.
   b. Select the **Maximum Refinement** check box to specify the maximum number of tetrahedra that can be added during an adaptive pass. By default, this unchecked, to that there is no maximum.
   c. Enter a value for the **Minimum Number of Passes** that you would like HFSS to perform. This value is a stopping criterion for the adaptive solution; if the maximum number of passes has been completed, the adaptive analysis stops. If the maximum number of passes has not been completed, the adaptive analysis will continue unless the convergence criteria are reached.
   d. Enter a value for the **Minimum Converged Passes.** An adaptive analysis will not stop unless the minimum number of converged passes has been completed. The convergence criteria must be met for at least this number of passes before the adaptive analysis will stop.
5. Specify the **Solution Options**.
   a. Use the **Order of Basis Functions** drop-down menu to select **Zero Order**, **First Order**, **Second Order**, or **Mixed Order**.
   b. If appropriate, use the check box to **Enable Iterative Solver**. When this is enabled, the **Relative Residual** value can be changed.
   c. If appropriate, use the check box to enable **Enhanced Low Frequency Accuracy**.
6. Click **OK**.

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Defining HFSS 3D Layout Advanced Meshing Options

To define HFSS 3D Layout options for simulation:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

2. Select the **Advanced Meshing** tab.

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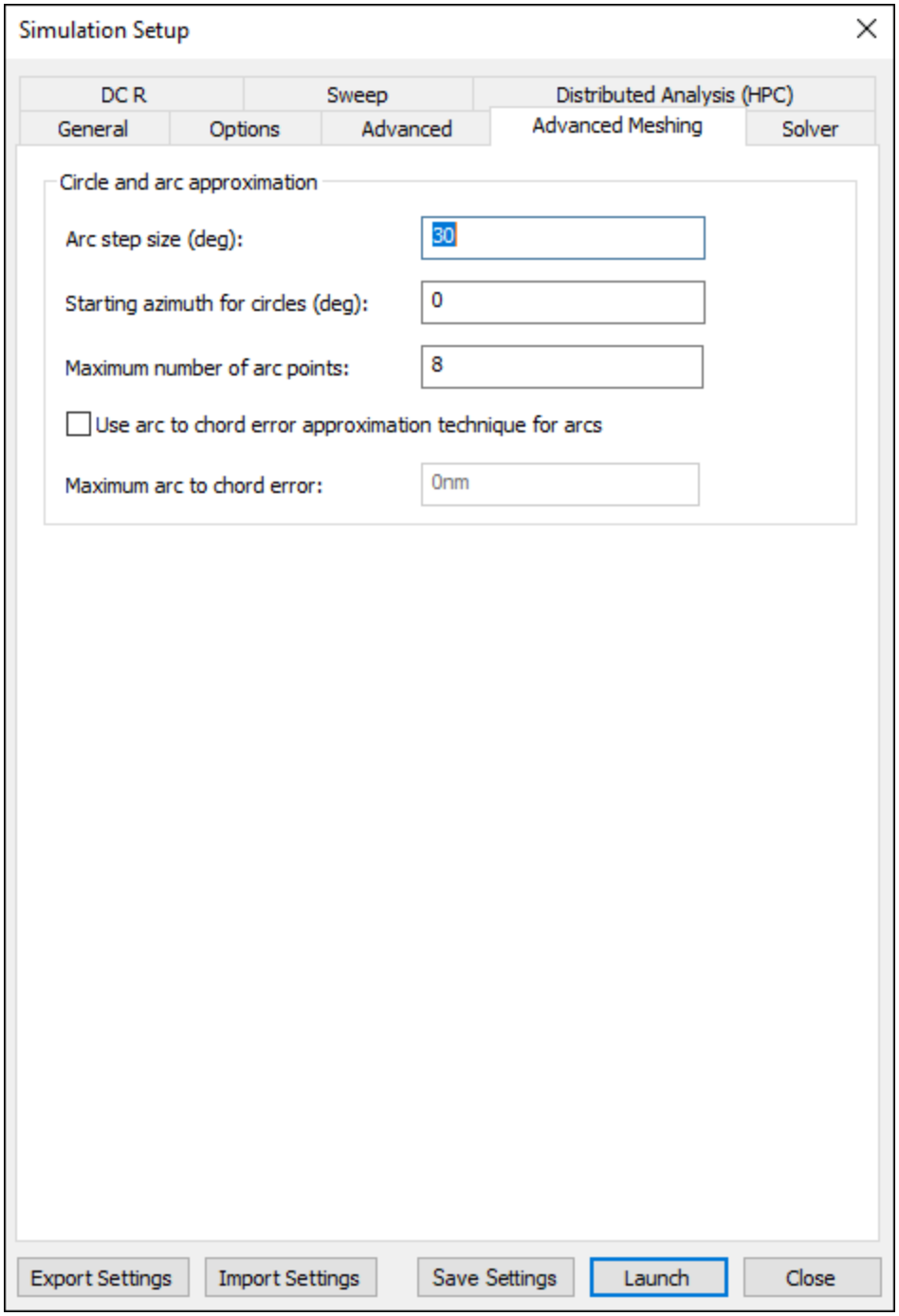

3. Specify the **Circle and arc approximation** values. Circles and arcs must be replaced with straight edge approximations before meshing. There is no attempt to match areas; points are simply introduced on the original arc at the locations specified by the following parameters.

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4. Enter a value for the **Arc setup size**. This is the angular interval below which mesh points are added.
5. Enter a value for the **Starting azimuth for circles**. This specifies the location of the first mesh point or circles.
6. Enter a value for the **Maximum number of arc points**. These are the maximum number of mesh points on a given arc segment.
7. Select the **Use arc to chord error approximation technique for arc** if you do not want: the resulting straight edge approximation to deviate from the original arc by more than the specified error.
8. Enter a value for the **Maximum arc to chord error**. This is the maximum distance permissible between a straight edge approximation (the chord) and the original arc.
9. Click **OK**.

Defining HFSS 3D Layout Solver Options

To define HFSS 3D Layout options for simulation:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

2. Select the **Solver** tab.

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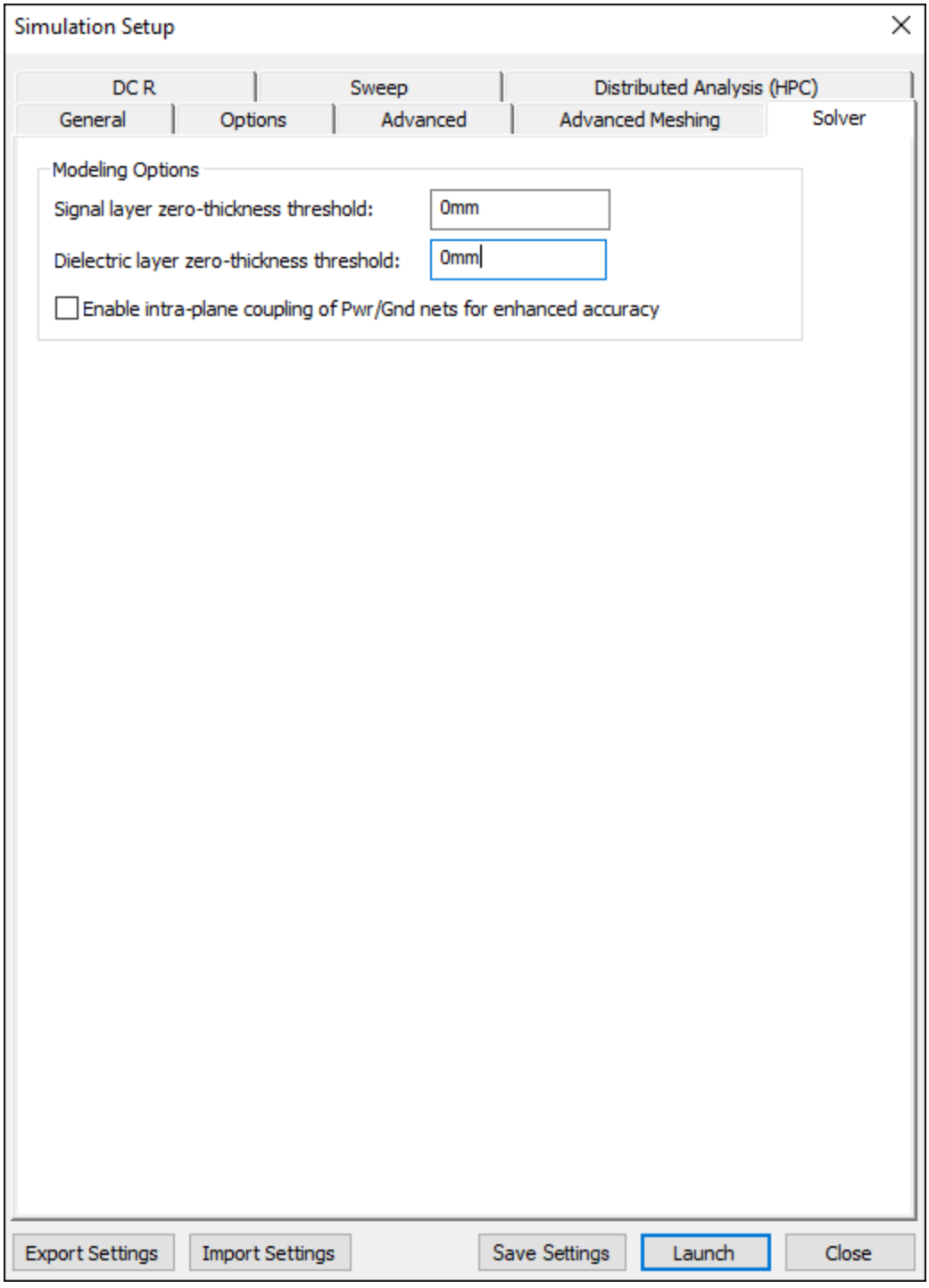

3. Enter a value for the **Signal layers zero-thickness threshold**. Negative signal layers in the design which are thinner than the given value are modeled as being infinitely thin in order to reduce simulation time.

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4. Enter a value for the **Dielectric layer zero-thickness threshold.** Dielectric layers in the design which are thinner than the given value are merged into an adjacent dielectric; material properties are accumulated using a weighted average.
5. If appropriate, use the check box to **Enable intra-plane coupling of Pwr/Gnd nets for enhanced accuracy**.
6. Click **OK**.

Defining HFSS 3D Layout Sweep Options

To define HFSS 3D Layout options for simulation:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

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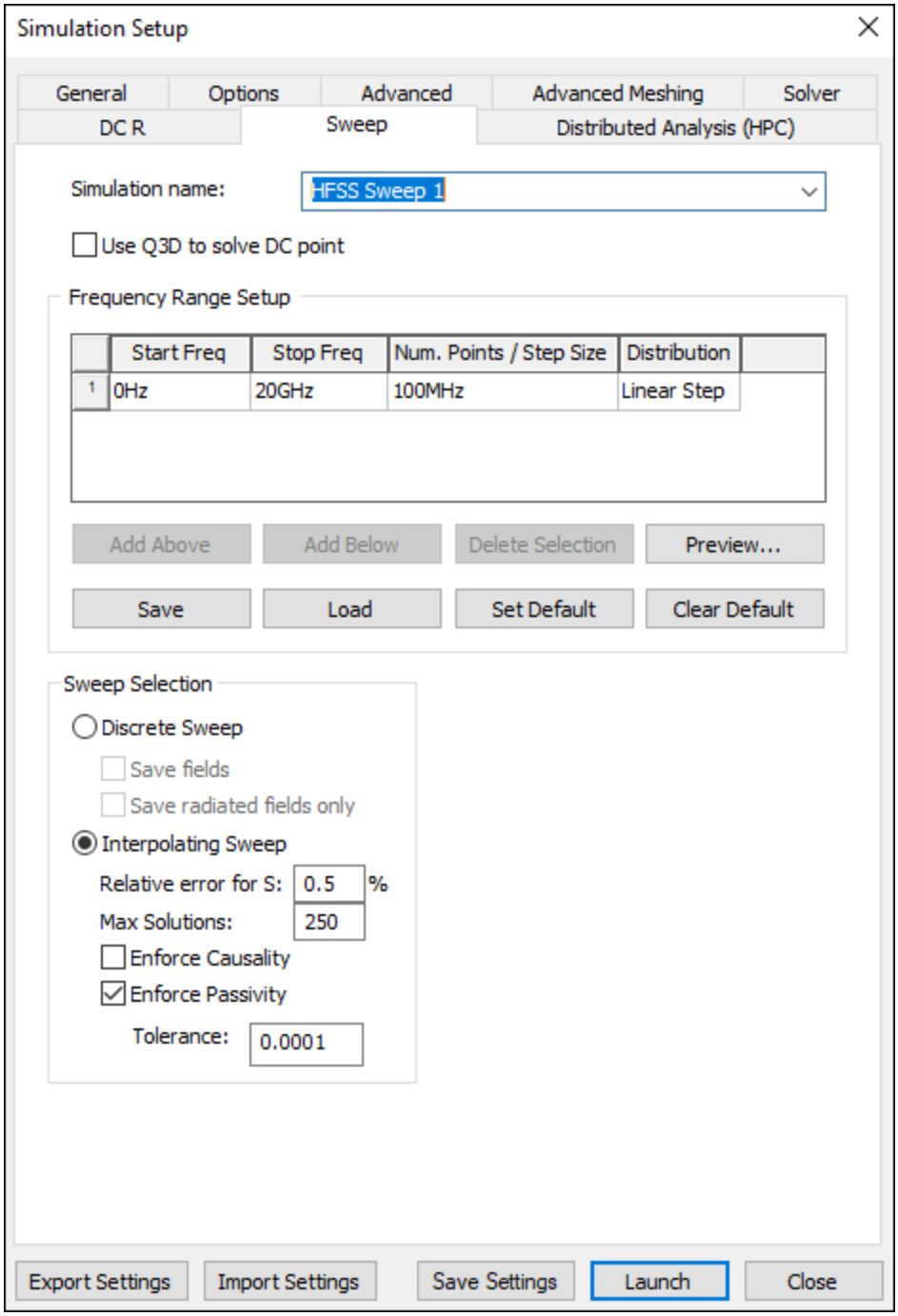
2. Select the **Sweep** tab.



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> **Note:**
>
> If you accessed this tab from the SYZ Sweep options window, the frequency range cannot be specified because it is defined in the SYZ setup.

3. Enter the **Simulation name**.
4. Optionally, click on the check box to **Use Q3D to solve DC point**.
5. Enter the value for **Start Frequency**.
6. Enter the value for **Stop Frequency**.
7. Specify the **Number of Solution Points**.
8. Select the method for distributing points from the **Distribution** option. You can select either:
   - **Linear** – the difference between the start frequency and the stop frequency is calculated and is divided by the number of solution points.
   - **By decade** – distributes the number of points specified logarithmically, over each decade.
9. To preview all the frequency points, click the **Preview** button. The **Frequency List Preview** window appears showing all the points.
10. Click **Save** to save the grid values to a file. The **Save As** window appears. Select the location to store the saved file. Enter the name for the file in the **File name** field. Select the file type from the **Save as type** list. You can save files with .sfsdf (SIwave Frequency Sweep Distribution File) extensions. Click **Save**.
11. Click **Load** buttons are to load the grid values from a file. The **Open** window appears. Select the file you want to open. You can open saved .sfsdf (SIwave Frequency Sweep Distribution File) files. Click **Open**.
12. Click the **Set Default** button to set the current grid settings as a default value for that simulation type. When a default value has been set, the window for that simulation type will always be populated with those settings when the window is opened.
13. Click the **Clear Default** button to remove the default setting and return the population of the grid to its normal behavior.
14. Select the type of sweep you want from the **Sweep Selection** box. You can select either:
    - Discrete
    - Interpolating - If you select this option, you will have to specify the **Relative error for S**.

    An interpolating sweep estimates a frequency response for an entire frequency range by solving at a relatively small number of frequency points within that range. Between the actual solution frequencies, the frequency response is obtained by rational interpolation. HFSS adaptively chooses the frequency points at which it computes the field solution. After a new frequency point is solved, a new interpolating fit is generated. This is compared to the

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interpolant from the previous step, and the maximum difference between the two is determined. If the difference exceeds the requested tolerance, then a new frequency point is chosen for a solution. The interpolating sweep is complete when the difference between successive interpolants is less than the error tolerance criterion.

15. Click **OK**.

Defining HFSS 3D Layout DC R Options

To define HFSS 3D Layout options for simulation:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

2. Select the **DC R** tab.

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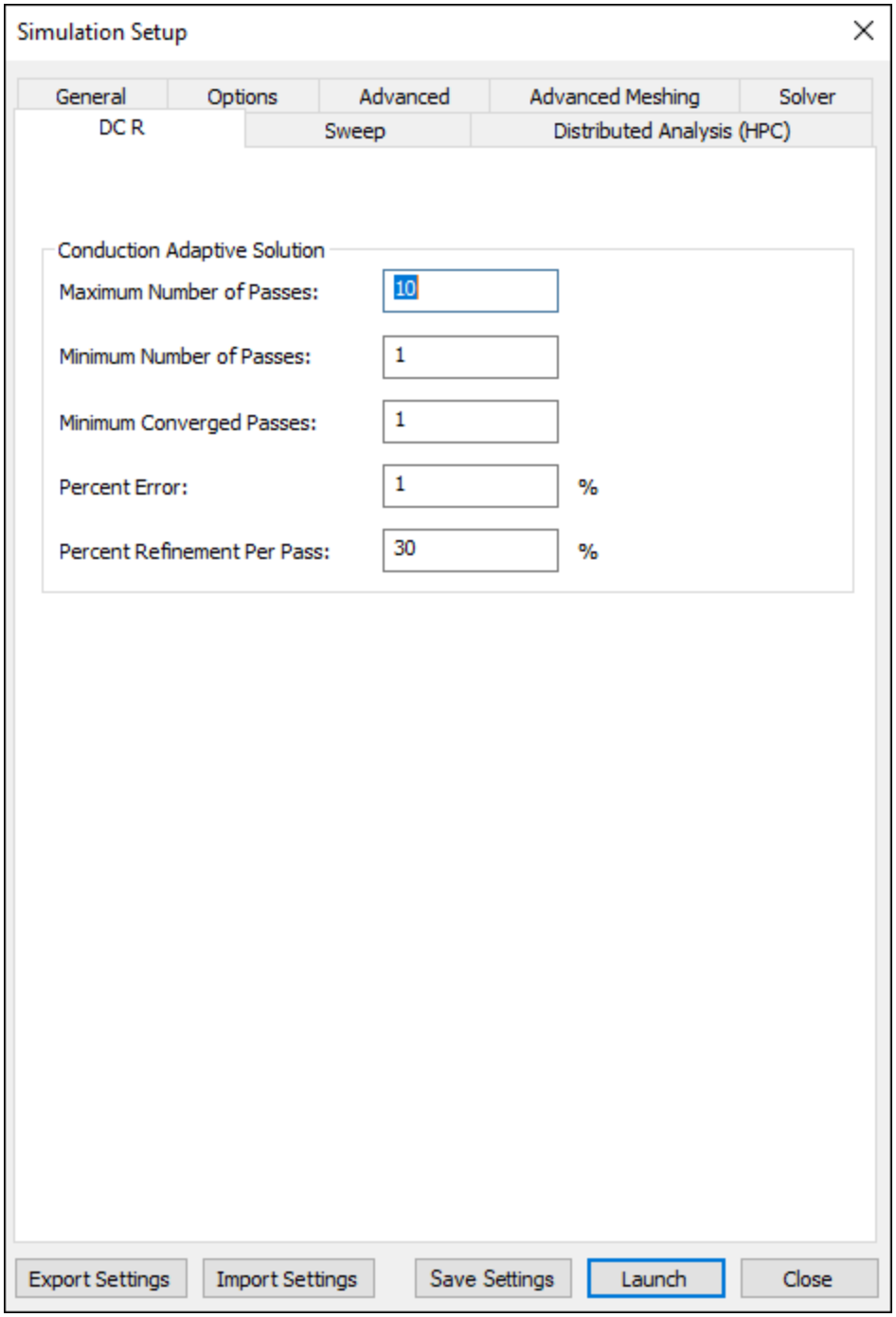

3. Enter the **Solver Residual**.
4. Specify the **Conduction Adaptive Solution** options:

   a. Enter a value for the **Maximum Refinement Per Pass**. This determines how many tetrahedra are added at each iteration of the adaptive refinement process. The

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tetrahedra with the highest error will be refined. The value is a percentage.

b. Enter a value for the **Minimum Number of Passes** that you would like HFSS to perform. This value is a stopping criterion for the adaptive solution; if the maximum number of passes has been completed, the adaptive analysis stops. If the maximum number of passes has not been completed, the adaptive analysis will continue unless the convergence criteria are reached.
c. Enter a value for the **Minimum Converged Passes.** An adaptive analysis will not stop unless the minimum number of converged passes has been completed. The convergence criteria must be met for at least this number of passes before the adaptive analysis will stop.
d. Enter a value for the **Percent Error**. This lets you control an appropriate solution accuracy. Smaller values produce more accurate (but slower) solutions; larger values produce less accurate (but faster) solutions.
e. Enter a value for the **Percent Refinement Per Pass**. This value determines how many mesh elements are added at each iteration of the adaptive refinement process. The mesh element with the highest error are refined.

5. Click **OK**.

Defining HFSS 3D Layout Distributed Analysis (HPC) Options

To specify a distributed analysis over multiple machines, click the Distributed Analysis (HPC) tab:

1. Click **Simulation** > **HFSS 3D Layout**.

   The **Simulation Setup** window appears, with the **General** tab selected.

2. Select the **Distributed Analysis (HPC)** tab.

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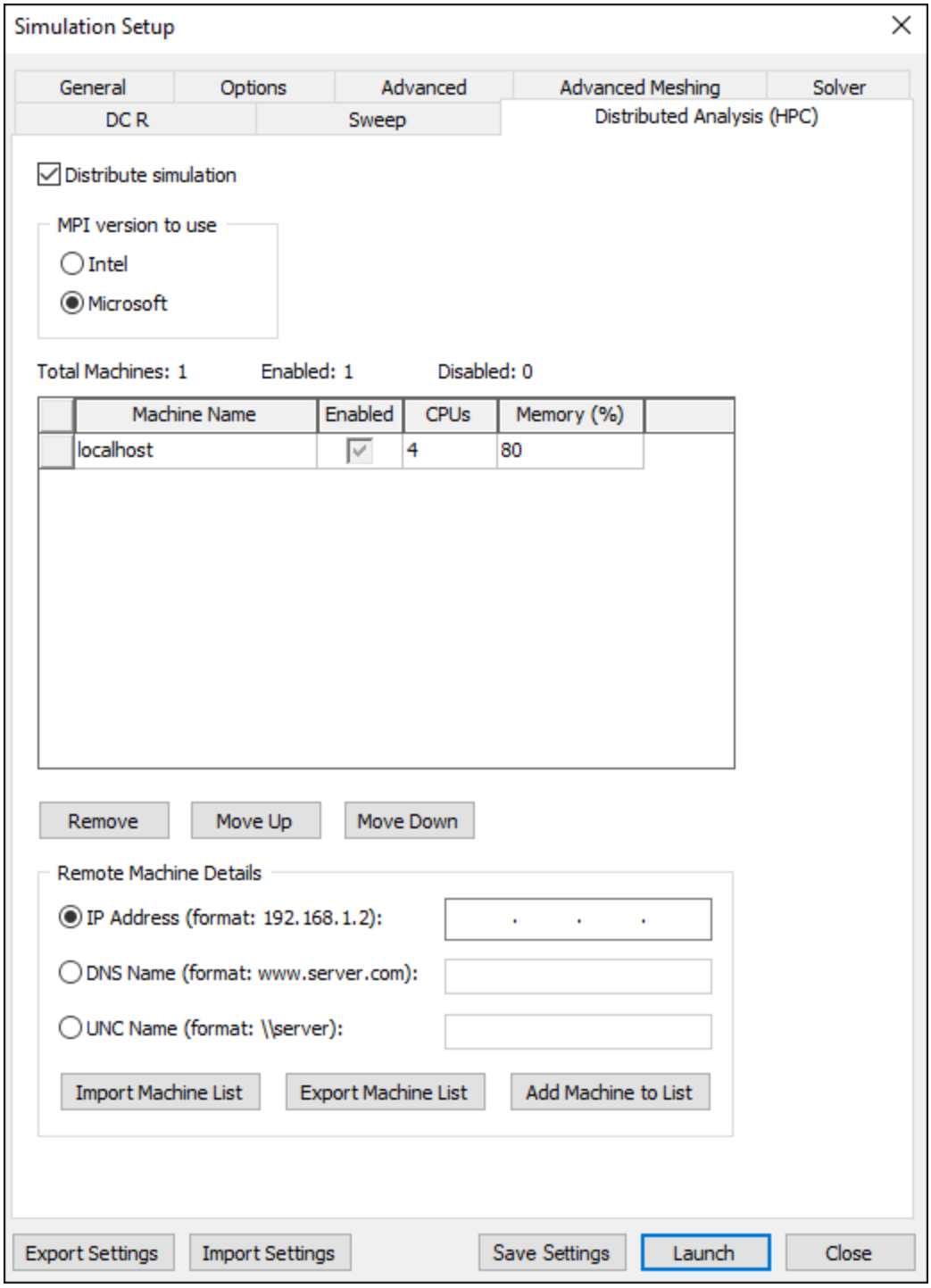

3. To enable distributed analysis, click the **Distribute simulation** check box.
4. For **MPI Version to use**, select either **Intel** or **Microsoft**.

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5. Use the window panels to specify the remote machines to be added to or removed from the simulation. You can add machines from a file, and save the machine list to a separate file.
6. Use the **Enabled** boxes to enable one or more machines for the distributed analysis. You can enable or disable the listed machines according to circumstance. Above the table, the window gives a count of the total machines along with how many are enabled/disabled. The HFSS solver in 3D Layout supports automatic settings and assigns resources automatically, based on the best use of them for the current analysis.
7. For each machine to add manually, specify the **IP Address**, the **DNS Name**, or the **UNC Name**. The remote machines must have the same version installed in the same OS and version, and have the RSM service active.
8. Use the **Move Up** and **Move Down** buttons to sequence the list of machines. Tasks are assigned to machines starting with the first enabled machine in the list.
9. After you have specified the remote machine details, you can **Import Machine List**. The **Select machine list file to load** window appears. Select the file you want to import, and click **Open**.

   Each line of the file can contain a machine specifier of the form:

   ```
   <MachineName>: Enabled: <NumCores> : <Mem%>
   ```

10. To export the machine list as a text file, click **Export Machine list**. The **Select machine list file output file name** window appears. Select the file you want to export, and click **Save**.
11. Click **OK**.

Exporting an HFSS Regions Schematic

HFSS simulations in **SIwave** are fully automated. When the solver launches, regions are clipped from the design, appropriate ports are placed on signal nets and HFSS is invoked on each region sequentially to generate S-matrices, which are then automatically wired into the SIwave simulation as n-port blocks. All of this happens behind the scenes.

> **Note:**
>
> Users can elect to export the HFSS setup as a schematic. This affords users greater control and visibility into the HFSS region setups.

Each HFSS region is modeled as a separate HFSS 3D Layout project, and an additional project is created to model what remains after the regions are separated. Ports at region interfaces are automatically created. Once the projects are created, a schematic is generated that connects the regions and the SIwave geometry. A Nexxim LNA sweep setup (matching the S-parameter sweep defined in SIwave) is inserted and the schematic is ready for simulation. Prior to initiating the simulation, which analyzes each associated project using the dynamic link framework, users can examine and modify the projects, as appropriate.

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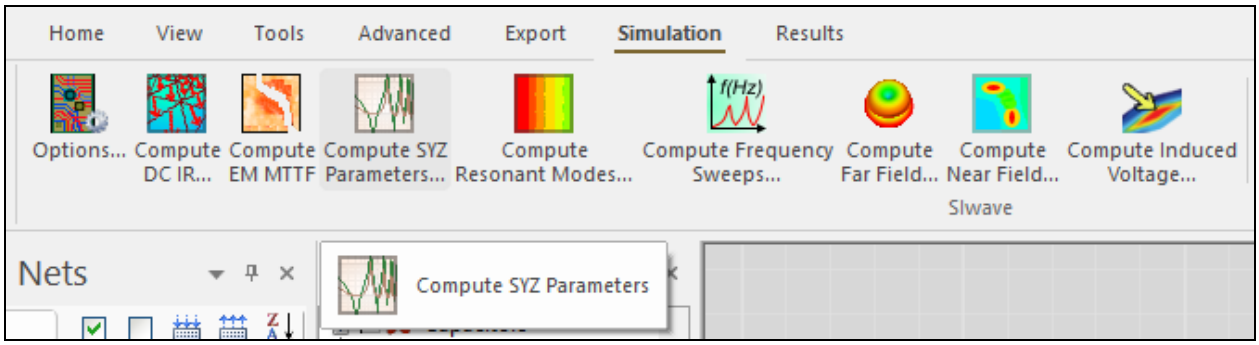
> **Important:**
>
> If done incorrectly, modifiying ports at region interfaces can invalidate the schematic level connections and will require user intervention to rectify.

Complete the following steps to export an HFSS regions schematic from SIwave.

1. If appropriate, open an appropriate project in **SIwave**.
2. From the **Simulation** tab, select **Compute SYZ Parameters**.



The **Compute SYZ-parameters** window opens.

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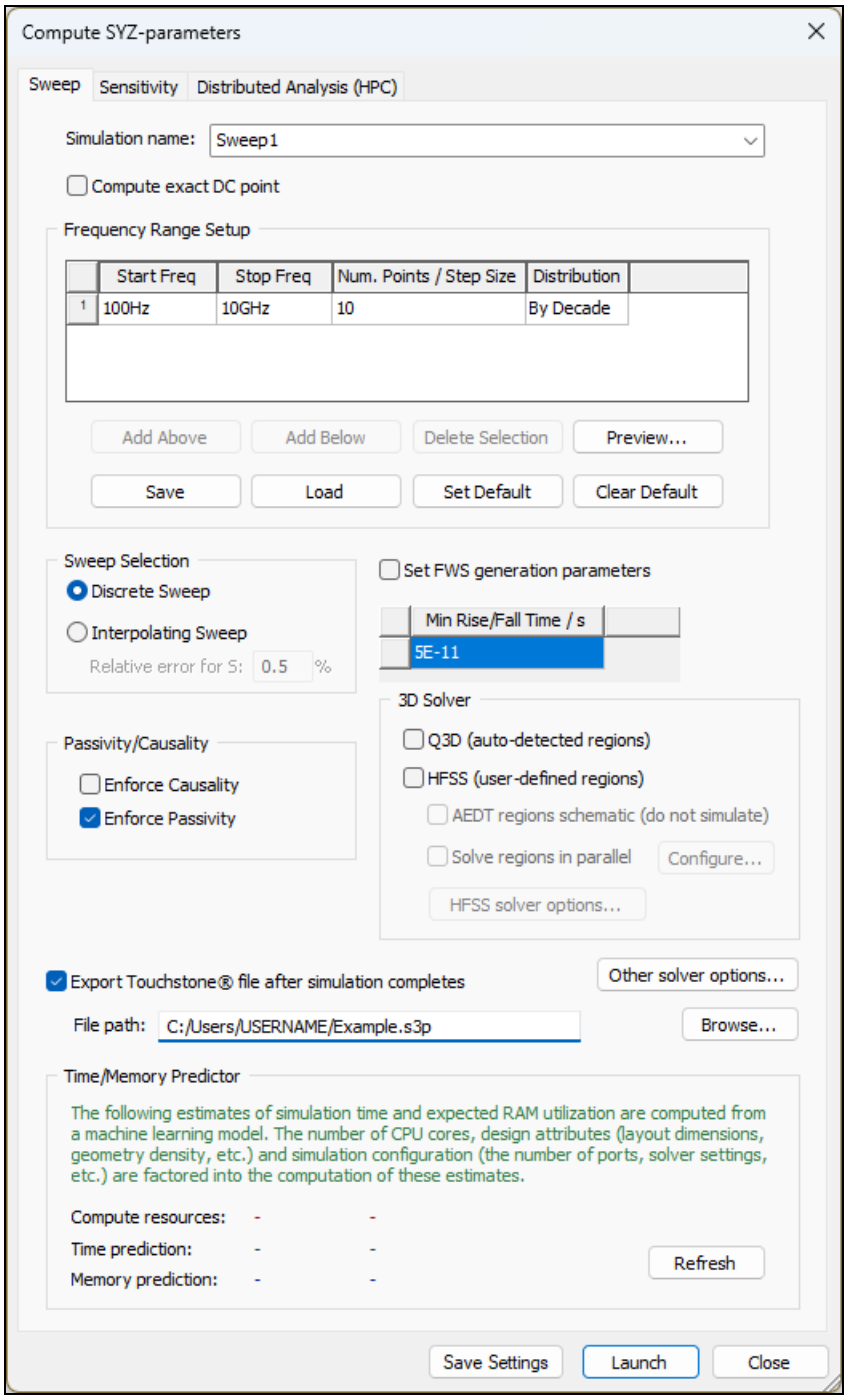

3. From the **3D Solver** area, check the **HFSS (user-defined regions)** box. Then check the **AEDT regions schematic (do not simulate)** box.
4. Click **Launch**. Instead of performing a simulation, **SIwave** exports the schematic and creates a **<project_name>_regions_sch** folder in the directory containing the project *.siw file. **3D Layout** and schematic projects are also created and placed within an 000X_<*sweep*

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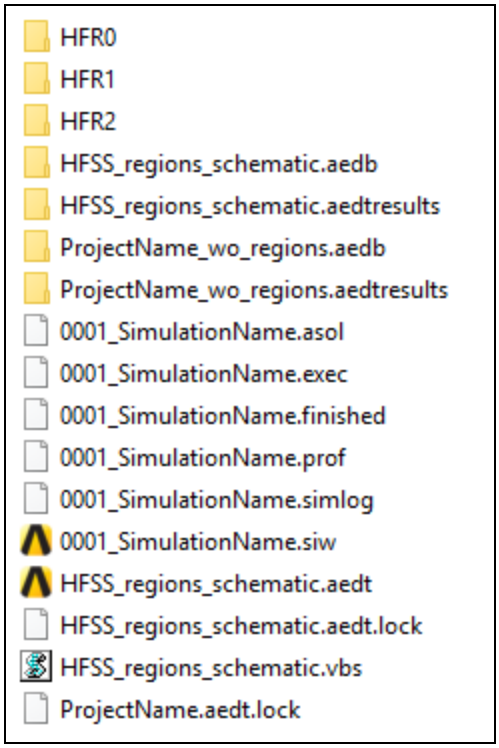
name> subfolder.



Each **HFR#** folder contains a **HFSS 3D Layout** project representing a region. **<project_name>_wo_regions.aedt** represents the **SIwave** project with the region geometry removed. In **Electronics Desktop**, each schematic block representing a 3D Layout-linked project is placed in a separate tab.

Note:

Consult the HFSS help for instructions on running a Nexxim LNA frequency sweep of the exported schematic.

Configuring Parallel HFSS Simulations

In order to reduce overall simulation time, you can configure HFSS region simulations to run in parallel.

First, you must specify compute resources (host machines) to use during the solve. Next, classify these resources into groups and specify which compute resource group to use when solving a particular region. You then select the number of regions to solve in parallel. The simulation loop queues up all of the regions in the design and launches HFSS solves in parallel. When one of these region solves completes, simulation of the next region in the queue is initiated. This continues until all HFSS regions in the design have been processed.

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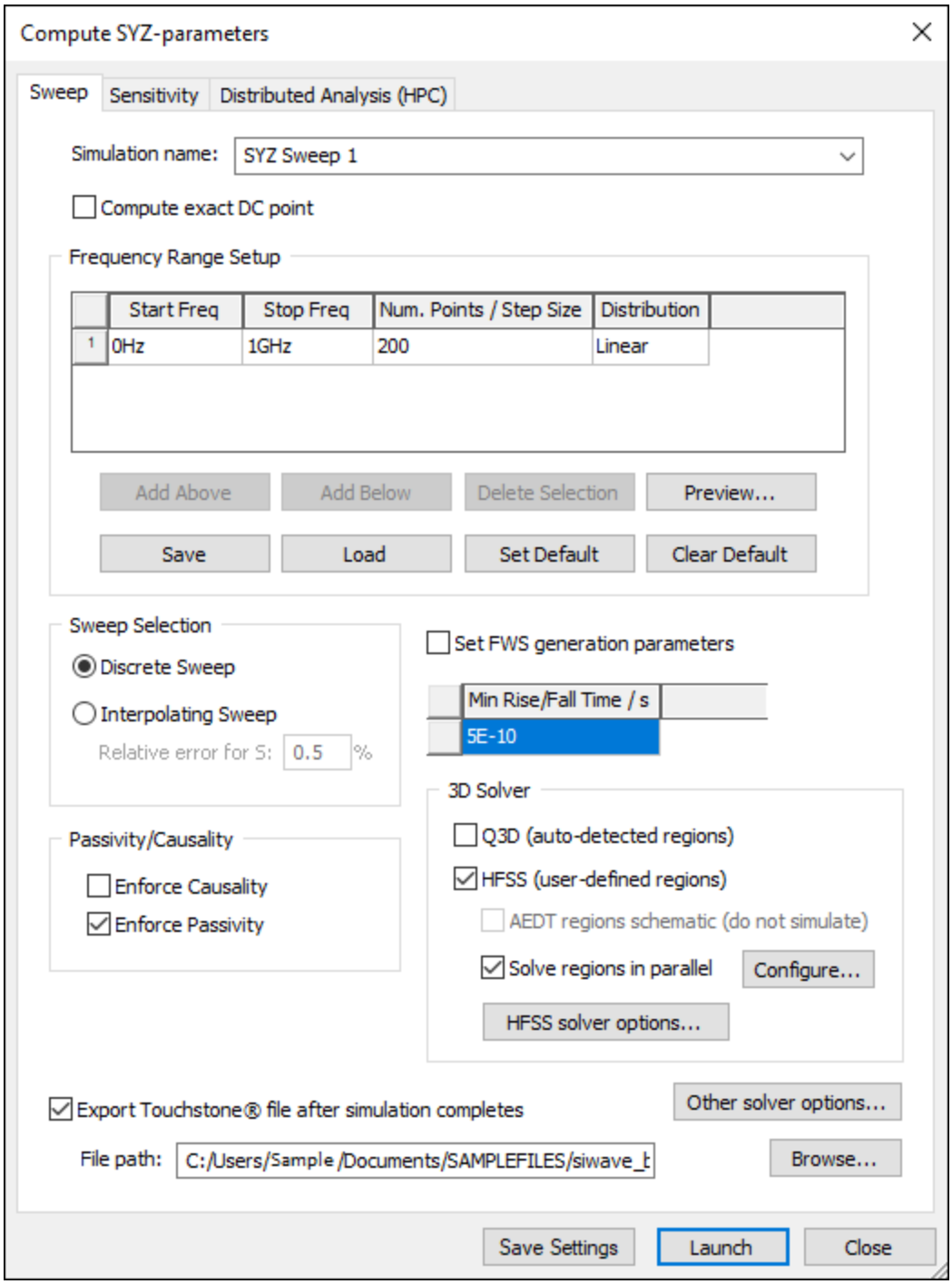
To configure parallel simulations:

1. Click **Simulation** > **Compute SYZ Parameters**.

   The **Compute SYZ-Parameters** window appears.



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2. Configure the SYZ simulation.
3. From the **3D Solver** area, select **HFSS (user-defined regions)** and **Solve regions in parallel**.

   > **Note:**
   >
   > If **AEDT regions schematic** is selected, **Solve regions in parallel** will be unavailable. These options are mutually exclusive.

4. Click **Configure**.

   The **Parallel HFSS Region Simulation Configuration** window appears.

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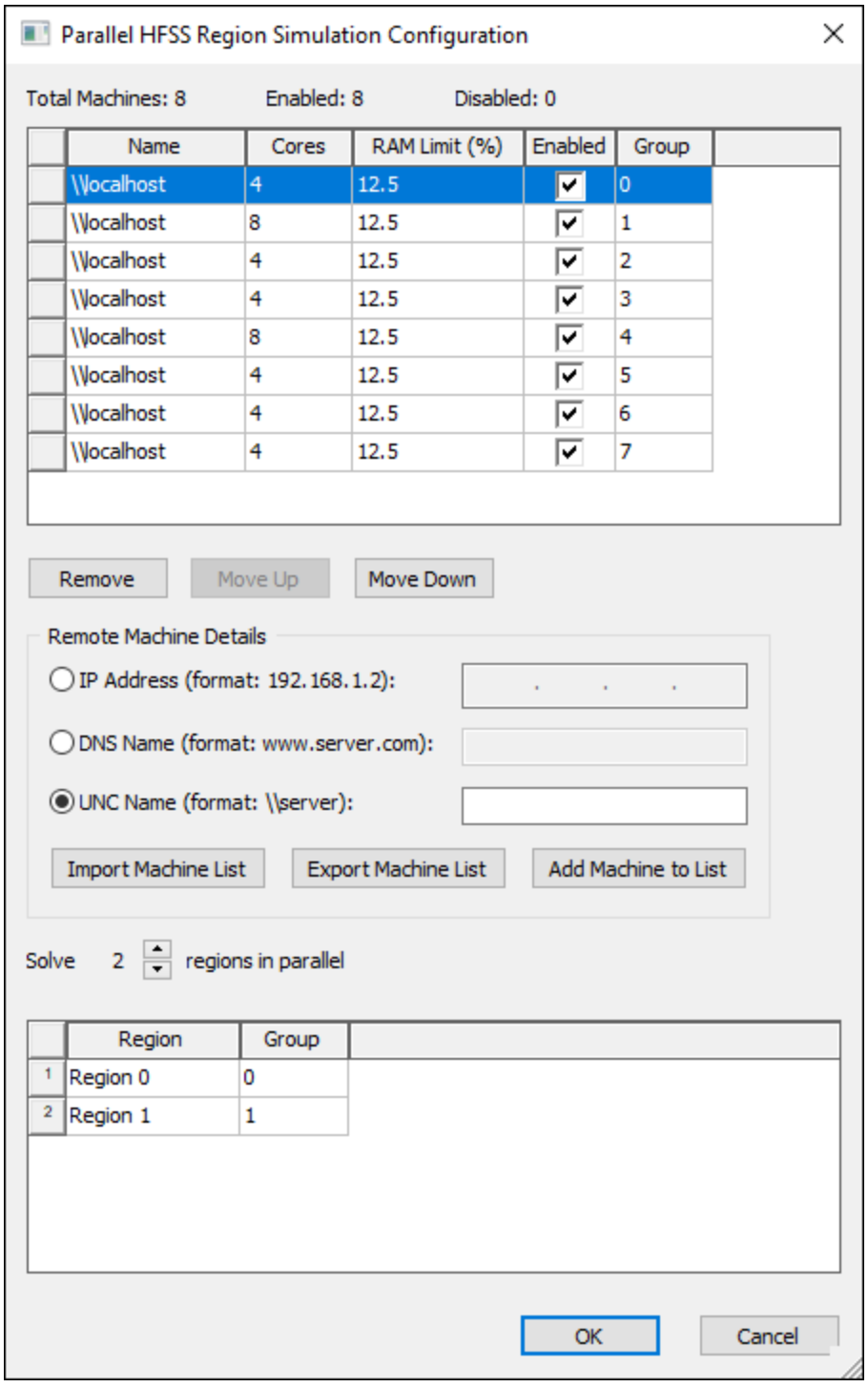

5. The top pane lists available machines. Adjust the settings as appropriate:
   - Use the **Enabled** check boxes to enable and disable machines.
   - Change the values the **Cores** and **RAM Limit (%)** fields.

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- Edit the **Group** values to group the machines as needed. Values can be any non-negative integer.
- Use the **Remove**, **Move Up**, and **Move Down** buttons to remove machines entirely or to adjust the order.

> **Note:**
>
> The same machine can be specified multiple times, as part of the same group or differing groups. However, you must ensure that core count and RAM percentage, when aggregated, do not exceed 100%.

6. The middle pane allows you to add new machines to the list, by **IP Address**, **DNS Name**, or **UNC Name**.

   Alternatively, click **Import Machine List** to import a list in *.txt format. You can also **Export Machine List** in *.txt format for later use.

   The text format is:

   ```
   "<Name>" <Enabled?> <Cores> <RAM Limit %> <group>
   ```

   Example:

   ```
   "\\localhost" 1 4 12.5 0
   "\\localhost" 1 8 12.5 1
   "\\localhost" 1 4 12.5 2
   "\\localhost" 1 4 12.5 3
   "\\localhost" 1 8 12.5 4
   "\\localhost" 1 4 12.5 5
   "\\localhost" 1 4 12.5 6
   "\\localhost" 1 4 12.5 7
   ```

7. The bottom pane lists available HFSS regions in the design. Use the **Group** drop-down menus to assign compute resource groups to regions. Available values are limited to groups that were assigned in the top pane.

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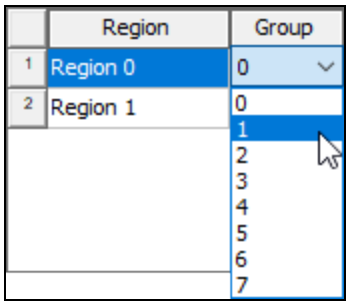

8. Use the **Solve** arrows to increase or decrease the number of regions solved in parallel.
9. Click **OK** to exit the configuration window.
10. Click **Launch** to begin simulation.
11. View results from the **Results** tab, as normal.

Cosimulation with Ansys Electronics Desktop

SIwave works with Ansys Electronics Desktop for three types of cosimulation:

- Cosimulation using DDR Wizard
- Cosimulation using SI Wizard
- Cosimulation using TDR Wizard

You can also dynamically link to SIwave from HFSS.

Cosimulation using DDR Wizard

DDR Wizard is a tool designed for DDR designs that can analyze the time domain transient response at drivers/receivers and analyze eye diagrams. DDR Wizard initiates a cosimulation with Ansys Electronics Desktop Circuit/Schematic using the Electronics Desktop-SIwave dynamic link. **The DDR Wizard automates the creation of pin groups for power/ground pins and adds ports on the signal and power nets.** Users can create a dynamic link or use the SSS/Touchstone workflow, which solves the design first in SIwave and uses the generated s-parameters as a schematic block in Electronics Desktop. The SSS can be adjusted from Network Data Explorer's Broadband settings before being used in Electronics Desktop.

> **Note:**
>
> Unless the design includes a dynamic link (e.g., a Circuit netlist, Touchstone, or State Space file), any ports generated during cosimulation are deleted after a solution is generated.

All settings in DDR Wizard can automatically be propagated to the Virtual Compliance toolkit within Electronics Desktop. To access this from Electronics Desktop's Project Manager, right-

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click a schematic design and select **Toolkit** > **Virtual Compliance Launch - Ansys DDRwizard**. For additional information on the Virtual Compliance toolkit, consult the Circuit help.

Nets are classified into one of the following types, based on search string:

- DQ
- DQS
- ADDR
- CLK
- OTHER

Each of these groups is driven by a specific input, which varies based on DDR speed. See: DDR Wizard Settings.

When the final schematic is generated, simulation setup (Transient, QuickEye, AMI) and reports all reflect 2 DDR modes: Read and Write.

- **Read Mode** – All sources are in sync.
- **Write Mode** – Extra delay added for sources which are fed in from project variables in Electronics Desktop. By default, DQS nets are delayed by 1/2 bit width of DQ, and CLK nets are delayed by 1 bit width of ADDR.

Using AMI Models

SIwave supports AMI Analysis, with the following caveats:

- Ensure the path containing IBIS AMI files is listed as an IBIS Buffer Directory in SIwave (**FILE** > **Options** > **Library Directories**).
- AMI IBIS models and non-AMI IBIS models cannot be combined.
- Both the driver and receiver side of the net(s) being analyzed must have an AMI model.

Running Simulations in DDR Wizard

To run a cosimulation in DDR Wizard:

1. Click **Simulation** > **DDRwizard**.

   DDR Wizard opens in a new window, on its **Basic Setup** screen:

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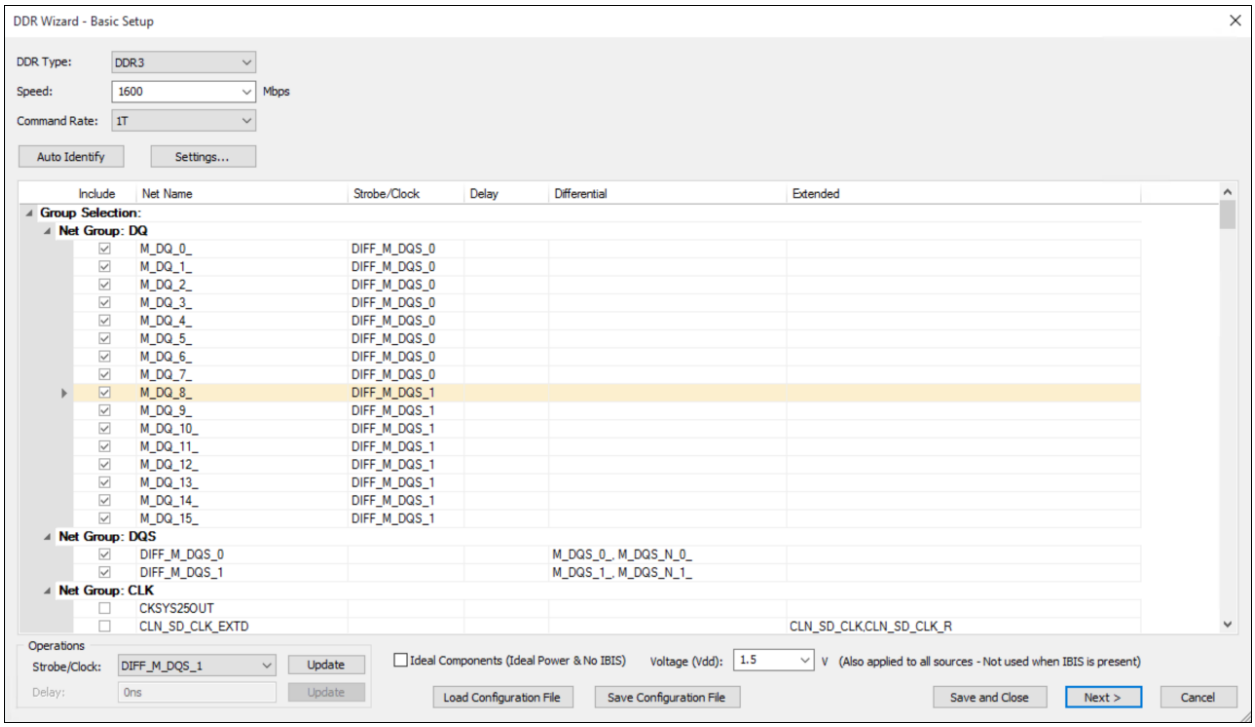

2. Use the drop-down menus to select the **DDR Type**, **Speed**, and **Command Rate**. If appropriate, you can manually enter a custom speed.
3. If appropriate, click Auto Identify to reclassify nets into new groups after updating the group identifiers (search string for group) in DDR Wizard Settings.
4. If appropriate, manually select or deselect nets in the table. Only selected nets will be analyzed.

   By default, all nets classified as DQ, DQS, ADDR, and CLK are selected; nets classified as OTHER are deselected.

> **Note:**
>
> Differential nets populate the **Differential** column, Extended nets populate the **Extended** column, and Differential-Extended nets populate both.

5. To update **Strobe/Clock** and **Delay**, highlight one or more rows and use the drop-down menus in the **Operations** area.
6. If appropriate, select the **Ideal Components** check box. This forces all ICs to have no IBIS model, and removes VRMs. Selecting **Ideal Components** also disables the **Ideal Power** check box in the next phase of setup (see: Step 9).
7. If appropriate, use the **Voltage** drop-down menu to customize the Vdd value and apply to all sources.

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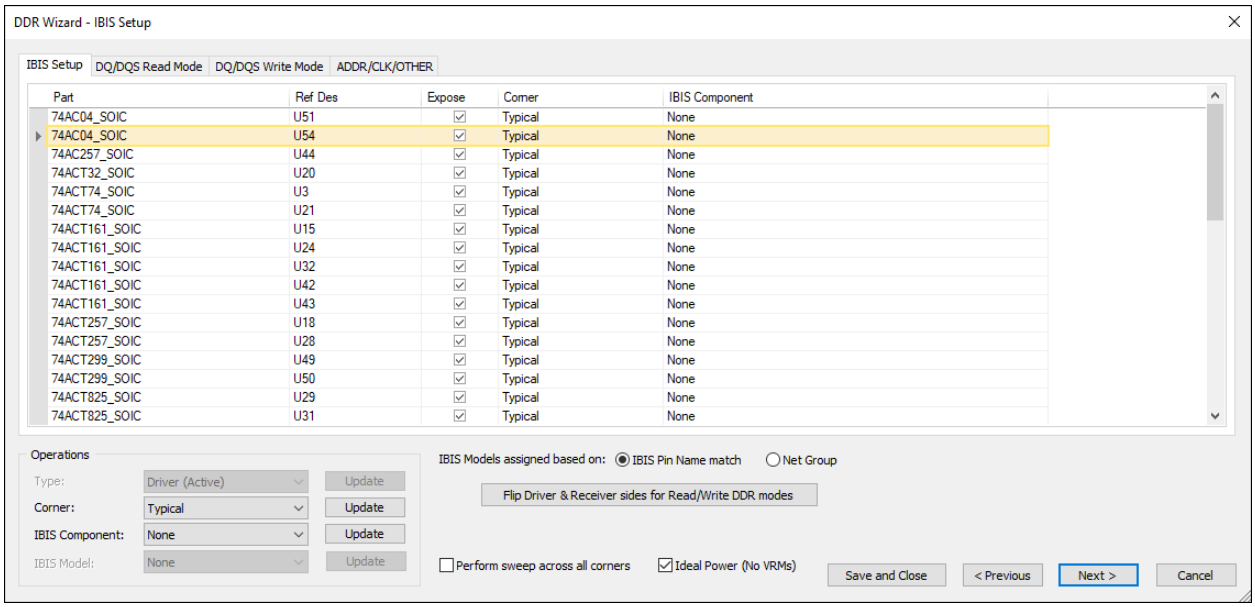
> **Note:**
>
> When IBIS model is present on the driver, DDR Wizard applies voltage of 1V.

8. If appropriate, click **Save Configuration File** to save your settings as a *.ddx file. These files can be loaded using **Load Configuration File**.
9. Click **Next**.

   DDR Wizard updates to display the **IBIS Setup** screen:



   This screen lists all components from nets selected on the previous screen.

   Driver and Receiver are automatically assigned with the IC with more pins being the driver. IBIS components are also automatically assigned based on IC properties. However, all of these settings can be changed using the options in the **Operations** area.

   If a new IBIS component is assigned, the IBIS models are automatically assigned to individual pins in the IC based on pin name match between the IC pins and IBIS component pins. Unmatched pins are assigned to the first single-ended model or the first differential model in the IBIS component.
10. If appropriate, change a component's **Type** and **Corner**, or specify an **IBIS Component**.

> **Note:**
>
> When IBIS components are specified, you can change the IBIS model on the Read Mode and Write Mode tabs.

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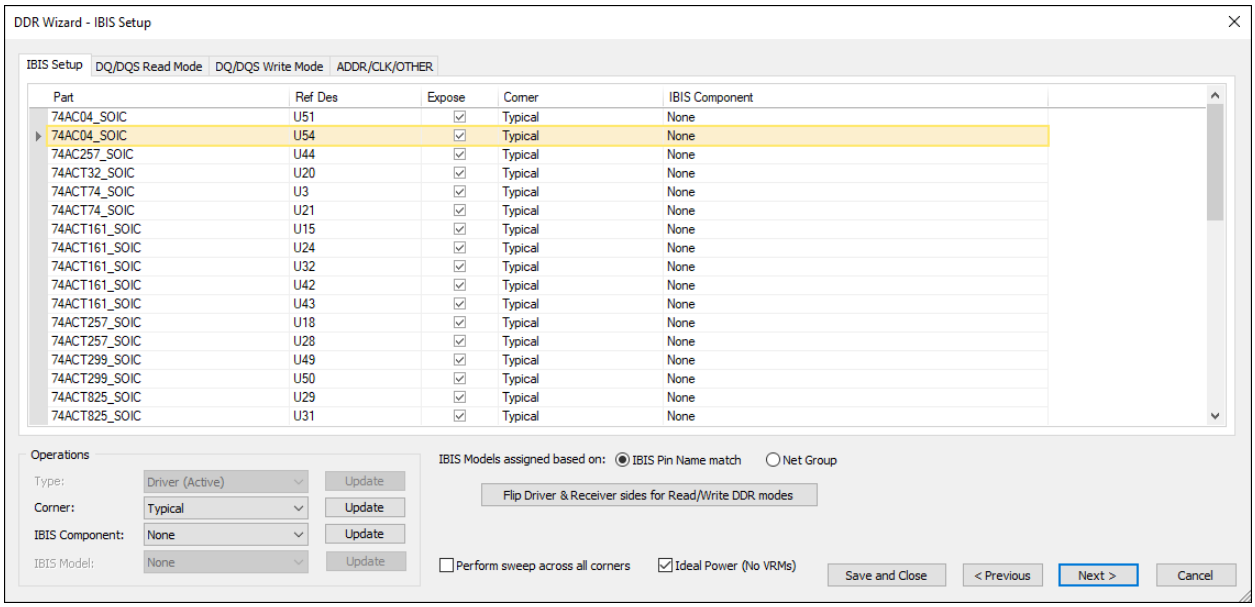
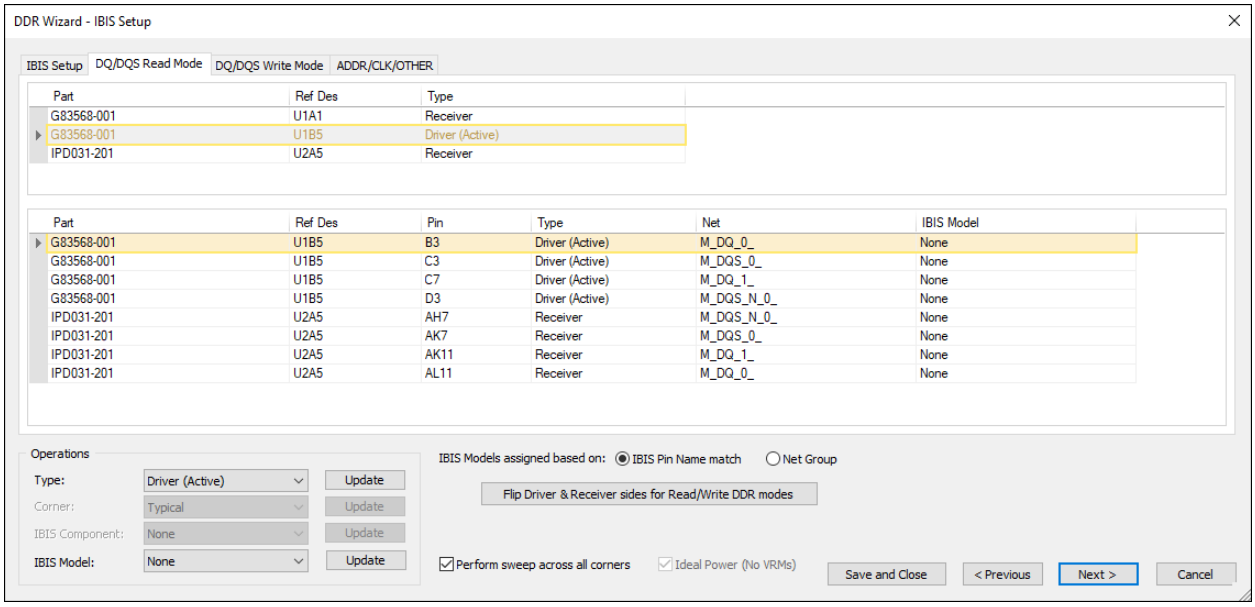
11. If appropriate, enable **Perform sweep across all corners**. From the Electronics Desktop simulation setup, a sweep is set up to use typical, minimum, maximum, fast, and slow. Reports generate five curves instead of one for every probe.
12. If appropriate, enable **Ideal Power** to remove VRMs.
13. Use the radio buttons to select whether IBIS models are assigned based on **IBIS Pin Name Match** or **Net Group**.
14. If appropriate, click the **DQ/DQS Read Mode**, **DQ/DQS Write Mode**, or **ADDR/CLK/OTHER** tabs to view more information.





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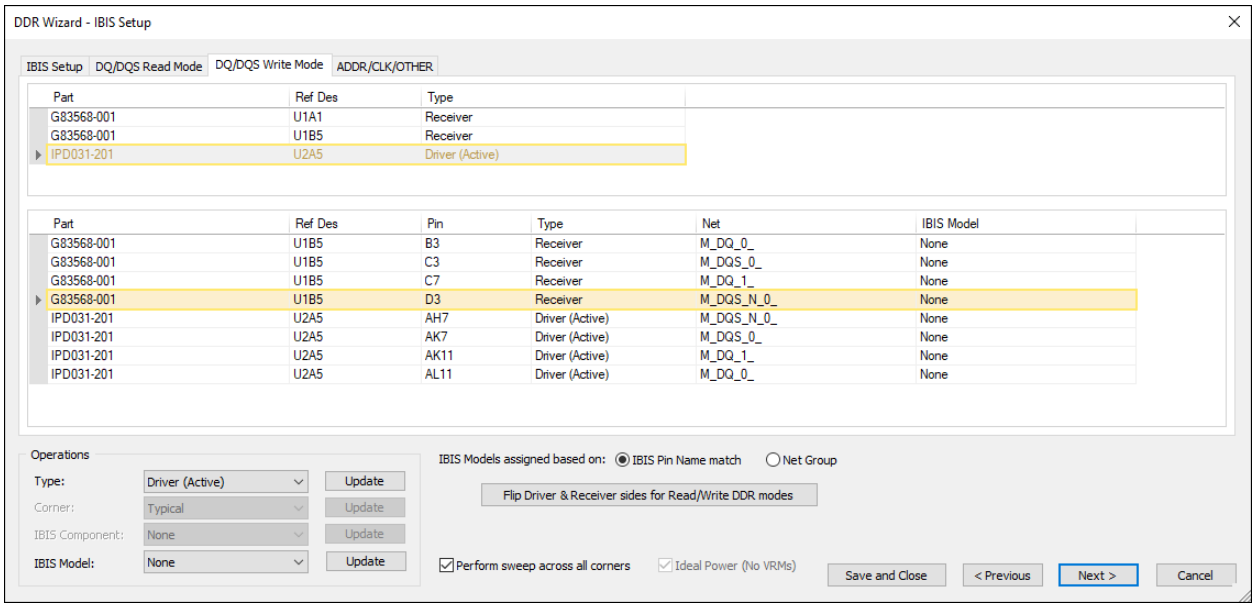

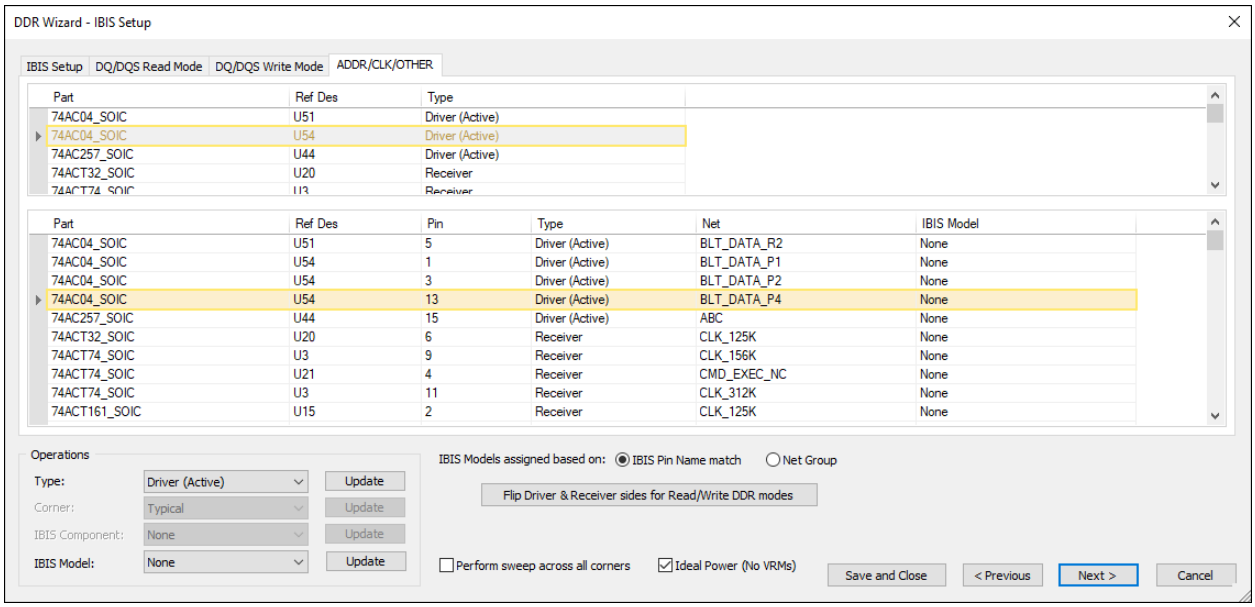

Drivers and receivers are chosen automatically, but can be changed.

- In **DQ/DQS Write** mode, the component with the largest number of pins is chosen as the driver. Thus the main microcontroller or the DIMM connector is usually the driver and the Memory ICs are the receiver.
- In **DQ/DQS Read** mode, the opposite is true.
- On the **ADDR/CLK/OTHER** tab, the driver and receiver sides are initially chosen the same as in DQ/DQS Write mode, but can be independently changed.

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The IBIS models assigned for DQ/DQS drivers will be the DRV models and for DQ/DQS receivers will be the ODT models.

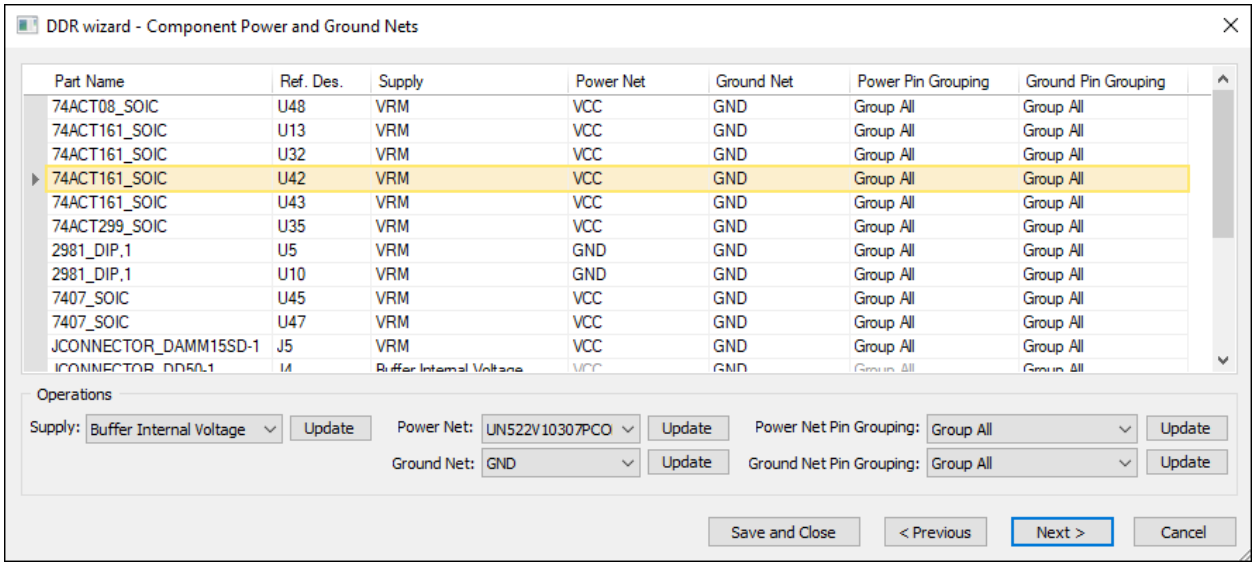
When IBIS components are specified on the **IBIS Setup** tab, the **IBIS Model** can be changed from the DQ/DQS Read Mode, DQ/DQS Write Mode, or ADDR/CLK/OTHER tab.

The IBIS component and IBIS model can be regular IBIS (defined using a .ibs file) or IBIS AMI (defined using .ibs/.ami/.dll/.so files)

15. Click **Next**.

    If **Ideal Power** was selected on the previous window, proceed to Step 16.

    If **Ideal Power** was not selected on the previous window,]DDR Wizard updates to display **Component and Ground Nets**.



Select one or more part(s) and use the **Operations** area to set:

- Power Supply
- Power Net
- Ground Net
- Power Net Pin Grouping
- Ground Net Pin Grouping

If there are no VRM parts, proceed to Step 16.

If the chosen **Supply** for any part is **VRM**, the **DDR wizard** displays a **VRM Parameters** step.

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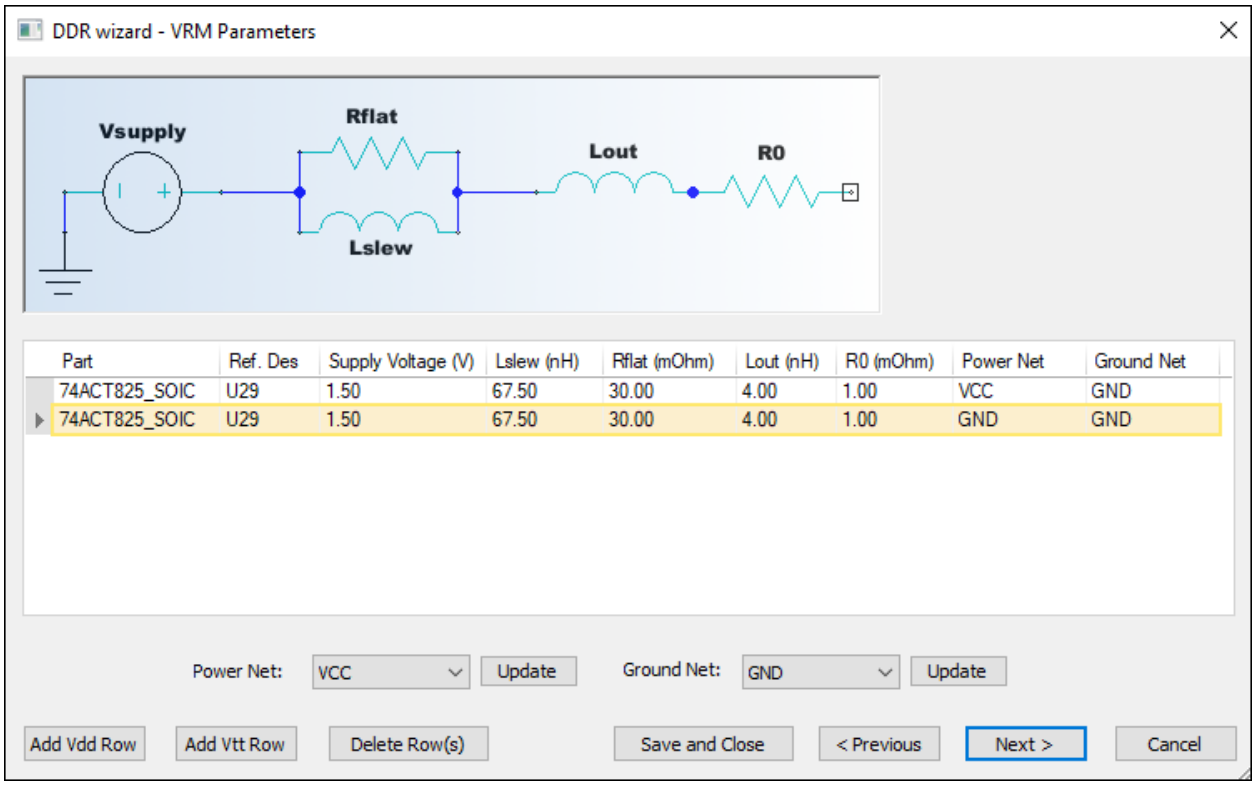

Here, you can adjust the **Power Net** and **Ground Net** for each VRM part.

16. Click **Next**.

    The DDR Wizard updates to display **Transient Simulation Options**:

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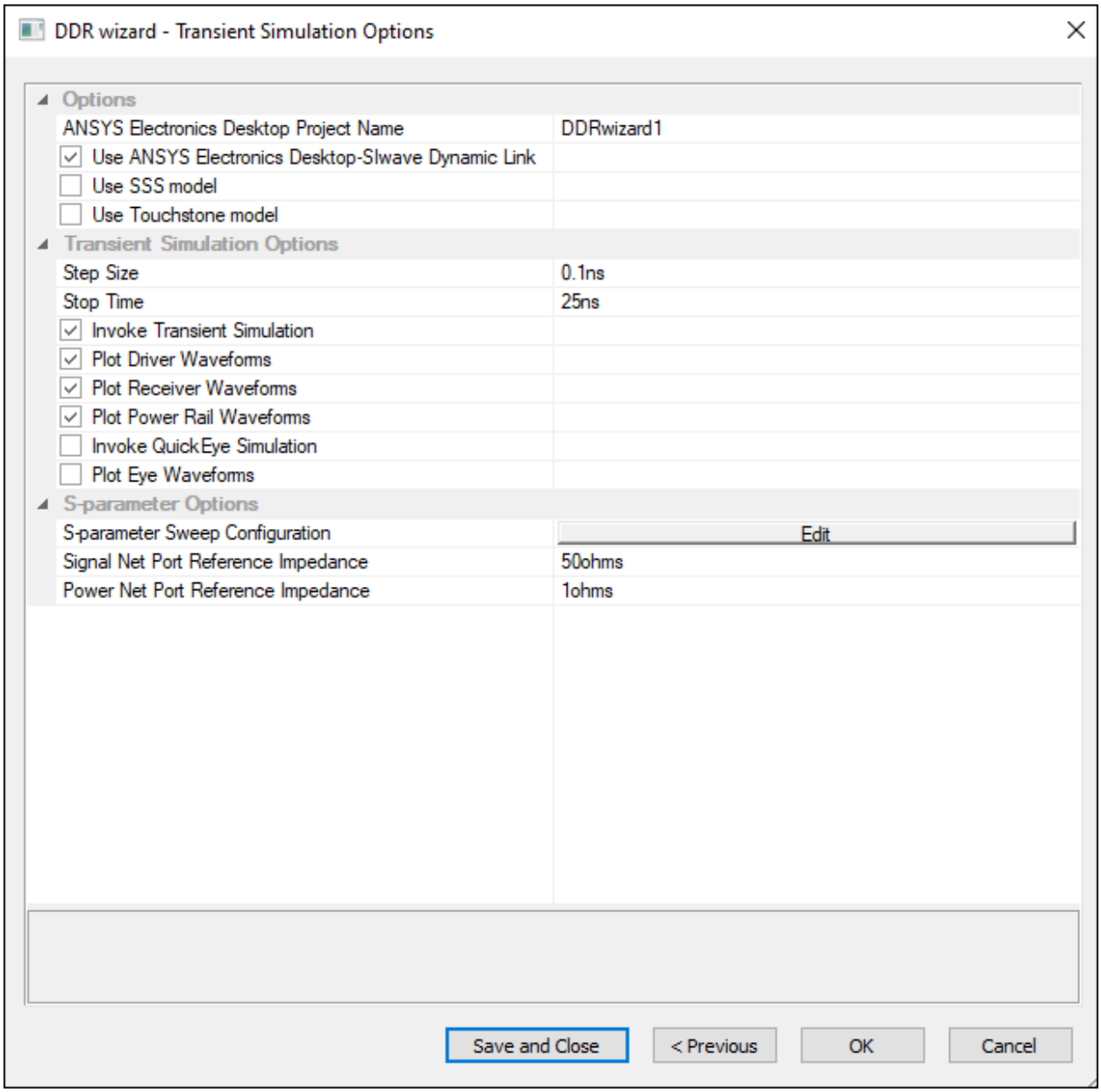

This step includes options for:

- **Project Name** – the name of the schematic generated in Electronics Desktop.
- **Use Ansys Electronics Desktop-SIwave Dynamic Link** – enable dynamic link.
- **Use SSS Model** – enable state space model.
- **Use Touchstone Model** – enable touchstone model.
- **Step Size** – specify the value and unit.
- **Stop Time** – specify the value and unit.

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- **Invoke Transient Simulation** – select whether to invoke Transient simulation. *This option must be enabled in order to use AMI sources*.
- **Plot Driver Waveforms** – select whether driver waveforms are plotted.
- **Plot Receiver Waveforms** – select whether receiver waveforms are plotted.
- **Plot Power Rail Waveforms** – select whether power rail waveforms are plotted.
- **Invoke QuickEye Simulation** – select whether to invoke QuickEye simulation.
- **Plot Eye Waveforms** – select whether to plot Eye waveforms.
- **S-Parameter Options** – enter reference impedance values and specify a frequency sweep by clicking **Edit**. See: Computing Frequency Sweep.

For more information on AMI, QuickEye, and Transient, consult the following sections of the Circuit Help:

- AMI Analysis
- QuickEye
- Transient

> **Note:**
>
> Electronics Desktop supports the use of DDR variables.

17. Assign settings as appropriate.
18. Click **OK**.

    SIwave generates two schematics (one for Read mode and one for Write mode), which open in Electronics Desktop.

    Each schematic contains multiple tabs:

    - **Main tab** – the center displays the dynamic link block. Voltage sources and VRMs appear at the top. IBIS component sub-circuit blocks display to the sides.
    - **Subsequent tab(s)** – contain driver/receiver blocks with each byte lane along with corresponding strobe. These are in individual tabs, organized by DQ/DQS, ADDR/CLK/OTHER, and IBIS. The number of tabs varies by schematic.

DDR Wizard Settings

DDR Wizard contains a detailed list of information for sources and nets. The sources are assigned to the nets as follows:

- DQ → Default PRBS
- DQS → Default Clock
- CLK → Default half-rate Clock
- ADDR → Default half-rate PRBS
- OTHER → Default half-rate PRBS

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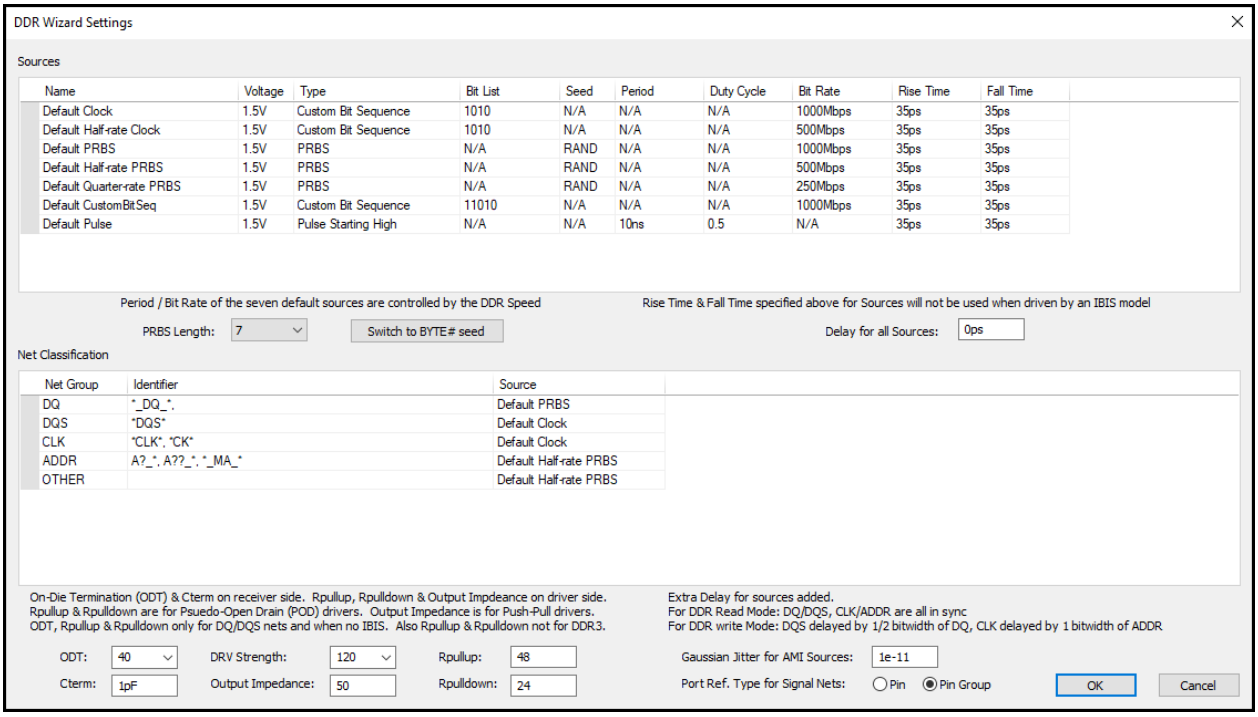
The source parameters can be partially customized. Nets can be classified into net groups based on identifier.

From the DDR Wizard, click **Settings** to view additional settings:



The number of **Sources** is locked and you cannot add or remove one. The Source **Name** and **Bit Rate** are also locked. All other fields can be updated.

PRBS Length, specified from the drop-down menu, can be from 7 bits to 31 bits.

PRBS Sources can have a seed that is an integer, BYTE#, or RAND.

- For **BYTE#**, the bit number within the byte lane is assigned as the seed (e.g., the first byte lane assigned to strobe DQS0 (DQ0 to DQ7) are assigned seeds 0 through 7. The next byte lane assigned to strobe DQS1 (DQ8 to DQ15) are also assigned seeds 0 through 7. The entire byte lane assigned to strobe CLK0 (ADDR0 to ADDR15) are assigned seeds 0 through 15).
- For **RAND**, a random seed value is assigned every time.

The **Switch to** [**RAND** / **BYTE#**] **Seed** button allows you to toggle between BYTE# and RAND for all PRBS seeds.

From the **Net Classification** area, only the **Identifier** is editable. *DQ* can be made *_DQ_* and so on. All net names are matched one-by-one with every search identifier and, if there is a match, the net belongs to the corresponding net group in the grid. An asterisk (*) can be used to

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match one or more of any character, while a question mark (?) will match just one of any character.

From this window, you can also:

- Sort the lists by any of the header criteria by clicking that header.
- Specify a common **Delay for all Sources**.
- Specify On-Die Termination (**ODT**) and **Cterm** for the receiver side.
- Specify **Rpullup**, **Rpulldown**, and **Output Impedance** for the driver side.
- Specify **Gaussian Jitter for AMI Sources**. The default is 1e-11. After simulation, you can verify that the correct setting was applied in Electronics Desktop by selecting an IBIS schematic tab, double-clicking the driver model to open its **Properties** window, and reviewing the information on the **Jitter_Clock** tab.
- Select the **Port Ref. Type for Signal Nets**. By default, ports on signal nets are connected to a reference **Pin Group**. If appropriate, change this setting to connect to an individual reference **Pin**.

Important:

- ODT is used only for DQ/DQS nets with no IBIS.
- Rpullup and Rpulldown are used for Pseudo-Open Drain (POD) drivers.
- POD drivers are used for DQ/DQS nets in DDR4 & above. In addition to DQ/DQS nets, the POD drivers are also used for ADDR nets in DDR5 & above.
- DRV Strength is the Drive Strength used for matching the IBIS model based on the value, if a match exists within the models in the selected IBIS component. It is used only for the driver side.
- Output Impedance is used for Push-Pull drivers.

DDR Variables

Electronics Desktop contains variables which can be customized to facilitate quick adjustments and re-run of Analysis directly within Electronics Desktop. To adjust variable values, right-click the schematic project in the **Project Manager** and select **Project Variables**.

The table below lists DDR variables. For more general information on using variables in Electronics Desktop, consult the Circuit help.

Variable	Description
$cornervals	A fixed enumeration array with values "typ" (typical), "min" (minimum), "max" (maximum), "fast", and "slow".
$corner	An index on the $cornervals array, where 0 = "typ", 1 = "min", 2 = "max", 3 = "fast", and 4 = "slow".

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Variable	Description
	If there is no common corner needed for all the IBIS models in the design, $corner is replaced with five variables: • $corner0 – will have a value of 0 and be used by all IBIS models that need corner value "typ". • $corner1 – will have a value of 1 and be used by all IBIS models that need corner value "min". • $corner2 – will have a value of 2 and be used by all IBIS models that need corner value "max". • $corner3 – will have a value of 3 and be used by all IBIS models that need corner value "fast". • $corner4 – will have a value of 4 and be used by all IBIS models that need corner value "slow". For example, you needed to force the corner for all IBIS models to "max", you would change the value of all five of these variables to 2.
$voltage	The VDD value. VTT will use $voltage/2.0.
$bitrate	DDR speed.
$odt	The On-Die Termination (ODT) value, in ohms.
$cterm	The receiver side termination capacitance value.
$driverRPullUp	The pull-up resistance value used in driver side Pseudo-Open Drains (PODs) for DDR4 and above.
$driverRPullDown	The pull-down resistance value used in driver side PODs for DDR4 and above.
$outputImpedanceDQDQS	Internal impedance on the driver side eye source for DQ and DQS nets.
$outputimpedanceADDRCLKOTHER	Internal impedance on the driver side eye source for ADDR, CLK, and OTHER nets.
$addrNetRes	Resistance termination value on the receiver side for ADDR nets.
$clkNetRes1	Positive net resistance termination value on the receiver side for CLK nets.
$clkNetRes2	Negative net resistance termination value on the receiver side for CLK nets.
$clkNetCap	Capacitance termination value on the receiver side for CLK nets.
$clkNetCapDiff	Differential Capacitance termination value on the receiver side for CLK nets.

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Variable	Description
$<netName>_delay	Delay applied based on strobe/clock assignments. For example: • $DIFF_DQS0_delay is applied to nets DQ0 through DQ7 and also to net DIFF_DQS0. • $DIFF_DQS1_delay is applied to nets DQ8 through DQ15 and also to net DIFF_DQS1. • $CK0_delay is applied to nets AD0 through AD15 and also to net CK0.
$DQ_nets_delay	Delay applied to every net in the DQ group. Default is 0 for both DDR modes.
$DQS_nets_delay	Delay applied to every net in the DQS group. Default is 0 for DDR Read Mode and half the bit width of the DQ net for DDR Write Mode.
$CLK_nets_delay	Delay applied to every net in the CLK group. Default is 0 for DDR Read Mode and one bit width of the ADDR net for DDR Write Mode.
$ADDR_nets_delay	Delay applied to every net in the ADDR group. Default is 0 for both DDR modes.
$OTHER_nets_delay	Delay applied to every net in the OTHER group. Default is 0 for both DDR modes.
$steprespnumui	Determines how long an AMI analysis runs and is used by all IBIS AMI sources. It can be determined by analyzing the impulse response of the AMI solve to see how many unit Intervals it takes to completely settle. For DDR simulations, the ideal values are used as default: • Value of 10 if DDR speed is within 3200Mbps • Value of 15 if DDR speed is between 3200Mbps and 4800Mbps • Value of 20 if DDR speed is above 4800Mbps. Change to a appropriate value, if appropriate.

Cosimulation using SI Wizard

SI Wizard initiates a cosimulation with Ansys Electronics Desktop Circuit/Schematic from SIwave. By default, SI Wizard uses a netlist that is opened in Ansys Electronics Desktop. You can also use an Ansys Electronics Desktop-SIwave dynamic link. The SI Wizard automates the creation of pin groups for power/ground pins and adds ports on the signal and power nets. The selected nets are given ports and buffer models and set up as netlist or S-parameter dynamic

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link N-ports in Ansys Electronics Desktop. The results show the time domain voltage waveforms at drivers, receivers, and power supply pins of all buffers, including eye diagrams.

> **Note:**
>
> Unless the design includes a dynamic link (e.g., a Circuit netlist, Touchstone, or State Space file), any ports generated during cosimulation are deleted after a solution is generated.

> **Note:**
>
> Before starting SI Wizard extraction, you must identify power and ground nets in your design. Additionally, running a Validation Check is recommended. If appropriate, you can assign IBIS buffer models to pins. See Simulation Setup for more information on these actions.

To run a cosimulation in SI Wizard:

1. If appropriate, use the Nets workspace to select one or more signal nets for cosimulation. You can also select a signal net by clicking a pin or component connected to the net.
2. Click **Simulation** > **SIwizard**.

   The **SIwizard Step 1: Select Nets to Analyze** window appears, on the **Single-Ended** tab.

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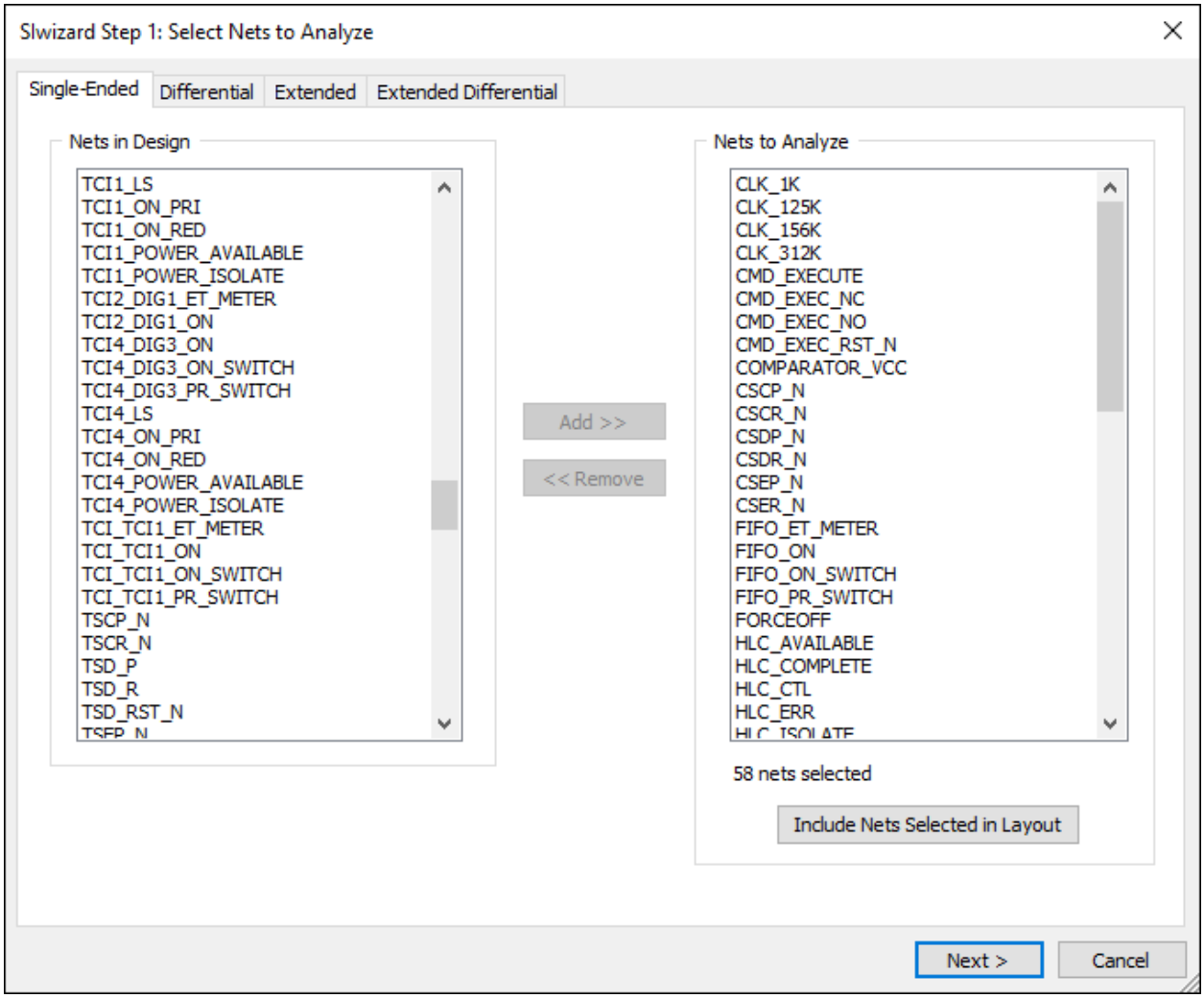

3. Navigate using the **Single-Ended**, **Differential**, **Extended**, and **Extended Differential** tabs. Use the **Add>>** and **<<Remove** buttons to select nets for analysis.
4. Click **Next**.

   The **SIwizard Step 2: Assign Driver and Receiver Models** window appears.

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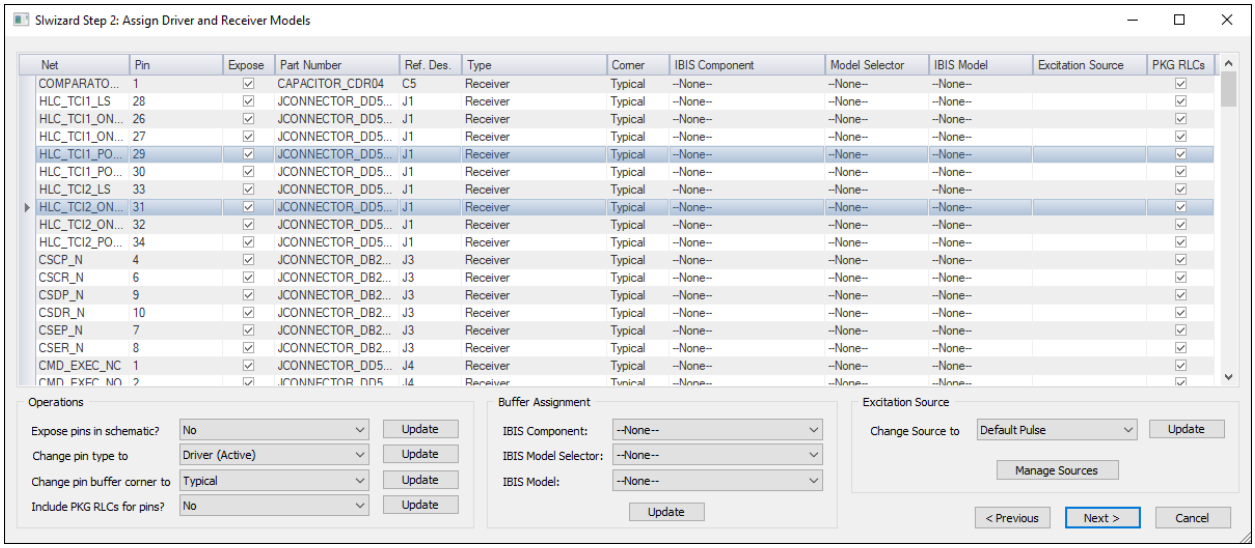

5. Click the column headers to sort the nets. Select a net by clicking the gray area to the left of its row. Select multiple nets using Ctrl+click.
6. For the selected net(s), you can set the following:
   - **Expose** – check this check box for any pin that is to be an external connection to the Ansys Electronics Desktop circuit/schematic.
   - **Type** – select the IBIS buffer type. Options include: Driver (active), Driver (inactive), Receiver, Receiver (with termination), and Passive termination.
   - **Corner** – select the range for parameters (typical, minimum, or maximum).
   - **IBIS Component** – select a component from the library of IBIS buffer elements. If the buffer type includes model selectors, the **Model Selector** field is populated. In this case, you must choose a model selector, then an **IBIS Model** as well. If no model selectors have been defined, leave the default setting (None).
   - **Excitation Source** – select the source for the input excitation to the net. If needed, you can click **Manage Sources** to view available sources, change existing source parameters, or define new sources.
   - **PKG RLCs** – check this check box to include the RLC Package model for the buffer model.
7. Click **Next**.

   The **SIwizard Step 3: Assign Any Additional Receiver Terminations** window appears.

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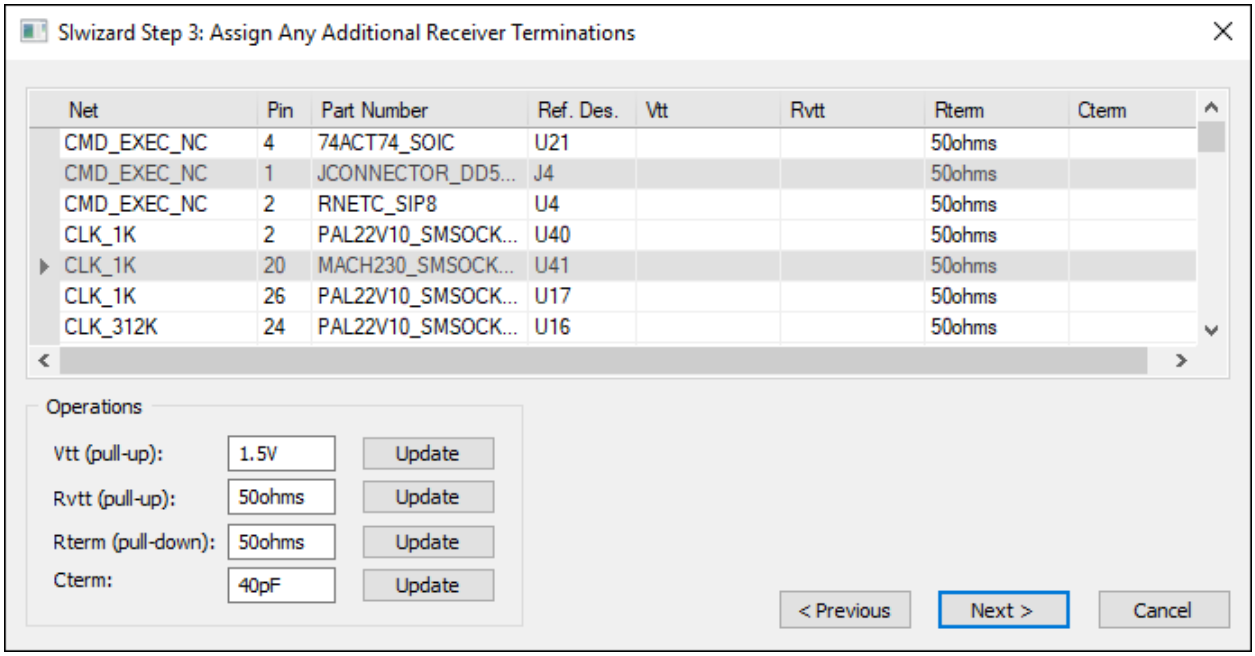
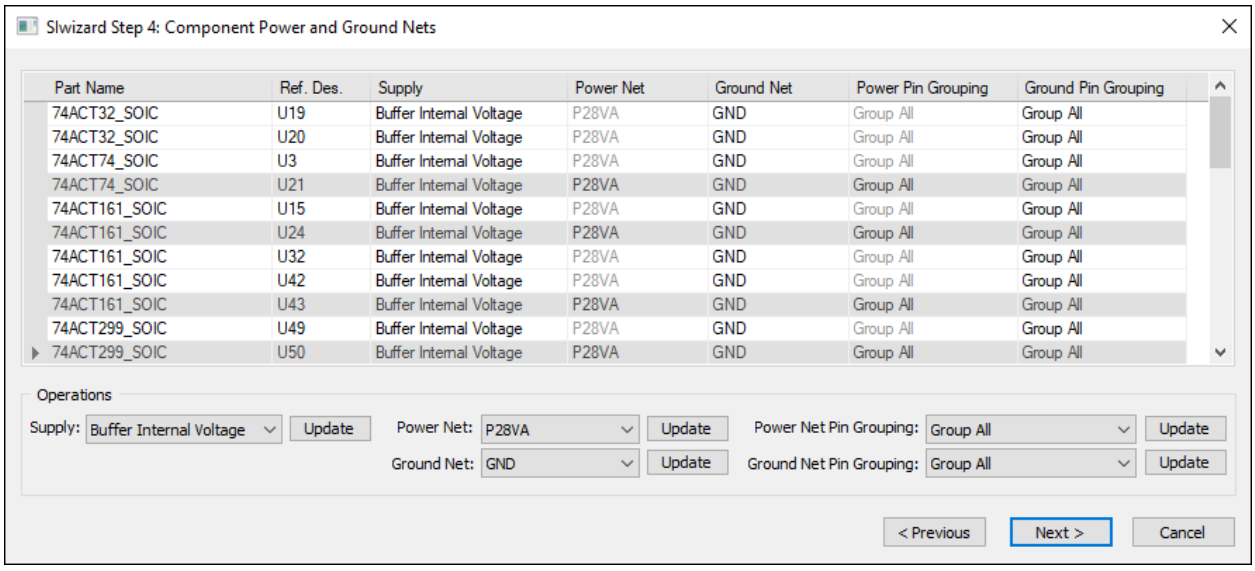


8. Update receiver terminations as appropriate.
9. Click **Next**.

   The **SIwizard Step 4: Component Power and Ground Nets** window appears.



10. Update the power and ground nets as appropriate.
11. Click **Next**.

    The **SIwizard Step 5: Transient Simulation Options** window appears.

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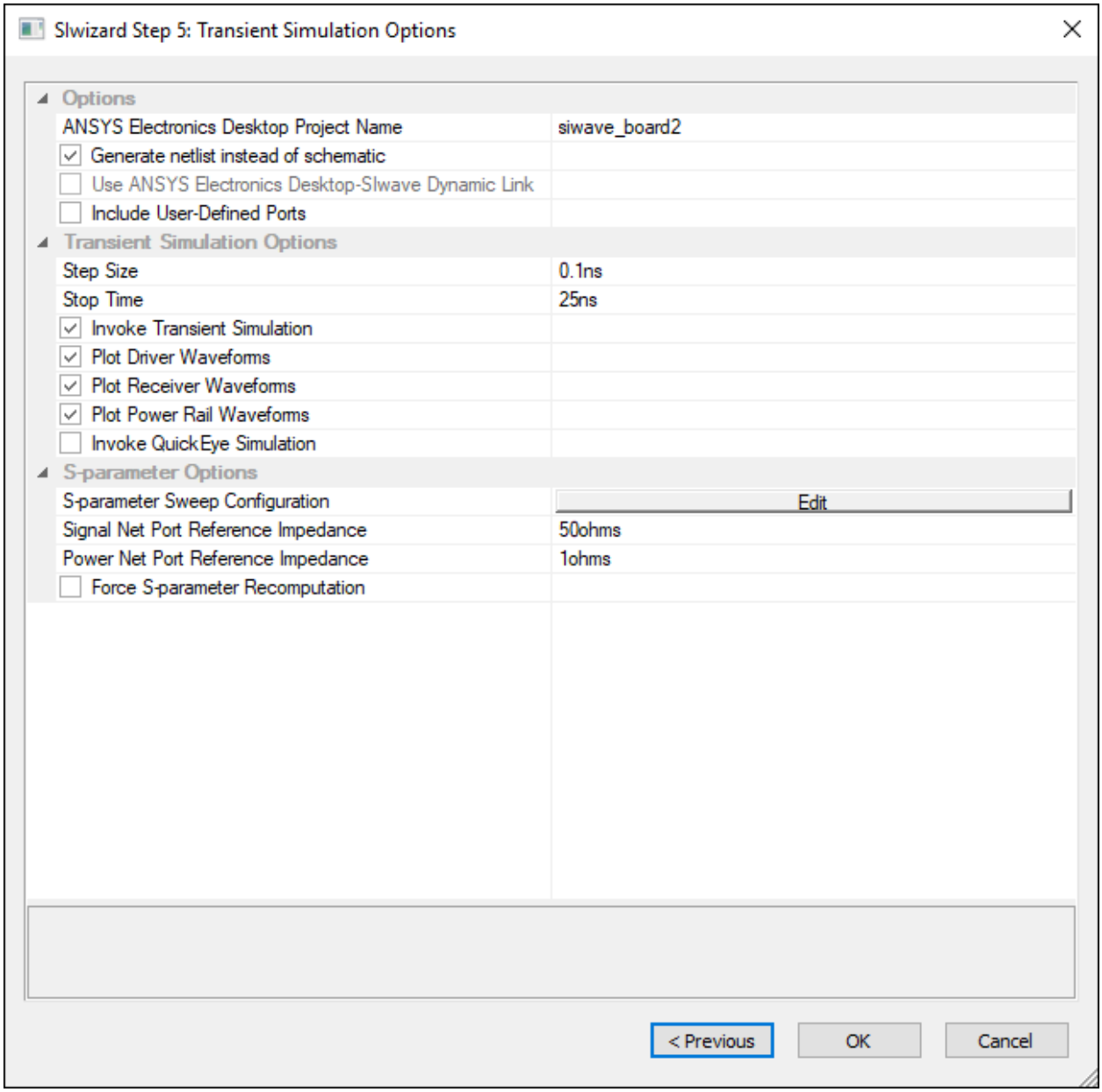

12. Verify your options and click **OK**.

    The **Messages** window updates with a **Process Monitor** tab that displays the progress.

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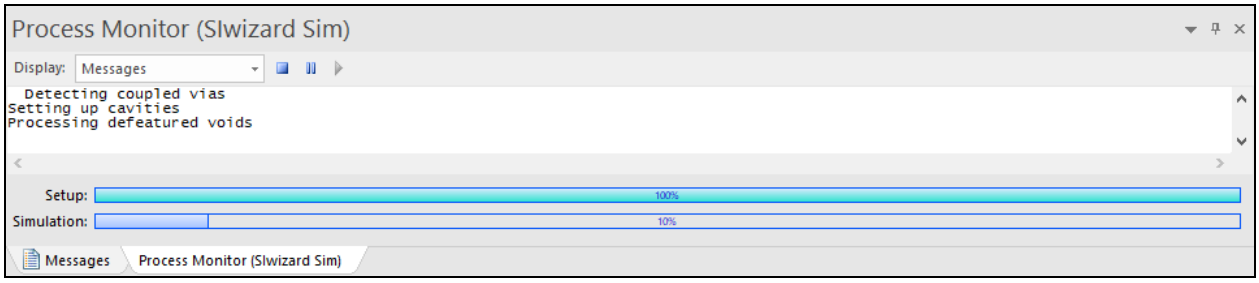

When the simulation has finished in SIwave, Ansys Electronics Desktop opens to run the cosimulation. If the netlist option is selected, the net is automatically imported into Ansys Electronics Desktop Circuit/Schematic as a netlist with associated IBIS buffer models, analyzed by SIwave to obtain the S-parameters, then handed off to Nexxim transient analysis for the time domain simulation. Time domain reports are displayed automatically in Ansys Electronics Desktop Circuit/Schematic. SYZ results are also available in SIwave.

Cosimulation using TDR Wizard

TDR Wizard initiates a cosimulation with Ansys Electronics Desktop Circuit/Schematic from SIwave. By default, TDRwizard uses a Nexxim netlist that points to an S-parameter touchstone file generated from SIwave. You can also use a schematic approach that has a Ansys Electronics Desktop-SIwave dynamic link. TDR Wizard automates the creation of pin groups for power/ground pins and adds ports on the signal and power nets. The selected nets are given page ports in Ansys Electronics Desktop that correspond to the nodes in the S-parameter file for netlist mode or the ports in SIwave for schematic mode. The driver side of nets is attached with TDR probes and the receiver side with Resistor/Capacitor /IBIS Buffer/Open/Short. The results show the time domain impedance waveforms at the TDR probes.

> **Note:**
>
> Unless the design includes a dynamic link (e.g., a Circuit netlist, Touchstone, or State Space file), any ports generated during cosimulation are deleted after a solution is generated.

To run a cosimulation in TDR Wizard:

1. If appropriate, use the **Nets** workspace to select one or more signal nets for cosimulation. You can also select a signal net by clicking a pin or component connected to the net.
2. Click **Simulation** > **TDRWizard**.

   The **TDR Wizard Step 1: Select Nets to Analyze** window appears, on the Single-Ended tab.

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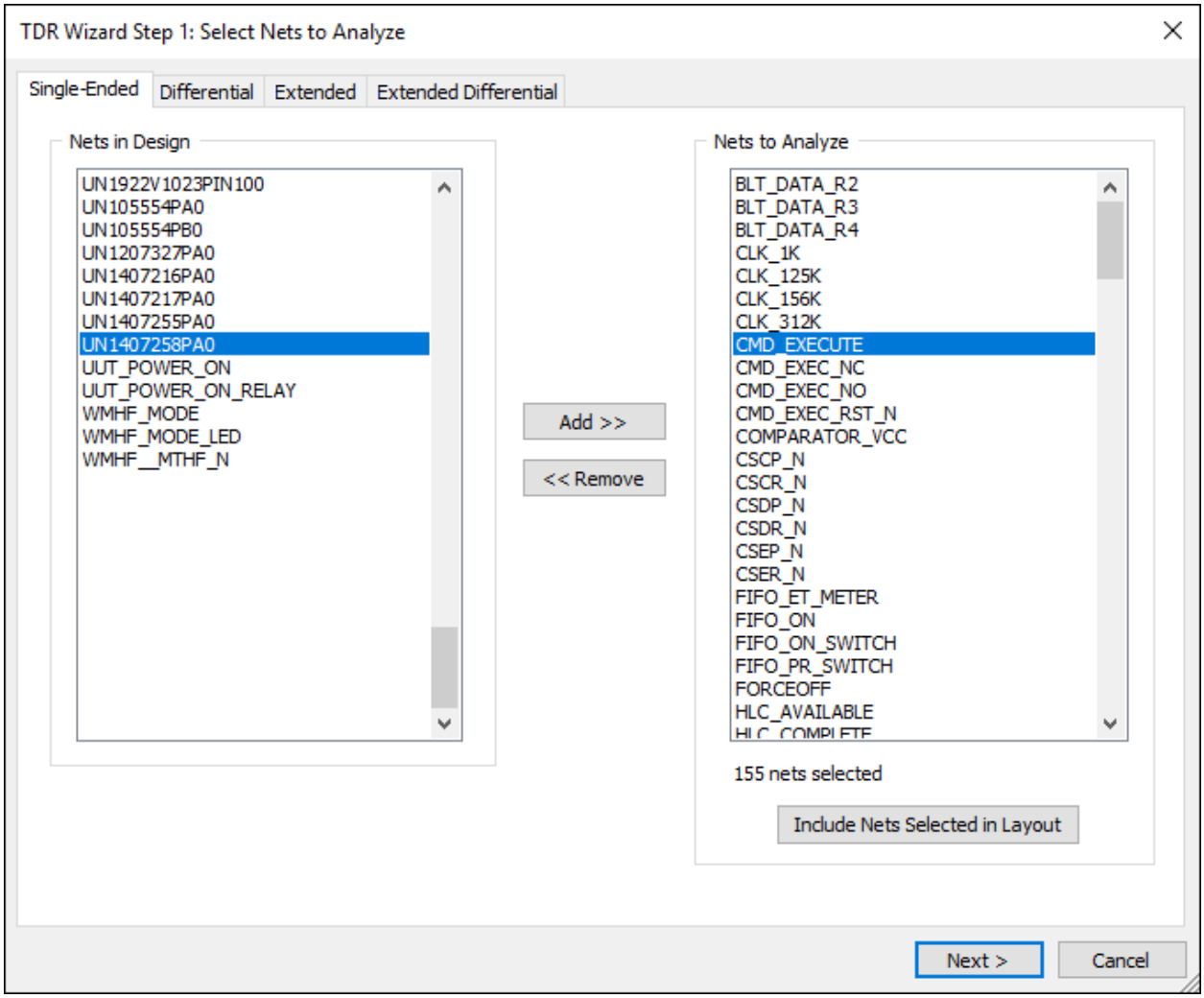

3. Navigate using the **Single-Ended**, **Differential**, **Extended**, and **Extended Differential** tabs. Use the **Add>>** and **<<Remove** buttons to select nets for analysis.
4. Click **Next**.

   The **TDR Wizard Step 2: Select TDR Probe Locations** window appears.

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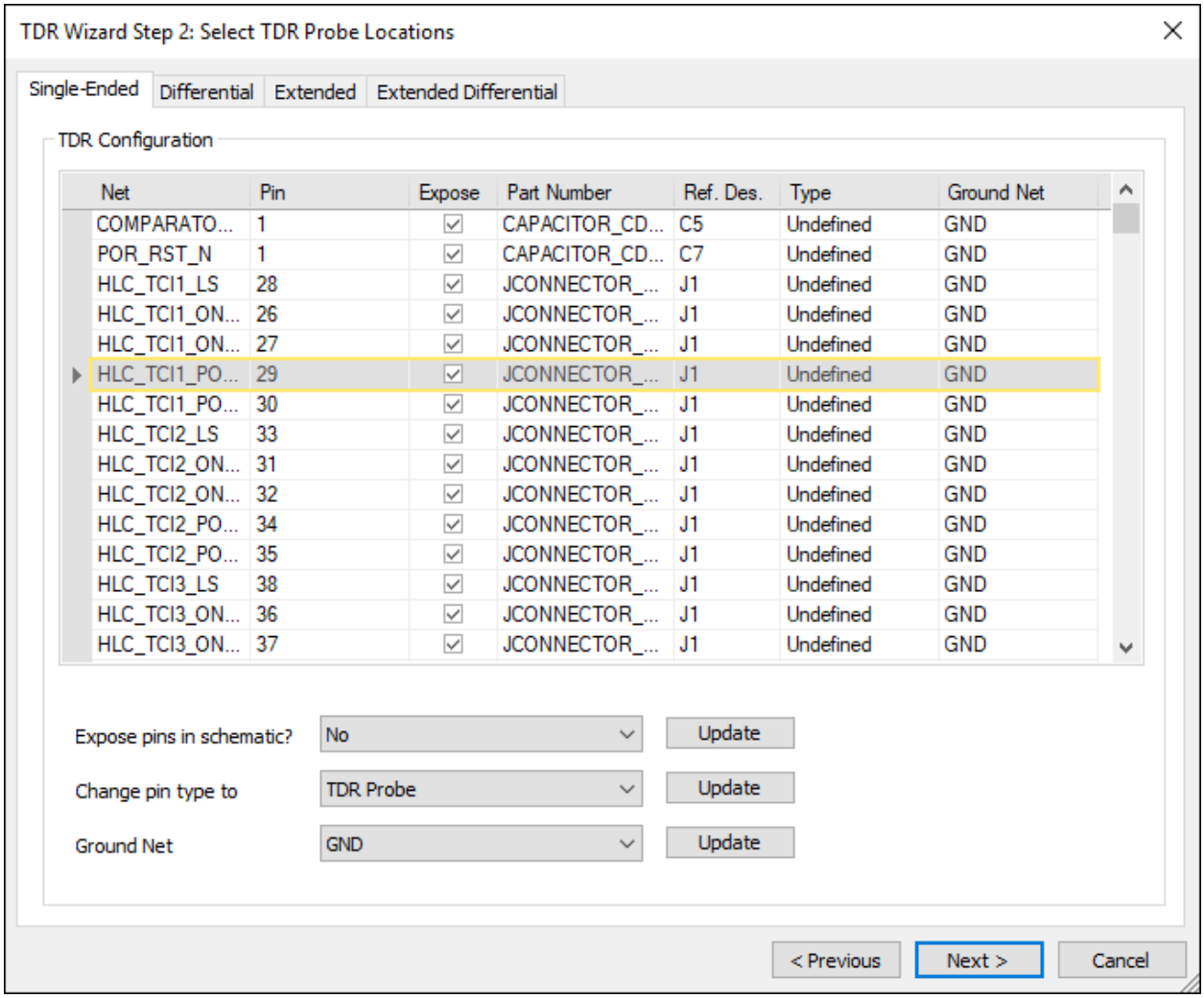

5. Select rows and edit information:
   - **Expose** – check this check box for any pin that should be an external connection to the Ansys Electronics Desktop circuit/schematic.
   - **Type** – use this field to set pins as either TDR probes or terminations.
   - **Ground Net** – use this field to select a pin's ground net.
6. Click **Next**.

   The **TDR Wizard Step 3: TDR Probe and Termination Configuration** window appears.

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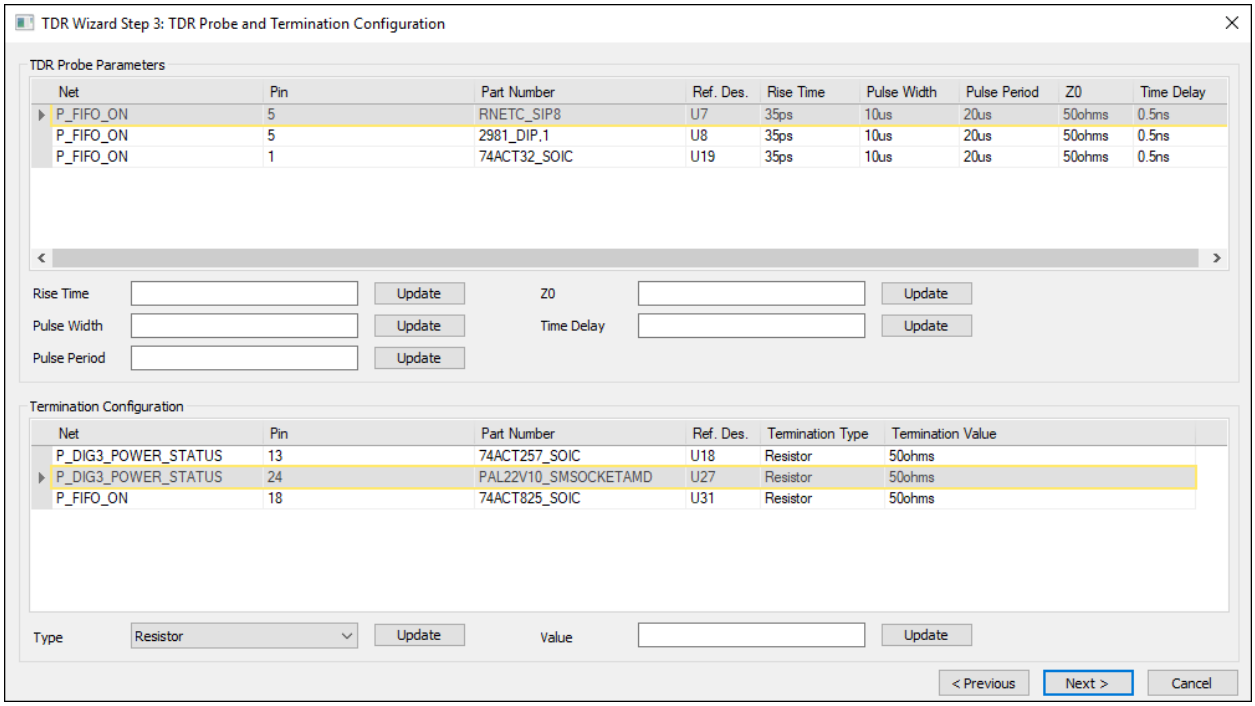

Probe pins display at the top of the window and termination pins display at the bottom.

7. Update the information as appropriate.
8. Click **Next**.

   The **TDR Wizard Step 4: Transient Simulation Options** window appears.

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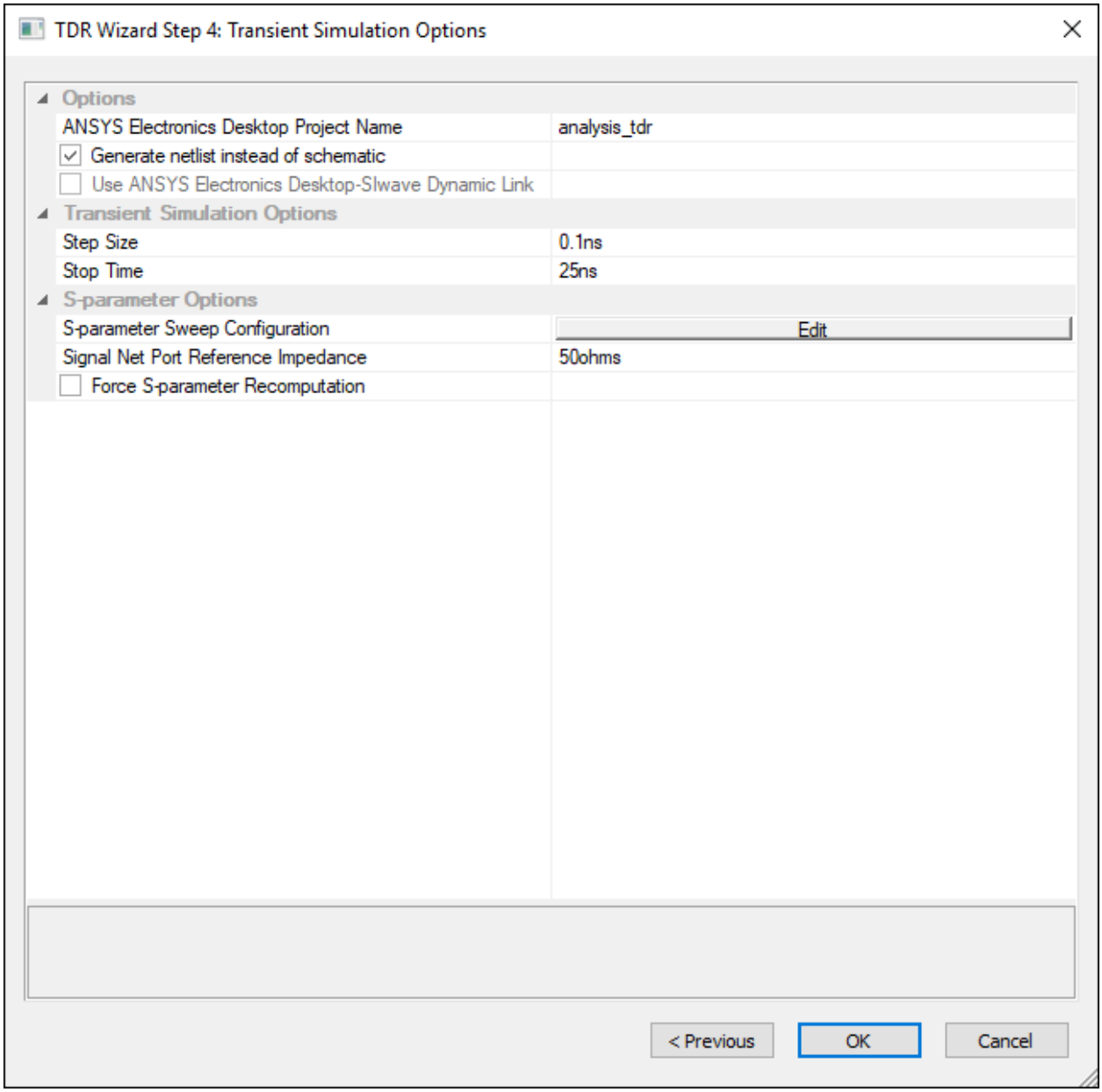

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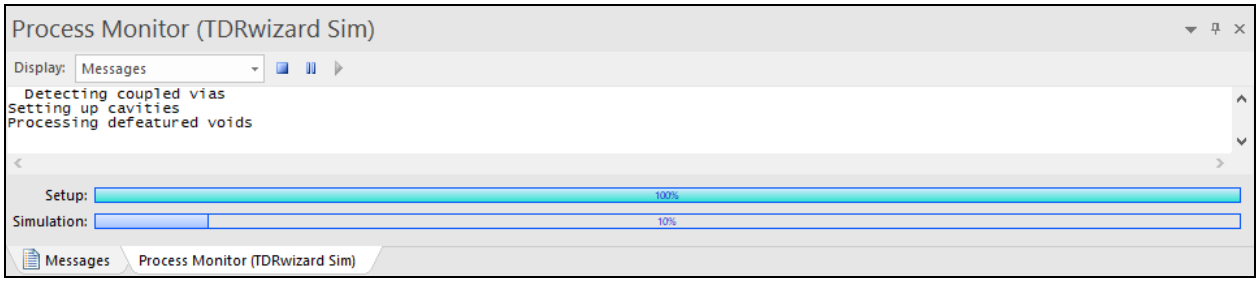
> **Note:**
>
> The **Use Ansys Electronics Desktop-SIwave Dynamic Link** option is only enabled in schematic mode. **Generate netlist instead of schematic** must be deselected in order to use the Dynamic Link.
>
> When Dynamic Link is enabled, the schematic in Electronics Desktop will have a co-simulation block (also called a field solver block) that in turn triggers a solve in SIwave when Electronics Desktop is doing a solve. When Dynamic Link is deselected, the schematic in Electronics Desktop will have an SYZ parameter model block that points to a static touchstone file generated by SIwave just prior to the creation of the schematic in Electronics Desktop.

9. Verify your options and click **OK**.

   The **Messages** window updates with a Process Monitor tab that displays the progress.



When the simulation has finished in SIwave, Ansys Electronics Desktop opens to run the cosimulation. If the netlist option is selected, the net is automatically imported into Ansys Electronics Desktop Circuit/Schematic as a netlist with associated TDR probes and terminations, analyzed by SIwave to obtain the S-parameters, then handed off to Nexxim transient analysis for the time domain simulation. Time domain reports are displayed automatically in Ansys Electronics Desktop. SYZ results are also available in SIwave.

Dynamically Linking from HFSS

An SIwave project can be defined as the source of an incident wave excitation in HFSS. HFSS can use field solutions from other simulations as sources for new simulations. The other simulations can be done in HFSS, SIwave or Maxwell 3D.

Radiated fields from the source project are imposed as an incident wave in the target project. The SIwave project is an excitation in the HFSS project. Therefore, HFSS calls and launches SIwave, but the reverse is not possible.

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As an example of the SIwave - HFSS link, consider a complicated printed circuit board causing EMC/EMI problems in and around its housing.

> **Note:**
>
> Unix operating systems (Linux) must have the environment variable SIWAVE_INSTALL_DIR set for the dynamic link to work. Set this environment variable to point to the directory where the Ansys EM Suite is installed, for example:
>
> `/opt/ansys_inc/v251/AnsysEM`

Remote Solve

SIwave can be run remotely from both Windows and Linux. However, there are some limitations:

1. The profile is not dynamically updated when simulation is running on remote server.
2. Server name definition is not saved (the next time you open a project, it resets to "localhost").
3. Network connection between client and server must be stable during simulation.

Running a Remote Solve on Windows

To run a remote solve on Windows:

1. Install SIwave on both the client machine (the one running SIwave) and the remote server (the one on which simulations are to be executed).
2. Log into the remote server.
3. Specify the location of the intermediate simulation data files by setting the SIWAVE_REMOTE_SOLVE_DIR environment variable:

   ```
   set SIWAVE_REMOTE_SOLVE_DIR=F:/Ansys/simdata
   ```

4. Start siwave_rs in a Console window: `siwave_rs <port number>`

   Enter 31000 as the port number.

   ```
   "C:\Program Files\ANSYS Inc\v251\AnsysEM\siwave_rs" 31000
   ```

   > **Note:**
   >
   > If you get an "siwave_rs: bind() failed with error 10048" message, siwave_rs is already running and listening for simulation requests on the specified port.

5. On the client machine, click **Simulation** > **Options** to open the **SIwave Options** window.

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6. Click the **Multiprocessing** tab and specify the parameters to run a remote solve:
   a. Enter the name or IP address of the **Simulation server name** (e.g., lnxsrv10 or 192.168.1.110).
   b. Enter the **Port** number. Ensure that this port number matches the one used as the parameter to siwave_rs running on the remote server (specified in step 4).
7. Run your simulations as you normally would. All data is compressed prior to transmission over TCP/IP, so transfer between servers is fast.

Running a Remote Solve on Linux

To run a remote solve on Linux:

1. Install SIwave on both the client machine (the one running SIwave) and the remote server (the one on which simulations are to be executed).
2. Log into the remote server.
3. Specify the location of the intermediate simulation data files by setting the SIWAVE_REMOTE_SOLVE_DIR environment variable:

   ```
   setenv SIWAVE_REMOTE_SOLVE_DIR /120gb1/Ansys
   ```

   By default, intermediate simulation data files are stored in the following directory on the remote server: /tmp/<username>/siwave_rs
4. Start siwave_rs in a Console window: `siwave_rs <port number>`

   Use 31000 as the port number.

   ```
   /opt/AnsysEM/v###/siwave_rs 31000
   ```

   > **Note:**
   >
   > If you get an "siwave_rs: bind() failed with error 10048" message, siwave_rs is already running and listening for simulation requests on the specified port.

5. Start siwave_rs in a Console window: siwave_rs <port number>. Try 31000 as the port number.

   ```
   /opt/AnsysEM/v###/siwave_rs 31000
   ```

6. On the client machine, click **Simulation** > **Options** to open the **Simulation Global Options** window.
7. Click the **Multiprocessing** tab and specify the parameters to run a remote solve:
   a. Enter the name or IP address of the **Simulation server name** (e.g., lnxsrv10 or 192.168.1.110).
   b. Enter the **Port** number. Ensure that this port number matches the one used as the parameter to siwave_rs running on the remote server (specified in step 4).

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8. Run your simulations as you normally would. All data is compressed prior to transmission over TCP/IP, so transfer between servers is fast.

CPA Simulations

Chip-Package-Analysis (CPA) is a 3D Finite Element Method (FEM)-based tool for fast and accurate extraction of power and signal distribution networks on IC packages. It can generate per-bump resolution models (thousands of bumps) or user-defined pin grouped models, while preserving ground bounce. The model consists of a passive RLCG Spice netlist and includes package-mounted decaps.

A CPA model comprises DC resistance and low frequency inductance and capacitance effects. High resolution resistance and inductance color maps generated after running a CPA simulation help in package probing. A comprehensive HTML reporting feature summarizes the layout geometry, setup and simulation results. The CPA model can be seamlessly imported into Ansys RedHawk for Chip + Package cosimulation.

This section covers:

- CPA RLGC Simulation Setup
- Computing CPA RLGC Simulations
- Viewing CPA RLGC Results
- Exporting CPA RLGC Results
- Reduce Matrix Operations

CPA RLGC Simulation Setup

Follow these steps to set up the options for a CPA simulation.

> **Note:**
>
> If the design model contains one or more solderballs, each solderball's height must be greater than 5um (i.e., approx 0.196850 mils). Refer to Adding Solderballs to a Package.

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1. Navigate to the **Simulation** tab.

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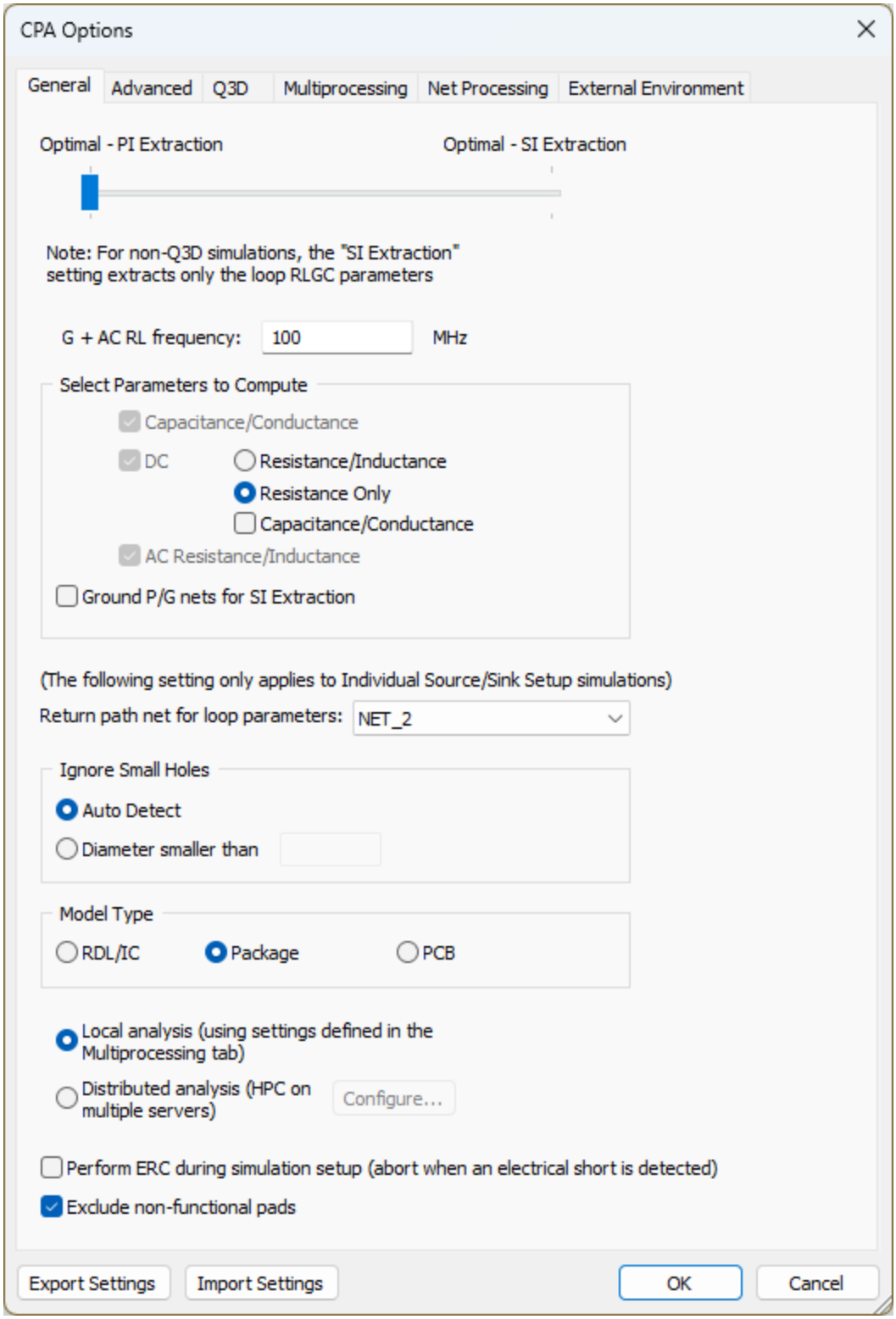
2. From the **CPA** area, click **Options** to open the **CPA Options** window.



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3. Use the slider to set the **Refinement** to either of the following:
   - **Optimal - PI Extraction** - provides a balanced trade-off between simulation performance and accuracy.
   - **Optimal - SI Extraction** - provides a final, exhaustive analysis. This option uses the most amount of computer memory and CPU time. When this option is selected, loop-based RLCG data is extracted. However, if the Q3D option is selected, only partial RLCG is extracted.
4. Enter a value greater than zero in the **G+AC RL frequency** field.
5. From the **Select Parameters to Compute** area, select any/all of the options that apply (i.e., **Capacitance/Conductance**, **DC Resistance/Inductance**, **DC Resistance Only** and **AC Resistance/Inductance**).
6. If appropriate, check the **Ground P/G nets for SI Extraction** box.
7. Use the **Return path net for look parameters** drop-down menu to select a net for CPA to use when computing loop resistance and inductance parameters. By default, **GND** or **VSS** are selected, if present in the design.

   Note:

   Channel setup automatically enables AC/DC resistance and CG extraction, which are required. For more accurate blend results, manually enable DC inductance.

   For Channel Setup:

   - If **FEM** solver is selected, the **Return path net for loop parameters** selection is ignored. This type of simulation always uses the negative VRM net for Loop results.
   - If **Q3D** solver is selected, the **Return path net for loop parameters**selection is respected.

   For Individual Source/Sink Setup:

   - **FEM** and **Q3D** solvers respect the **Return path net for loop parameters** selection.
8. From the **Ignore Small Holes** area, choose whether to **Auto Detect** small holes or select **Diameter smaller than** and specify a value below which holes will be ignored.
9. From the **Model Type** area, select **RDL/IC** for structures containing micron level routing (e.g., RDL structures). The user-configurable **Terminal Diameter** field is ignored and an adaptive 1um or smaller value is used (e.g., dependent on the diameter of the design's terminal facet) to ensure metal is always fully touching. To set a **Terminal Diameter** value, select **Package** or **PCB**. Refer to step 22 to set the Terminal Diameter value.

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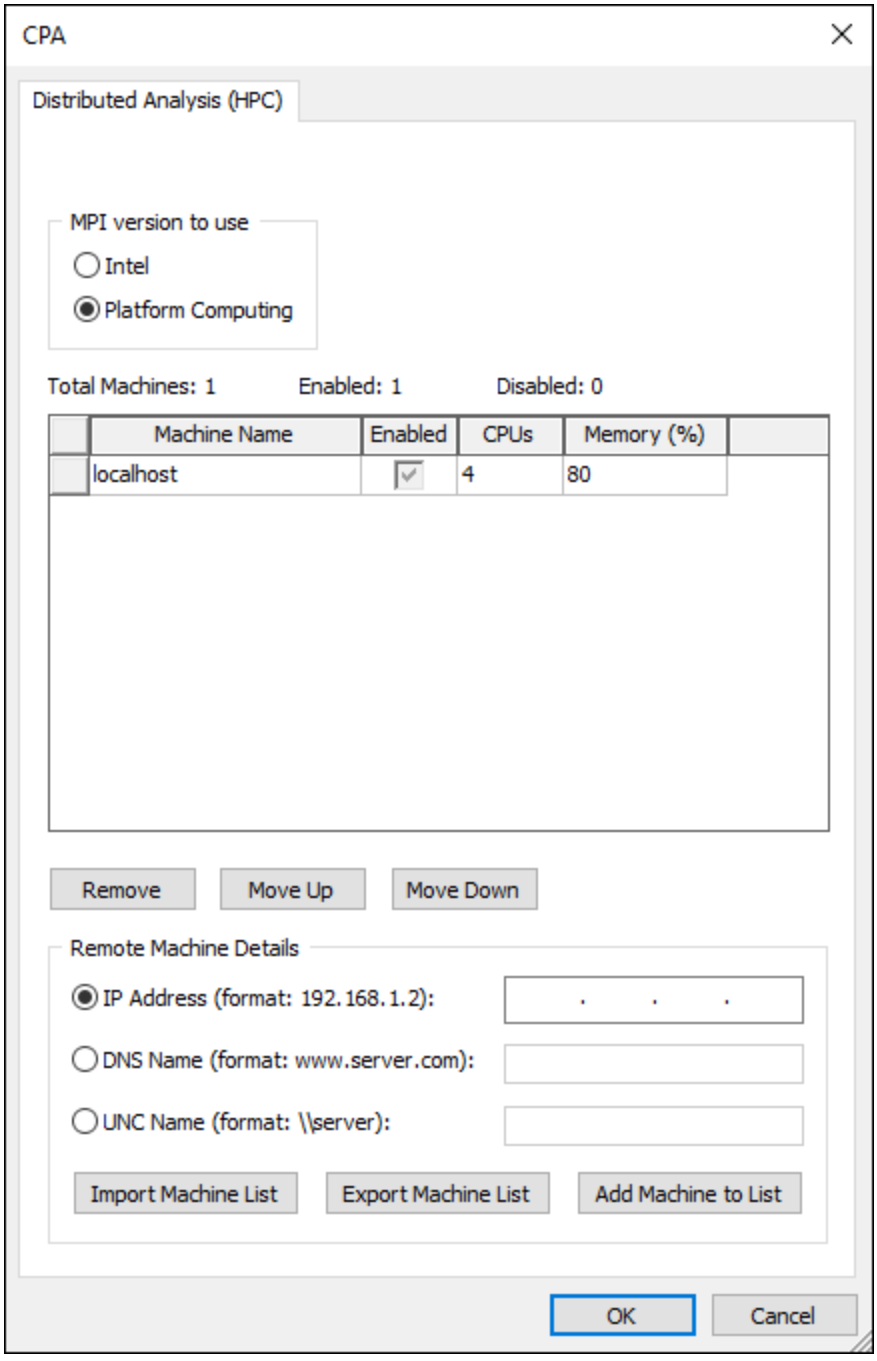
10. Select **Local analysis** or **Distributed analysis**. If users select **Distributed analysis**, click **Configure** to open the **CPA** window and set up remote machines.



11. Once remote machines are set up, click **OK** to return to the **CPA Options** window.
12. Choose whether to check **Perform ERC during simulation setup (abort when an electrical short is detected)**. The ERC (Electrical Rule Check) will analyze the design for

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shorted nets and abort the simulation if shorts are detected. If the box is not checked, the design may detect shorts and will notify users in the **Information/Errors/Warnings** window, but the simulation will continue. If appropriate, also check **Exclude non-functional pads** (checked by default). Doing so will exclude non-functional nets from ERC.

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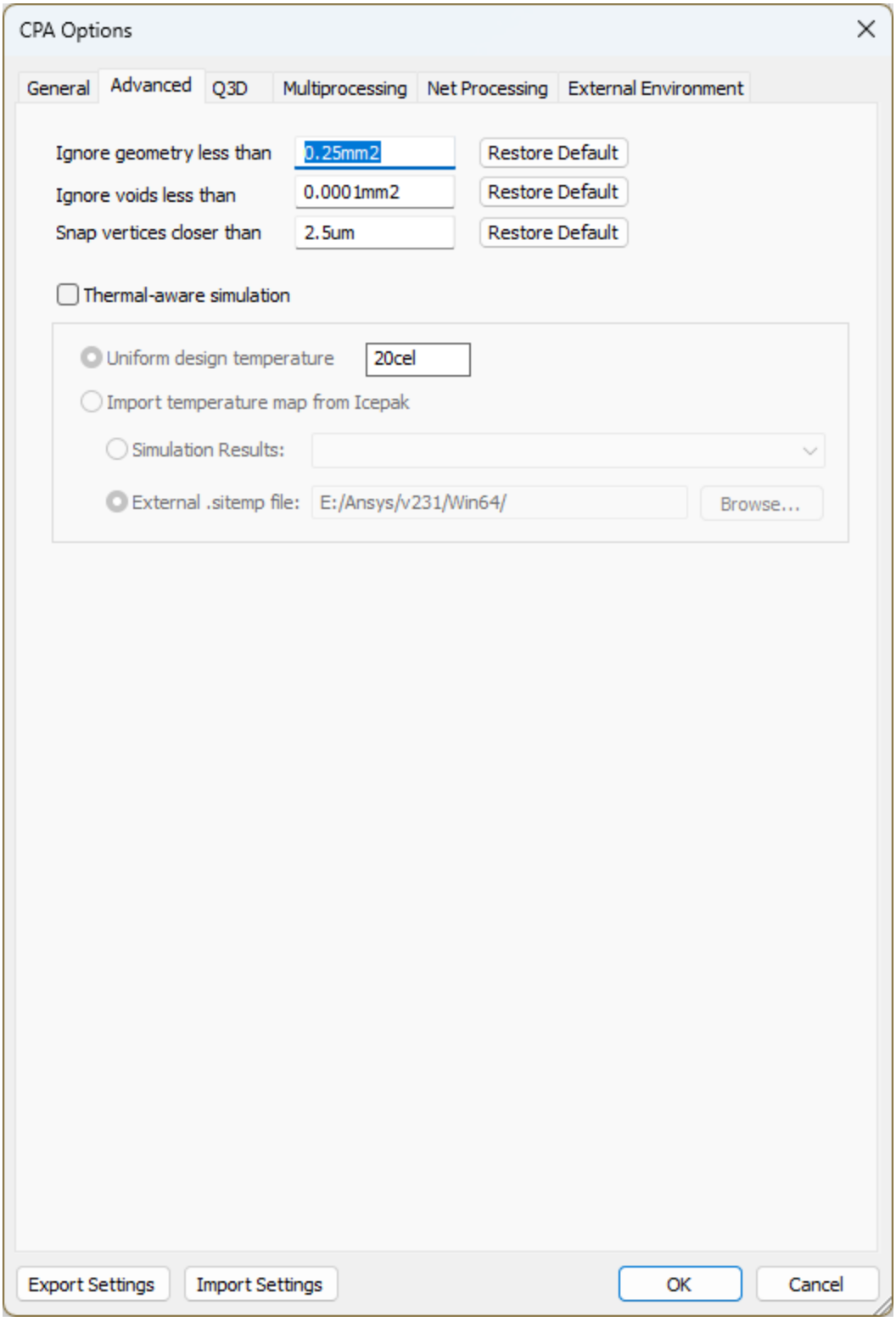
13. Select the **Advanced** tab.



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14. Enter a value in the **Ignore geometry less than** box. Geometry with an area (after being combined with any overlapping geometry) below this specified threshold is ignored during simulation.
15. Enter a value in the **Ignore voids less than** box. Voids whose area (after being combined with any overlapping geometry) falls below this specified threshold is ignored during simulation.

> **Note:**
>
> Ansys recommends using the default settings. Refer to Advanced Geometry Processing Options.

16. Enter a value in the **Snap vertices closer than** box. Entities and vertices that are separated by less than the distance specified in this box may be snapped together during solver pre-processing.
17. Check the **Thermal-aware simulation** box to activate the corresponding options (i.e., step 17).
18. Select **Uniform design temperature** or **Import temperature map from Icepak**.
    - **Uniform design temperature** - sets a global design temperature. Also used to modify the conductivity of metallization during DC IR simulation (i.e., in general, a higher temperature aserts a lower conductivity, implying a higher resistance). Enter a value in Celsius in the field (e.g., 20cel). Temperatures below absolute zero cannot be simulated (e.g., -273.15cel).
    - **Import temperature map from Icepak** - choose **Simulations Results** and select an Icepak temperature distribution file (i.e., a sitemp file) from the drop-down menu (e.g., **Icepak Sim 1**), or choose **External .sitemp file**, then **Browse** to an appropriate directory and select a saved or exported .sitemp file (e.g., **E:\Ansys\v251\board.1.sitemp**). The temperature data is used to locally adjust DC conductivity.

> **Note:**
>
> Temperature modifiers (selected per material for the project) must be defined before launching a thermal aware simulation or the CPA simulation will complete without temperature dependence. Completing a DC IR simulation, then an Icepak simulation before a CPA simulation is the simplest path. Refer to "Computing DC IR Simulations" on page 9-78 and "Computing Icepak Simulations" on page 9-163.

19. Select the **Q3D** tab.

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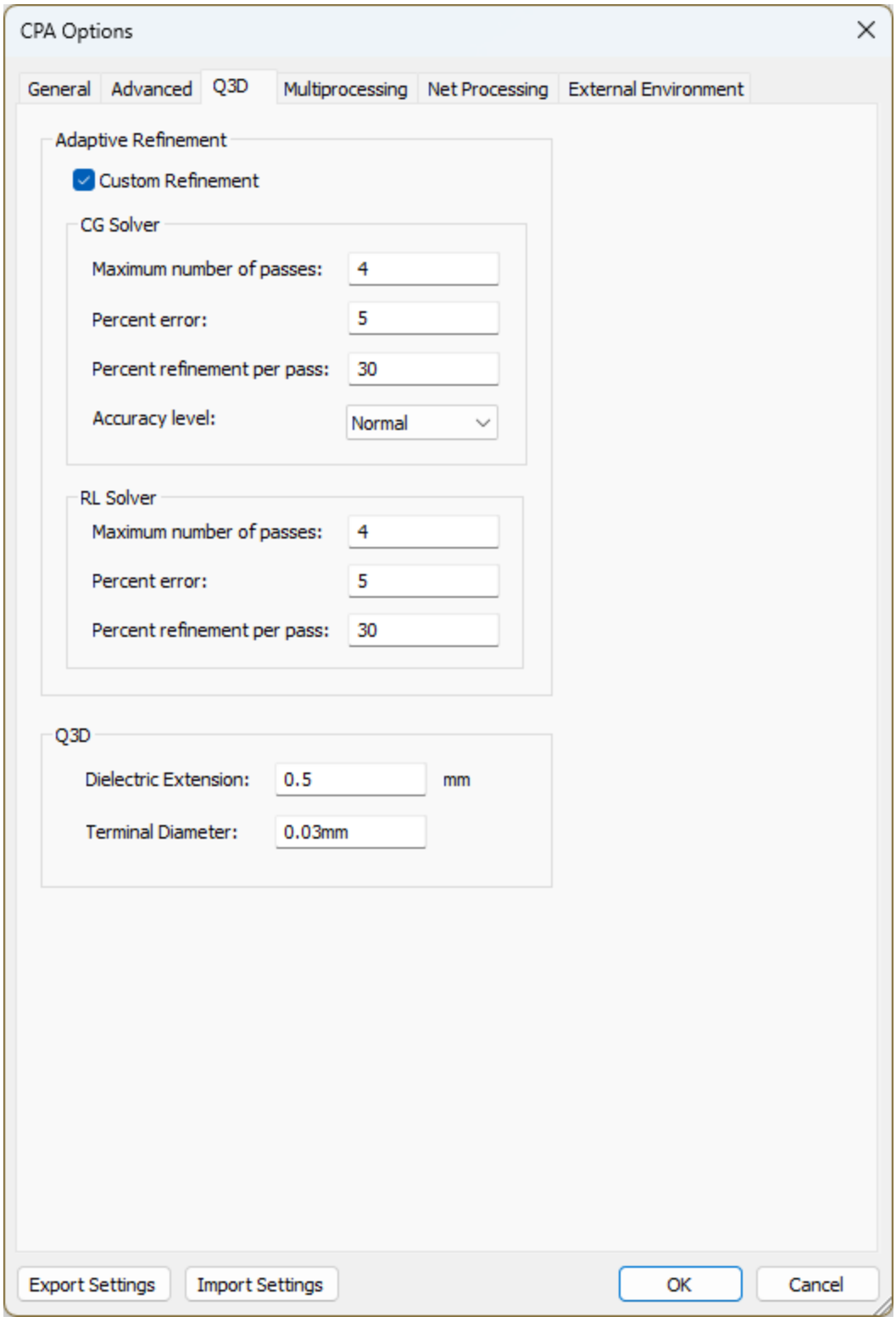

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20. From the **Adaptive Refinement** area, check the **Custom Refinement** box to activate the **CG Solver** and **RL Solver** areas.
21. Enter the following **CG Solver** and **RL Solver** parameters:
    - **Maximum number of passes** and **Percent error** - specify stopping criteria. SIwave exits the adaptive loop as soon as one of these criteria is satisfied.
    - **Percent refinement per pass** - specify what percentage of high-error triangles should be refined during each iteration.
    - **Accuracy Level** - select **Normal** or **High** from the drop-down menu. If **Normal** is selected, the solver will give accurate results for most applications. If **High** is selected, the solver provides greater accuracy at the expense of speed and memory.
22. From the **Q3D** area, specify the following options:
    - **Dielectric Extension** – defines how much additional dielectric material should be added surrounding the geometry.
    - **Terminal Diameter** – defines the size of sources and sinks for RL extraction, except those defined on solderballs and bumps. For sources and sinks defined on solderballs/bumps, the respective diameters of the solderballs/bumps are used to set the sizes. *This option is not applicable if the selected **Model Type** is **RDL/IC***.

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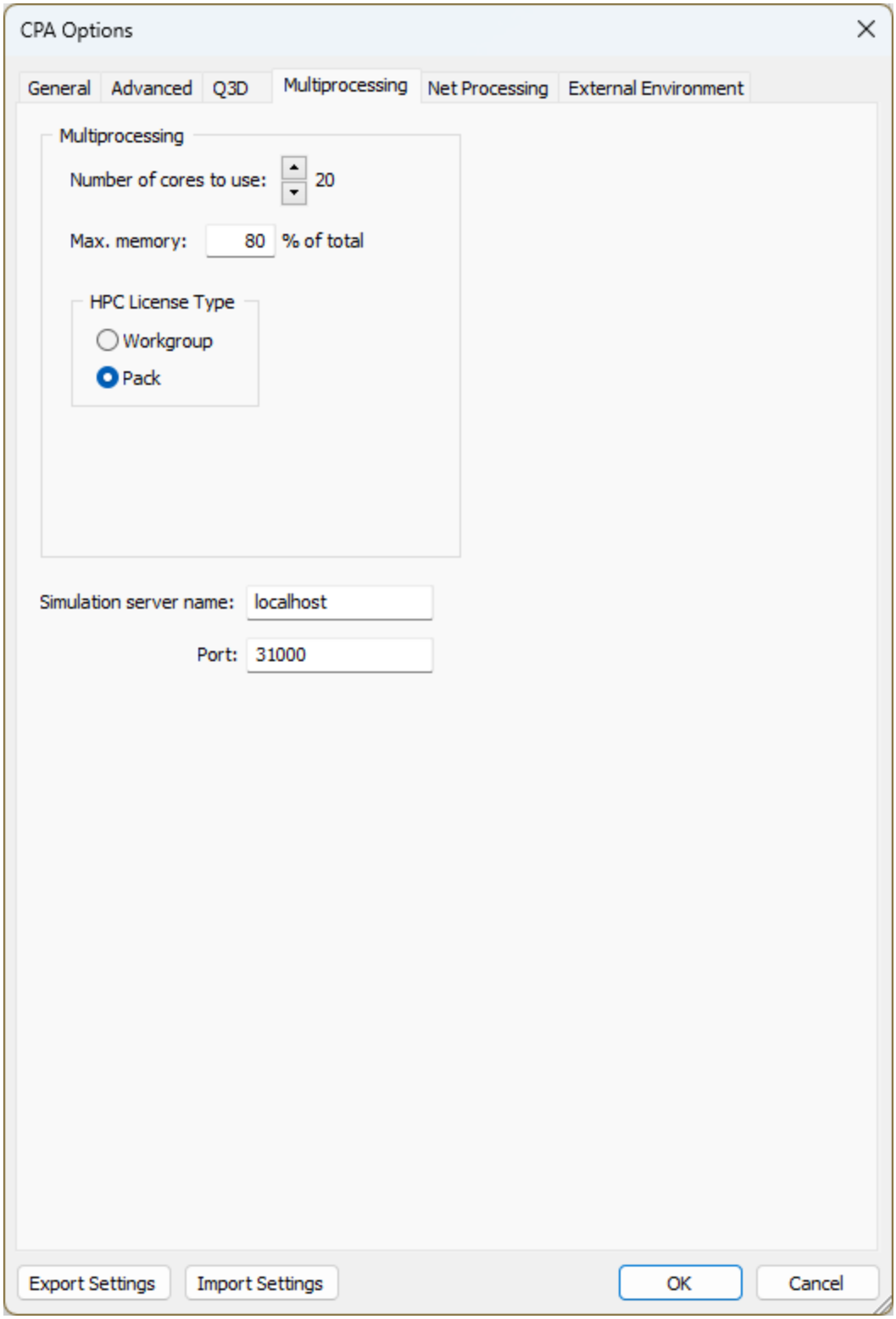
23. Select the **Multiprocessing** tab.



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24. Set the **Number of cores to use** when computing the solution. This feature is available only if users purchased the multiprocessing or HPC license option for SIwave.
25. Enter a value in the **Max. Memory** field to set the memory used as a percentage of total RAM. This option is only available if **Use HPC licensing** is selected (i.e., step 24.).
26. Check the **Use HPC licensing** box to enable shared memory multiprocessing.
27. Select **Use Ansys HPC licenses** or **Use legacy Electronics HPC licenses**.

> **Note:**
>
> The option to choose a license type (either Ansys HPC or Electronics HPC) is not available when SIwave is running in Pro/Premium/Enterprise licensing mode.

28. From the **HPC License Type** area, select **Pool** to use HPC licenses for distribution or **Pack** to use HPC Pack licenses.
29. Enter the name or IP address of the simulation server in the **Simulation server name** field.
30. Enter the **Port** number. See: Remote Solve for details on setting up for remote solves.

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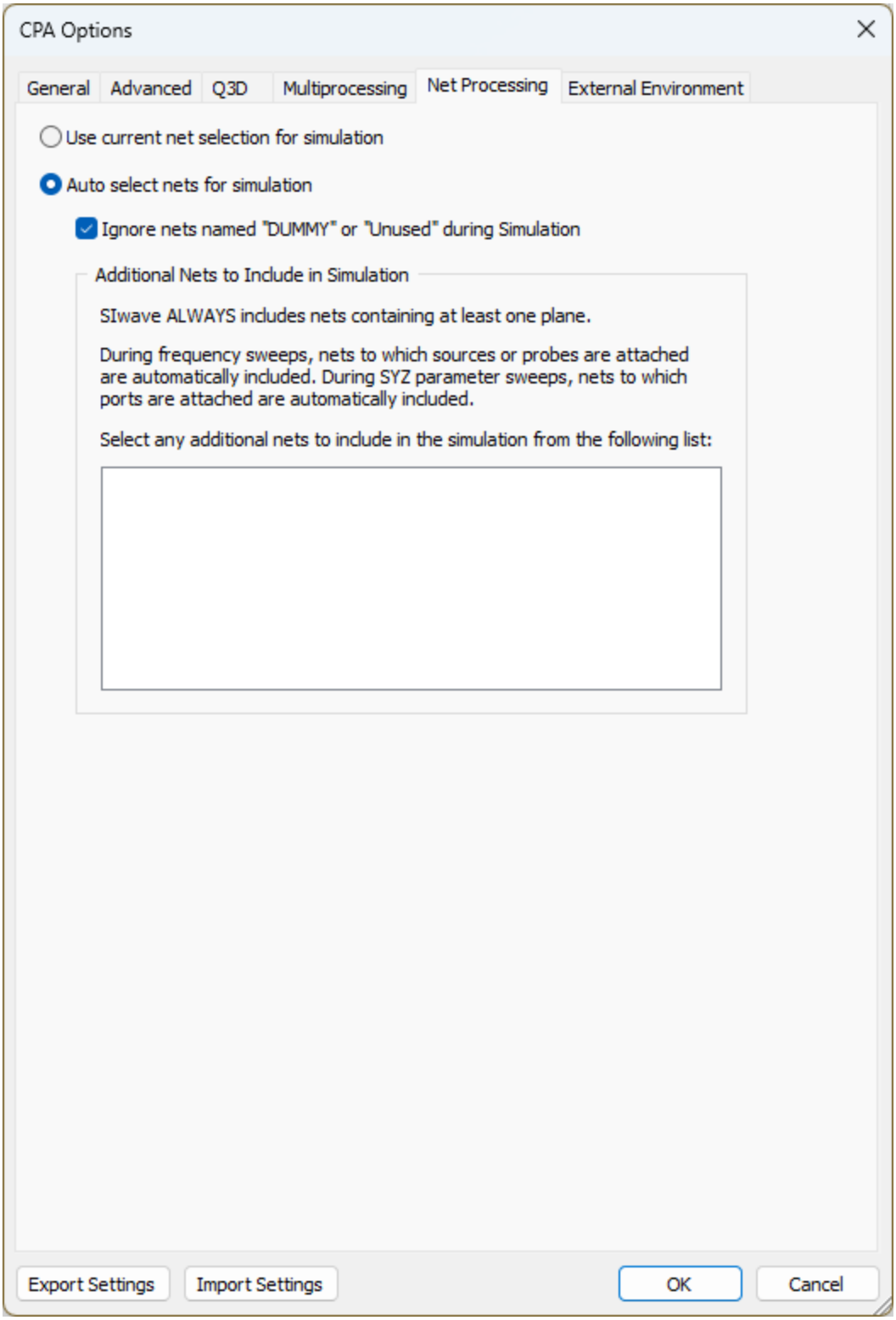
31. Select the **Net Processing** tab.



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32. Select **use current net selection for simulation** to run a simulation including only the nets that are selected in the **Nets** workspace. Otherwise, leave the default setting of **Auto select nets for simulation**.To include dummy/unused nets in the simulations, clear the **Ignore nets named "DUMMY" or "Unused" during Simulation** check box. By default, these nets are ignored.

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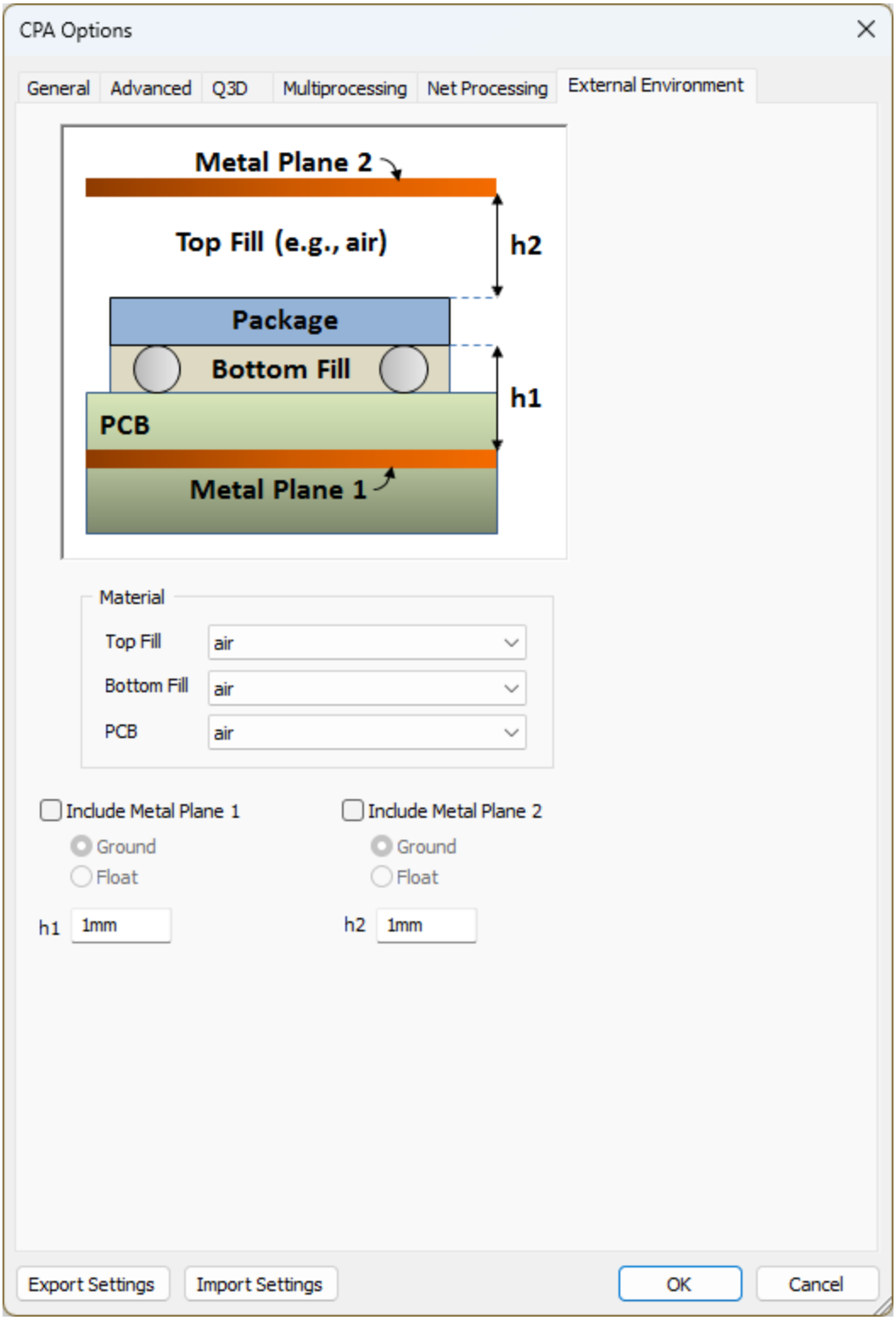
33. Select the **External Environment** tab.



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34. From the **Material** area, use the **Top Fill**, **Bottom Fill**, and **PCB** drop-down menus to select materials.
35. Check the **Include Metal Plane 1** and/or **Include Metal Plane 2** boxes to add up to two metal planes to the model. This option is applicable to the Q3D solver choice only. **Metal Plane 1** represents the upper PCB Ground or VDD plane. **Metal Plane 2** can represent a metal cover, a heat sink, or any other metal plane located above the package. This metal plane behaves similarly to **Metal Plane 1**.
36. For each selected metal plane, select **Ground** or **Float**.
    - **Ground** - uses the metal plane as part of the return path. This configuration affects the inductance and capacitance of the package nets.
    - **Float** leaves the metal plane floating. This configuration affects only the capacitance of the package nets.
37. For each selected metal plane, enter a value for height.
    - **h1** - distance from the bottom layer of the package stackup to the top of **Metal Plane 1**. The solder balls included in this space add to the inductance and capacitance effects on the package nets.
    - **h2** - distance from the top layer of the package stackup to the bottom of **Metal Plane 2**.
38. Click **OK** to save CPA options and exit the **CPA Options** window.

CPA Control XML File

Use a **cpa_control.xml** file to set other options. *This file should be placed in the same folder as the *.siw project file*.

A sample file is shown below:

```
<?xml version="1.0" encoding="utf-8"?>

<!-- Individual sections can be disabled by setting Enable=No -->

<CPA_Control_Specs>

<!-- If enabled, the annotated ploc file would use this chip layer
name -->

<Chip_Layer_Name Enable="yes" Name="ic_m1_layer">

<!-- All units in mm and are in package DIE coordinates -->

<!-- Only the die pins (having PLOC connections) falling within this
polygon region are extracted -->

<Partial_DIE_Region Enable="no">

    <Point x="-5.0" y="5.36"/>

    <Point x="-5.0" y="0.37"/>
```


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```
    <Point x="5.5" y="0.37"/>
    <Point x="5.5" y="5.36"/>
</Partial_DIE_Region>
<Partial_DIE_Region Enable="no">
    <Point x="-5.0" y="5.36"/>
    <Point x="-5.0" y="0.37"/>
    <Point x="5.5" y="0.37"/>
    <Point x="5.5" y="5.36"/>
</Partial_DIE_Region>
<Partial_DIE_Region Enable="no">
    <Point x="-5.0" y="5.36"/>
    <Point x="-5.0" y="0.37"/>
    <Point x="5.5" y="0.37"/>
    <Point x="5.5" y="5.36"/>
</Partial_DIE_Region>
<!-- Voltage values are in volts -->
<!-- The unconnected PLOC pins corresponding to these Chip nets are
terminated with voltage supplies -->
<Open_PLOCpins_VoltageSupply Enable="no">
    <Net Name="NewNet1" Voltage="1.2847"/>
    <Net Name="NewNet2" Voltage="2.384"/>
</Open_PLOCpins_VoltageSupply>
</CPA_Control_Specs>
```

Computing CPA RLGC Simulations

CPA setup comprises three parts: Die, Channel Components, and the VRM. You can compute an RLGC simulation for the CPA Channel Setup, or for individual sources and sinks.

To compute an RLGC simulation in SIwave:

1. Click **Simulation**.
2. From the CPA area, click **Compute RLGC**.

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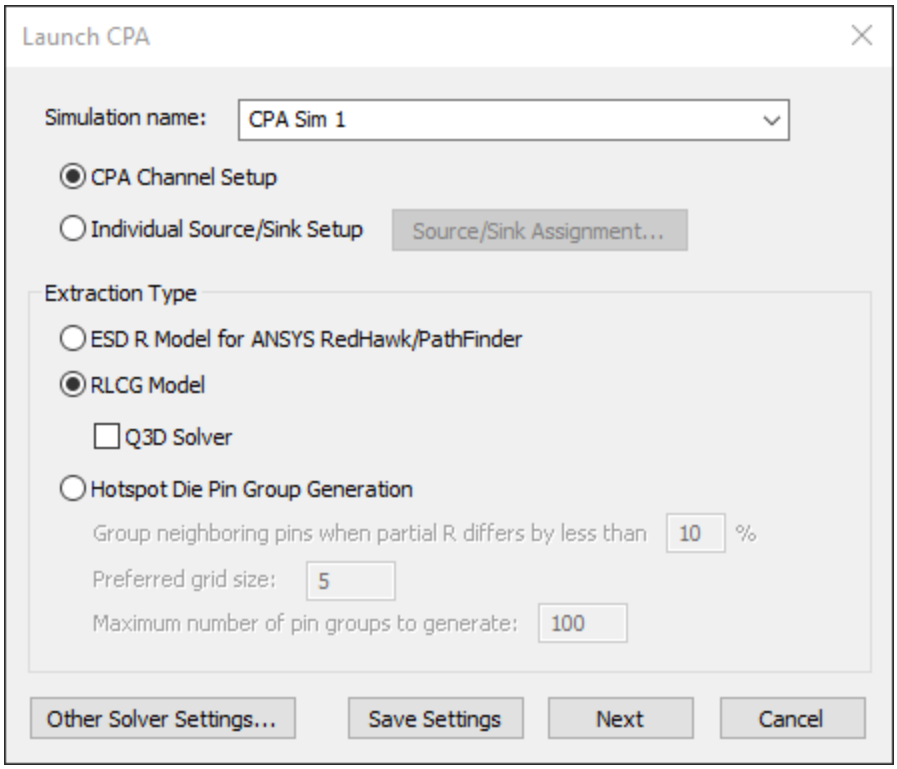
The **Launch CPA** window appears.



3. Enter a name for the simulation, or leave the default.
4. Select either **CPA Channel Setup** or **Individual Source/Sink Setup**.

> **Note:**
>
> If you select **Individual Source/Sink Setup**, the **Next** button becomes a **Launch** button.

5. If you wish to compute for individual sources and sinks, click **Source/Sink Assignment** and set the options:

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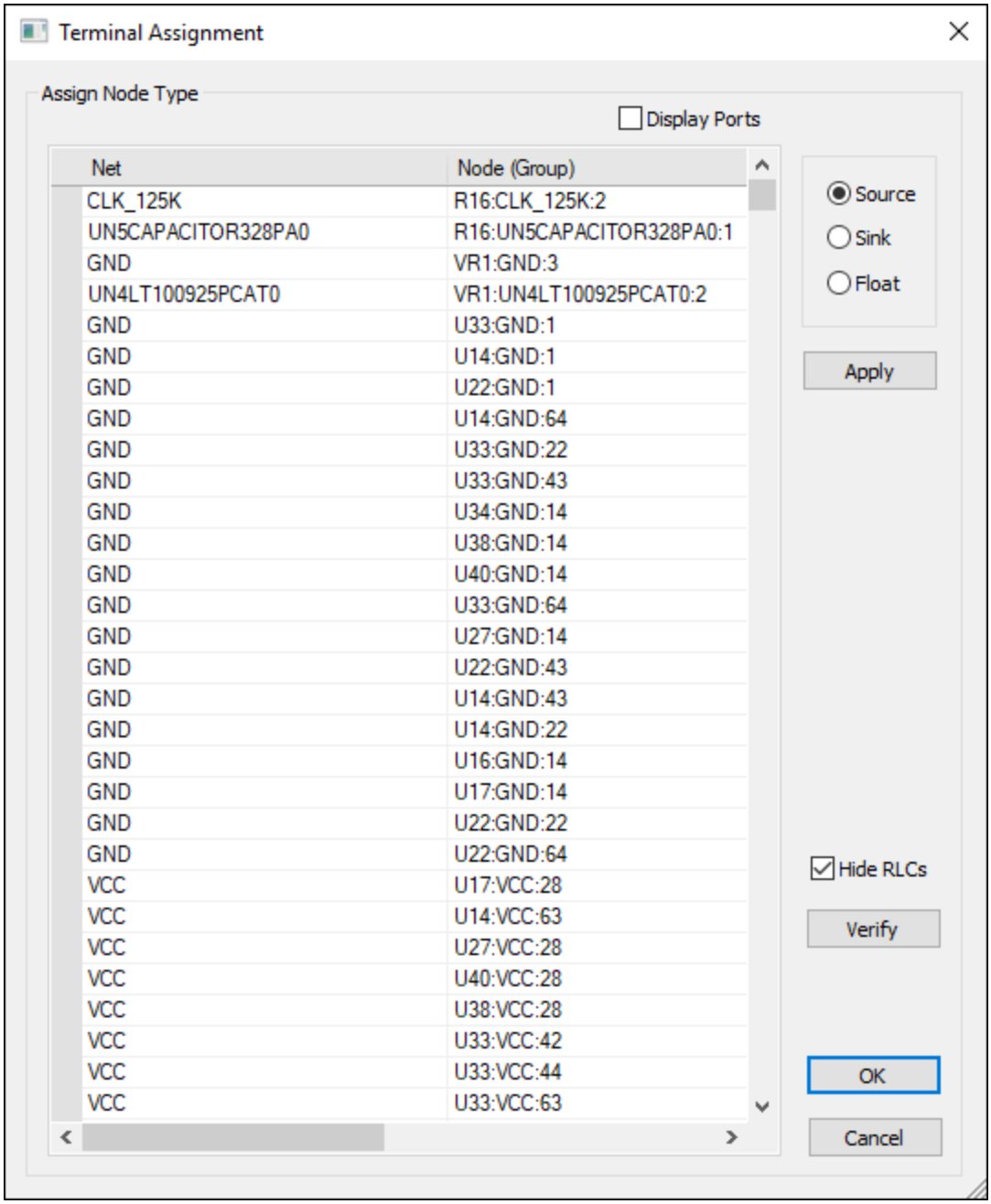

Each net is automatically assigned a Node Type. Dummy and unused nets (named NC, DNU, Dummy, etc.) are set to Float by default.

To change the settings:

- Select one or more rows, select **Source**, **Sink**, or **Float**, and click **Apply**.
- Click **OK** to verify the settings and return to the **Launch CPA** window.

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> **Note:**
>
> If a net has only sources or only sinks, the **Source/Sink Count** error window appears. You must correct the listed errors before proceeding.

6. Select the **Extraction Type**:
   - **ESD R Model** – select for Pure DC resistance extraction with the Spice netlist customized for Chip ESD applications.
   - **RLCG Model** – select to use the FEM solver. This has a high capacity and fast turn-around time, and is recommended for large PDN structures and/or having several hundreds of source terminals.
   - **Q3D Solver** – select to use the Q3D MoM solver with adaptive meshing. This is recommended for high accuracy applications, and is ideal for lead frames and small scale packages.
   - **Hotspot Die Pin Group Generation** – Rather than extracting every pin (which can make the netlist prohibitively large) or using a grid (which can omit hot spots), this option identifies hotspots and generates pin groups according to the specified partial R percentage, preferred grid size, and maximum number of groups appropriate. This option is only compatible with **CPA Channel Setup**. If you select **Individual Source/Sink Setup**, this option will be unavailable. Selecting this option removes the **Simulation Name** field, as it is not appropriate for pin generation.

   > **Note:**
   >
   > Pin groups created using this method have names beginning with SmartG.
   > See: Grouping Pins.

7. Click **Other Solver Settings** to launch the **SIwave Options** window with the **CPA** tab selected.
8. If you selected individual sources and sinks, click **Launch** to run the simulation. The messages window updates and the simulation completes.
9. If you selected CPA Channel Setup, click **Next**.

   The **SIwave-CPA Simulation** window appears. Navigate through the tabs to set options.

   > **Note:**
   >
   > For Hotspot Die Pin Group options, see: Grouping Pins.

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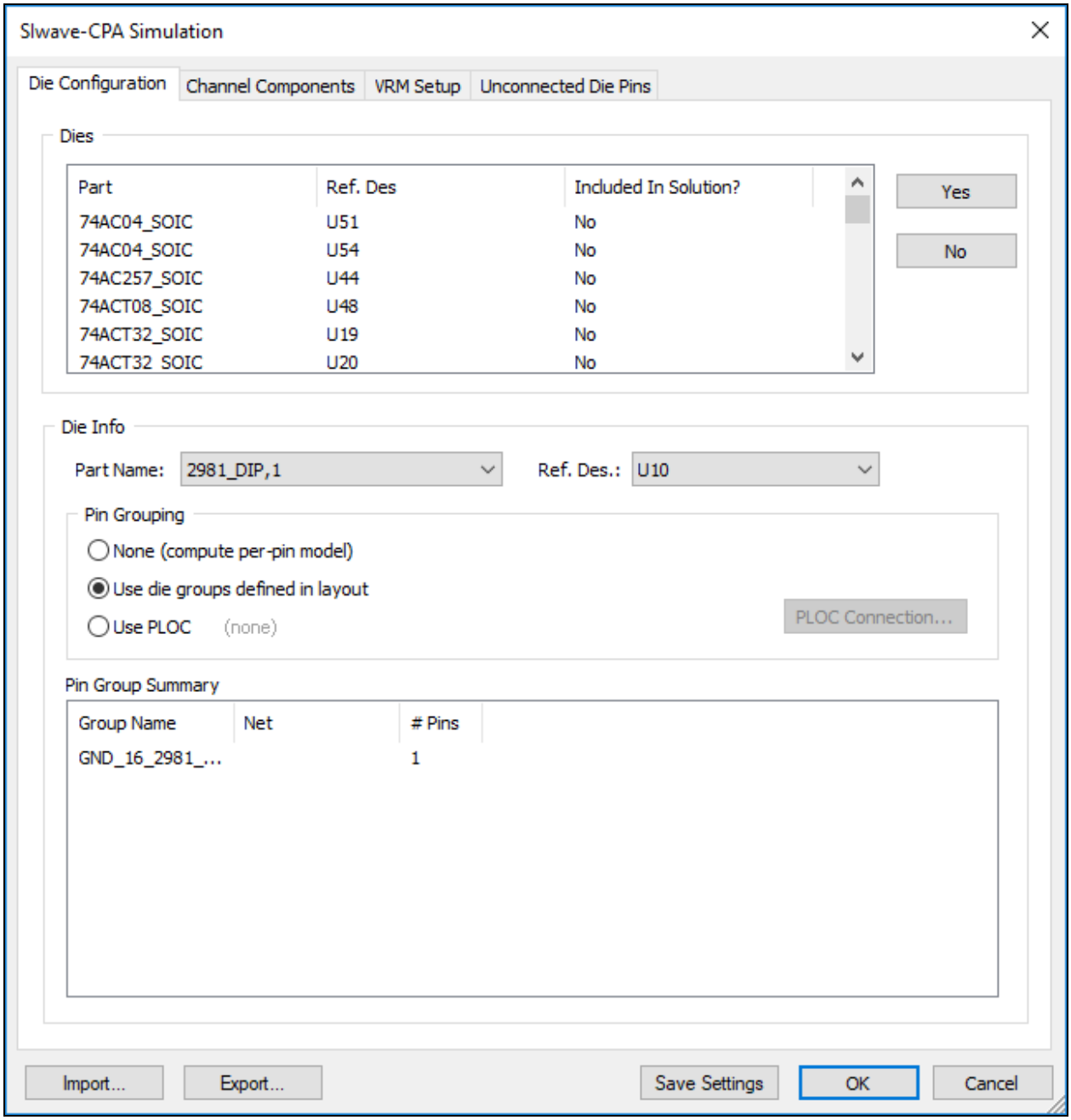
10. On the **Die Configuration** tab:



The **Dies** area lists available dies. Each die can be set up independently to use per-pin model, die pin groups defined in layout, or PLOC. Dies showing **Yes** in the **Included in Solution** field are extracted.

- Select dies in the list and use the **Yes** and **No** buttons to select whether they are included in the simulation.

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- Selecting a die from the list populates its **Part Name** and **Ref Des** in the **Die Info** area below.
- Specify **Pin Grouping** for each selected die.
  - **None** – computes per-pin model.
  - **Use die groups defined in layout** – select and extract only the die pins that belong to a group. To extract all pins, use a sufficiently dense grid. Create a pin group for each of the die pins.
  - **Use PLOC** – import and automatically connect to the die component using the **PLOC Connection** button. Selecting this option enables the options on the **Unconnected Die Pins** tab.
- Review the **Pin Group Summary**.

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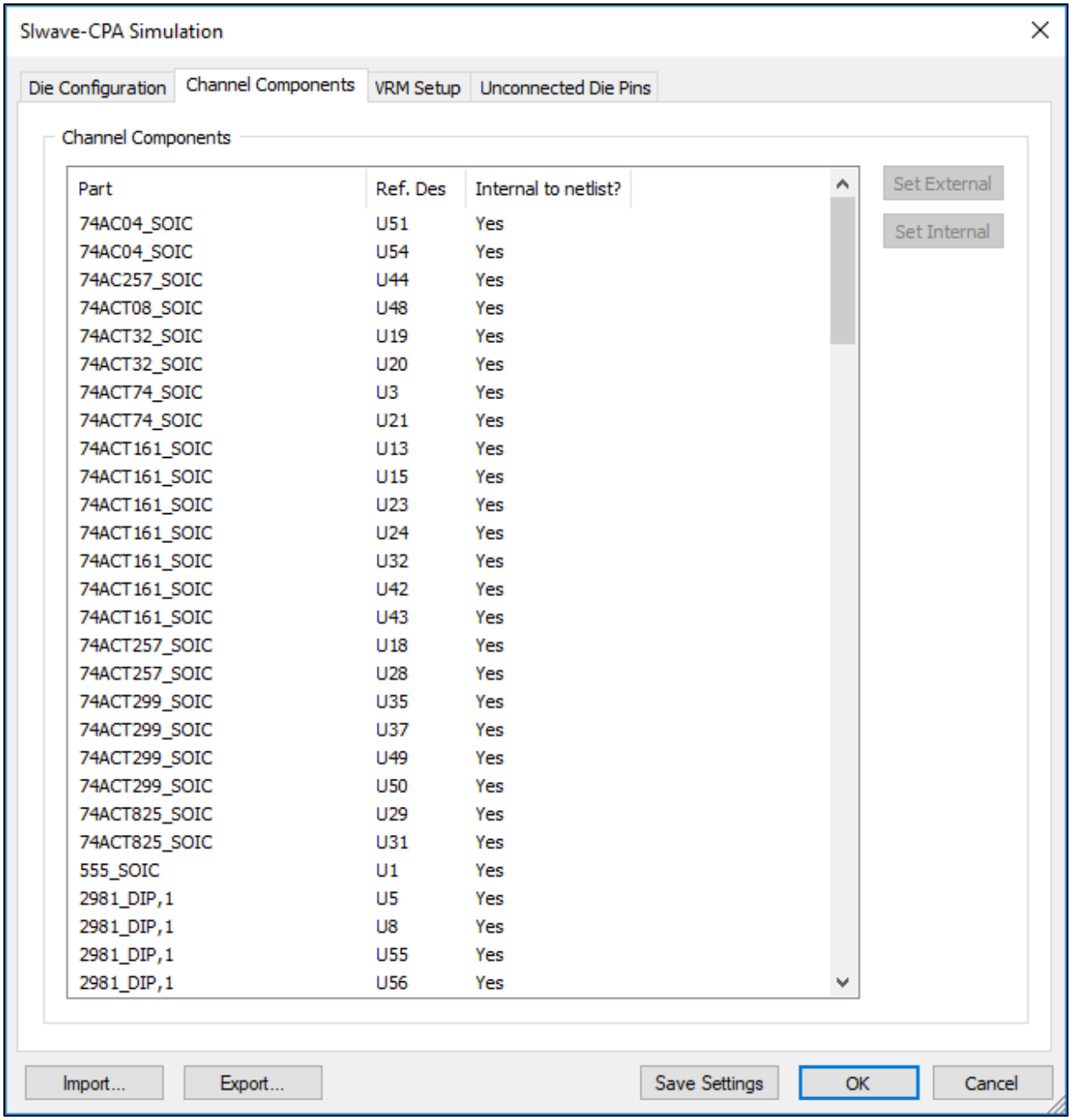
11. On the **Channel Components** tab:



- Review the **Channel components**. These are passive components mounted on the package (other than the Die and BGA). If any passive component has a capacitor models specified, those component pins are automatically extracted and exposed in the Spice netlist. This helps in studying subsequent what-if scenarios without having to go through the extraction again. If a component contains simple R and L elements, these components are absorbed into the extraction and not exposed at the Spice netlist level.

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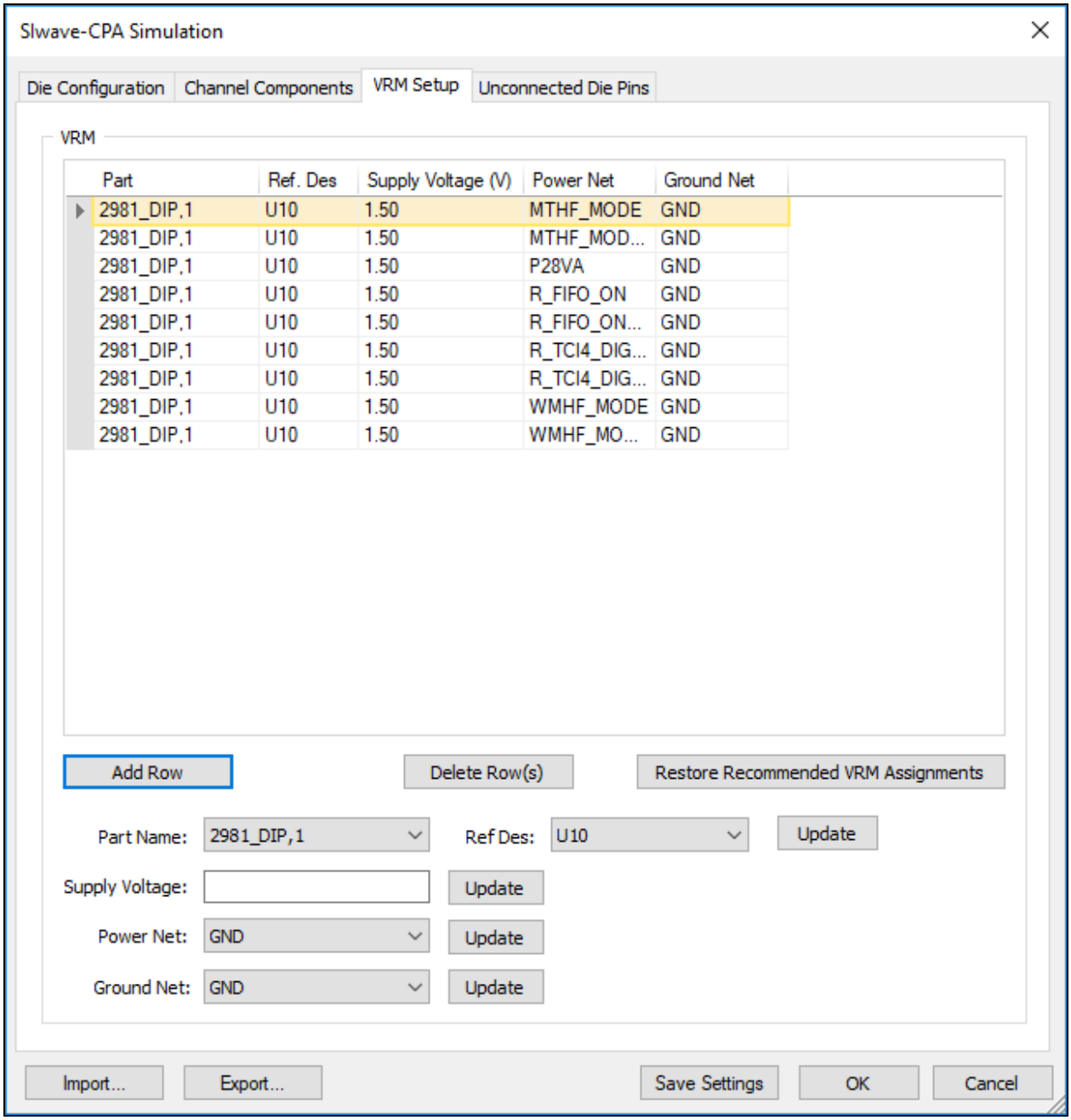
12. On the **VRM Setup** tab:



- Specify BGA components and pins that supply voltage and ground to the die. To select parts, use the **Part** and **Ref. Des** drop-down menus, or click the gray area adjacent to a row. You can select multiple rows using Ctrl+click.
  - Select a **Power Net** and **Ground Net** to be extracted, and specify the **Supply Voltage**. Use the **Add Rows** and **Delete Rows** buttons to add and remove parts as appropriate. You can also **Restore Recommended VRM Assignments**.

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- The net with the largest number of BGA component pins is designated as the Reference (Ground) net. Other nets are routed to BGA component, and are terminated with a DC supply voltage of 1.5V by default. This value can be edited independently for each net, and the voltage level can be modified even after the extraction. If a suitable PCB model is available, it can replace the VRM model after the extraction is done.
- The pin groups defined on the BGA component are extracted and VRM supply voltages are distributed to these groups. If no pin groups are defined, all the pins for each net are grouped automatically, and the supply voltages are connected on net-by-net basis.

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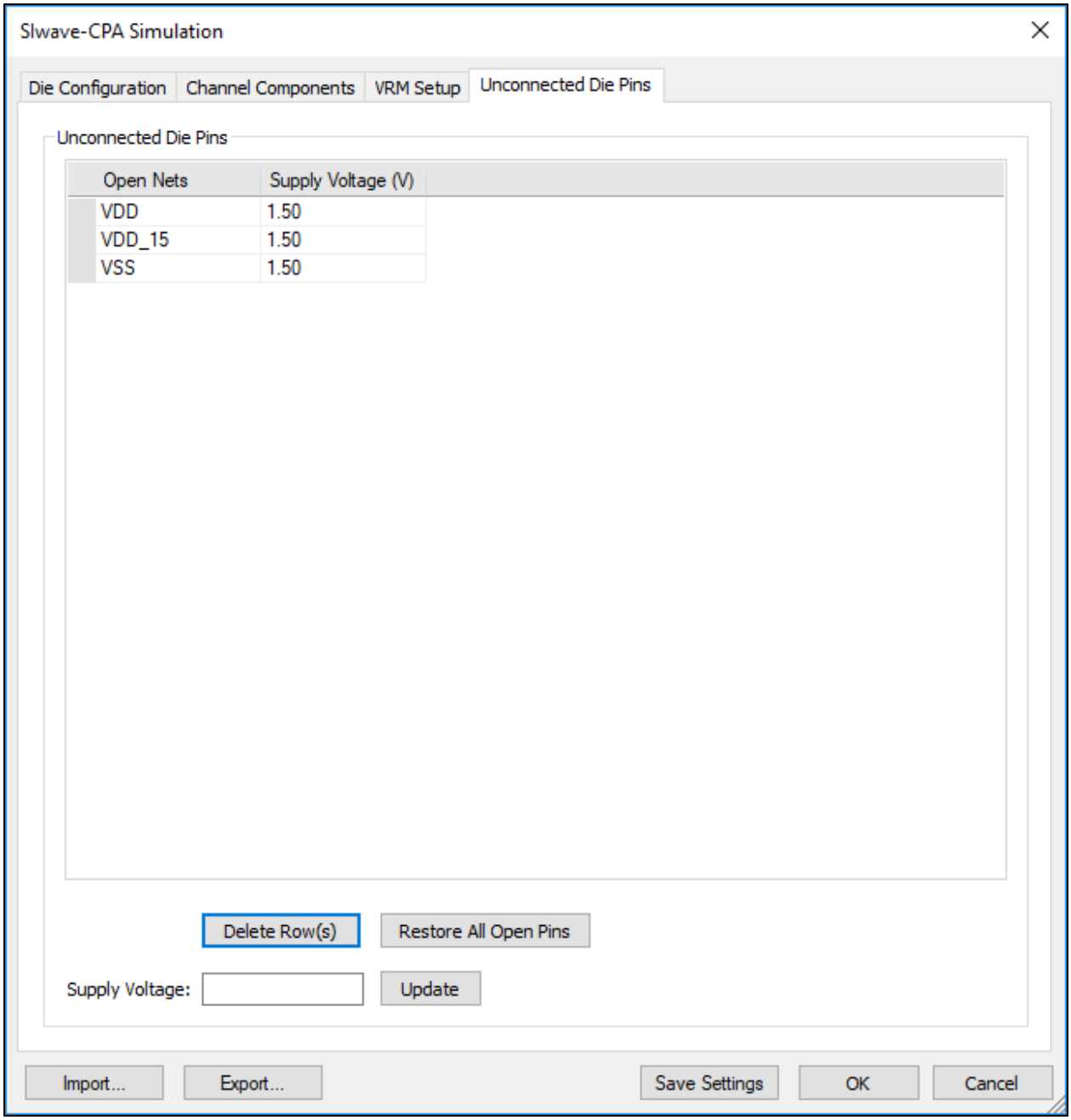
13. On the **Unconnected Die Pins** tab:



- Specify Supply Voltage values for any unconnected PLOC nets. To update a voltage value, select a net, enter a value in the **Supply Voltage** field, and click **Update**.

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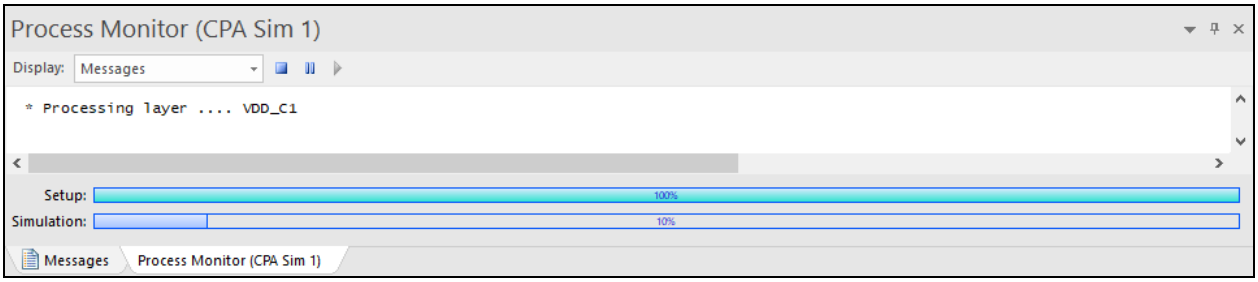
> **Note:**
>
> The controls on the **Unconnected Die Pins** tab are only available if **Use PLOC** has been selected for a die on the **Die Configuration** tab.

14. From any tab, use the **Export** button to save the settings as an XML file. Use the **Import** button to load settings from an existing XML file.
15. Click **OK** to start the CPA model extraction.

The **Messages** window updates with a Process Monitor tab that displays the progress.



If any errors are encountered, the **Simulation Log** appears, summarizing them.

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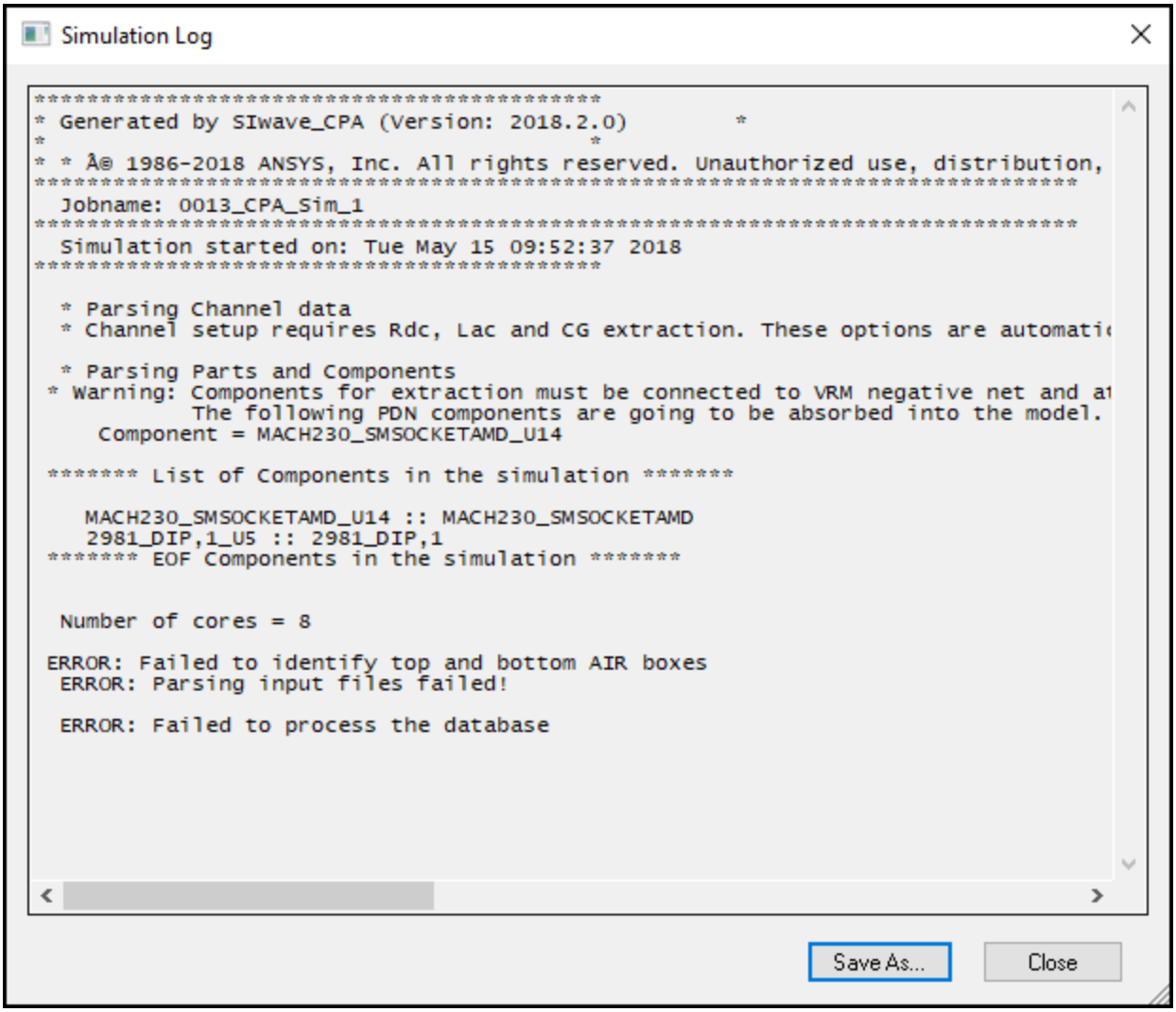

CPA RLGC Results Menu Options

Navigate to the RLGC Results Menu:

1. Click **Results**.
2. From the CPA area, select **RLGC** > **[Simulation Name]**.

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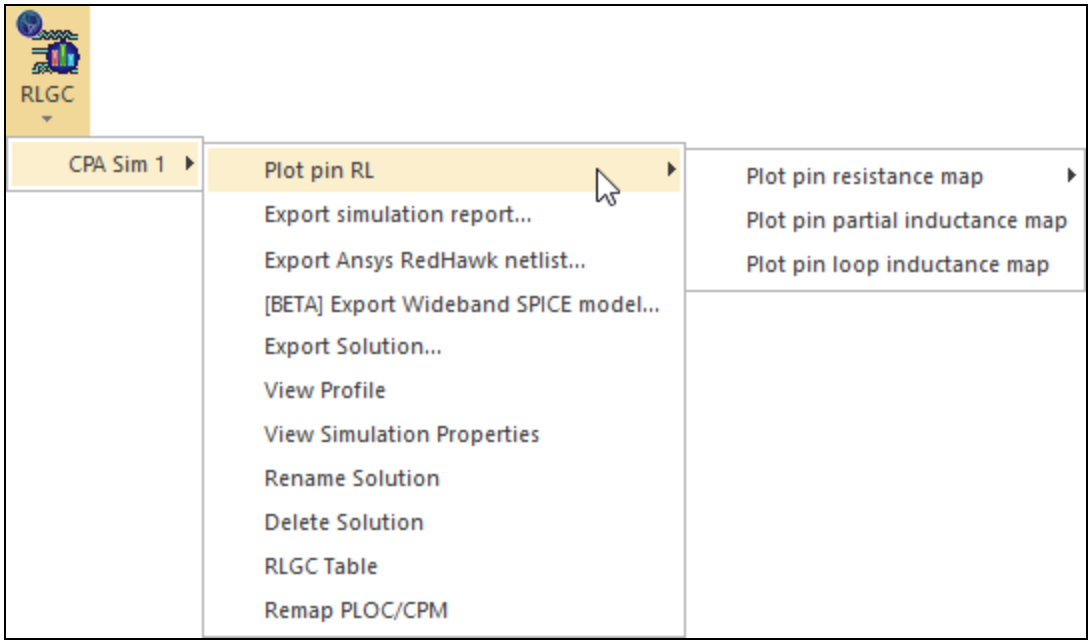

Menu options include:

- **Plot Pin RL** – allows you to plot results. See: Viewing CPA RLGC Simulation Results.
- **Export Simulation Report** – exports the simulation report. See: Exporting CPA RLGC Simulation Results.
- **Export Ansys Redhawk Netlist** – exports a netlist. See: Exporting CPA RLGC Simulation Results.
- **Export Wideband SPICE Model** (BETA) – exports a wideband SPICE model. See: Exporting CPA RLGC Simulation Results.
- **View Profile** – opens the simulation profile.
- **View Simulation Properties** – opens the Simulation Properties window on the Launch CPA tab.
- **Rename Solution** – allows you to rename the solution.
- **Delete Solution** – deletes the solution.
- **RLCG Table** – displays results in tabular format. See: Viewing CPA RLGC Simulation Results.
- **Remap PLOC/CPM** – allows you to import and remap die connections in the model using a new PLOC/CPM file, without having to perform the extraction again. See also: Remapping a Package Netlist.

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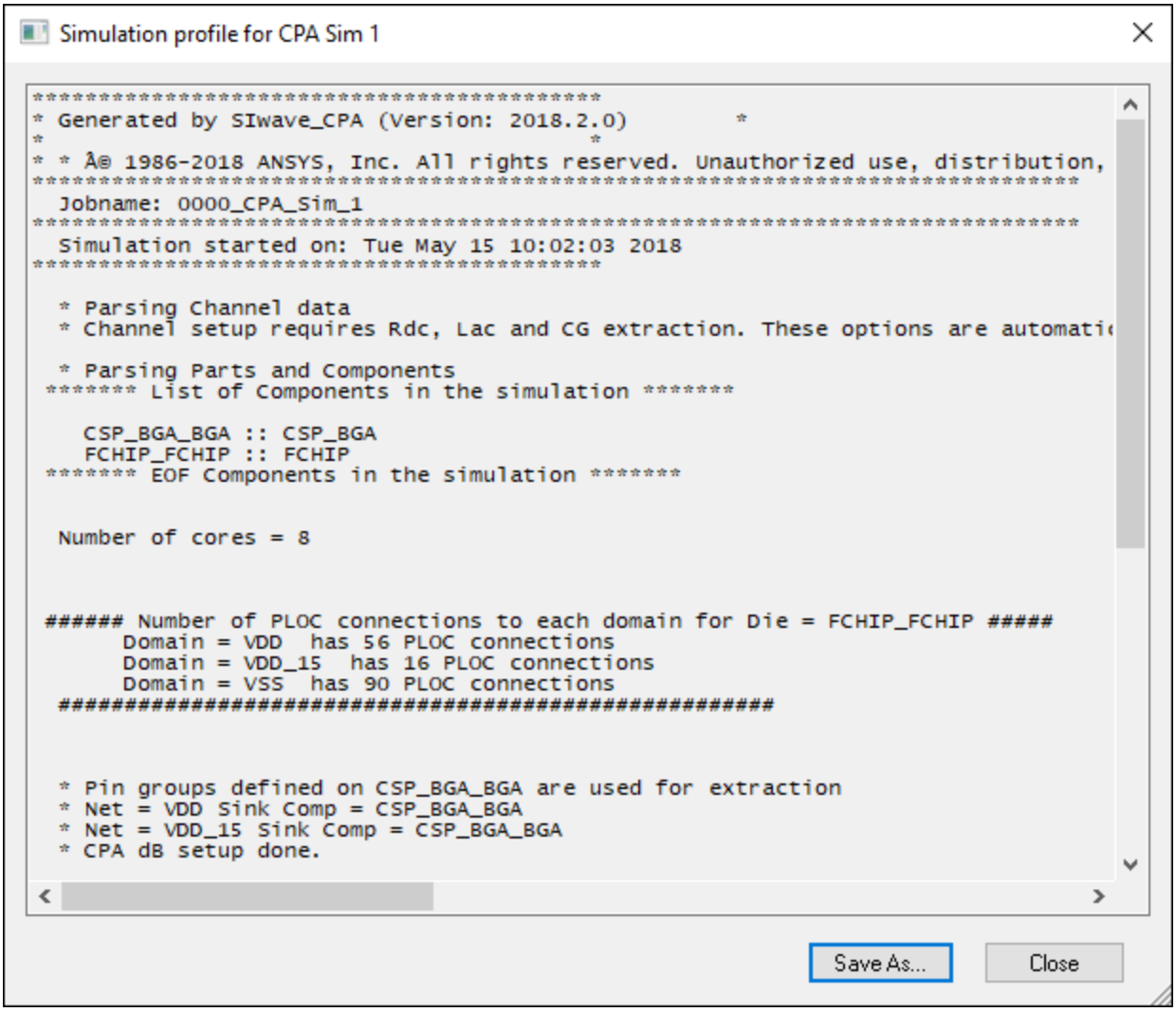
Simulation Profile



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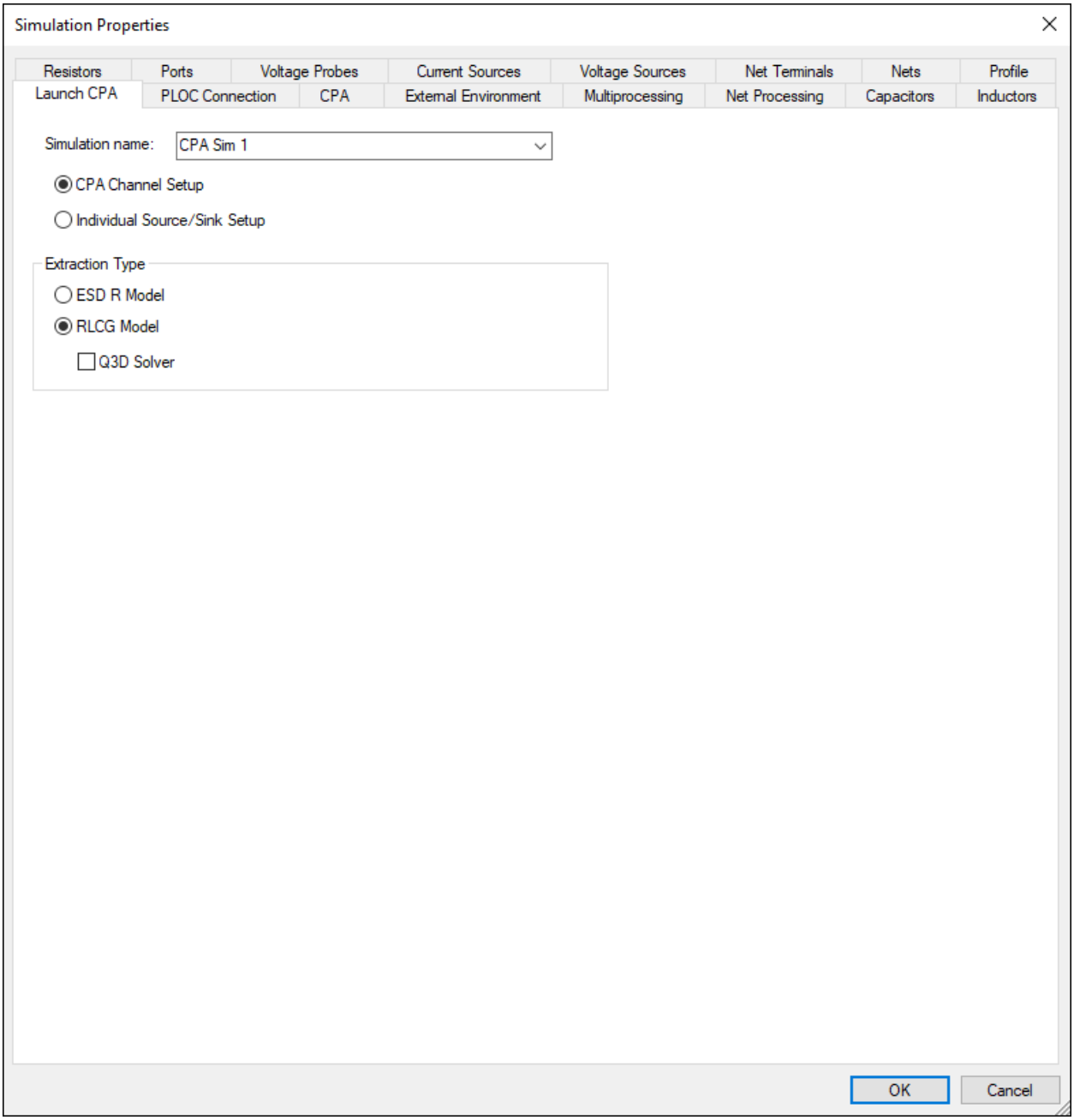
Simulation Properties



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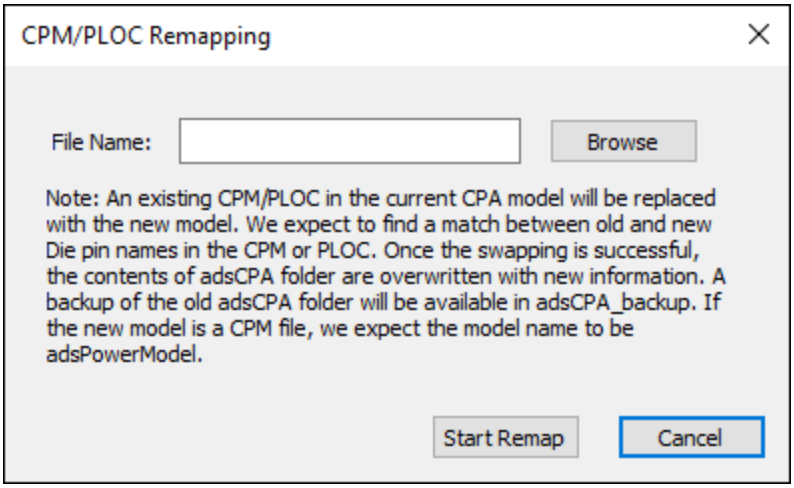
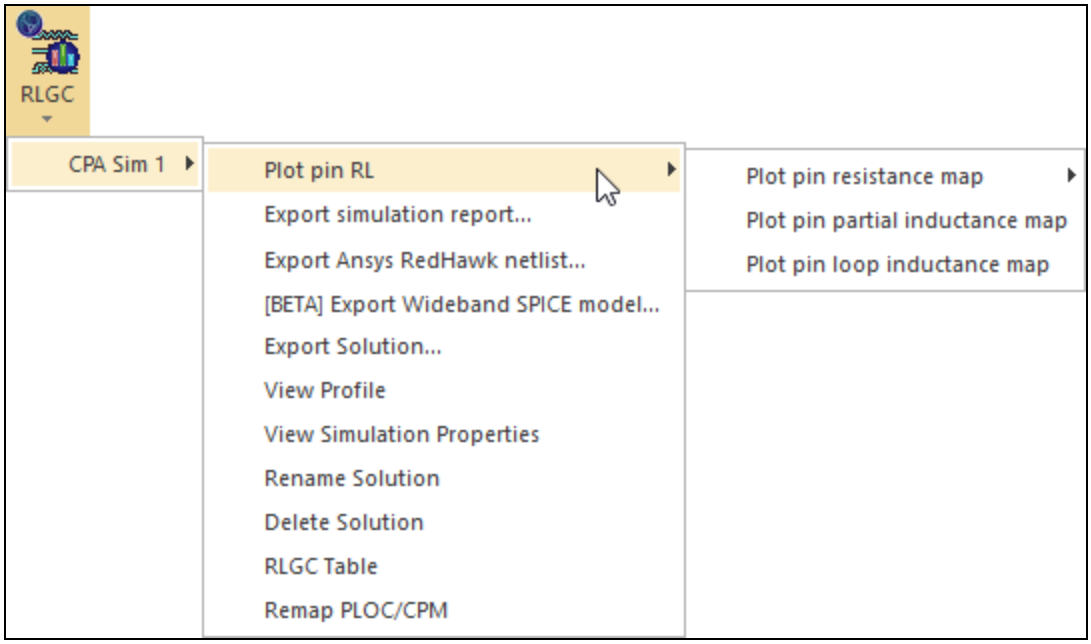
Remap PLOC/CPM



Viewing CPA RLGC Simulation Results

After running an RLGC simulation, you can view and export the results:

1. Click **Results**.
2. From the CPA area, select **RLGC** > **[Simulation Name]**.



Result options include:

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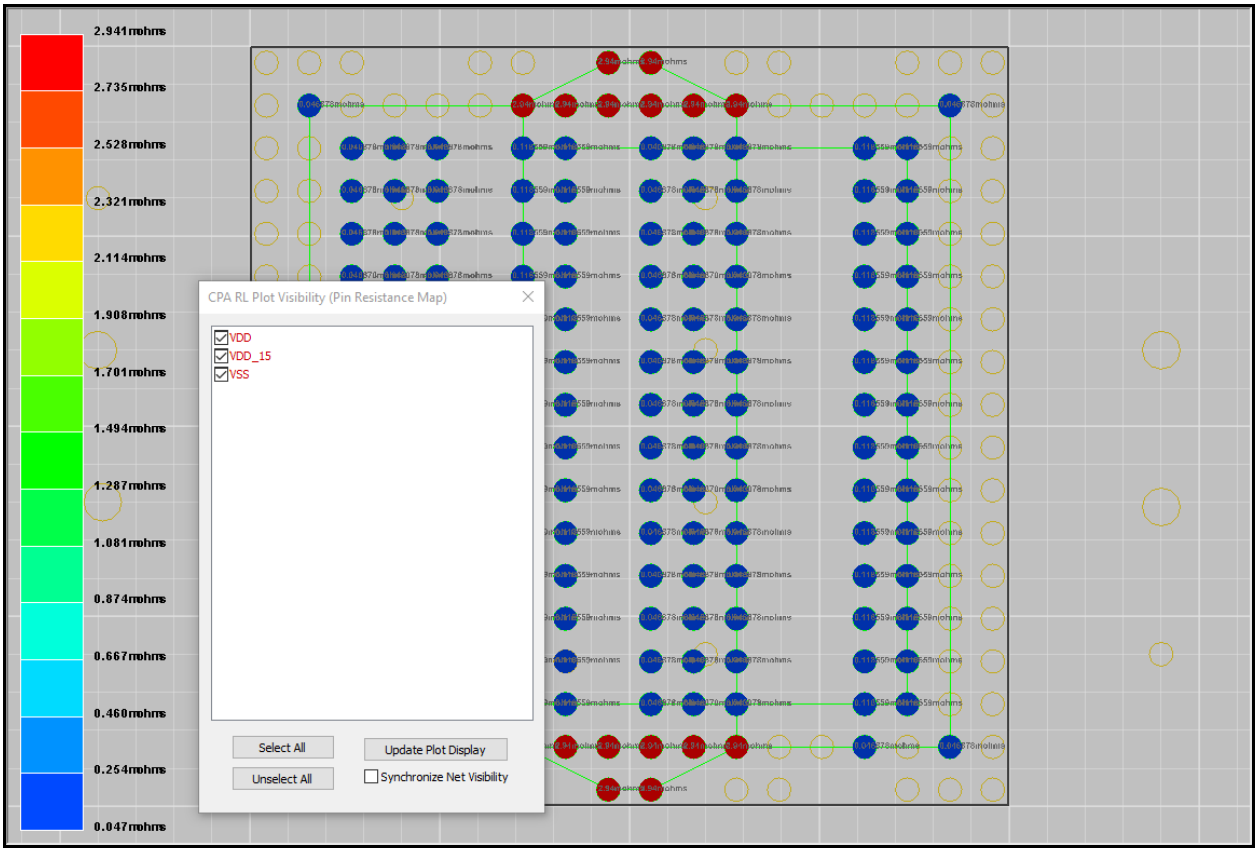
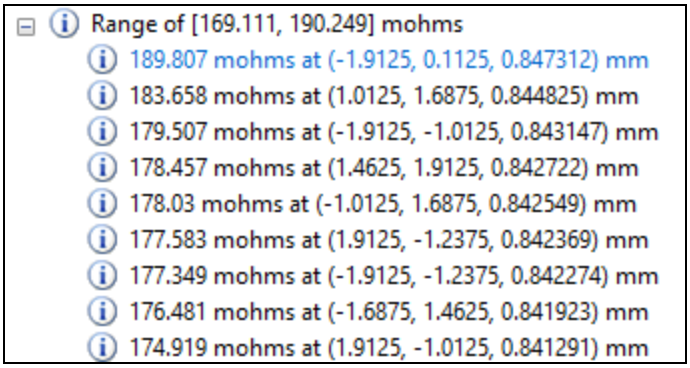
- **Plot Pin RL** – updates the Modeling workspace to display a color map of pin or pin group resistance, partial inductance, or loop inductance.
- **RLCG Table** – opens the RLCG Matrices window, where you can view RLCG values for terminals and nets.

Plot Pin RL:



When viewing the RL plot, right-clicking any color band populates the **Info / Errors / Warnings** pane with a list of nodes in that range:



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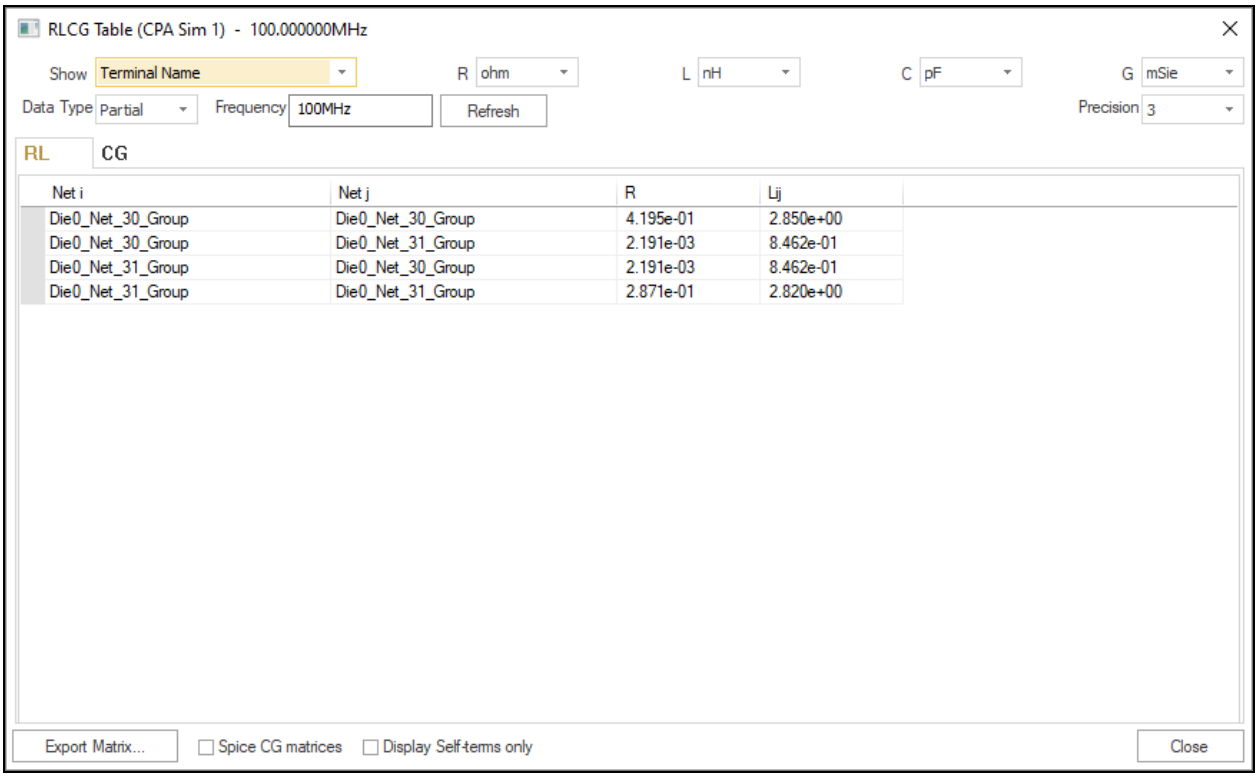
Clicking any node will zoom the Modeling workspace to that node.

RLCG Table:

The RLCG Table contains two tabs, one for RL and one for CG.



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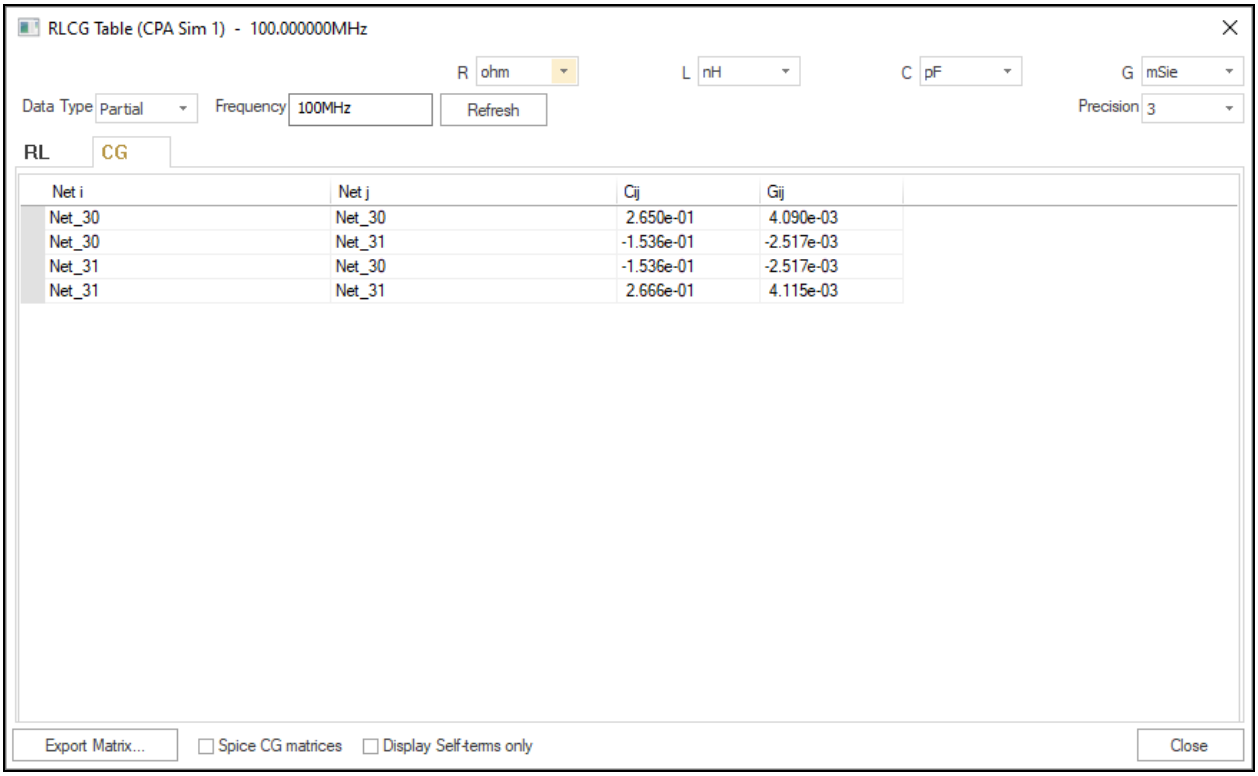
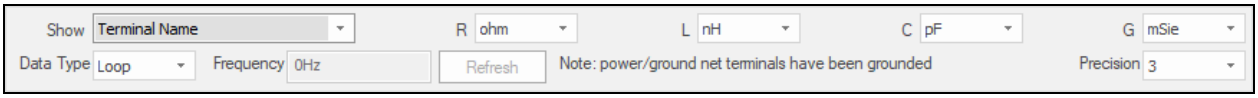


- On the RL tab, you can choose to **Show** by either **Terminal Name** or **Net Name**.
- On the CG tab, entries are always net-based.
- For either tab, use the **R**, **L**, **C**, and **G** drop-down menus to adjust units; the **Precision** drop-down menu to select a precision value; the **Data Type** drop-down menu to select **Partial** or **Loop**; and the **Frequency** field to adjust frequency (you will need to click **Refresh**).

If you selected **Ground P/G nets for SI Extraction** in the CPA Simulation Setup, a reminder note appears at the top of the window:



From the RLGC Results Menu, you can also export the solution or access additional menu options.

Exporting CPA RLGC Simulation Results

Navigate to the RLGC Results Menu:

1. Click **Results**.
2. From the CPA area, select **RLGC** > **[Simulation Name]**.

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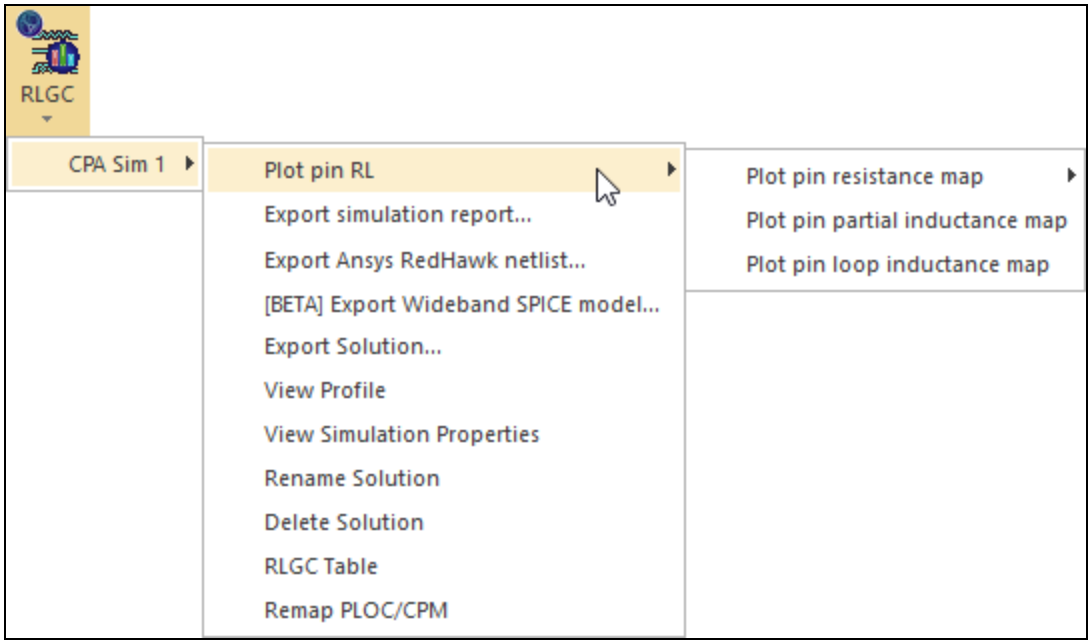

Export options include:

- **Export Simulation Report** – open a settings window where you can configure and export an HTML report of the layout, setup, and results.
- **Export Solution** – opens a settings window where you can configure and export an Ansys Electronics Desktop Circuit file (*.cir).
- **Export Ansys RedHawk Netlist** – saves the CPA model as a compressed file archive (*.zip). Inside is a folder labeled adsCPA, containing the files listed below.

Contents of Extraction folder	Description
cpa_rh_pkg_wrapper_ASCII.sp	Top-level Spice netlist.
cpa_rh_pkg_wrapper.sp	Encrypted wrapper for RedHawk.
mult_whole.lvl	AC RLGC data.
mult_whole_dcres.lvl	DC RL data.
RLGC_Consolidated.txt	Consolidated RLGC data.
cpa_annotated*.ploc	ASCII and encrypted PLOC files for system level connectivity.
0000_CPA_Sim_1.sp	Package RLGC netlist.
0000_CPA_Sim_1_*.sp	Individual Spice models for each of

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Contents of Extraction folder	Description
	the extracted components.
Loop_L.txt	Loop inductance for all the extracted components.
0000_CPA_Sim_1.pkg	Package IBIS model.
Cmatrix.txt; Gmatrix.txt	Maxwell's CG matrices.

- **Export Wideband SPICE Model** (BETA) – saves a wideband model, fitted from DC to 5GHz, based on the extracted DC and AC RLGC data. Ansys recommends using this option only when the number of sources is small (typically around 50 or so), as the model generation time and complexity increase significantly with the number of extracted terminals. Note that the Wideband SPICE model uses controlled sources and is compatible with general Spice simulators such as HSPICE.

From the RLGC Results Menu, you can also view results or view and change simulation properties.

Exporting a Simulation Report

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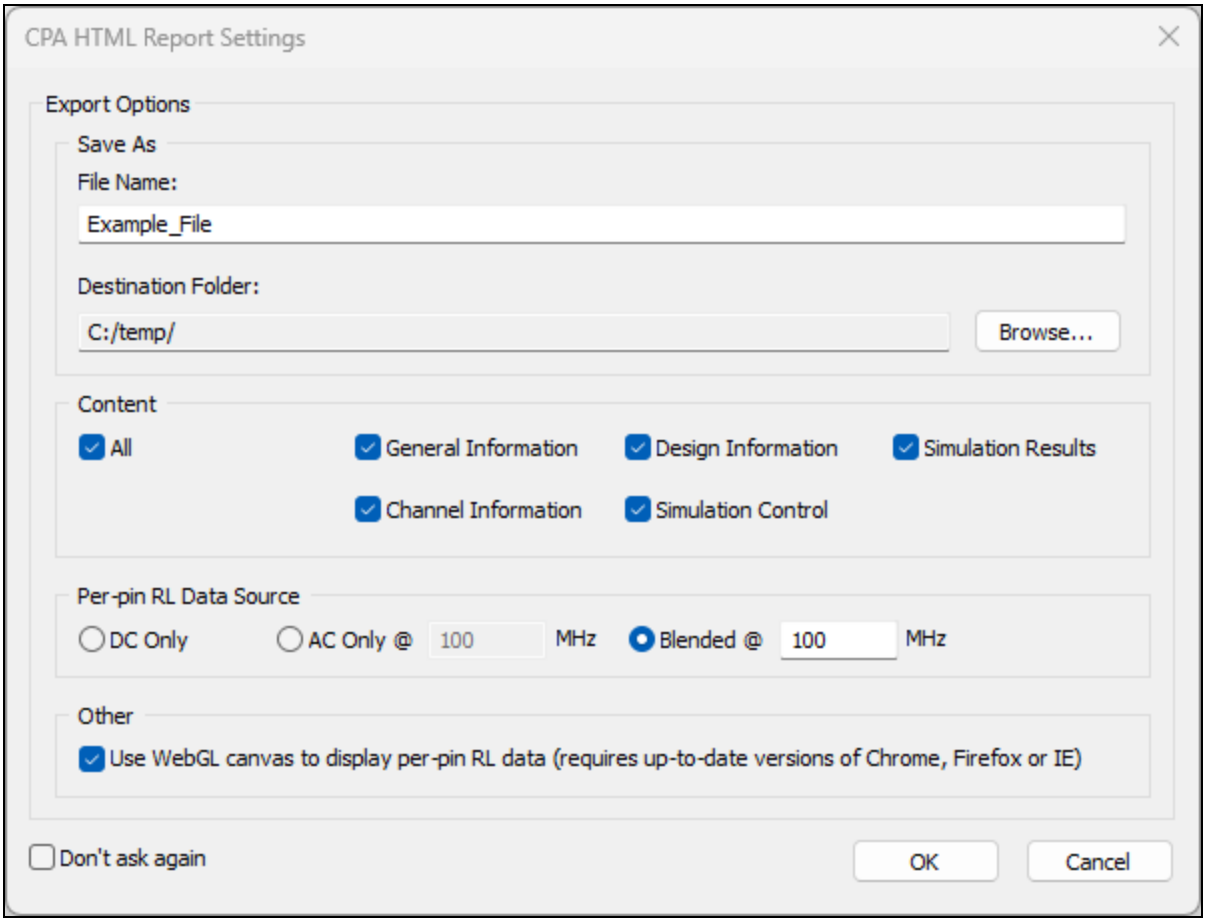

Choose a name for the exported report file, an appropriate directory to save the file, and all/specific contents to include in the report.

From the **Per-pin RL Data Source** area, select the source of the measured resistance/inductance to include in the report:

- DC Only – values are derived from DC only.
- AC Only – values are derived from AC only, at a specified frequency (e.g., 100 MHz).
- Blended – values are derived from both DC/AC, at a specified frquency.

The **Use WebGL canvas to display per-pin RL data** check box exports to a format that embeds a WebGL canvas for interactive visualization of per-pin RL plots, allowing zoom, pan, rotation, tool tips, net filtering and linear/logarithmic scale settings.

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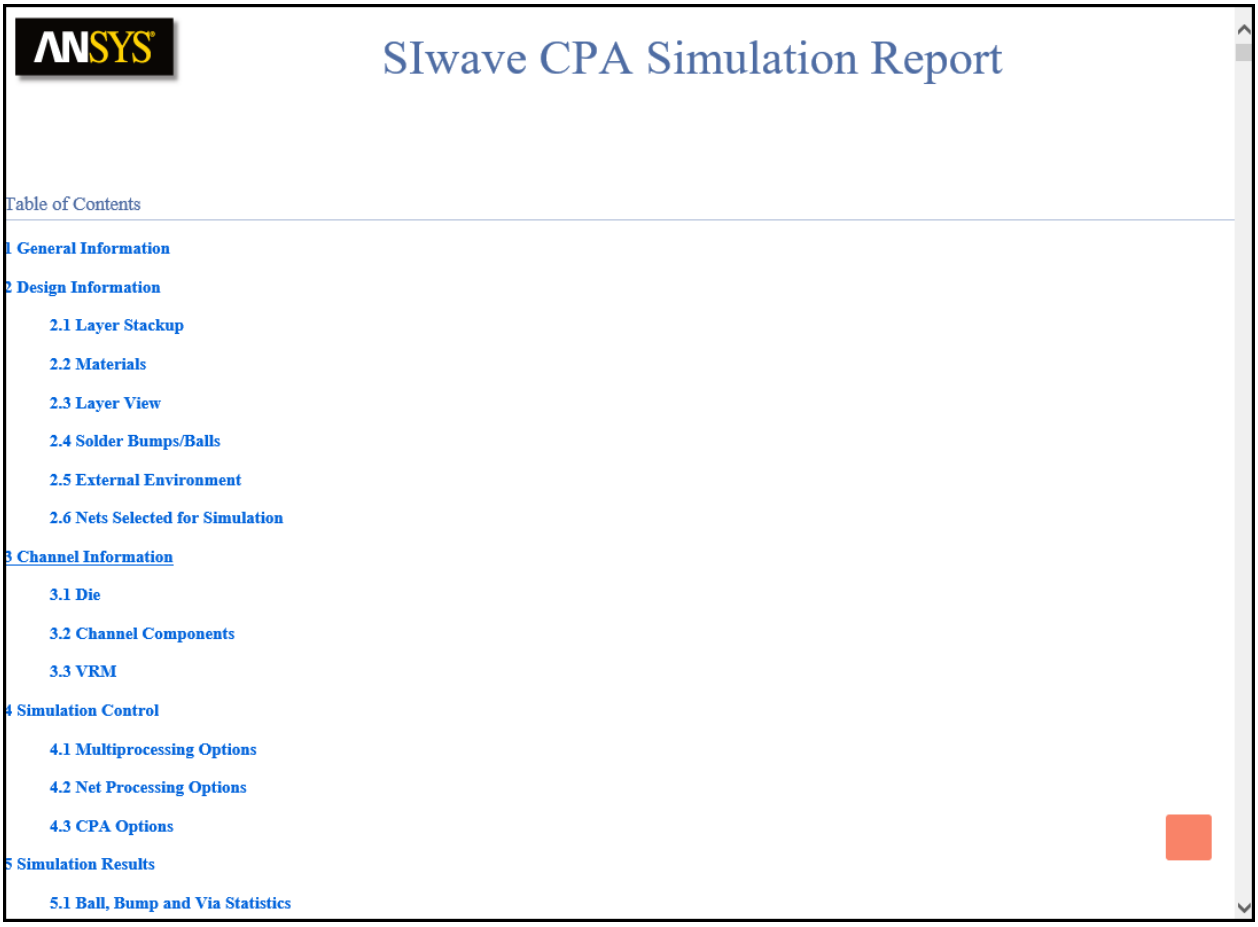

Exporting a Solution (Circuit)

This export window is accessible either via the **Results** menu, or from the Reduce Matrix window.

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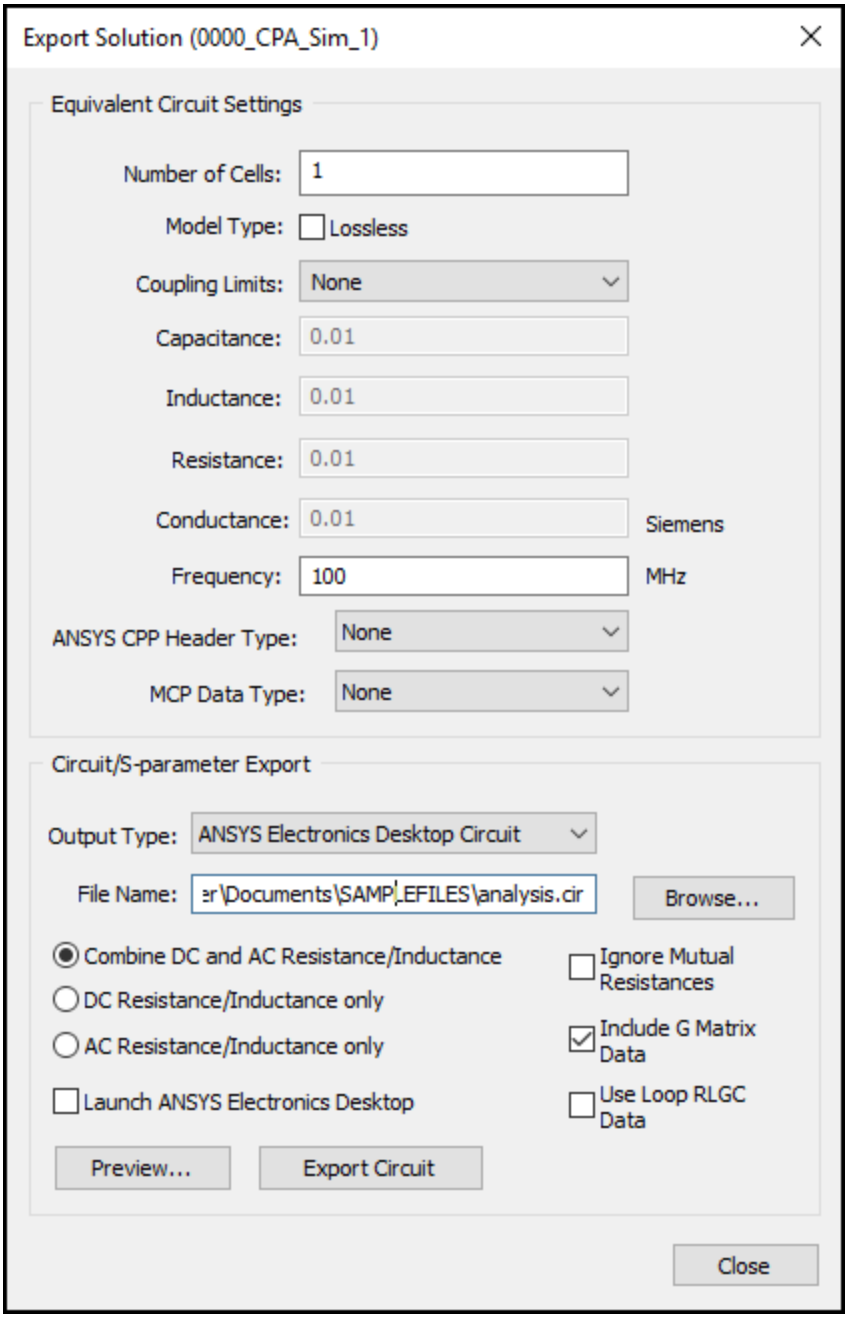

Specify the Equivalent Circuit settings:

- **Number of Cells** – Enter the number of cells (sections) to be used while exporting the circuit. Finer discretization (i.e., a larger number) gives a closer approximation to the underlying partial differential equations. However, this also leads to increased simulation time.
- **Model Type** – Select **Lossless** if a lossless model is appropriate.

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- **Coupling Limits** – Select either **None**, **By Value**, or **By Fraction of Self Term**. When **None** is selected, the options below are unavailable:
  - **Capacitance** – If you selected **By Value**, enter a value in Farads. If you selected **By Fraction of Self Term**, enter a percentage value.
  - **Inductance** – If you selected **By Value** above, enter a value in Henries. If you selected **By Fraction of Self Term**, enter a percentage value.
  - **Resistance** – If you selected **By Value** above, enter a value in Ohms. If you selected **By Fraction of Self Term**, enter a percentage value.
  - **Conductance** – If you selected **By Value** above, enter a value in Siemens. If you selected **By Fraction of Self Term**, enter a percentage value.
- **Frequency** – Enter a frequency in MHz.
- **Ansys CPP Header Type** – Select **None**, **Wirebond Dieup**, **Wirebond Diedown**, **Flipchip Dieup**, or **Flipchip Diedown**.
- **MCP Data Type** – Select **None**, **DIE**, **PKG**, or **PCB**, based on the SIwave model type.

Specify the export settings:

- **Output Type** – Select a circuit model type from the drop-down menu.
- **File Name** – Click **Browse** to specify a file name and path.
- **Resistance/Inductance** – Select *one* of the following matrix types:
  - **Combine DC and AC Resistance/Inductance**
  - **DC Resistance/Inductance Only**
  - **AC Resistance/Inductance Only**
- **Ignore Mutual Resistances** – Select to ignore mutual resistances.
- **Include G Matrix Data** – Select to include G Matrix data.
- **Use Loop RLGC Data** – Select to use Loop RLGC data.
- **Launch Electronics Desktop** – Select this option if you want to launch Ansys Electronics Desktop and open the file upon export.

Click either **Preview** to preview the export, or **Export Circuit** to export it.

Reduce Matrix Operations

SIwave provides a subset of the Reduce Matrix operations available in Electronics Desktop, including the ability to ground nets and set others as the return path. Using these operations, SIwave can generate SPICE netlists modeling the behavior of groups of nets within the package.

To access Reduce Matrix operations:

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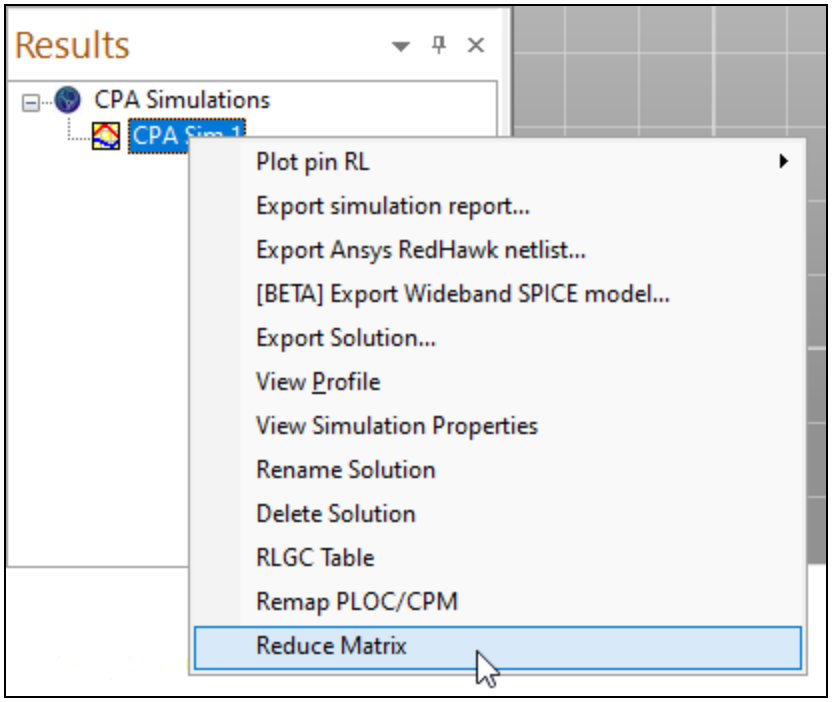
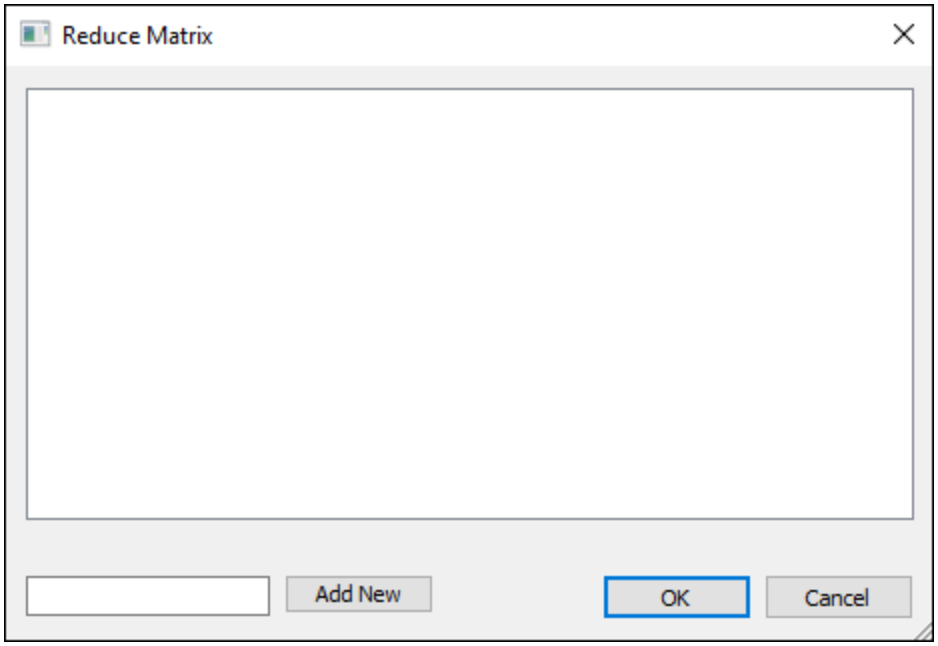
1. Set up and run a CPA RLGC simulation.
2. From the **Results** window, right-click the simulation results and select **Reduce Matrix**.



An empty **Reduce Matrix** window appears.



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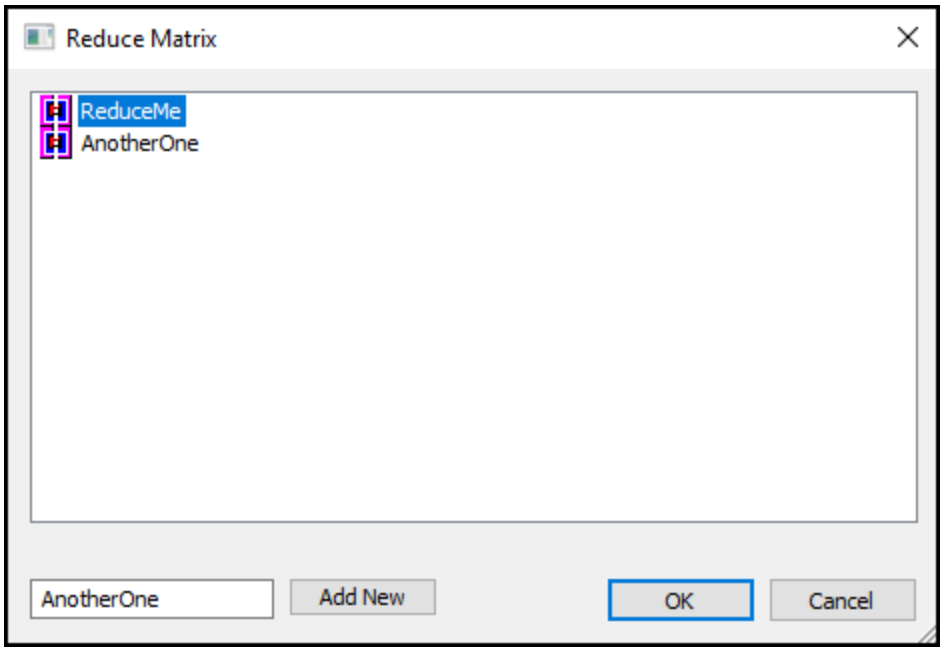
3. From the blank field at the bottom, type a name for the matrix reduction and click **Add New**.

   The new matrix reduction appears in the list. Multiple matrix reductions can be added.



4. Right-click a matrix reduction and select from the menu:
   - **Export Solution** – exports a SPICE netlist that takes into account any Ground Net or Return Path operations applied.
   - **Ground Net** – launches the **Reduce Matrix - Ground Net** window, which allows you to ground nets.
   - **Return Path** – launches the **Reduce Matrix - Return Path** window, which allows you to set nets as the return path.
   - **Delete** – deletes the operation from the list.
5. Specify Ground Net or Return Path settings, as described below.

   Added operations appear beneath the matrix reduction:

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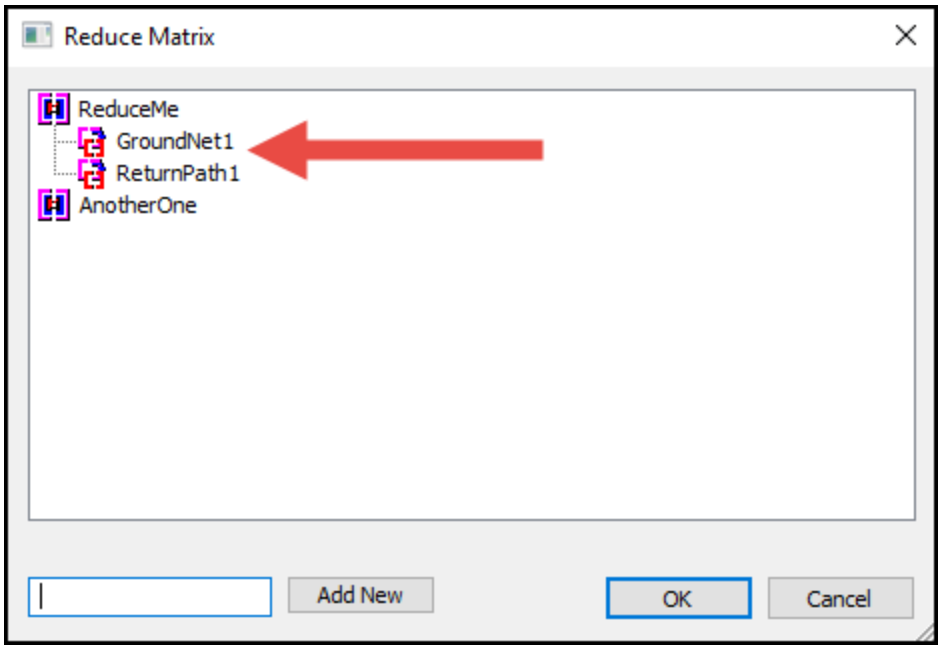

6. Right-click the matrix reduction and select **Export Solution**.
   The **Export Solution** window appears.

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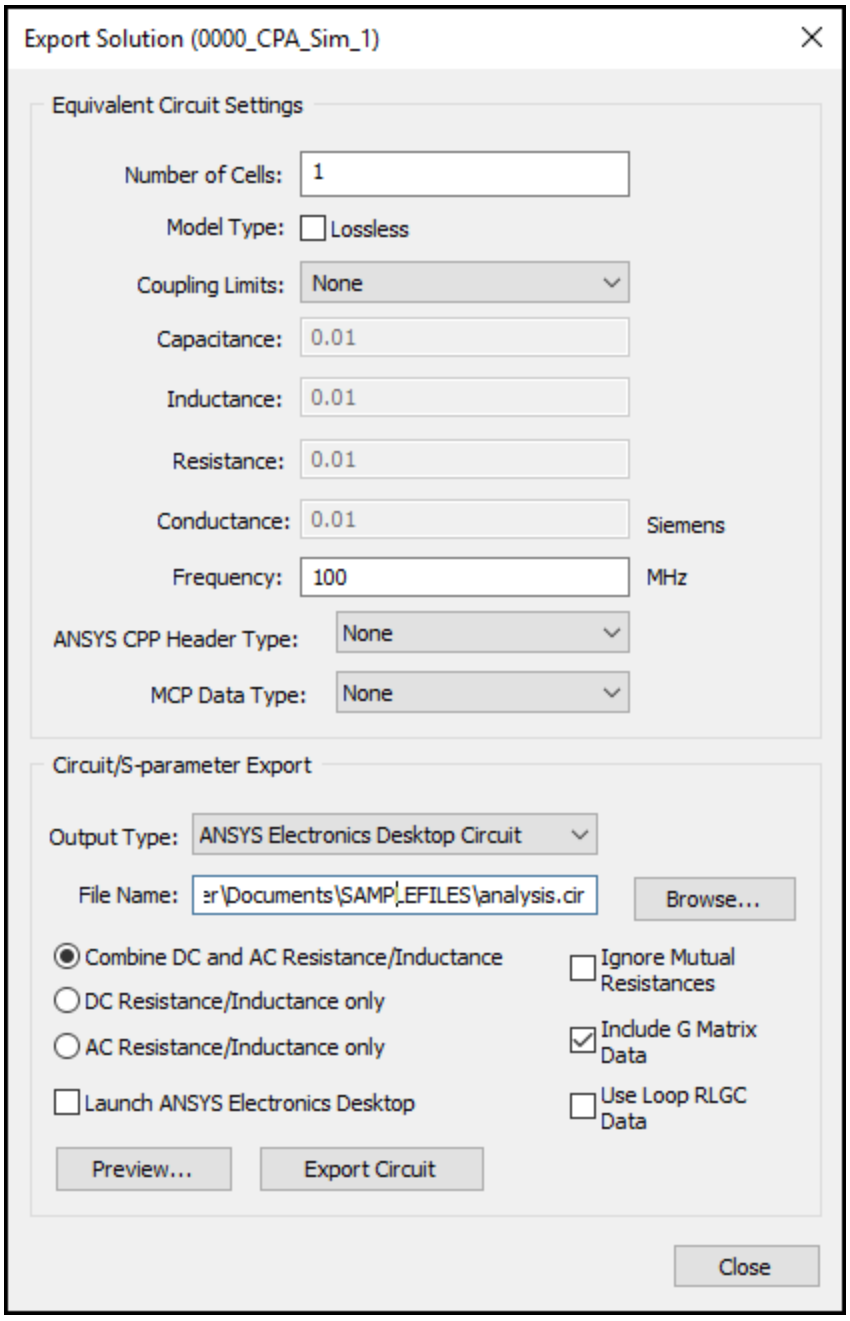

7. Click **Preview** to view the netlist. If the preview appears to be correct, click **Export Circuit**. See: Exporting CPA RLGC Simulation Results.
8. Click **OK** to close the window.

Specifying Ground Net

Launch the **Reduce Matrix - Ground Net** window.

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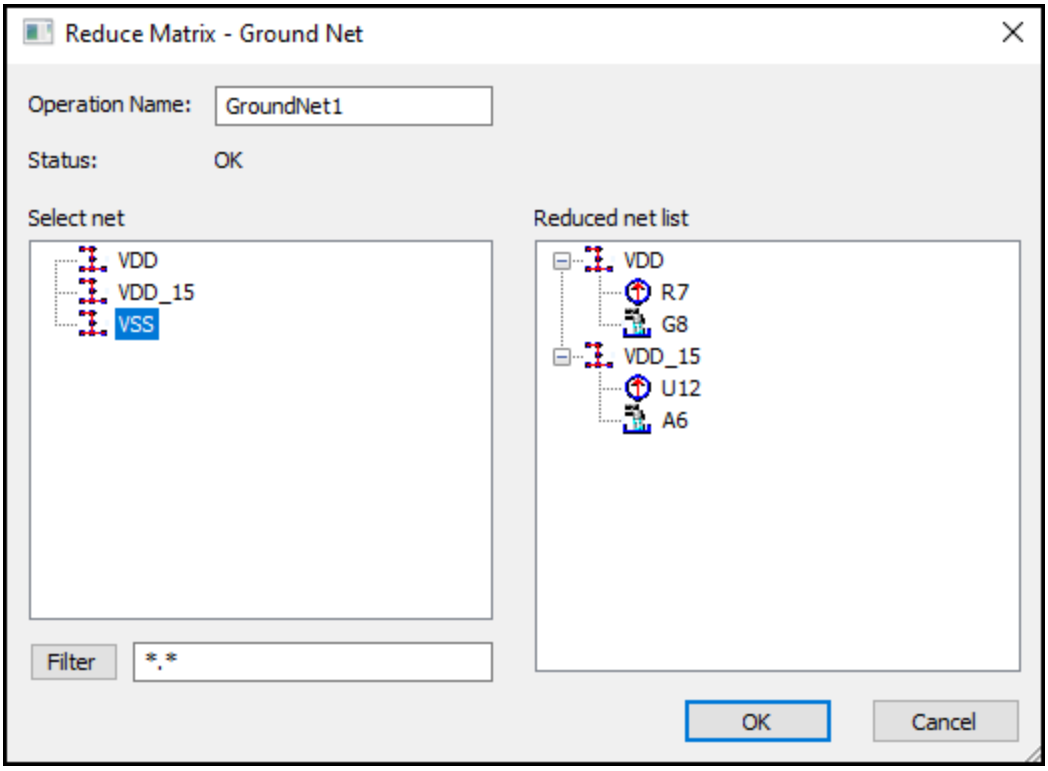

From the **Select Net** list, click a net to ground it. The net disappears from the **Reduced Net List** on the right.

If appropriate, you can filter the **Select Net** list by entering a regular expression in the blank field and clicking **Filter**.

*	Matches any sequence of characters. For example, **net*** selects objects **net_1a**, **net_1b**, **netLength**.
?	Matches any character. For example, **net_?** selects objects **net_1**, **net_2**, **net_a**, **net_b**.

To restore the full list, type an asterisk (*) and click **Filter**.

Click **OK** to close the window.

Specifying Return Path

Launch the **Reduce Matrix - Return Path** window.

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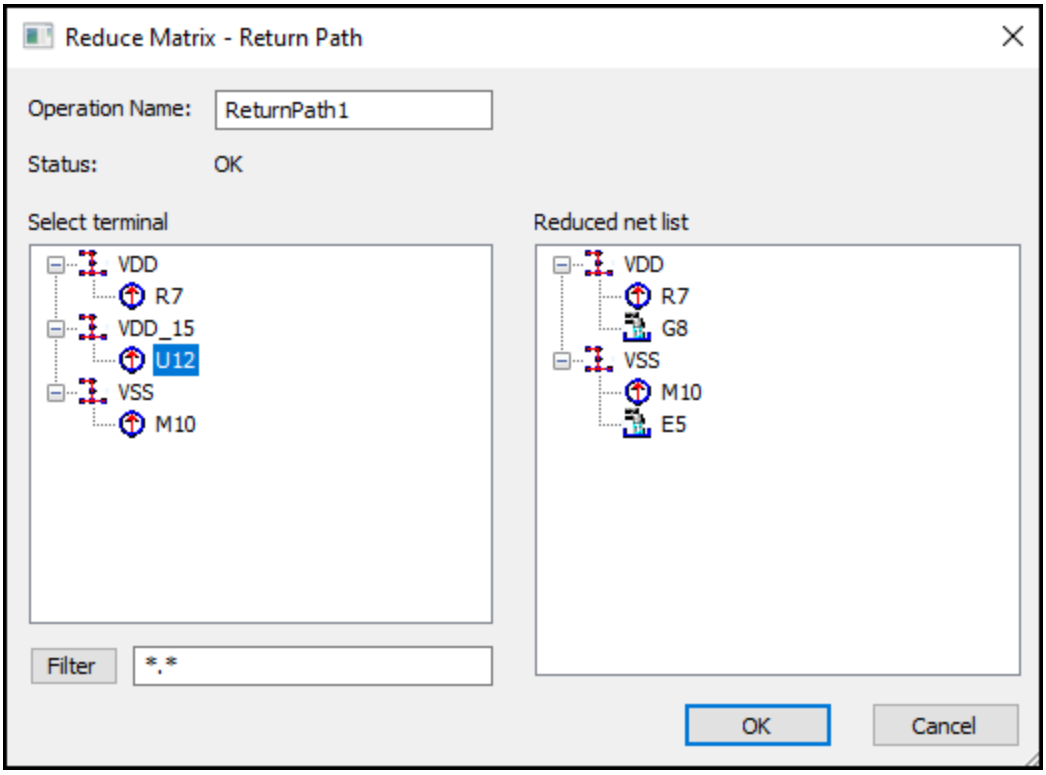

From the **Select Terminal** list, click a net to specify the return path. The net disappears from the **Reduced Net List** on the right.

If appropriate, you can filter the **Select Net** list by entering a regular expression in the blank field and clicking **Filter**.

*	Matches any sequence of characters. For example, **net*** selects objects **net_1a**, **net_1b**, **netLength**.
?	Matches any character. For example, **net_?** selects objects **net_1**, **net_2**, **net_a**, **net_b**.

To restore the full list, type an asterisk (*) and click **Filter**.

Click **OK** to close the window.

SUtility

SUtility provides visualization, analysis, and manipulation tools for manipulating S-parameter data. It is a post-processing application that enables you to analyze the scattering, impedance,

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and admittance parameters. You can graph and compare the parameters from multiple analyses.

SUtility also provides a set of S,Y,Z-parameter processing tools such as shorting, opening, and lumping ports, adjacent structure coupling, and converting ports from single to differential.

With increasingly large and complex designs, SUtility provides an efficient and alternate way of generate results for small manipulations to certain ports (e.g., after performing an analysis for a 10-port net, you may want to see the effects if you short a certain port). Instead of running through the analysis process again with the small change, you can use the **Port Tools** utility to quickly calculate the new effects.

SUtility provides convenient graphing tools to help you analyze different parameters and compare results. With basic functions such as x and y-axis scaling, log graphing units, color differentiation, and easy access parameter plotting, SUtility makes post-processing easy and powerful.

Launching SUtility

You can launch **Sutility** in one of two ways:

- Click **Tools**. From the **S-Parameter Tools** area, click **SUtility**.
- Run an SYZ or PSI simulation. From the Results workspace, right-click the solution name and select **Export to SUtility**.

  The **S-Parameter Utility** window appears. If you launched from the Results workspace, the solution data is automatically loaded.

Interface Overview

The SUtility window is divided into the following panes:

1. **Options Pane** – allows you to configure SUtility and access various utilities.
2. **Control Pane** – allows you to select one or more projects and apply changes to the graph.
3. **Plot Pane** – displays the plotted information.
4. **X-Axis Pane** – allows you to alter the scale of the graph and its x-axis.
5. **Parameters Pane** – allows you to choose between different parameter types and set their options. You can also export Touchstone information from this pane.

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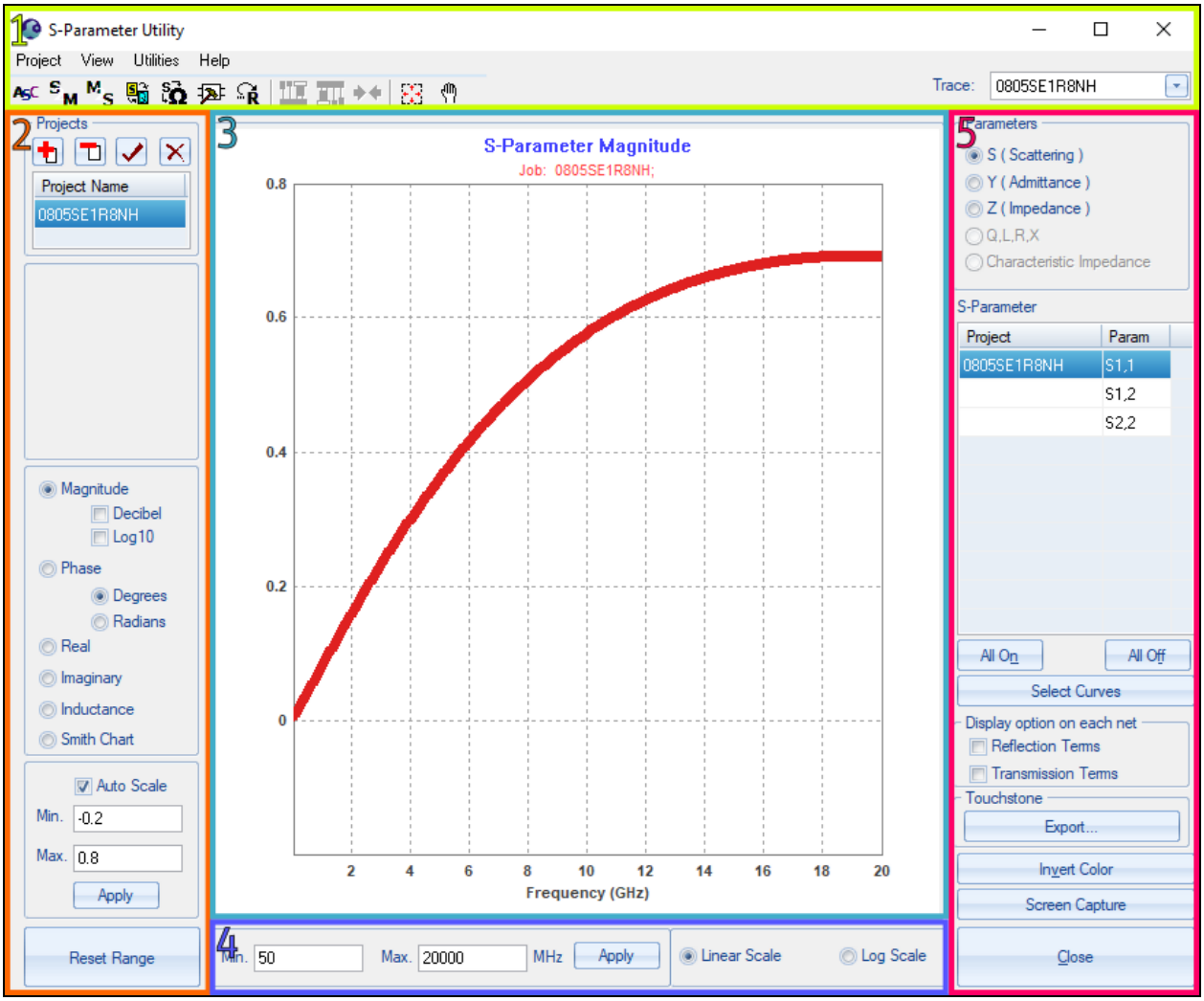

Options Pane

The Options Pane provides four menus to access SUtility functions:

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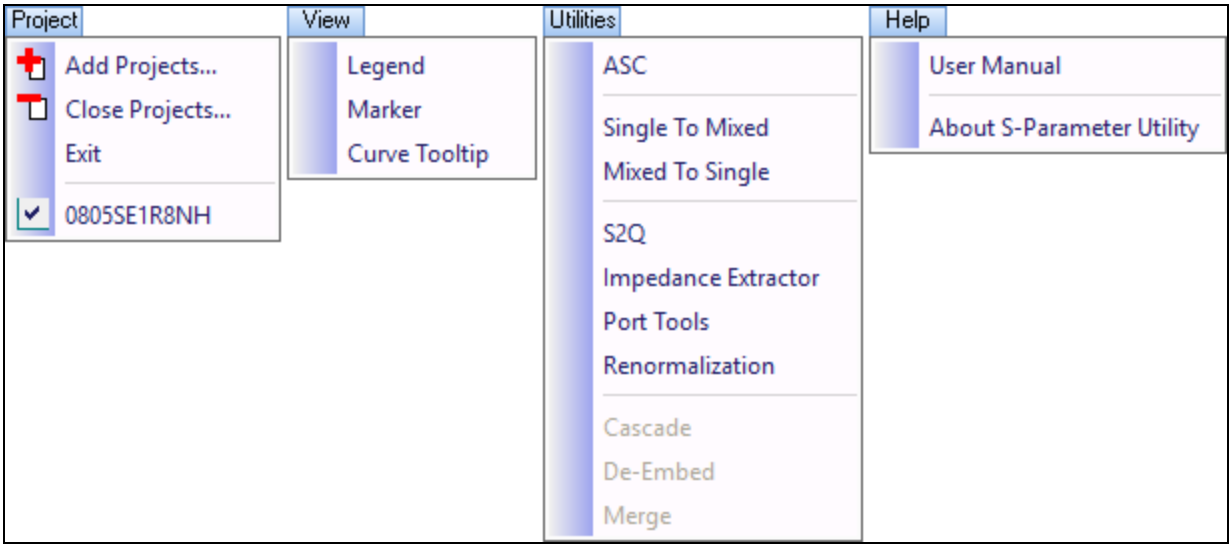

Use the Project Menu to add and close projects, or to exit SUtility.

Use the View menu to toggle the chart legend, add markers, and toggle the tooltip displayed when the cursor hovers over the curve.

Use the Utilities menu to access SUtility utilities. Utilities and parameters are also accessible via the toolbar:

These include:

- Adjacent Structure Coupling (ASC)
- Single to Mixed (S2M)
- Mixed to Single (M2S)
- S-Parameter to QRLX Conversion (S2Q)
- Impedance Extractor
- Port Tools
- Renormalization
- Cascade (only available when you've selected multiple projects with the same number of ports)
- De-Embed (only available when you've selected multiple projects with the same number of ports)
- Merge (only available when you've selected multiple projects with the same number of ports)

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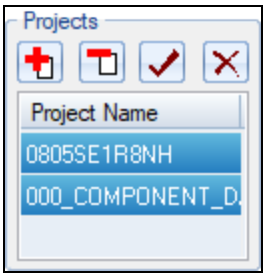
Use the Help menu to open the SUtility User Manual or to learn more about the software version.

Control Pane

The Control Pane consists of several areas:

Under **Projects**, you can select one or more Touchstone files.

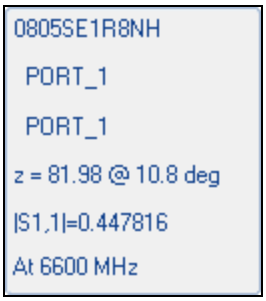


Click the icons to **Add**, **Close**, **Select All** or **Deselect All** projects.

- Select a project from the list to load its parameters.
- Hold down the Ctrl key as you drag the mouse to select multiple projects .
- Right-click a project for options to **View File** (in a text editor) or **Export**.

Depending on the type of Touchstone file input (Z , Y, or S-parameter), the other two parameter types are calculated (e.g., if you input a S-parameter file, SUtility will automatically calculate the corresponding admittance (Y) and impedance (Z) parameters). By default, the S11 parameter for the input file are also plotted.

As you move the cursor across the Plot Pane, the Projects area updates to display additional information about the file name, reference impedance, and frequencies.



The next area of the Control Pane allows you to select from y-axis values.

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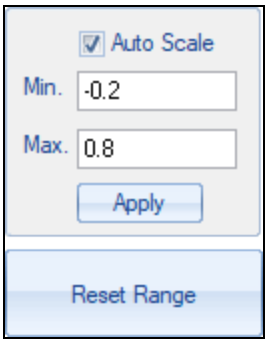
If you select **Phase**, you must also select the phase units (degrees or radians). The **Smith Chart** option is available only for S (Scattering) parameters.

At the bottom of the Control Pane, you can change the y-axis scale.



Click **Reset Range** to return the y-axis scale to its default settings.

Plot Pane

The Plot Pane displays the graph. It automatically updates as new settings are applied.

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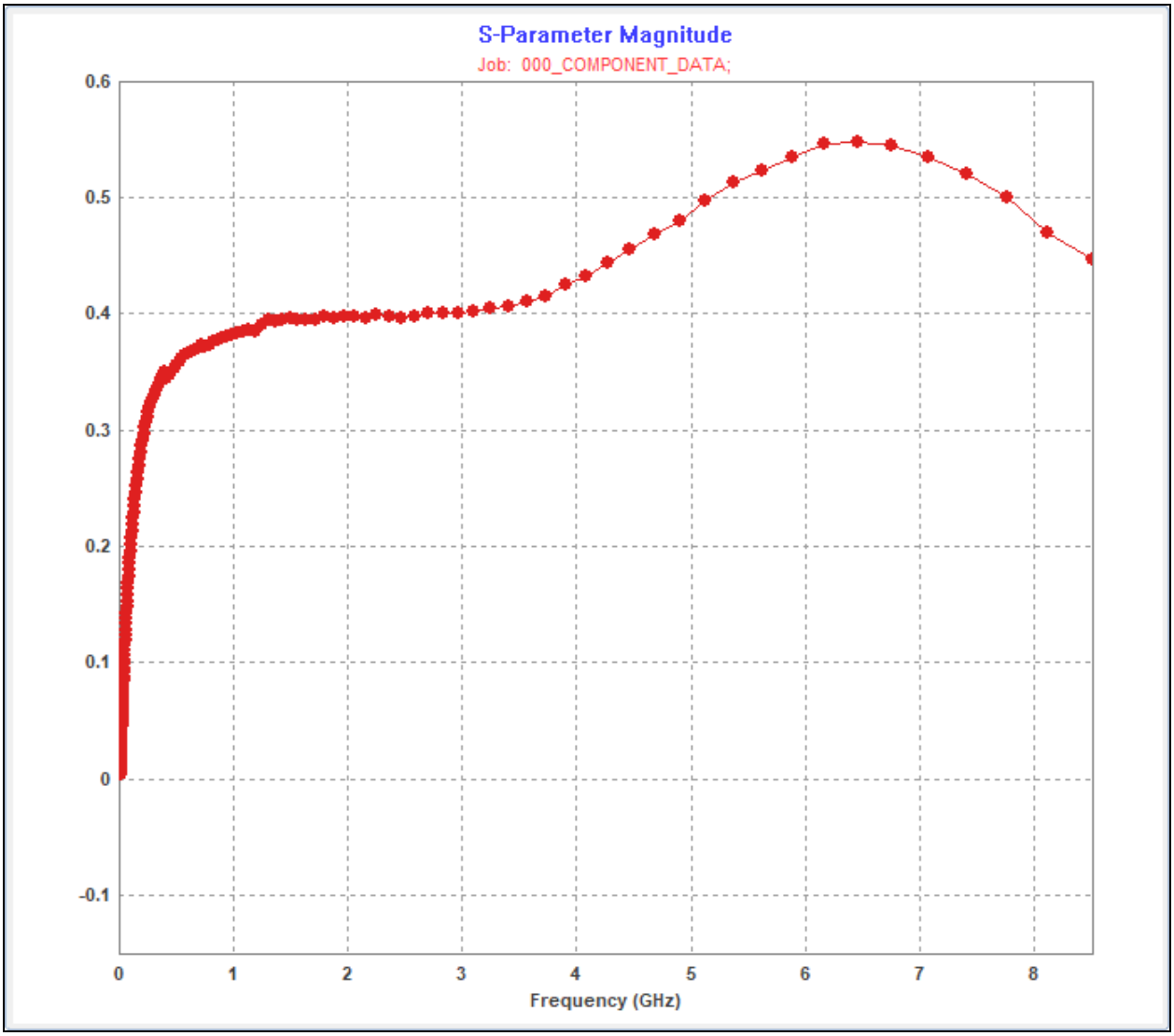

X-Axis Pane

The X-Axis pane allows you to set a range for the x-axis scale.

Additionally, you can choose between linear and log scales.

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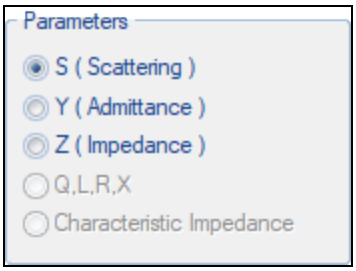
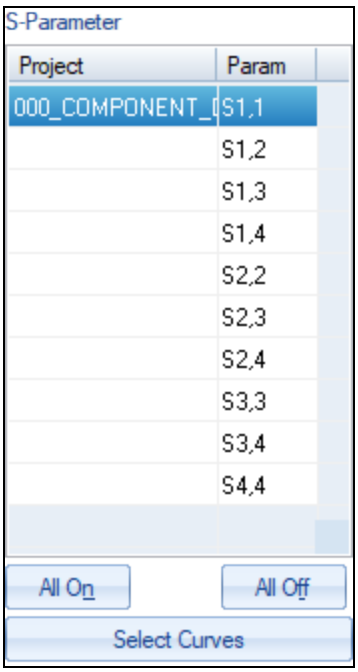
Parameters Pane

The **Parameters** area allows you to determine which parameters to plot. S, Y, or Z files are generated based on the type of input file. Scattering, admittance, and impedance parameters are also generated. If the input matrix is singular, the other radio buttons are disabled.



Click any parameter to load it into the parameter list.



- Plot a parameter by clicking it.
- Plot multiple parameters using **Ctrl+click**.
- Use the **All On** and **All Off** buttons to display or hide all the parameters in the parameters list.

The Touchstone area allows you to export your information for viewing in either Notepad or Excel.

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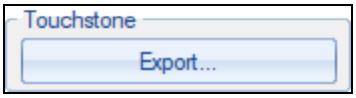
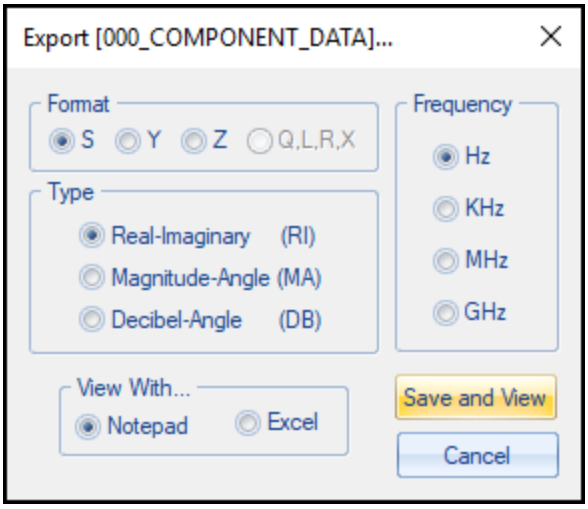


Click **Export** to open the **Export Options** window.



Choose the **Format**, **Type**, and **Frequency**. Note that Type options are unavailable for Q,L,R,X format.

At the bottom of the Parameters Pane, you can invert the color of the graph or copy a screen capture to the clipboard.

Using the ASC Utility

The Adjacent Structure Coupling (ASC) utility allows you to combine S-parameter solutions into a composite S-parameter solution. You can extract adjacent structure models for applications such as simultaneous switching noise and ground bounce analysis. This utility provides an easy way to create an adjacent structure S-parameter model with accurate power/ground plane resonance and accurate coupling between signal nets and the power/ground nets.

To open the ASC Utility from within SUtility:

1. Click **Utilities** > **ASC**.

   The **ASC Utility** window appears. You can open multiple files at a time. However, the displayed data always corresponds to the dataset indicated in the **Projects** pane.

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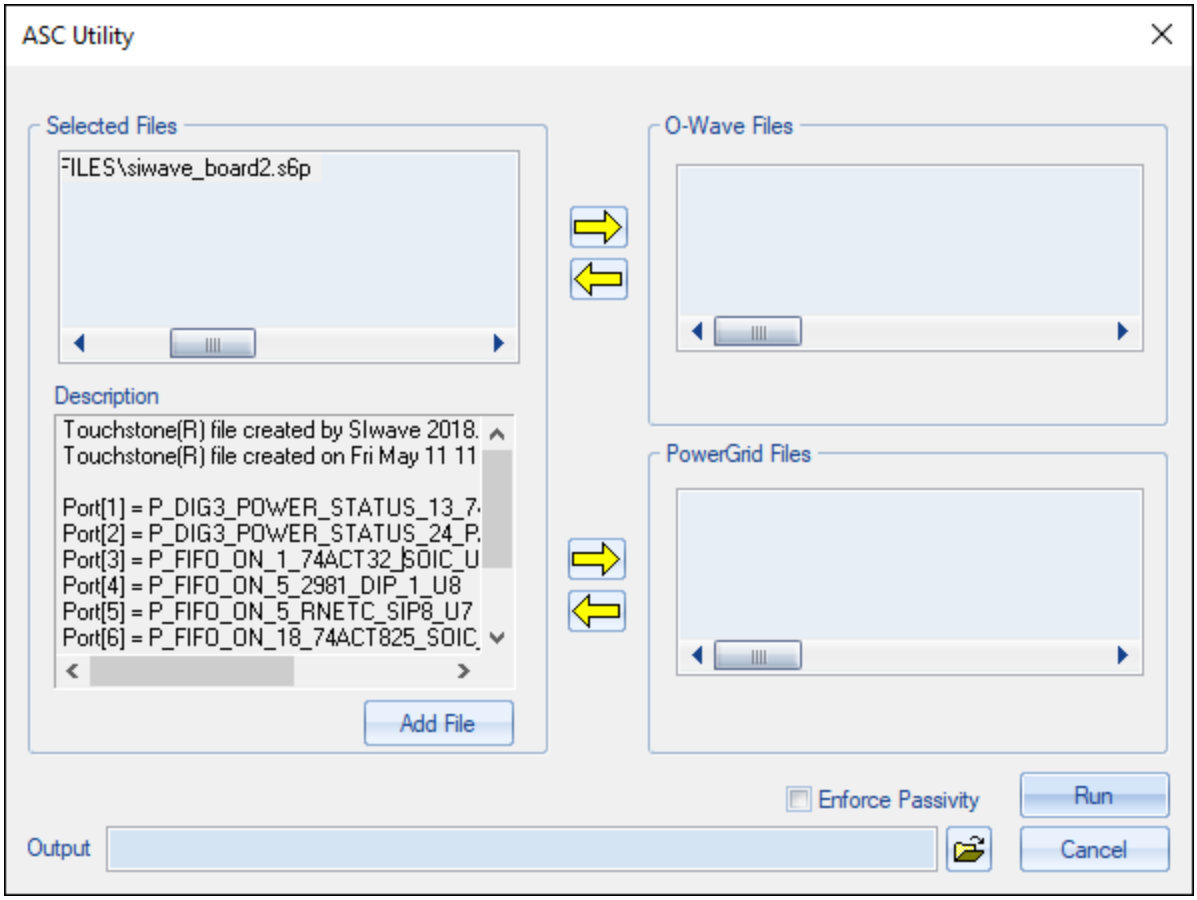

2. From the **Selected Files** area, click **Add File** to select one or more files. When a file is selected, the **Description** field updates to display its Touchstone header items.
3. Use the arrows to designate/un-designate files as O-Wave or PowerGrid.
4. Browse to select an **Output** file name and destination.
5. If appropriate, check **Enforce Passivity**.
6. Click **Run** to begin the analysis.

   The ASC output file is loaded and plotted in the main SUtility window.

Using the S2M Utility

The Single to Mixed (S2M) module converts single-ended parameters into mixed-mode parameters. Multi-port single-ended ports are then paired to generate differential positive or negative ports. These ports can then be excited in common mode or differentially.

To access the S2M Utility from SUtility:

1. Select one single-ended project from the projects list. Ensure that the number of ports is a multiple of four.

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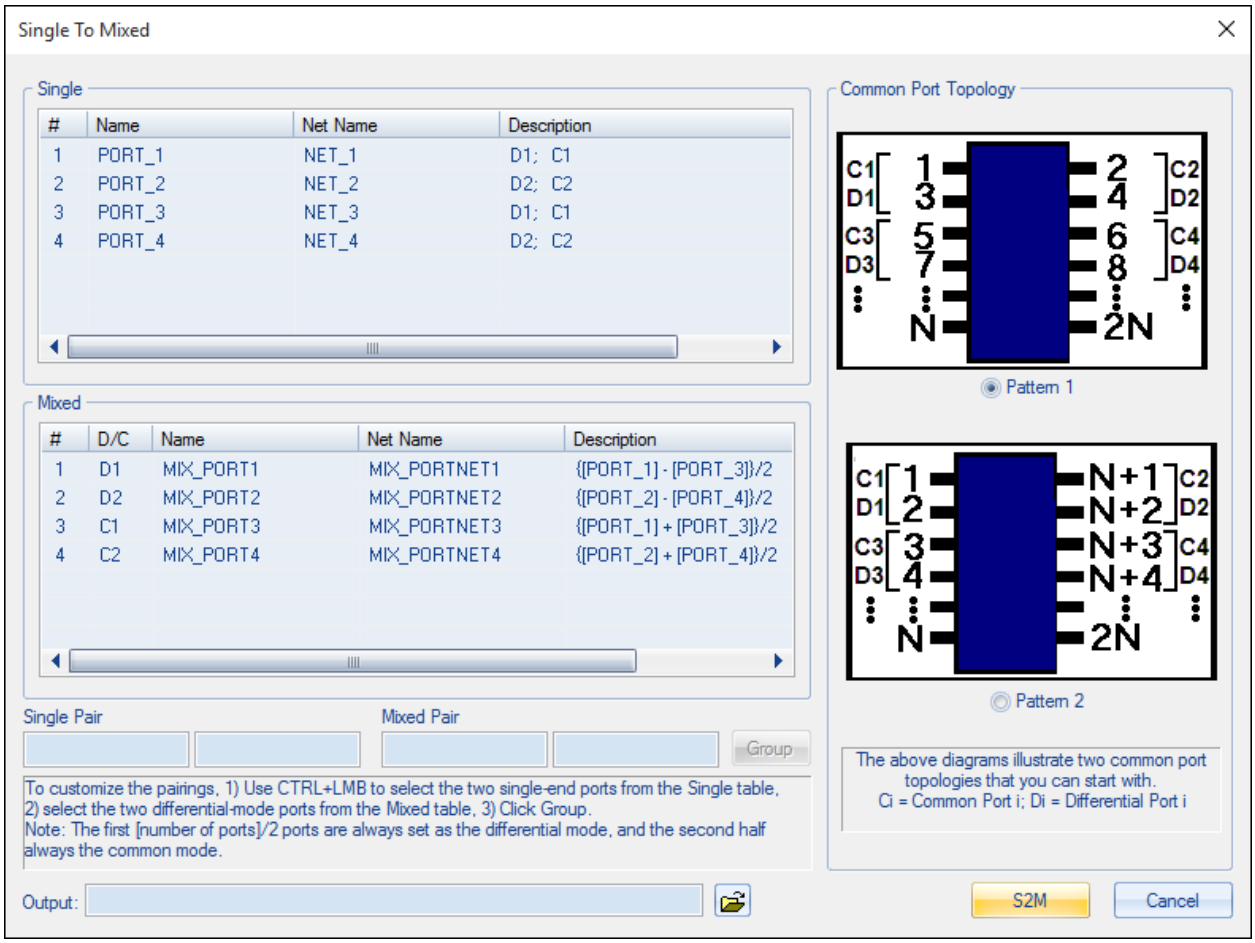
2. Click **Utilities** > **Single To Mixed**.

   The **Single To Mixed** window appears.



   The **Single** table shows single-ended ports, and the **Description** column shows the differential and common modes to which it belongs.

   The **Mixed** table shows mixed-mode ports that will be generated. The **D/C** column indicates whether the mixed-mode port is the differential-mode or common-mode excitation of the paired single-ended S-Parameters. Port and net names are editable by double clicking on the cell. The **Description** column shows how the differential and common-mode voltages are being defined.

   From the mixed-mode output port sequence, the first ([number of ports]/2) ports are always defined as the differential-mode voltages and currents; the next half are always defined as the common-mode values.

To specify port pairings and begin analysis:

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1. Use the radio buttons to select a **Common Port Topology**:
   - **Pattern 1** pairs single-ended port 1 and 3 together and generate the common and differential-modes 1. Similarly, single-ended port 2 and 4 are paired to generate the common and differential modes 2, and so on.
   - **Pattern 2** topology indicates that the single-ended port 1 and port 2 will be paired together to generate the common and differential modes 1. Single ended ports 3 and 4 will be paired to make common and differential modes 3, and so on. The mixed mode port sequence is always arranged in the alternating fashion, regardless of the single-ended port pairings.
2. Alternatively, you can customize the pairing using the **Mixed** table. To set up a pairing, select two single-ended ports (from the **Single** table) that you want to pair and the mixed differential and common mode ports (from the **Mixed** table) that you want associated with the selected single-ended ports. Click **Group** to apply the pairing. The **Description** fields for both the **Single** and **Mixed** table should be updated for the selected items to reflect the new grouping. Mixed-mode ports are always arranged such that the first ([number of ports]/2) ports are the differential ports, and the second half are the corresponding common-mode ports. When you click on any mixed-mode ports, the other mode is automatically selected as well.
3. Enter the **Output** file name to specify the output file containing the results.
4. Click **S2M** to start the analysis.

   The results are loaded and plotted in the main SUtility window.

Using the M2S Utility

The Mixed to Single (M2S) utility converts mixed-mode ports to single-ended ports.

To access the M2S Utility from SUtility:

1. Select the mixed-mode S-parameter file to be converted. Please ensure that the number of ports is a multiple of four.
2. Click **Utilities** > **Mixed To Single**.

   The **Mixed To Single** window appears.

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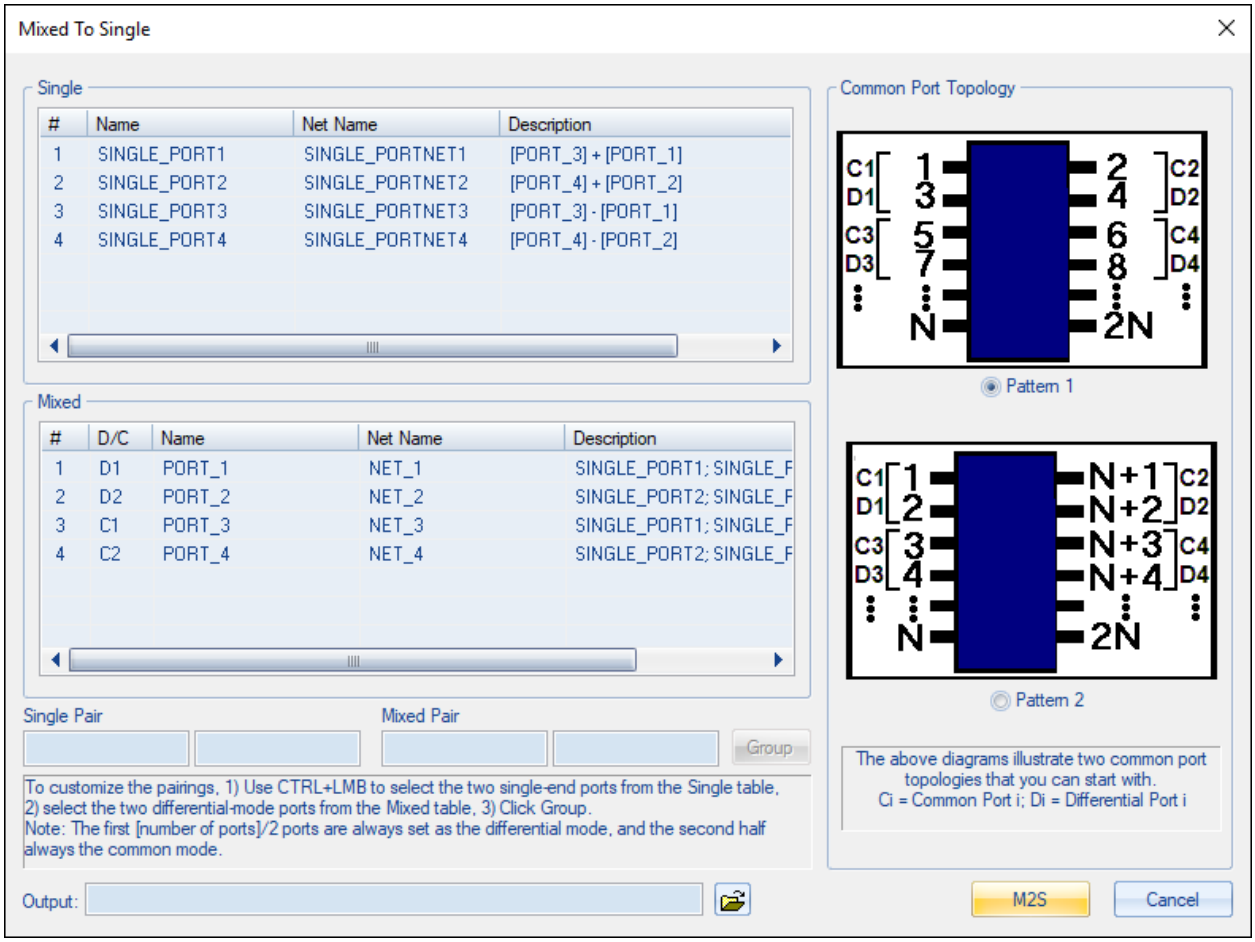

The **Description** column shows how values are calculated from the mixed-mode pairs.

The mixed-mode input follows the same port numbering as specified by the **D/C** field in the **Mixed** table. The first ([number of ports]/2) ports are the differential-modes, and the second half are the corresponding common modes. You can use the **Port Tools** utility to get your ports to follow the same sequence.

From the mixed-mode output port sequence, the first ([number of ports]/2) ports are always defined as the differential- mode voltages and currents; the next half are always defined as the common-mode values.

To specify the port pairings and run the analysis:

1. Use the radio buttons to select a **Common Port Topology**:
   - **Pattern 1** pairs single-ended port 1 and 3 along with common and differential-modes C1 and D1, respectively. Similarly, single-ended port 2 and 4 are paired and will be derived from the common and differential modes 2, and so on.

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- **Pattern 2** indicates that the single-ended port 1 and port 2 are paired together and their values derived from the common and differential modes 1. Single ended ports 3 and 4 are paired and derived from common and differential modes 3, and so on. The mixed mode port sequence is always arranged in the alternating fashion, regardless of the single-ended port pairings.

2. Alternatively, you can customize the pairing using the **Mixed** table. To set up a pairing, select the two single-ended ports (from the **Single** table) that you want to pair and the mixed differential and common mode ports (from the **Mixed** table) that you want associated with the selected single-ended ports. Click **Group** to apply the pairing. The **Description** fields for both the **Single** and **Mixed** table should be updated for the selected items to reflect the new grouping. Mixed-mode ports are always arranged so that the first ([number of ports]/2) ports are the differential ports, and the second half are the corresponding common-mode ports. When you click on any mixed-mode ports, the other mode is automatically selected as well.
3. Enter the **Output** file name to specify the output file containing the results.
4. Click **M2S** to start the analysis.

   The results are loaded and plotted in the main SUtility window.

Using the S2Q Utility

The S-Parameter to QLRX Conversion (S2Q) utility takes an S-parameter Touchstone file and generates the corresponding Quality, Inductance, Resistance, and Reactance (QLRX).

The **Q factor** indicates the amount of resistance to resonance in a system. Systems with a high Q factor resonate with larger amplitude at the resonant frequency.

The inductance, resistance, and reactance are calculated as follows:

$L=X/(2.PI.freq)$

$Q=X/R$

For single-ended computations, the effective reactance (X) and resistance (R) are calculated as:

$R + jX = 1/Y11$

$R = Re(1/Y11)$

$X = Im(1/Y11)$

To run the S2Q module from SUtility, select any input file containing only one or two ports. Then click **Utilities > S2Q**.

A text file is generated with the Q, L, R, and X parameter data. This file is loaded and plotted into the main SUtility window.

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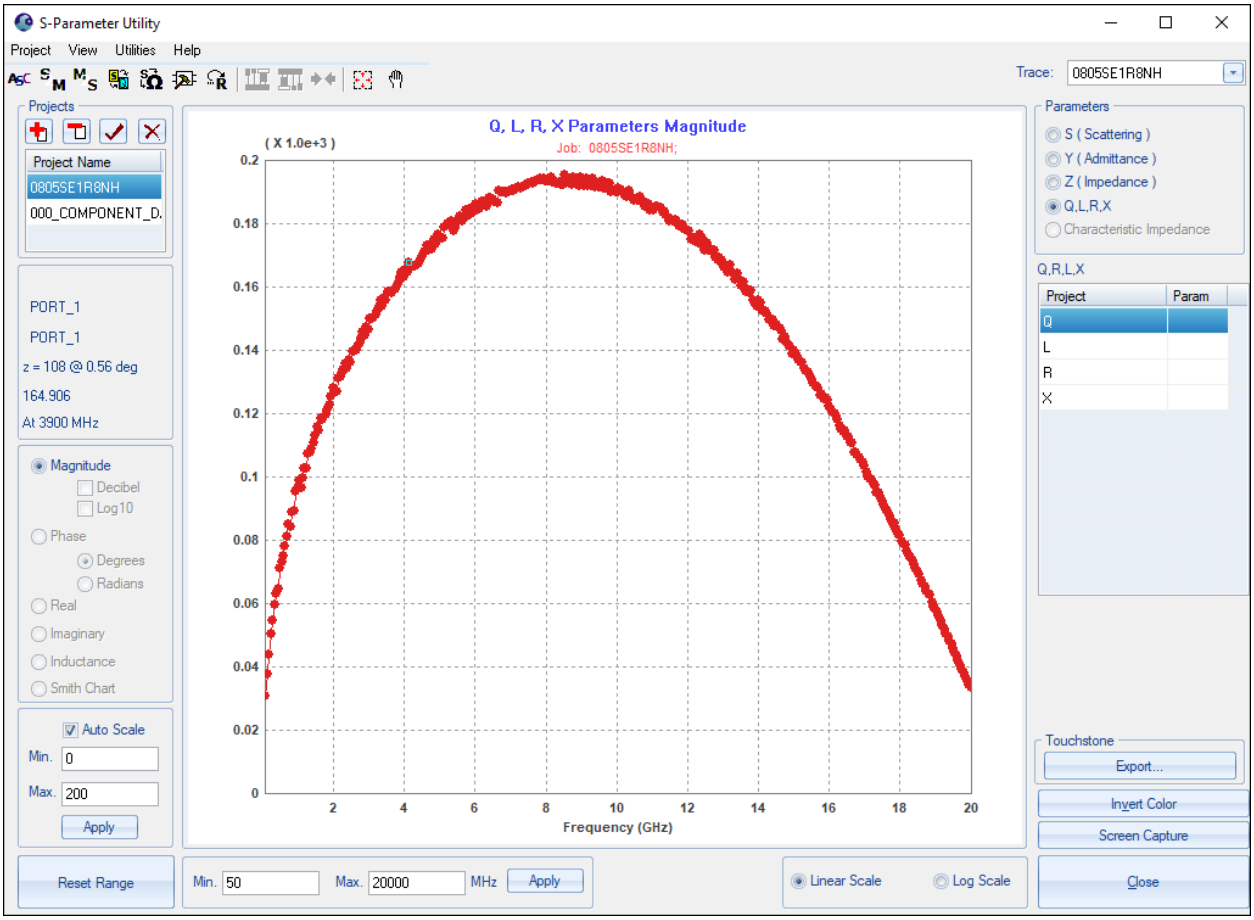

Using the Impedance Extractor

The Impedance Extractor calculates the characteristic impedance for the transmission line defined by the specified port pair.

To access the Impedance Extractor from SUtility:

1. Select the project file.
2. Click **Utilities** > **Impedance Extractor**.

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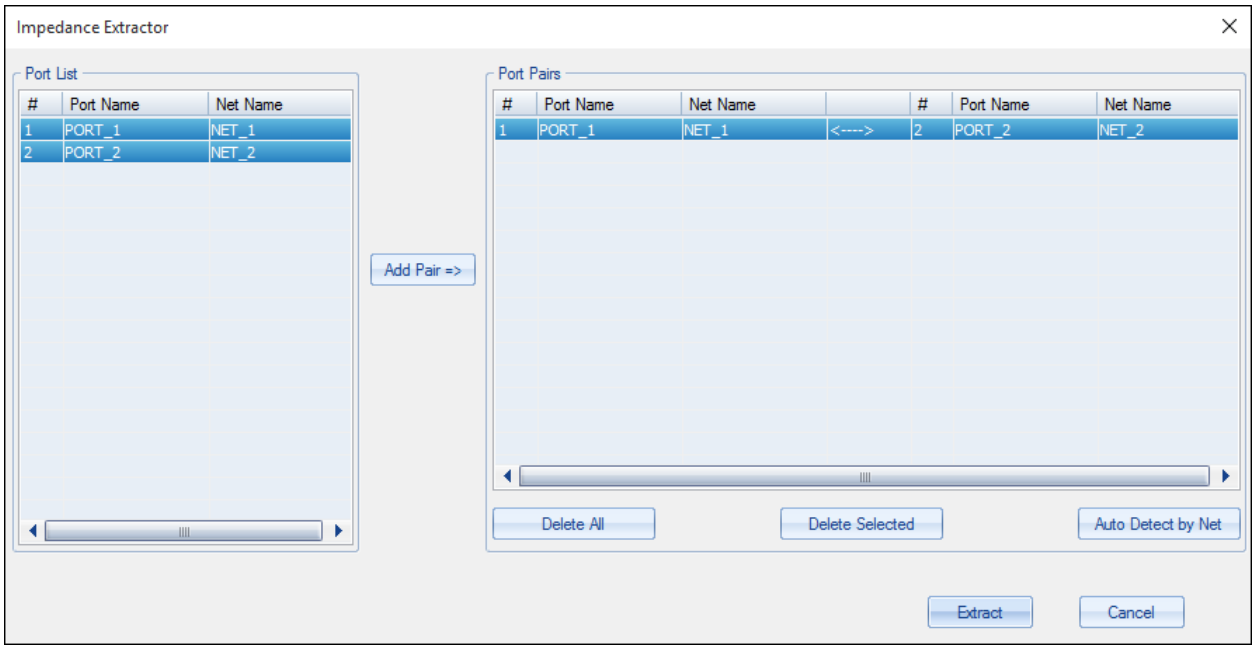
The **Impedance Extractor** window appears.



To run the analysis:

1. Select two ports from the **Port List**.
2. Click **Add Pair** to apply the pairing.

   The **Port Pairs** box updates to reflect the new pairing.
3. Alternatively, click **Auto Detect by Net** to automatically generate ports.
4. Click **Extract** to start the analysis.

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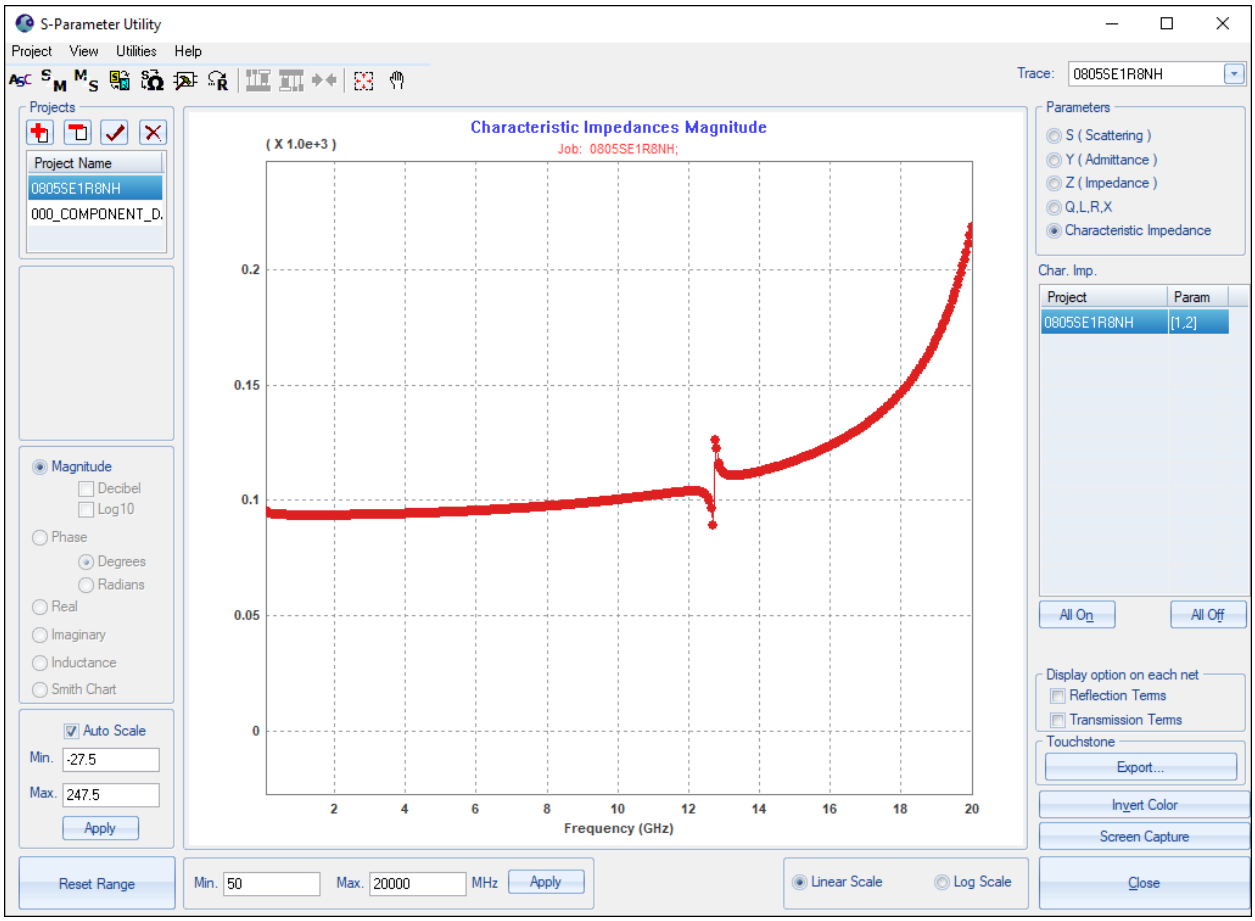
The results are loaded and plotted in the main SUtility window.



Using the Port Tools Utility

The Port Tools utility helps you rename, open, short, terminate, renumber or lump ports.

To access the Port Tools utility from SUtility:

1. Select the project file.
2. Click **Utilities** > **Port Tools**.

   The **Port Tools** window appears.

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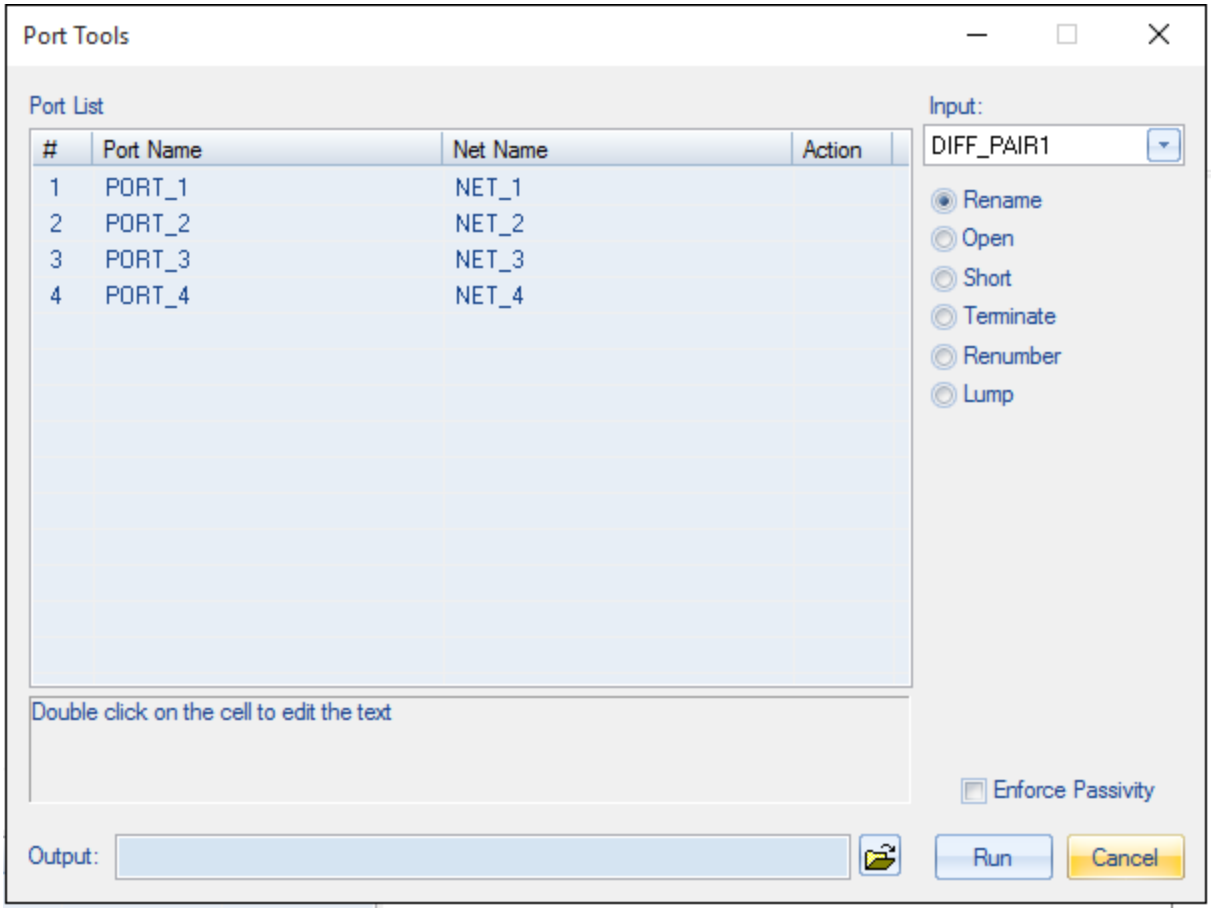

3. Select port(s) from the **Port List**.
4. Use the radio buttons to select an appropriate operation.
5. If appropriate, check **Enforce Passivity** to enforce the passivity of the result.
6. Browse to select an **Output** file name and destination.
7. Click **Run** to perform the operation.

   The results are loaded and plotted in the main SUtility window.

Using the Renormalization Utility

The Renormalization utility enables you to change the reference impedances for each port in your design.

To access the Renormalization utility from SUtility:

1. Select the project file.
2. Click **Utilities** > **Renormalization**.

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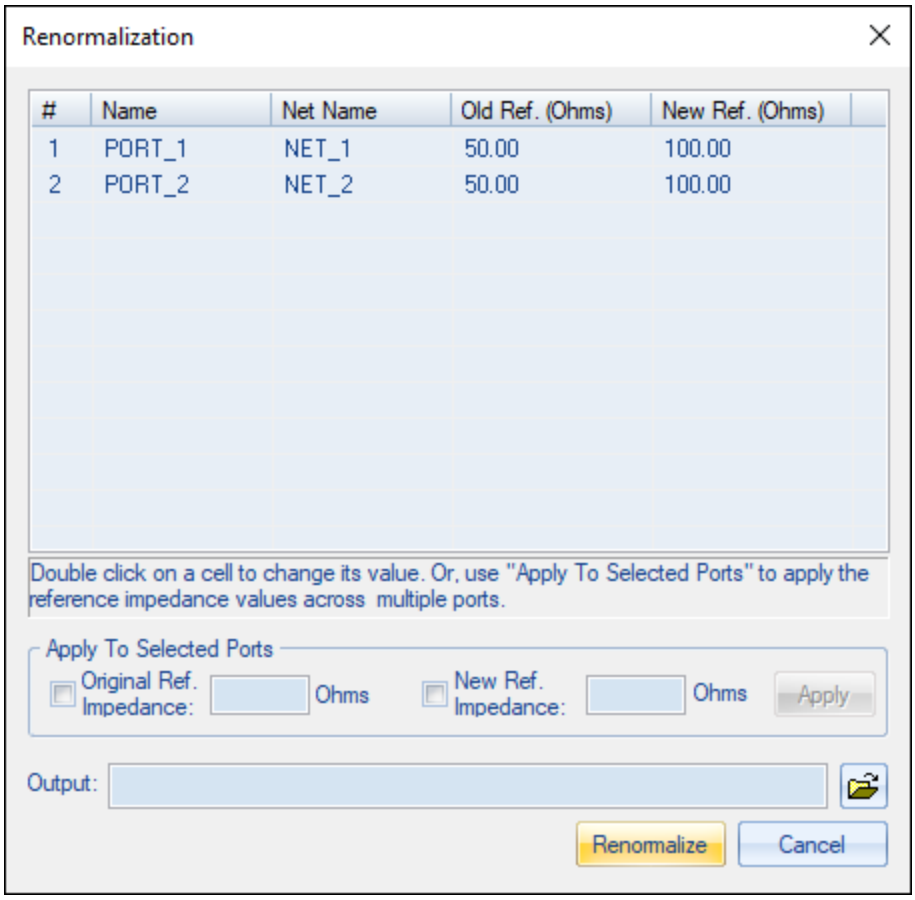
The **Renormalization** window appears, showing the list of ports.



To run a renormalization:

1. Change the port or net name: double-click a cell and enter the new name.
2. Change the reference impedance for any ports: double-click a the cell and enter the new value.
3. To change the values for multiple ports, specify values in the **Apply To Selected Ports** box. Then click **Apply**.
4. Browse to select an **Output** file name and destination.
5. Click **Renormalize** to start the analysis.

   The results are loaded and plotted in the main SUtility window.

Chip Model Analyzer (CMA)

Ansys Chip Model Analyzer (CMA) is an advanced Chip Power Model (CPM) creation tool for performance checking and failure diagnosis of the Power Delivery Network (PDN). CMA can use

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either HSpice or Nexxim simulators. HSpice and external Nexxim require licenses, but the Nexxim Internal simulator does not.

CMA does not currently interact with SIwave. However, you can launch CMA from within SIwave by clicking **Tools**. From the **External Tools** area, click **CMA**.

From there, you can import CPM files for analysis or create a pseudo CPM.

For more information about using CMA, consult the CMA training documentation by launching CMA and selecting **Help** > **Content**.

SPISim

Ansys SPISim is a simulation technology that performs modeling and signal integrity analysis. It features:

- IBIS Modeling Suite, a simplified workflow for generating new IBIS and IBIS-AMI models and for inspecting existing components, and
- COM and USB Channel Compliance Testing, a wizard-based approach for setting up and reviewing criteria for channel performance.

SPISim does not currently interact with SIwave. However, you can launch SPISim from within SIwave by clicking **Tools**. From the **External Tools** area, click **SPISim**.

For more information about using SPISim, consult the Ansys Electronics Circuit help.

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10 - Creating Reports and Plots

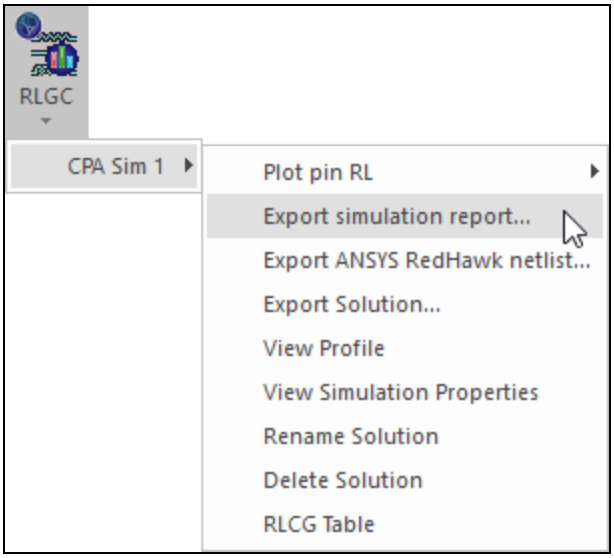
After running a simulation in SIwave, you can analyze simulation results and create various exportable reports.

Report types differ based on the type of simulation, but include:

- 2D and 3D Plots
- Statistics
- Animated Reports

To view or export a report in SIwave:

1. Run a simulation.
2. Click **Results**.
3. Use the drop-down menu for the simulation type you ran to select the option for viewing or exporting a report.



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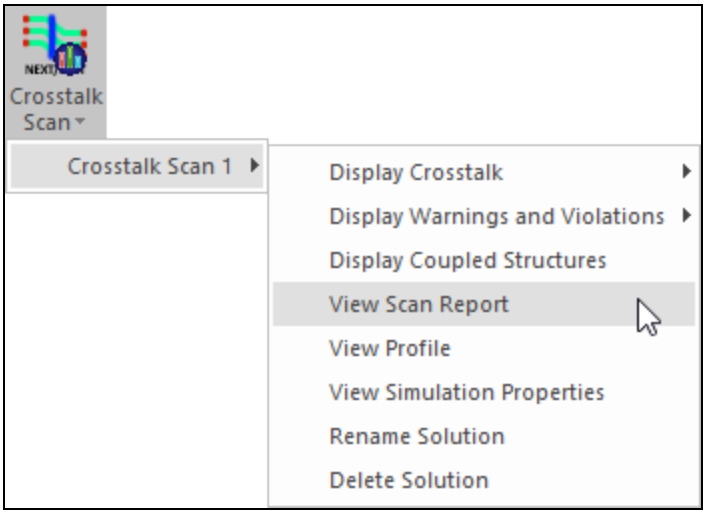
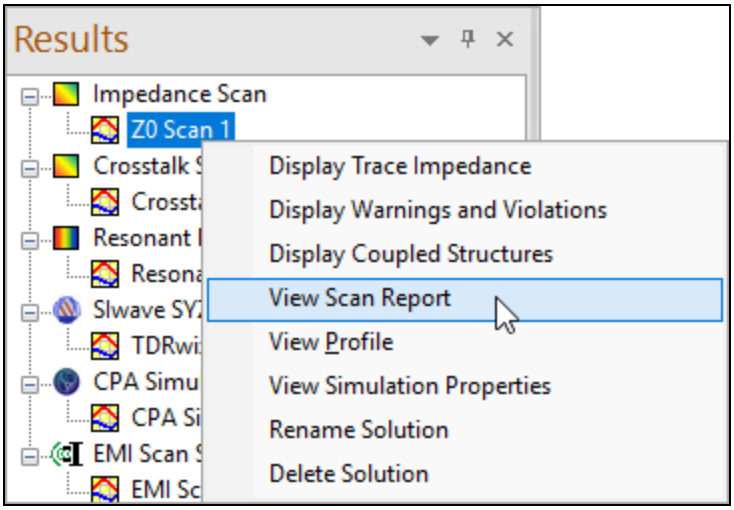


Alternatively, right-click a simulation in the **Results** window and select the option for viewing or exporting a report.



Information on reports for each simulation type can be found in **Running a Simulation**.

> **Note:**
>
> Some reports, such as SIwizard and TDRwizard reports, open in Ansys Electronics Desktop. These may take a few moments to load.

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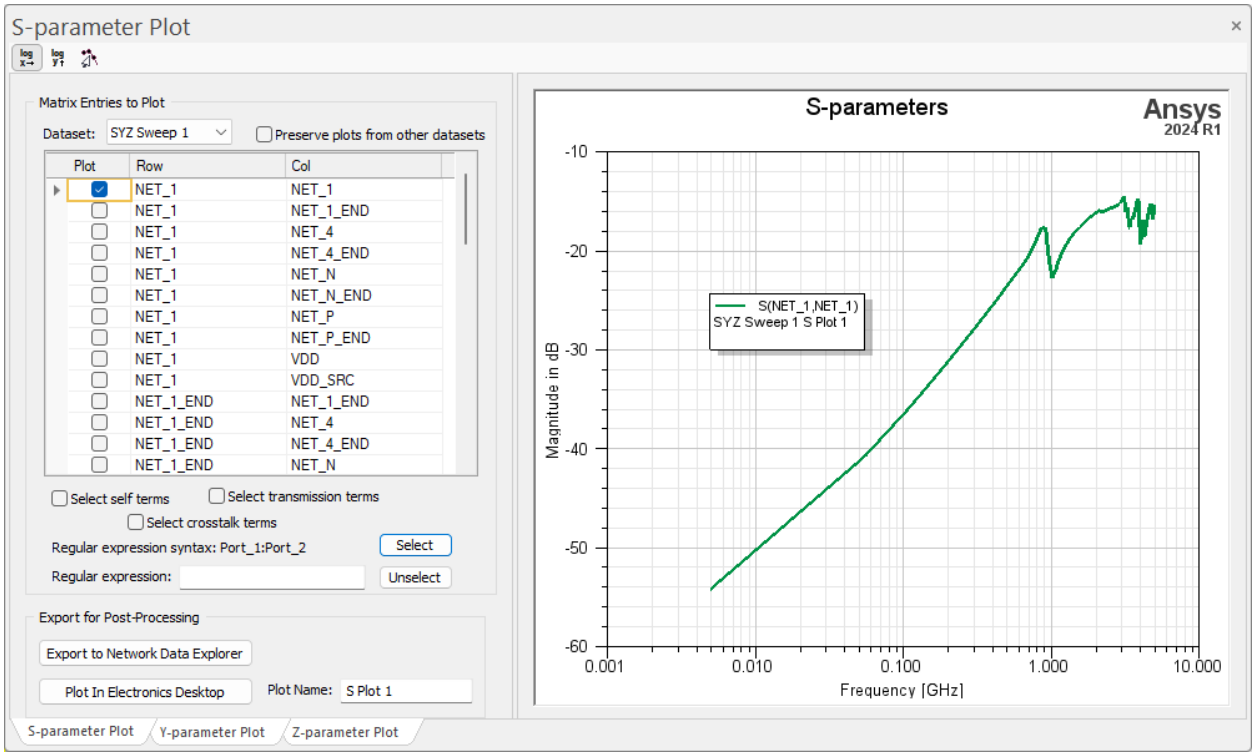
Plotting Magnitude

Following SYZ, PSI SYZ, or HFSS 3D Layout simulation, SIwave can generate S-, Y-, and Z-parameter magnitude plots. After running multiple simulations, complete these steps to pool the SYZ simulation results, plot multiple curves from different datasets, and compare the results.

1. From the **Results** window, right-click the simulation and select **Plot Magnitude** to open the **S-parameter Plot** window.



2. Check/uncheck boxes in the **Matrix Entries to Plot** area (i.e., the **Plot** table, **Select self terms**, **Select transmission terms**, and **Select crosstalk terms** boxes) to select/deselect data to plot.
3. If appropriate, enter a **Regular expression** in the field (i.e., **NET_1:NET_1**). Then click **Select** to automatically check all the rows in the **Plot** table specified by the expression and simultaneously populate the graph.

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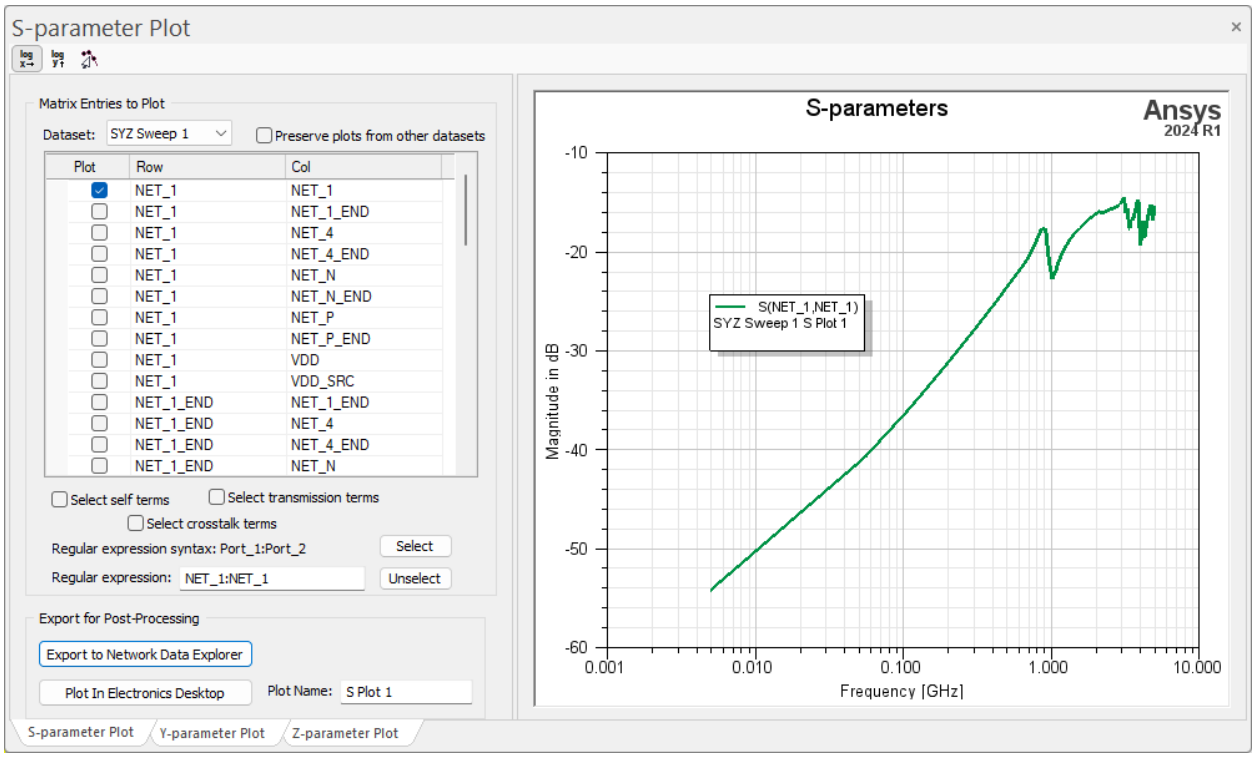

a. Click **Unselect** to uncheck all of the boxes activated by a **Regular Expression** and clear the graph.

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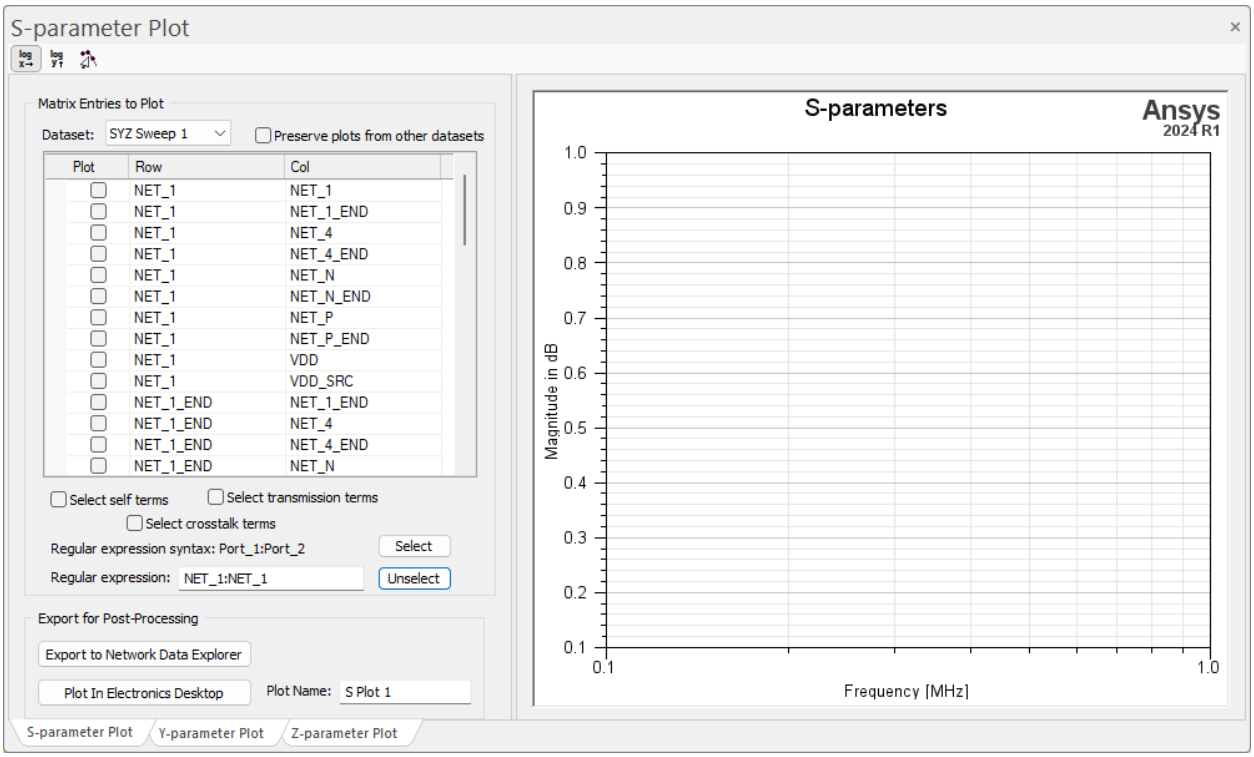

Log X and **Log Y** allow users to select the plot's scale.

> **Note:**
>
> **Log X** and **Log Y** only work if the values on the specified axis are greater than 0. Otherwise, the plot is cleared.

Show Marker allows users to choose between displaying data points or lines.

> **Note:**
>
> Selecting a curve in the plot highlights the ports and connected nets, and zooms the **Modeling** workspace to fit.

4. Click the **Y-parameter Plot** or **Z-parameter Plot** tab to switch to an appropriate information. The options available on these tabs are the same.

Comparing Datasets

Complete these steps to compare datasets.

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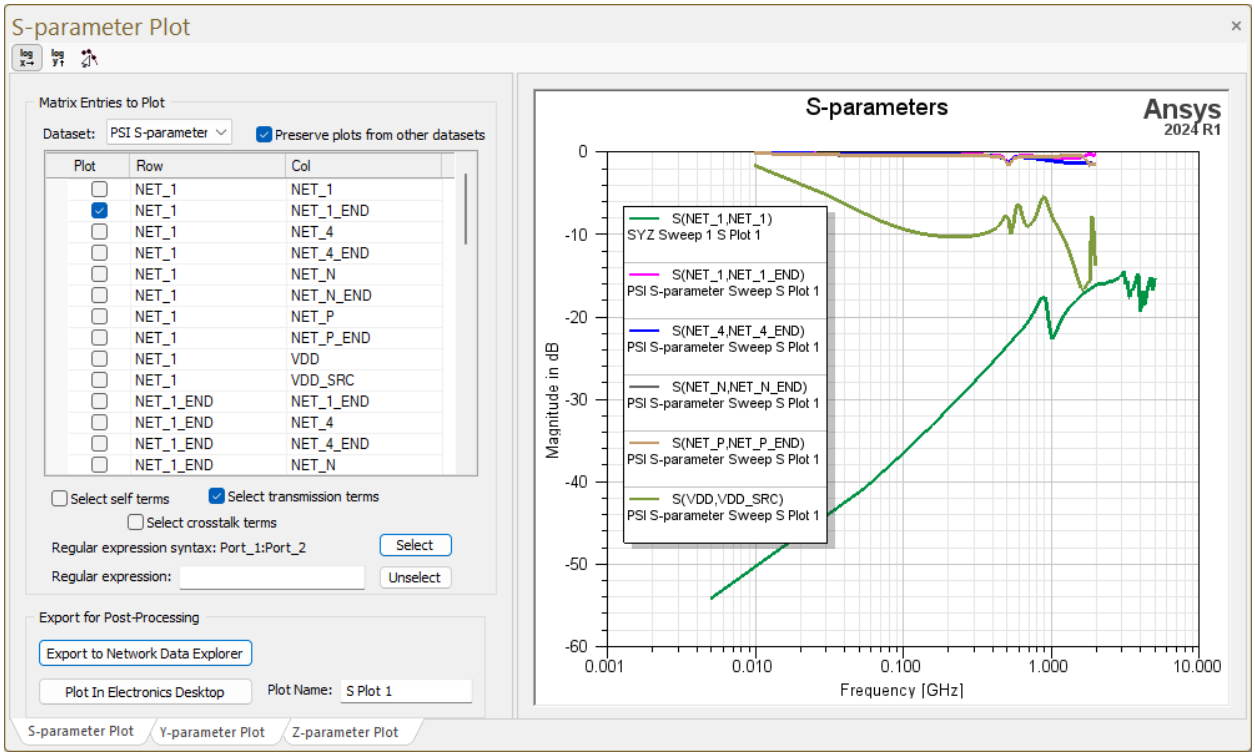
1. The **Dataset** drop-down menu preselects the simulation from which users navigated to the **S-parameter Plot** window. If there are multiple complete SYZ simulations (e.g., SYZ, PSI SYZ, or HFSS SYZ) in the **Results** window, all of the simulation results will be pooled together. Select any dataset and the results of that simulation populate the graph, making it inappropriate to relaunch the **SYZ Parameter Plot** window from the **Results** window to load new datasets.
2. Select **Preserve plots from other datasets** and then select a new dataset from the **Dataset** drop-down menu. Checking the **Preserve plots from other datasets** box maintains the curves in the graph when a new data set is loaded, so multiple simulation results can be compared at once.



If boxes are deselected, the curves are cleared when a new dataset is loaded.

> **Note:**
>
> **Click+drag** the plot legend to an appropriate location. Right-click in the plot to select from additional actions.

Exporting a Plot

Complete these steps to export a plot.

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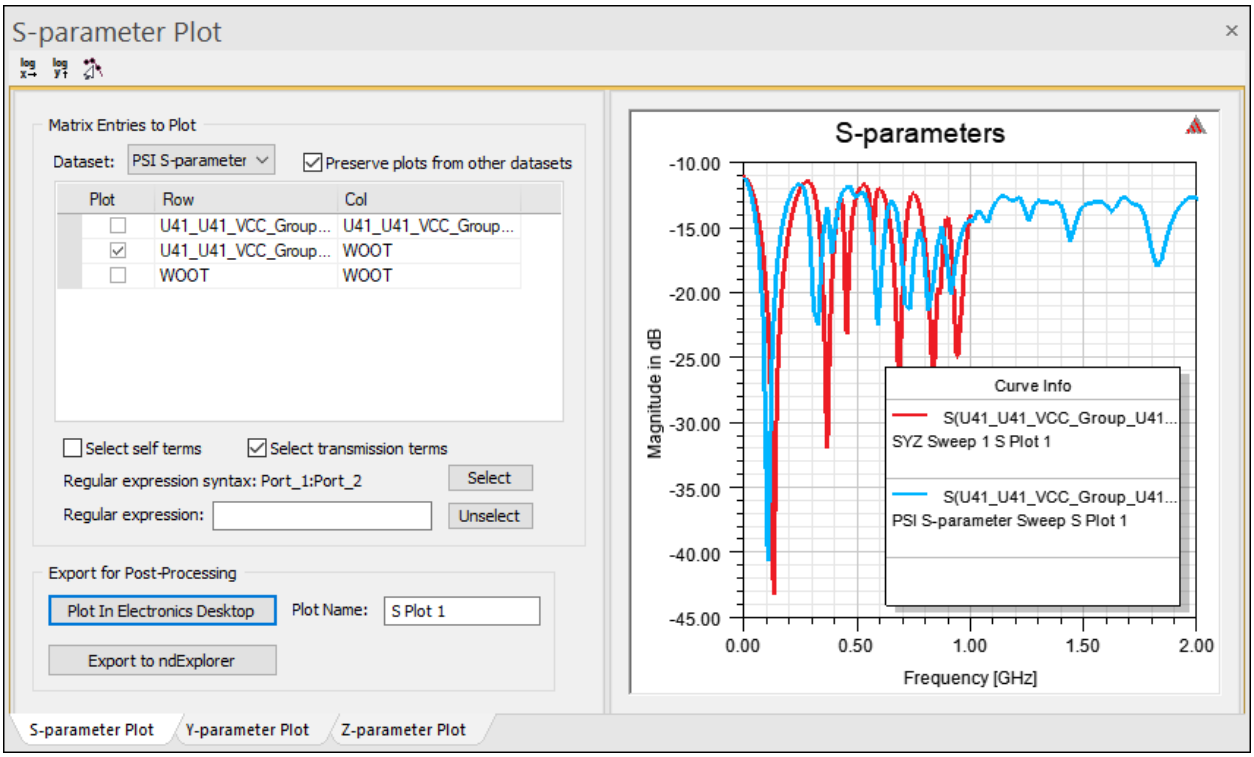
1. Enter a **Plot Name**.
2. Click either **Plot In Electronics Desktop** or **Export to ndExplorer**, as appropriate.

Changing Plot Display Options

For certain SIwave plots, such as S-, Y-, and Z-parameter magnitude plots and IL/RL/NEXT/FEXT plots, you can change how the plot displays.



Double-clicking within the plot enables opens the **Properties** window on the relevant tab.

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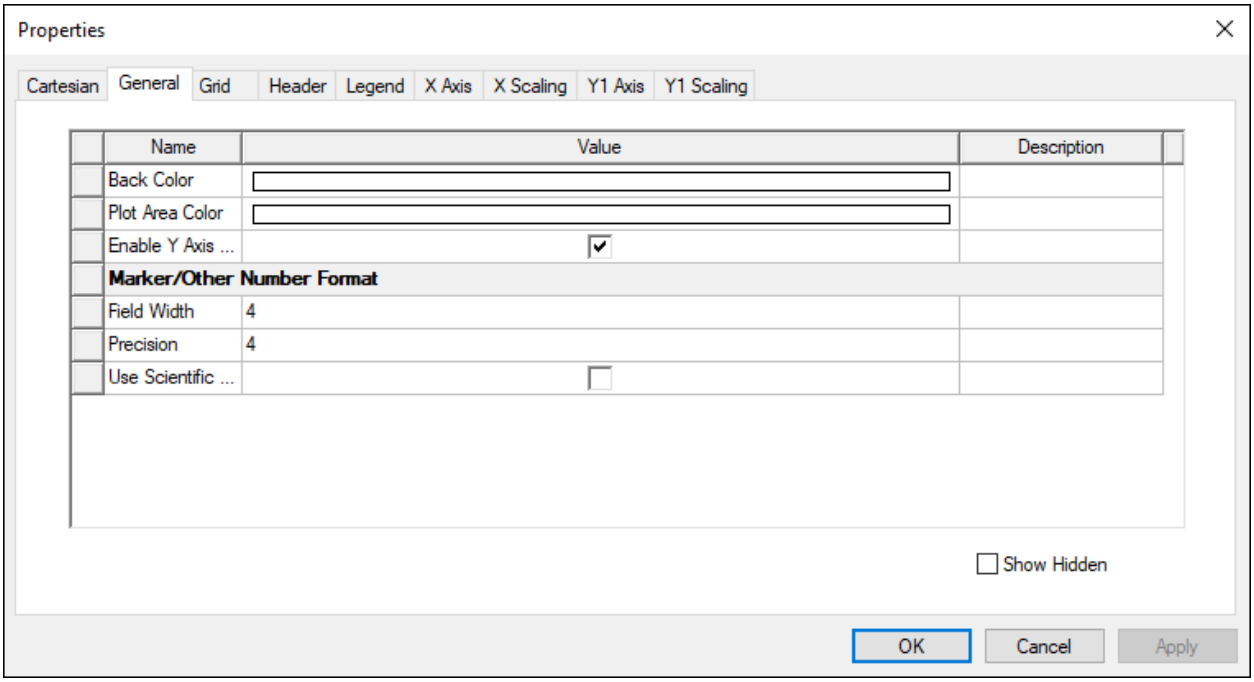

Tabs include:

- Cartesian
- General
- Grid
- Header
- Legend
- X Axis
- X Scaling
- Y Axis
- Y Scaling

Each tab allows you to specify display units, colors, fonts, and scaling for the relevant plot element. Select **Show Hidden** on any tab to view additional options.

Additional Plotting Actions

For certain SIwave plots, such as S-, Y-, and Z-parameter magnitude plots and IL/RL/NEXT/FEXT plots, right-clicking enables additional plotting actions.

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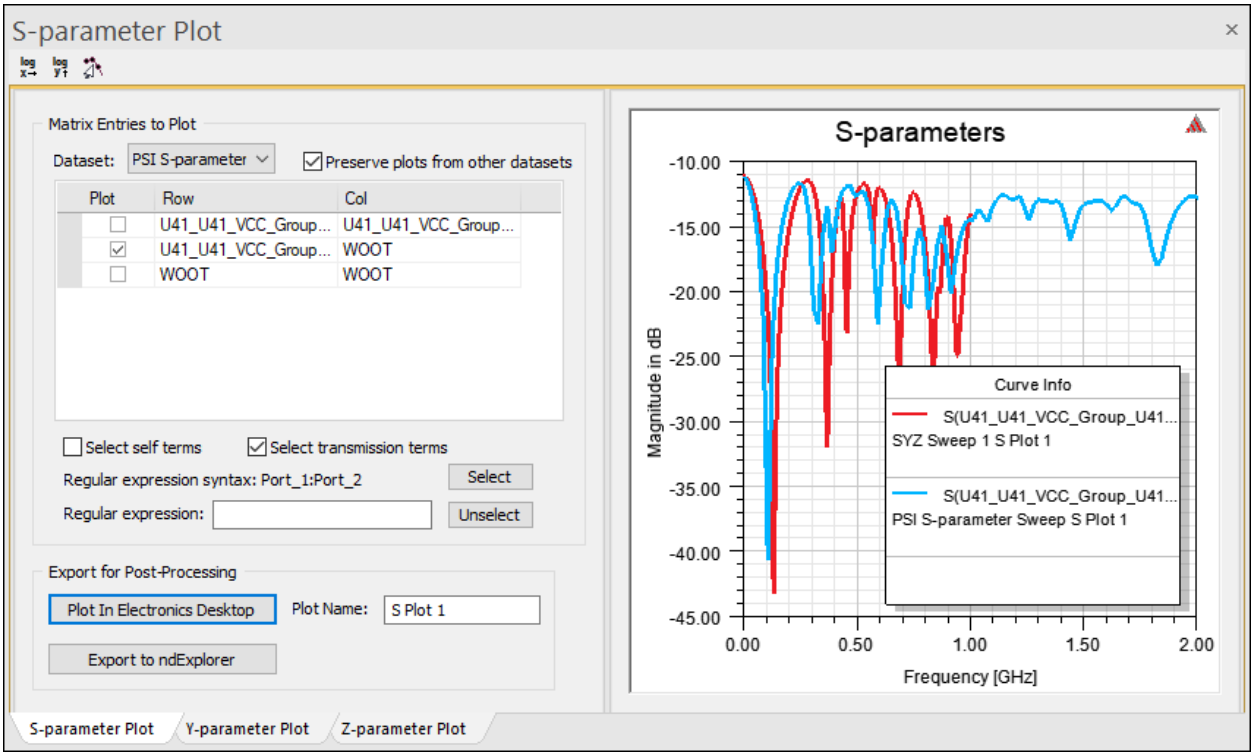
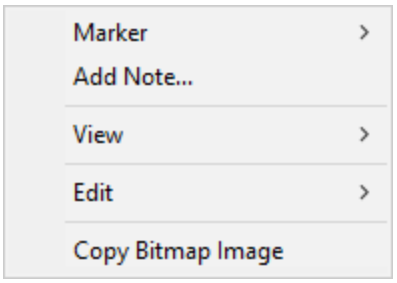


Right-clicking within the plot enables options for adding markers and notes, changing the display, and editing settings.



Menu options include:

- **Marker** – Submenu containing marker options.
  - **Add Marker** – transforms the cursor into a crosshair, allowing you to click and place a marker at an appropriate point. When you are finished placing markers, right-click and select **End Marker Mode**. Markers appear on the plot and in a table showing their coordinates.

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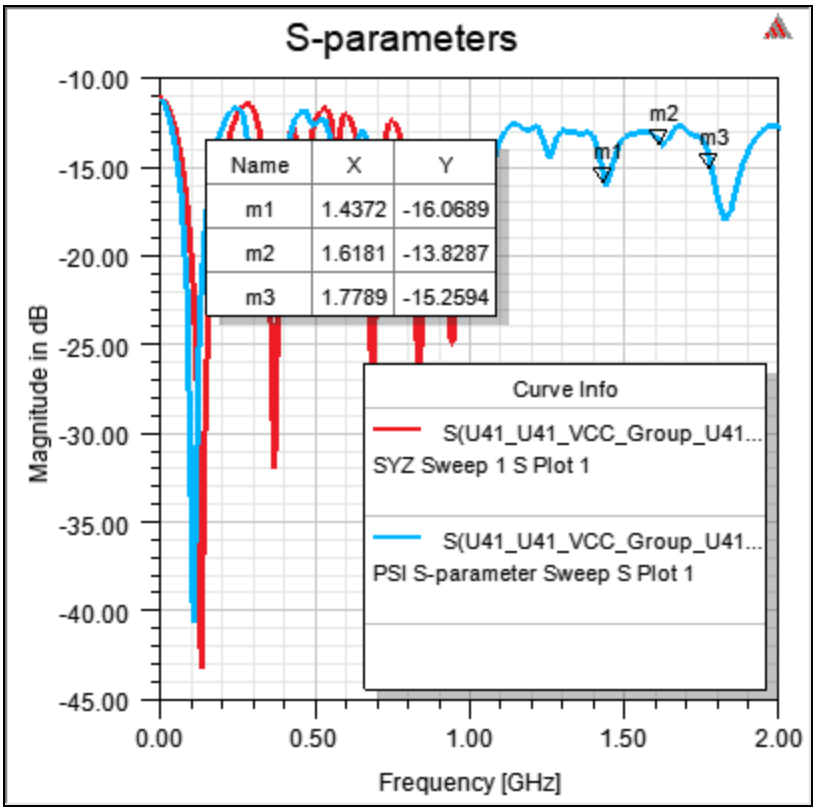

- **Add Delta Marker** – transforms the cursor into a crosshair, allowing you to click and place a marker at an appropriate point. You must then click a second point, and a table appears showing deltas and slopes. When you are finished placing markers, right-click and select **End Marker Mode**.

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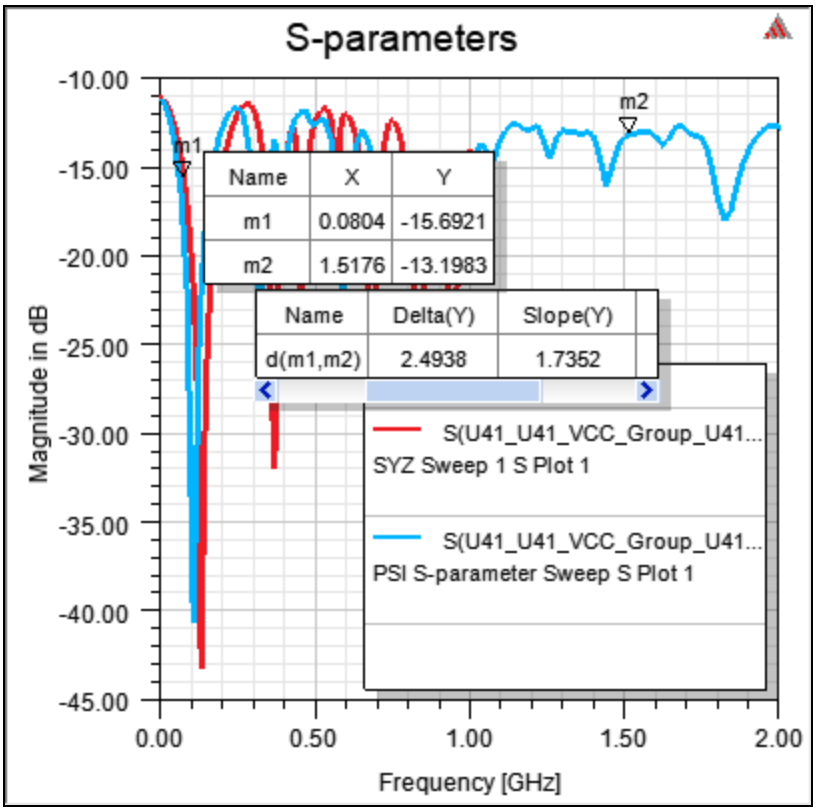

- **Export Marker Table** – exports the marker coordinate table in *.csv or *.tab format.
- **Export Delta Marker Table** – exports the delta marker table in *.csv or *.tab format.
- **Add Maximum** – places a marker at the maximum value along the X-axis.
- **Add Minimum** – places a marker at the minimum value along the X-axis.
- **Add X Marker** – adds up to 10 movable markers as vertical lines rising from the X axis. Each added marker has its own color and editable properties. To move an X marker, click on the X label and drag it to an appropriate location. The label at the bottom of the line gives the X coordinate, and flag on the vertical line identifies the Y coordinate.
- **Bring X Marker Into View** – when one or more X markers is not visible, this option allows you to bring them into view.
- **Add Y Marker** – adds up to 10 movable markers as horizontal lines extending from the Y axis. Each added marker has its own color and editable properties. To move a Y marker, click on the Y label and drag it to an appropriate location. The label at the bottom of the line gives the Y coordinate, and flag on the vertical line identifies the X coordinate.
- **Bring Y Marker Into View** – when one or more Y markers is not visible, this option allows you to bring them into view.
- **Next Peak** – selects the next high point along the X-axis, before the next dip.
- **Next Minimum** – selects the next lowest point along the X-axis, after the next high point.

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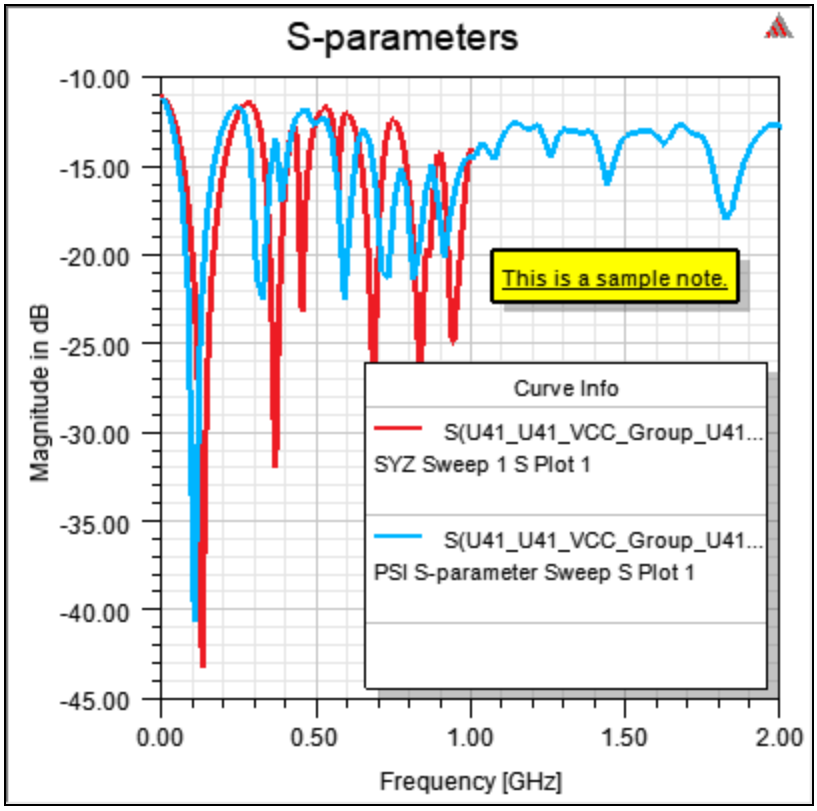
- **Previous Peak** – selects previous next high point along the X-axis, before the previous dip.
- **Previous Minimum** – selects the previous lowest point along the X-axis, after the previous high point.
- **Go to Start** – selects the first marker on the plot, along the X-axis.
- **Go to Previous** – selects the previous marker on the plot, along the X-axis.
- **Go to End** – selects the last marker on the plot, along the X-axis.
- **Next Curve** – selects the next curve on the plot, based on the order in the legend.
- **Previous Curve** – selects the previous curve on the plot, based on the order in the legend.
- **Clear All** – removes all markers from the plot.

- **Add Note** – Allows you to add a note to the plotting area. You can click and drag the note to your appropriate location.



Select the note and press the **Delete** key to remove it.

- **View** – Submenu containing view options.
  - **Pan** – Changes the cursor to move the plot within the window. Right-click and deselect **Pan** to exit this mode.

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  - **Zoom** – Changes the cursor to zoom the entire plot in or out within the window. Right-click and deselect **Zoom** to exit this mode.
  - **Zoom In / Zoom Out** – Changes the cursor to a crosshair. Click a point in the plot to zoom in to it or out from it. Right-click and deselect **Zoom In** or **Zoom Out** again to exit this mode.
  - **Fit All / Fit X Window / Fit Selection / Best Vertical Fit** – Automatically scales the plot to an appropriate size.
  - **Show / Hide Selection / Show All** – When a dataset is selected on the plot, **Show / Hide Selection** allows you to hide or show that dataset. Select **Show All** to return to the original plot displaying all datasets.
  - **Visibility** – Opens a window where you can set the visibility of traces, notes, and legends.
  - **Animate** – This functionality is not yet present in the plot window.
- **Edit** – Submenu containing edit options.
  - **Copy Settings** – Copies the display settings in text format for use in scripts.
  - **Reset Settings** – Resets the plot window to its original view, including scale, colors, etc.
  - **Delete** – Allows you to delete a marker.
  - **Properties** – Opens the **Properties** window, where you can change display options.
- **Copy Bitmap Image** – Copies a bitmap image of the plot to the clipboard for pasting into a graphics editor or other compatible software.

Displaying and Editing the Color Scale

Displaying the Color Scale

The color scale helps you correlate the colors in a 3D voltage plot with specific numerical values. After the simulation is run, the color scale is visible by default.

To enable or disable the color scale:

1. Click **View**.
2. From the Show/Hide area, click the **Display Color Scale** icon ( ) .

Editing the Color Scale

To edit the color scale:

1. Click **Advanced** > **Color Scale**.

   The **Edit Color Scale** window appears.

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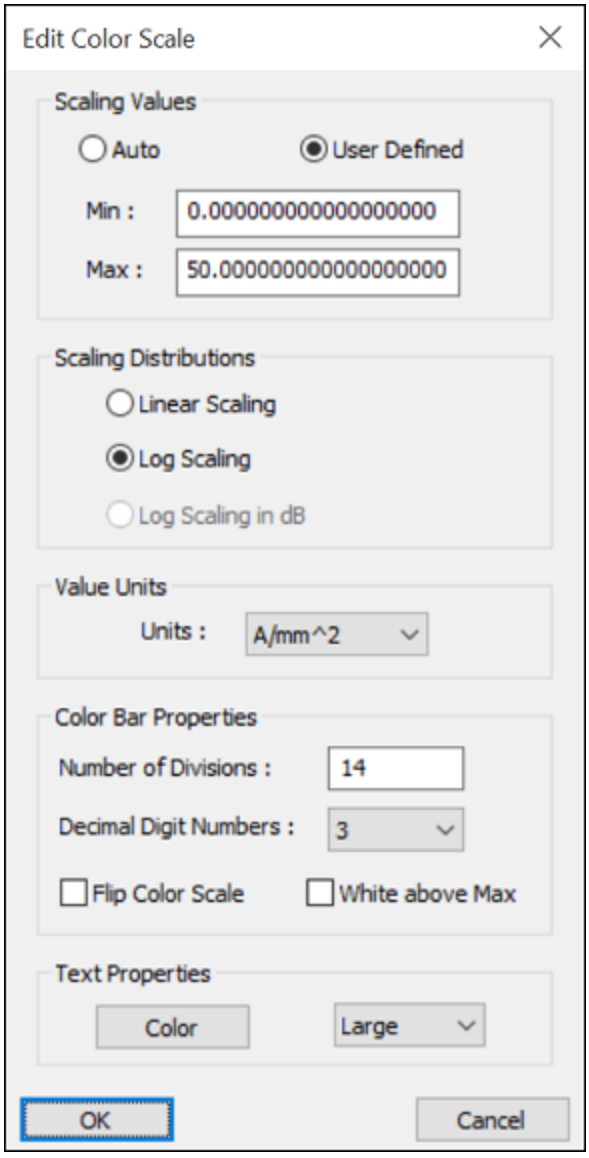

2. From the **Scaling Values** options, select **User Defined**.
3. Enter the **Minimum Value**.
4. Enter the **Maximum Value**.
5. From the **Scaling Distributions** options, select a scaling type (linear, logarithmic).
6. From the **Value Units** area, use the drop-down menu to select a unit of measure.
7. From the **Color Bar Properties** area, select the **Number of Divisions** and **Decimal Digit Numbers**.
8. If appropriate, select **Flip Color Scale** to reverse the scale.
9. If appropriate, select **White Above Max** to display areas greater than the specified maximum value in white.

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> **Note:**
>
> When **Flip Color Scale** is selected, this option changes to **White Below Min** and displays areas lower than the specified minimum value in white.

10. From the **Text Properties** area, select a color and size for text.
11. Click **OK**.

    The graph displays as defined.

SIwave Reports in Ansys Electronics Desktop

Some reports, such as SIwizard and TDRwizard reports, open in Ansys Electronics Desktop. This section contains information about working with those reports.

Topics include:

Modifying Reports

Changing Report Display

Exporting Reports

Sweeping a Variable in a Report

Modifying Reports

To modify the data that is plotted in a report:

1. From the **Project Manager**, expand **Results** and select the report you want to modify.
2. Right-click and select **Modify Report**.

   The **Report** window appears, on the **Trace** tab.

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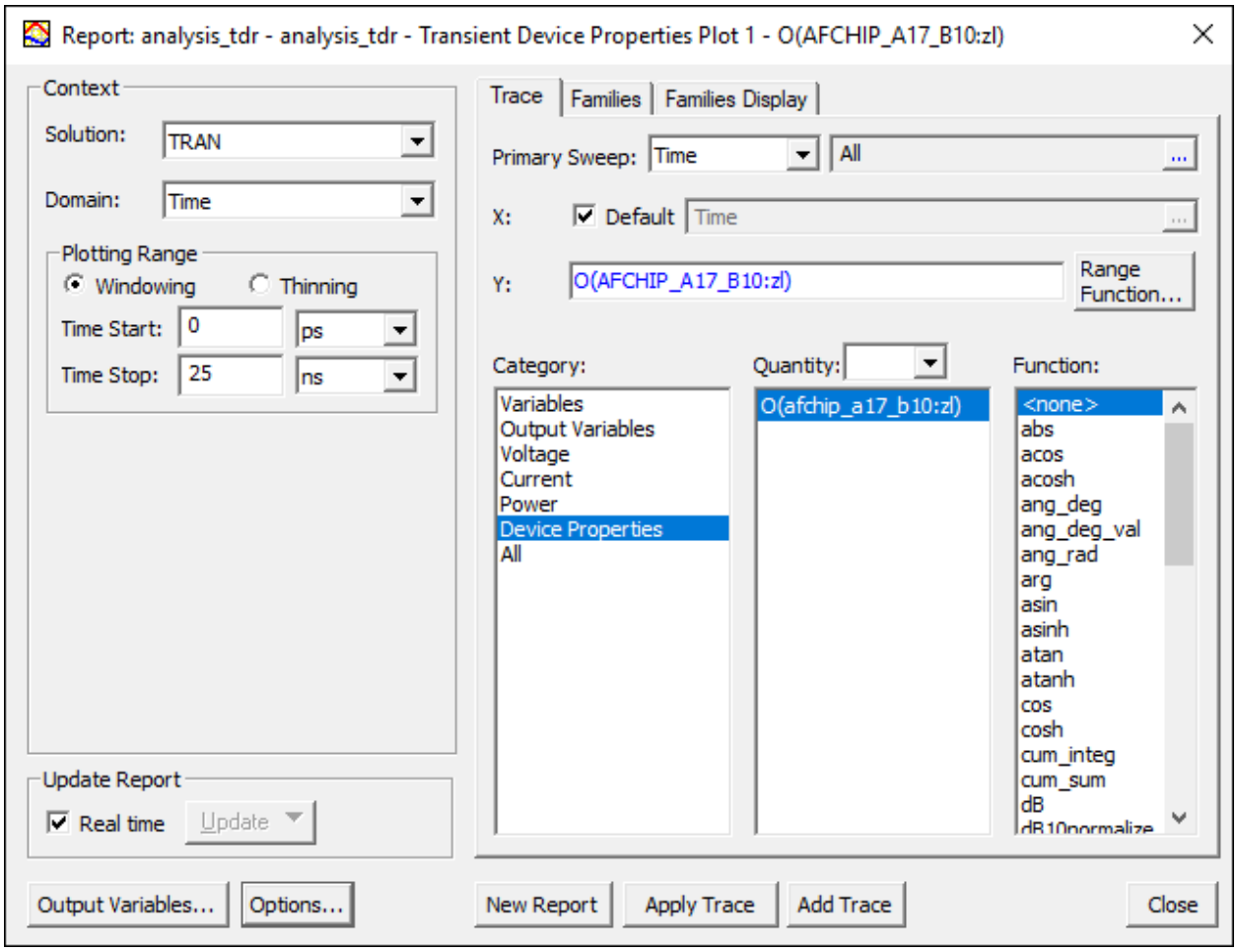

3. **Report** window buttons allow you create a new report with the settings you provide, or to modify the existing report.
   - **Output Variables** – opens the **Output Variables** window.
   - **Add Trace** – this is enabled when you have created or selected a report. See: Working with Traces.
   - **Apply Trace** – updates the selected traces in a report based on further processing or changes.
   - **New Report** – adds a report to the Project tree under the Results icon. The new Report is displayed in the main window.
   - **Options** – opens the **Report Setup Options** window. This contains a check box for using the advanced mode for editing and viewing trace components. This mode is automatic if the trace requires it. It also contains a field for setting the maximum number of significant digits to display for numerical quantities.
   - **Close** – closes the **Report** window.

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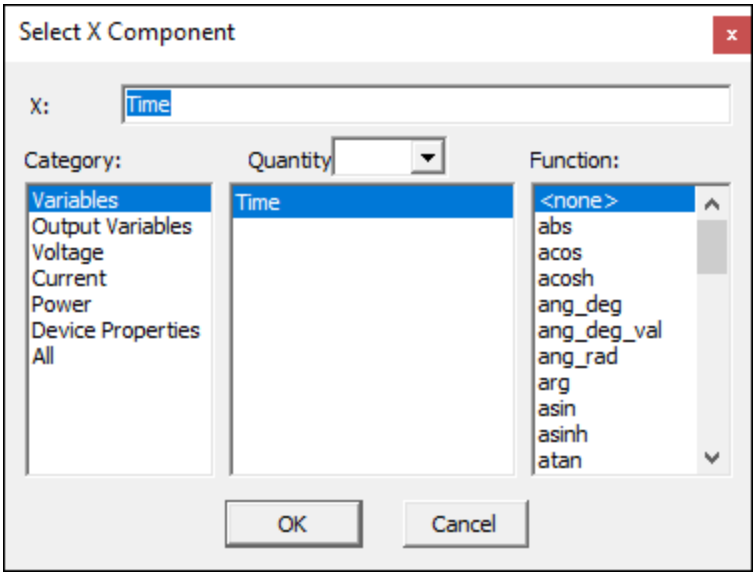
4. The **Update Report** area contains the **Real Time** check box and **Update** drop-down menu.
   - **Real Time** – when selected, enables real time updates for all reports while the reports are being edited. When deselected, enables the drop-down menu to **Update Report** or **Update All Reports** manually. This can be useful if you expect a trace to take time to display. You can then add additional traces without having to wait.
5. The **Context** area allows you to make selections depending on the design and solution type.
6. The **Trace** tab provides trace options.
   a. From the **Primary Sweep** drop-down menu,
   b. From the **X** component field, leave **Default** selected to maintain SIwave's default settings, or deselect it and click **...** to open the **Select X Component** window.
      1. The **Select X Component** window appears.



      2. Use the **Category**, **Quantity**, and **Function** lists to make new selections.
      3. Click **OK** to apply your selections and close the window.

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c. From the **Y** component field, make selections for:
   1. **Categories** – These depend on the solution type and design.
   2. **Quantity** – These are relative to the selected category.

> **Note:**
>
> The Quantity text field can be used to filter the Quantity list by typing in text, or by using the four predefined selections. This is useful if the Category selected produces a lengthy Quantities list. See Filtering Quantity Selections for the Reporter.
>
> When the matrix is very large, the number of quantities can be correspondingly huge. Therefore, the Quantities field can optionally use a tree structure to divide matrix quantities into groups by their first element name. The initial display shows groups, without initially listing group members.

   3. **Function** – Selects the function(s) to apply to Y quantities.

   The **Y** component field displays the currently selected **Quantity** and **Function**. You can edit this field directly, or click **Range Function** to open the **Set Range Function** window. See: Function List.

> **Note:**
>
> Color shows valid expression.

7. The **Families** tab provides a way to select from valid solutions for sweeps where a simulation has multiple variables defined (e.g., for a parametric sweep). If so, the variables other than the one chosen as the **X (Primary sweep)**, are listed under the **Families** tab with columns for the variable, the value, and an Edit column with a **[...]** button.
8. The **Families Display** tab

You can also view and edit the properties of Reports and their traces via their Properties windows. See: Changing Report Display.

Specifying Output Variables

You can access the **Output Variables** window in several ways:

- Click **Results** > **Output Variables**.
- From the **Project Manager**, right-click **Results** and select **Output Variables**.
- From the **Solution Setup** window, select the **Expression Cache** tab, click **Add...** to display the **Add to expression cache** window, and click the **Output Variables** button.

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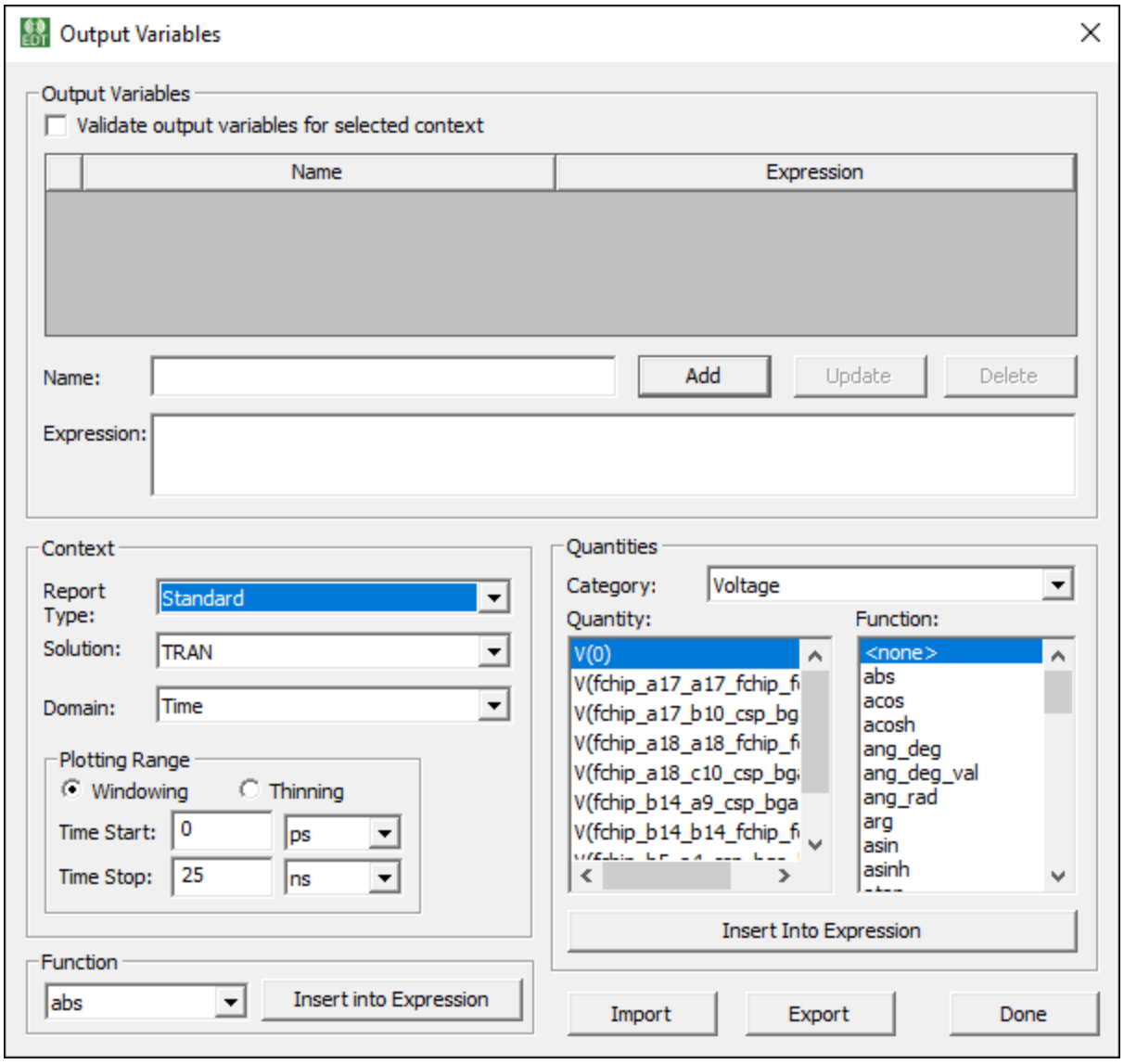
- Click the **Output Variables** button in the **Reports** window.

  The **Output Variables** window appears.



The **Output Variables** window contains four sections:

- **Output Variables** – where you can specify the name and expression for a new output variable. Existing variables appear in the list at the top of the window. You can also use a check box to **Validate output variable for selected context**.
- **Context** – where you can specify the report type, the solution, and the domain (if applicable). Changing the report type to Near Fields or Far Fields causes a Geometry menu to appear. Selecting Emission tests require a digital signal. All selections affect the Functions listed.

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- **Quantities** – where you can insert quantities into the Expression area of the **Output Variables** section.
- **Function** – where you can insert completed expressions into the Expression area of the **Output Variables** section.

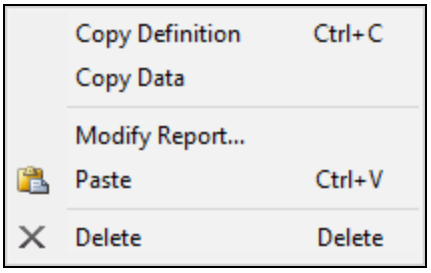
Working with Traces

A trace in a 2D or 3D report defines one or more curves on a graph. A trace in a data table defines part of the displayed matrix of text values.

The values used for a plot's axes (which may be X, Y, Z, phi, theta, or R) can be variables in the design (such as frequency) or functions and expressions based on the design's solutions. If you have solved one or more variables at several values, you can "sweep" over some or all of those values, resulting in a curve in 2D or 3D space.

A report can include any number of traces and, for rectangular graphs, up to four y-axes.

Traces appear in the Project Tree under their report, where they can be selected, copied, pasted, and deleted from the shortcut menu.



Note:

- You must copy and paste trace definitions between reports of one type (e.g., you cannot paste a Modal Solution Data report into a Far Fields report).
- If you copy and paste a report or trace definition to a design containing a definition with the same name, an incremented number is appended to the pasted item.
- If the report or trace definition contains properties that do not exist in the target design (e.g., a port name), an error will state that a solution does not exist for this trace.

When you move a cursor over a trace in a report, the cursor changes to show that you can make a selection:

- For PC systems, the cursor changes to the color of the selectable trace.
- For Unix systems, the cursor changes to a solid black arrow, rather than the default black outline.

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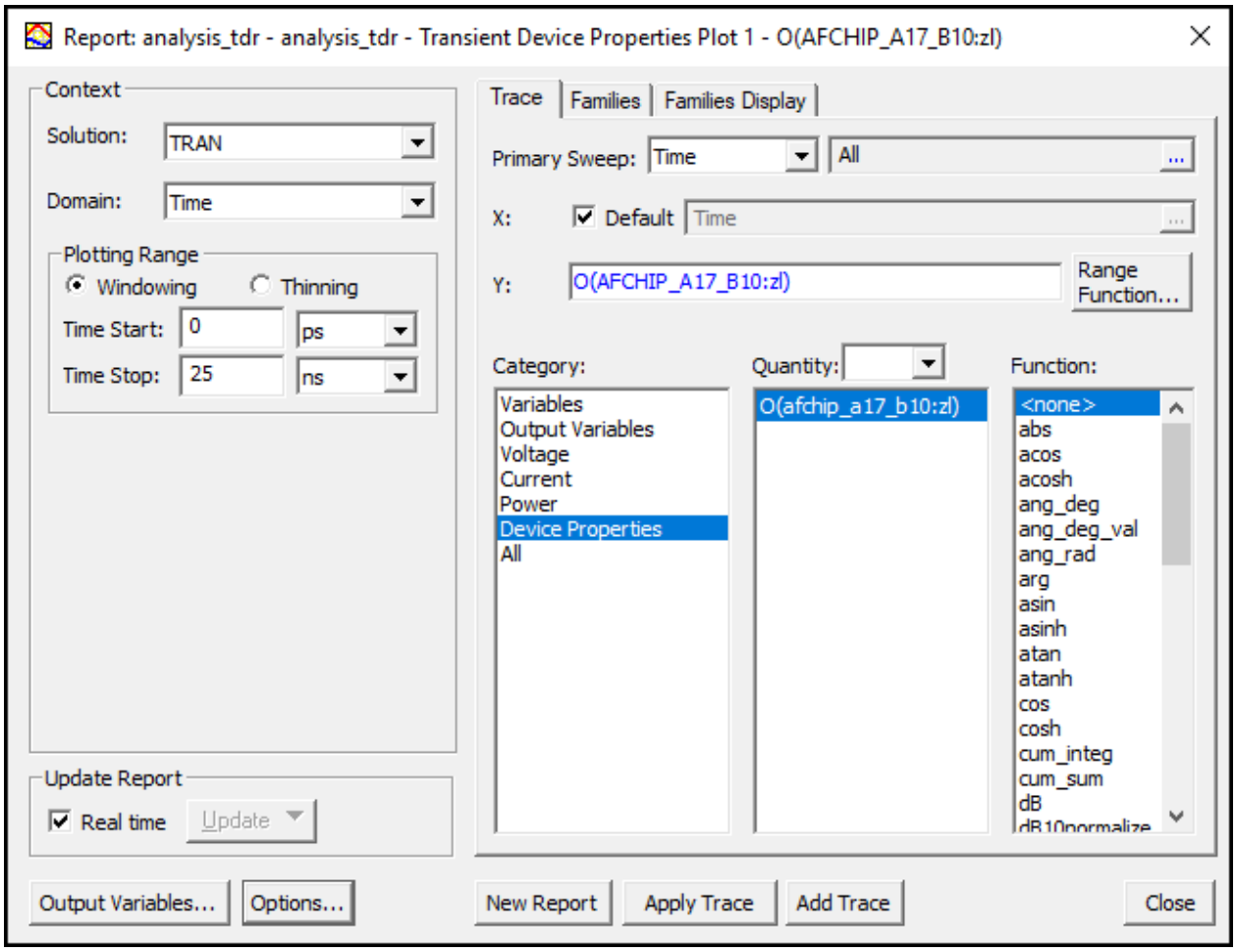
To add a trace to a report:

1. Right-click a report and select **Modify Report**.

   The **Report** window appears, on the **Trace** tab.



2. Specify an appropriate information. See: Modifying Reports.
3. Click **Add Trace**.

A trace is added to the traces list under its report icon in the Project Tree. The trace represents the function of the quantity you selected and will be plotted against other quantities or swept variable values. Selecting a trace in the Project Tree displays the Properties window for that trace.

By the default, the trace name is the definition (category, quantity and function). Trace properties can be edited directly in the **Properties** window or in the **Report** window.
See: Editing Trace Properties.

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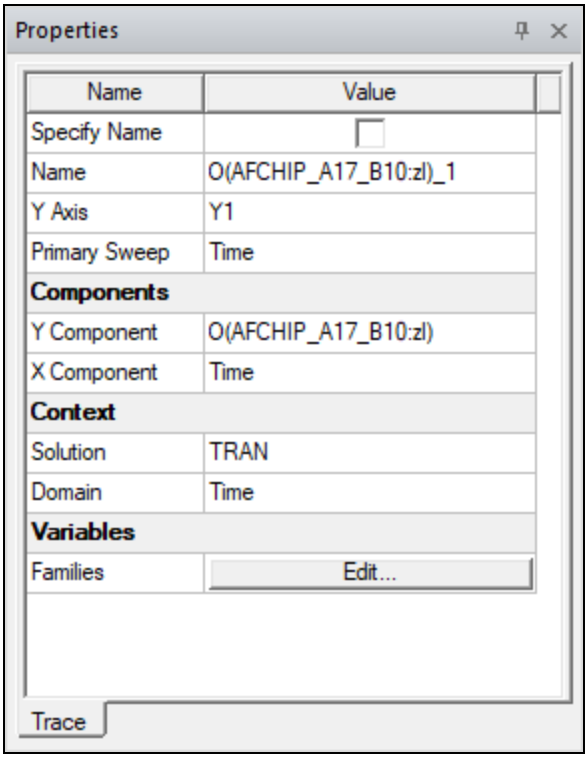
Editing Trace Properties

To edit trace properties or variables, select the trace in the Project Manager

The **Properties** window updates to display trace information.



From this window, you can rename the trace, edit component definitions, edit the context, and edit variables.

You can also modify the trace display. See: Changing Report Display.

Adding Data Markers to Traces

You can add markers to traces from the **Report2D** > **Marker** menu.

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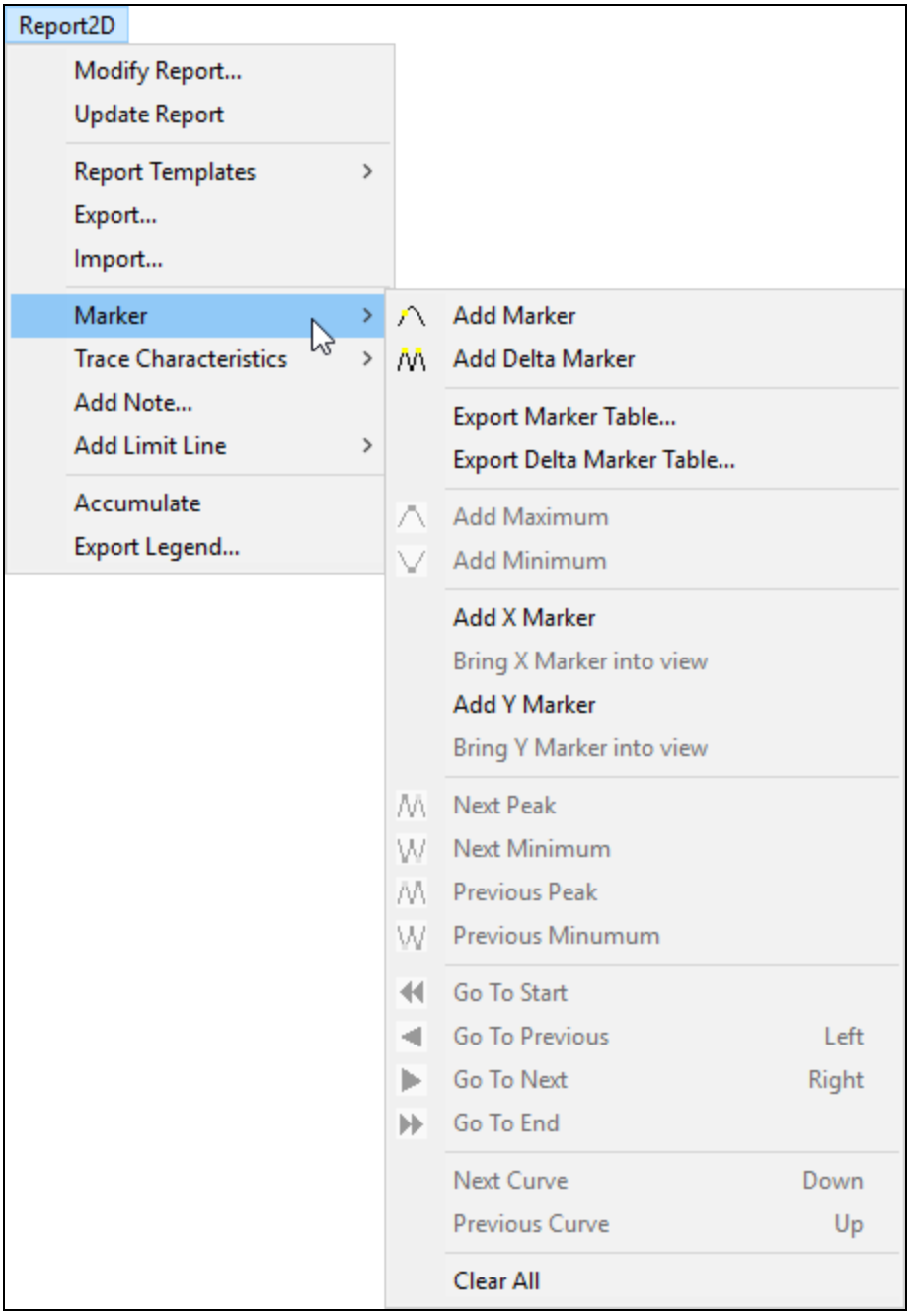

A marker appears as "m*N*" at the marked point, where *N* increments from 1 as you place additional markers. Each marker can be selected and has editable properties, including name, font, background, and color. As you place markers, one or more marker legends may appear, depending on the **View** > **Active View Visibility** settings for the legends. The main marker legend appears in the upper-left area of the plot, and lists all marker names and their X and Y

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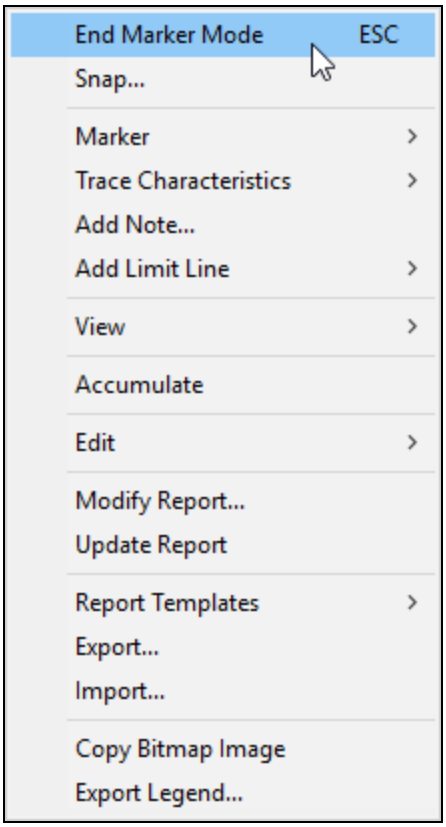
values in a table. You can control the number format for the table values via the Properties window.

When you enter Marker mode, the cursor arrow is accompanied by an "m" while a circle on the selected trace shows the current position for a potential marker.

To end Marker mode, right-click to display the shortcut menu and select **End Marker Mode**, or press **Esc**.



Available Marker commands include:

- **Add Marker** – allows you place a marker at an arbitrary point on a selected trace.
- **Add Delta Marker** – enters delta marker mode, placing a circle on the selected trace. Clicking on the trace sets an initial point and subsequent clicks on arbitrary points on the trace place additional markers until you leave marker mode. These markers have their own legend, which includes delta and slope information.
- **Export Marker Table** – exports a *.csv or *.tab file listing markers and their points on the X and Y axis.
- **Export Delta Marker Table** – exports a *.csv or *.tab file listing markers and their deltas, slopes, and inverted slopes.
- **Add Maximum** – places a marker at the maximum value on the selected trace.

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- **Add Minimum** – places a marker at the minimum value on the selected trace.
- **Add X Marker** – adds up to 10 movable markers at the origin of the plot with a vertical line rising from the X axis. Each added marker has its own color and editable properties. You can change the X marker value either by dragging or by editing the X marker property "X value." To move an X marker, click on the X label and drag it to an appropriate location. The label at the bottom of the line gives the X coordinate, and a flag on the vertical line identifies the Y coordinate on the trace. A **Lock Drag** trace property lets you lock the drag feature to leave the marker in place. X markers are cleared by the **Clear All** command.
- **Bring X Marker into View** – if an X Marker is not visible on the plot, allows you to bring it into view.
- **Add Y Marker** – adds up to 10 movable markers at the origin of the plot with a horizontal line extending from the Y axis. Each added marker has its own color and editable properties. You can change the Y marker value either by dragging or by editing the Y marker property "Y value." To move a Y marker, click on the Y label and drag it to an appropriate location. The label at the side of the line gives the Y coordinate, and a flag on the horizontal line identifies the Y coordinate on the trace. A **Lock Drag** trace property lets you lock the drag feature to leave the marker in place. Y markers are cleared by the **Clear All** command.
- **Bring Y Marker into View** – if a Y Marker is not visible on the plot, allows you to bring it into view.
- **Next Peak** – moves a selected marker on the next peak on a trace. You must exit marker mode and select a marker to enable this command.
- **Next Minimum** – moves a selected marker to the next minimum on a selected trace. You must exit marker mode and select a marker to enable this command.
- **Previous Peak** – moves a selected marker on the previous peak on a selected trace. You must exit marker mode and select a marker to enable this command.
- **Previous Minimum** – places a marker on the previous minimum on a selected trace. You must exit marker mode and select a marker to enable this command.
- **Go to Start** – moves the selected marker to the first data point.
- **Go to Previous** – moves the selected marker to the previous data point.
- **Go to Next** – moves the selected marker to the next data point.
- **Go to End** – moves the selected marker to the last data point.
- **Next Curve** – selects the next curve in the report, based on the order in the trace legend.
- **Previous Curve** – selects the previous curve in the report, based on the order in the trace legend.
- **Clear All** – clears all markers on a report except X Markers.

Adding Trace Characteristics

You can add characteristics to a selected trace or clear existing characteristics.

To add additional characteristics to a selected trace:

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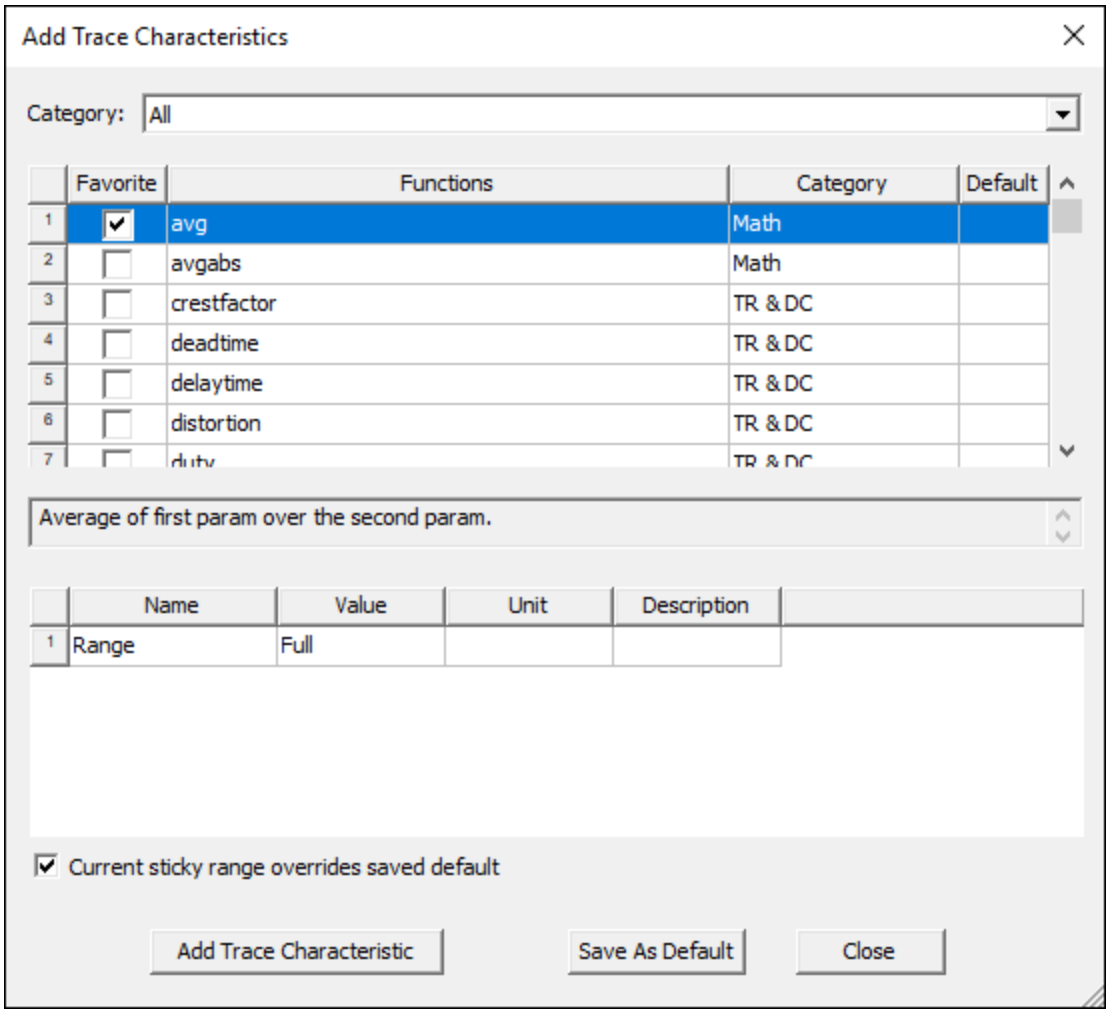
1. Select a trace in a report plot or legend.
2. Click **Report 2D** > **Trace Characteristics** > **All**.

   The **Add Trace Characteristics** window appears.



3. Use the **Category** drop-down menu to select a category. Then select an associated Function from the list to apply it.

   Available categories depend on the plot.

Category	**Functions for the Category**
Recent	Any recently used functions.
Favorites	Functions you have marked **Favorite** in the functions list.

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Category	Functions for the Category
Math	avg, avgabs, integ, integabs, max, mean, min, pk2pk, pkavg, ripple, rms, rmsAC, stddev, sum, variance, XAtYMax, XAtYMin, XAtYVal, XWidthAtYVal, YAtXMax, YAtXMin, YAtXVal
PulseWidth	pulsefall9010, pulsefront1090, pulsefront3090, pulsemax, pulsemaxtime, pulsemin, pulsemintime, pulsetail50, pulsewidth5050, pw_minus, pw_minus_avg, pw_minus_max, pw_minus_min, pw_minus_rms, pw_plus, pw_plus_avg, pw_plus_max, pw_plus_min, pw_plus_rms
Overshoot/Undershoot	overshoot, OvershootAbs, undershoot, UndershootAbs
TR & DC	crestfactor,deadtime, delaytime, distortion, duty, formfactor, fundamentalmag, risetime, settlingtime
Error	iae, ise, itae, itse
Period	per, pmax, pmin, prms
Radiation	lSidelobeX, lSidelobeY, rSidelobeX, rSidelobeY, xdb10Beamwidth, xdb20Beamwidth
TDR	Series_L_in_nH, Shunt_C_in_pF

Given a selected Function, and Category, the **Add Trace** window displays a text field that explains the Purpose of the function.

For a full list of functions and their definitions, see Function List.

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4. Some categories and functions call for you to specify one or two additional values in a table. You can save these values using the **Save As Default** button.
5. Click the **Add** button to add the specified characteristics to the Trace.

To remove existing trace characteristics:

1. Select a trace in a report plot or legend.
2. Click **Report 2D** > **Trace Characteristics** > **Clear All**.

Trace characteristics are cleared from the selected trace.

Function List

The value of a quantity being plotted depends upon its mathematical function, which you select from the **Trace** tab **Function** list in the **Report** window. The available, valid functions depend on the type of quantity (real or complex) that is being plotted. The function is applied to the quantity which is implicitly defined by all the swept and current variables (e.g., "S(11)" is the value of the S-parameter for every swept combination of variables (e.g., "height", "frequency")).

Some of these functions can operate along an entire curve. These are: min, max, integ, avg, rms, pk2pk, cang_deg and cang_rad.

You can select from the following functions in the **Trace** tab **Function** list or type them directly into the Y or X field, if appropriate.

abs	Absolute value of the simulation quantity which results in a number that is always positive.
acos	Arc cosine i.e. the inverse function of a cosine.
acosh	Inverse hyperbolic arc cosine.
ang	Magnitude of an angle.
ang_deg	Angle (phase) of a complex number, cut at +/-180.
ang_rad	Angle in radians.
arg	Argument of a complex number. It is the angle the complex number makes with the positive x axis. Same as **ang_deg**.
asin	Arc sine i.e. inverse function of sine.
asinh	Inverse hyperbolic sine.
atan	Arc tangent i.e. the inverse function of a tan.
atanh	Inverse hyperbolic tan.

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atan2	Two argument function. For non-0 x,y, the function returns the angle between the + x-axis and the given x,y coordinates.
avg	Returns the average of the values of the selected quantity. avg = (Area between the curve and the X-axis) / (X length of the curve)
avgabs	Returns the mean of the absolute value of the selected quantity.
bandwidth	Returns the 3dB bandwidth of the selected simulation quantity. For bandwidth, the calculation is based on 3dB below the maximum peak.
cang_deg	Cumulative angle (phase) of the first parameter (a complex number) in degrees, along the second parameter (typically sweep variable). Returns a double precision value cut at +/-180.
cang_rad	Cumulative angle of the first parameter in radians along a second parameter (typically a sweep variable). Returns a double precision value.
cmplx(*re*, *im*)	A complex number, where *re* is the real part and *im* is the imaginary part.
conjg	Conjugate of the complex number.
cos	Cosine.
cosh	Hyperbolic cosine.
crestfactor	Returns the crest factor (peak/RMS) for the selected quantity.
dB(x)	20*log10(|x|) to base 10.
dBc	Decibels relative to the carrier. It is the power ratio of the signal to a carrier signal. Gives the relative signal strength.
dBm(x)	10*log10(|x|) +30.
dBW(x)	10*log10(|x|).
dB10	10*log(|x|) to base 10.
dB10normalize	10*log [normalize(mag(x))].

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dB20	20*log(x) to base 10.
dB20normalize	20*log [normalize(mag(x))].
deadtime	Obtains the latest time when the qtyl is within a tolerance of zero.
delaytime	Obtains the time from zero to 50% of the target point.
degel	Conversion from degrees electrical to seconds with respect to Hz.
deriv	Derivative of a given parameter.
distortion	Returns the total distortion for the selected simulation quantity and an additional argument frequency, which is the frequency in Hz at which to calculate the fundamental RMS of the simulation quantity.
even	Returns 1 if integer part of the number is even; returns 0 otherwise.
exp	Exponential function (the natural anti-logarithm) of the simulation quantity.
formfactor	Returns the form factor (RMS/Mean Absolute Value) for the selected quantity.
fundamentalmag	Returns the RMS value of the fundamental frequency for the selected quantity, and an additional argument, Frequency, which specifies the fundamental frequency.
gaincrossover	Returns the gain crossover frequency (where the gain is 0 dB) of the selected simulation quantity in Hz.
gainmargin	Returns the gain margin in dB at the phase crossover frequency of the selected simulation quantity. It also requires a reference simulation quantity to which the measured quantity is compared and the AC magnitude and phase angle of the reference quantity. These are entered as the arguments Reference Channel, Base Source Magnitude, and Base Source Angle.

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iae	Returns the integral of the absolute deviation of the selected quantity from a target value that is entered via the additional argument.
if	if(cond_exp,true_exp, false_exp).
im	Imaginary part of the complex number.
int	Truncated integer function.
integ	Integral of the selected quantity. Uses trapezoidal area.
integabs	Absolute value of integral.
ise	Returns the integral of the squared deviation of the selected quantity from a target value that is entered via an additional argument.
itae	Returns the time-weighted squared deviation of the selected quantity from a target value that is entered via an additional argument.
itse	Returns the time-weighted squared deviation of the selected quantity from a target value that is entered via an additional argument. To use this function, you need to open the Add Trace Characteristics window and select the Error category.
j0	Bessel function of the first kind (0^{th} order).
j1	Bessel function of the first kind (1^{st} order).
jn	Bessel function of the first kind (nth order).
ln	Natural logarithm.
log	Natural logarithm (same as ln).
log10	Logarithm base 10.
lowercutoff	Returns the lower 3dB frequency of the selected simulation channel in Hertz.
lsidelobeX	The 'x' value for the left side lobe: the next highest value to the left of the max value.
lsidelobeY	The 'y' value for the left side lobe: the

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	next highest value to the left of the max value.
mag	Magnitude of the complex number.
max	Returns maximum value of the simulation quantity.
max_swp	Returns maximum value of a sweep.
max2	Maximum value of the two simulation quantities (e.g., **max2(a,b)** will plot maximum of **a** and **b** for a particular instance).
mean	Returns the average in the set of quantities selected. mean = sum(all y-value) / (number of y-values)
min	Returns the minimum value of the simulation quantity.
min_swp	Returns the minimum value of a sweep.
min2	Minimum value of the two simulation quantities (e.g., **min2(a,b)** will plot minimum of **a** and **b** for a particular instance).
mod	Returns the modulus or absolute value of the simulation quantity.
nint	Nearest integer.
none	Returns null value.
normalize	Divides each value within a trace by the maximum value of the trace. ex. normalize(mag(x)).
odd	Returns 1 if integer part of the number is odd; returns 0 otherwise.
overshoot	Calculates peak overshoot given a threshold value and number of evenly spaced points over entire time range.
peakgain	Returns the peak value of gain of the selected simulation quantity in dB.
peakgainfreq	Returns the frequency in Hz at which the peak gain of the selected simulation quantity occurs.

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polar	Coverts the complex number in rectangular co-ordinates to polar co-ordinates.
per	Returns the period of a simulation quantity.
phasecrossover	Returns the phase crossover frequency, at which the phase is -180 degrees, in Hz for the selected simulation quantity.
phasemargin	Returns the phase angle in degrees at the gain crossover frequency of the selected simulation quantity.
pk2pk	Peak to peak. Difference between max and min of the first parameter over the second parameter. Returns the peak-to-peak value for the selected simulation quantity.
pkavg	Returns the ratio of the peak to peak-to-average for the selected quantity.
pmax	Maximum period of the selected simulation quantity.
pmin	Minimum period of the selected simulation quantity.
pow	Raises x to the power of y; pow(x,y).
prms	Period Root Mean Square.
pulsefall9010	Returns the pulse fall time of the selected quantity according to the 90%-10% estimate.
pulsefront1090	Returns the pulse front time of the selected quantity according to the 10%-90% estimate.
pulsefront3090	Returns the pulse front time of the selected quantity according to the 30%-90% estimate.
pulsemax	Returns the pulse maximum from the front and tail estimates for the selected quantity.
pulsemaxtime	Returns the time at which the maximum pulse value of the selected quantity is reached.

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pulsemin	Returns the pulse minimum from the front and tail estimates for the selected quantity.
pulsemintime	Returns the time at which the minimum pulse value of the selected quantity is reached.
pulsetail50	Returns the pulse tail time of the selected quantity from the virtual peak to 50%.
pulsewidth5050	Returns the pulse width of the selected quantity as measured from the 50% points on the pulse front and pulse tail.
pwl	Piecewise Linear.
pwl_periodic	Piecewise Linear for periodic extrapolation on x.
pwlx	Piecewise Linear x with linear extrapolation on x.
pw_minus	Pulse width of the first negative pulse.
pw_minus_avg	Returns the average of the negative pulse width input stream.
pw_minus_max	Returns the maximum pulse width of the negative pulse of input stream.
pw_minus_min	Returns the minimum pulse width of the negative pulse of input stream.
pw_minus_rms	RMS of the negative pulse width input stream.
pw_plus	Pulse width of the first positive pulse.
pw_plus_avg	Average of the positive pulse width input stream.
pw_plus_max	Max. Pulse width of the positive pulse of input stream.
pw_plus_min	Min. Pulse width of the positive pulse of input stream.
pw_plus_rms	RMS of the positive pulse width input stream.
re	Real part of the complex number.
rect	Converts the complex number in polar to rectangular co-ordinates.
rem	Returns the fractional part of a decimal

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	number such that rem(x) = x-int(x).
ripple	Returns the ripple factor (AC RMS/Mean) for the selected quantity.
risetime	Obtains the time taken to go from 10% to 90% of target point.
rms	Returns the root mean square value of the selected quantity.
rmsAC	Returns the AC RMS for the selected quantity.
root	nth root function.
rSidelobeX	Returns the X value of right side-lobe occurrence.
rSidelobeY	Returns the Y value of right side-lobe occurrence.
settlingtime	Returns the latest time at which the value of the selected simulation quantity fell outside its tolerance band. The target value of the quantity and the +/- bandwidth of the tolerance band are the additional args.
sgn	Sign extraction.
sin	Sine.
sinh	Hyperbolic sine.
slidingmean	Returns the moving average value of the selected simulation quantity (specified by the first argument). The average is calculated over a period (specified by the second argument).
slidingrms	Returns the moving RMS value of the selected simulation quantity (specified by the first argument). The RMS value is calculated over a period (specified by the second argument).
sqr	Square of the selected simulation quantity.
sqrt	Square root of the selected simulation quantity.
stddev	Returns the standard deviation of given values.

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sum	Returns the sum of the given values.
tan	Tangent.
tanh	Hyperbolic tangent.
undershoot	Calculates peak undershoot given a threshold value and number of evenly spaced points over entire time range.
uppercutoff	Returns the upper 3dB frequency of the selected simulation channel in Hz.
variance	Calculates the variance of the given values.
XAtYMax	Threshold crossing time: report first time (x value) at which an output quantity crosses YMax.
XAtYMin	Threshold crossing time: report first time (x value) at which an output quantity crosses a user definable threshold.
XAtYVal	Returns the X value at the first occurrence of Y value.
XWidthAtYVal	Returns the X width between the first 2 occurrence of Y value.
xdb10Beamwidth	Width between left and right occurrences of values 'x' db10 from max. Takes 'x' as argument (3.0 default). To use this function, you need to open the Add Trace Characteristics window and select the Radiation category.
xdb20Beamwidth	Width between left and right occurrences of values 'x' db20 from max. Takes 'x' as argument (3.0 default). To use this function, you need to open the Add Trace Characteristics window and select the Radiation category.
YAtXMax	Returns the X value at maximum value of Y.
YAtXMin	Returns the Y value at minimum value of X.
YAtXVal	Returns the Y value at the first occurrence of X value.

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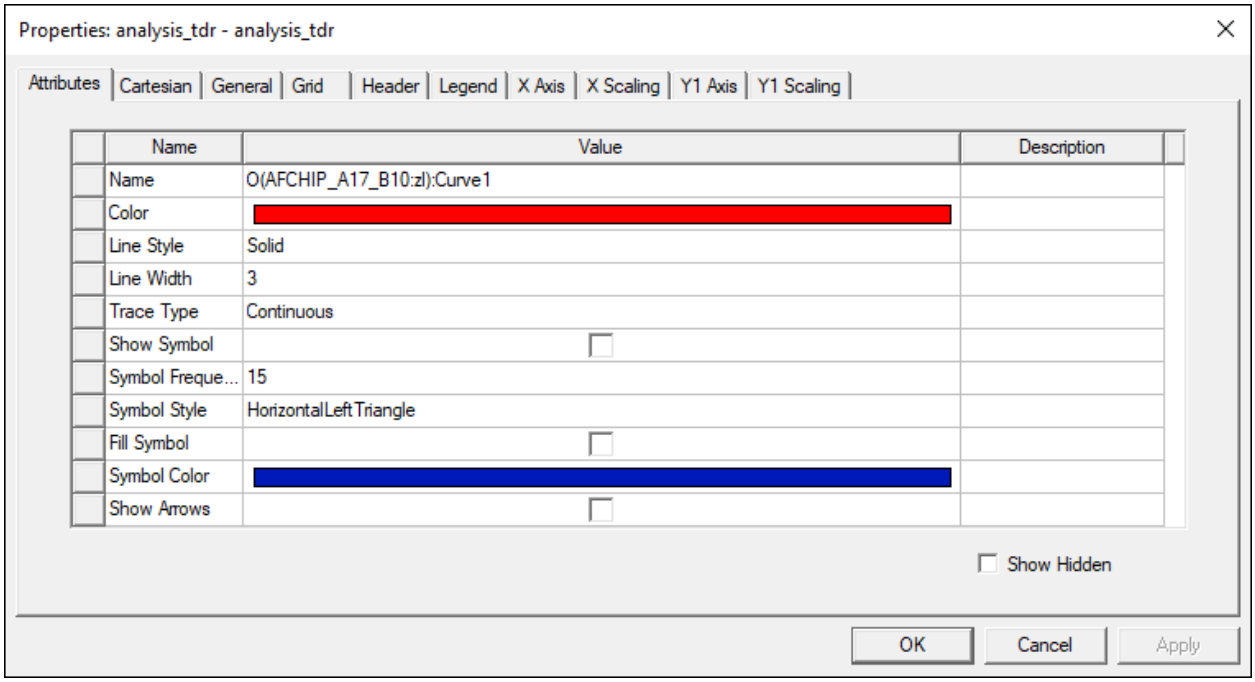
y0	Bessel function of the second kind (0^{th} order).
y1	Bessel function of the second kind (1^{st} order).
yn	Bessel function of the second kind (nth order).

Changing Report Display

To modify the appearance of a report, or the display properties an object in a report.

1. Open the report you want to modify.
2. Select an editable object in the report (x-axis, legend, etc.) to view its properties in the docked **Properties** window. To open a floating **Properties** window, double-click an object or click **View** > **Workspaces** > **Properties**.



Properties window tabs include:

- **Attributes** – allows you to edit the report's trace type, line color and style, and symbol and arrow preferences.
- **Cartesian** – allows you to set the display of the x-axis scrollbar.
- **General** – allows you to set the background and plot area colors, enable or disable y-axis stripes, and set number formatting.
- **Grid** – allows you to set grid visibility and colors.

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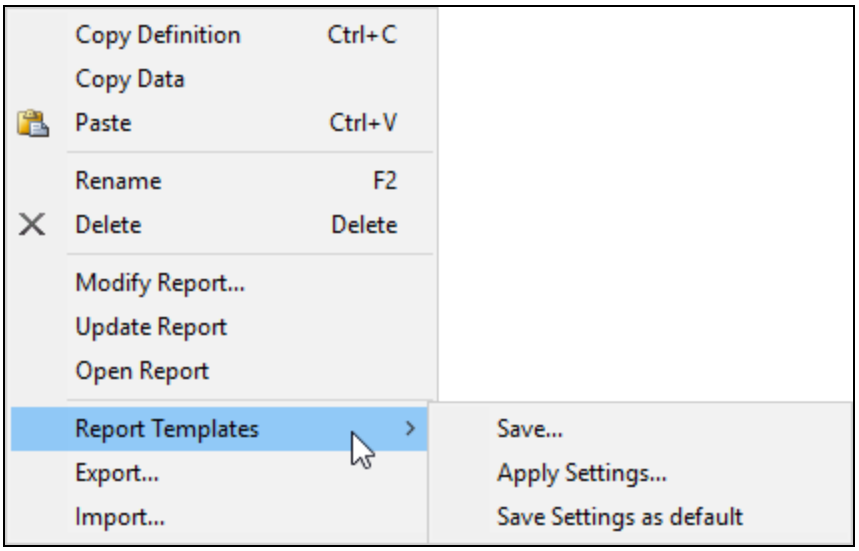
- **Header** – allows you to select fonts for the report's title and subtitle, and decide whether to display a company name and the design name.
- **Legend** – allows you to select which elements display in the legend, as well as their fonts and colors.
- **X Axis** – allows you to set the x-axis display name, units, color, window and field width, and field precision. You can also
- **X Scaling** – allows you to modify how the x-axis scales.
- **Y Axis** – allows you to set the y-axis display name, units, color, window and field width, and field precision.
- **Y Scaling** – allows you to modify how the y-axis scales.

3. Click **Apply** to apply changes.
4. Click **OK** to close the **Properties** window.

To save any report format as a template, right-click the report in the Project Tree and select **Report Templates** > **Save**.

To apply a previously saved template, right-click the report in the Project Tree and select **Report Templates** > **Apply**.

To make your settings the default for all reports, right-click the report in the Project Tree and select **Report Templates** > **Save Settings as Default**.



Limit Lines in Cartesian Plots

Limit lines are simple graphical representation of constraints on XY plots. These are modeled as a sequence of XY point pairs, or as offsets from a selected curve. You can designate a single limit line to delineate an upper limit, or two lines to delineate upper and lower limits, or upper and lower offset lines simultaneously.

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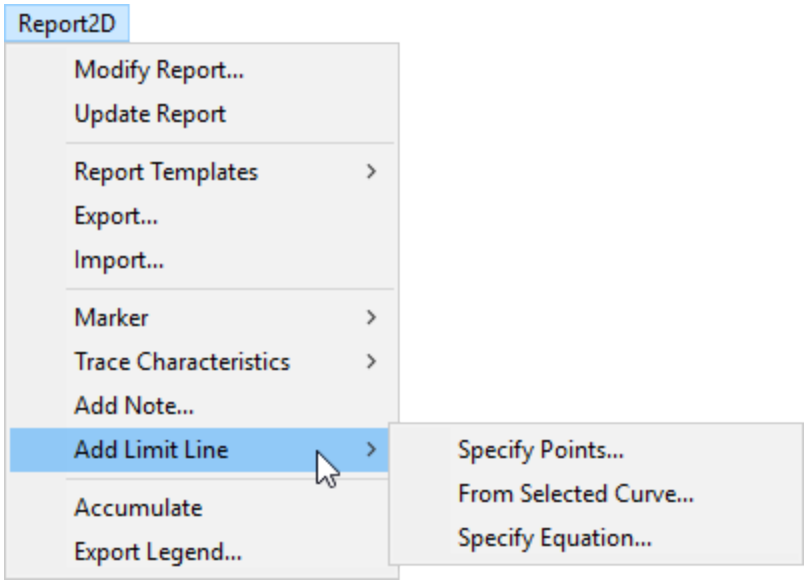
You can control the display properties of the line including color and hatch width in pixels. These lines are available only on XY plots (and not on the XY-like plots: bode, stacked etc).

> **Note:**
>
> Limit lines are available only on Rectangular (XY) plots, not on XY-like plots such as Bode or Rectangular Stacked.

To create a limit line:

1. Click **Report2D** > **Add Limit Line** or right-click on an XY plot and select **Add Limit Line...** from the shortcut menu.



You can **Specify Points**, **Specify Equation**, or create limit lines **From a Selected Curve**.

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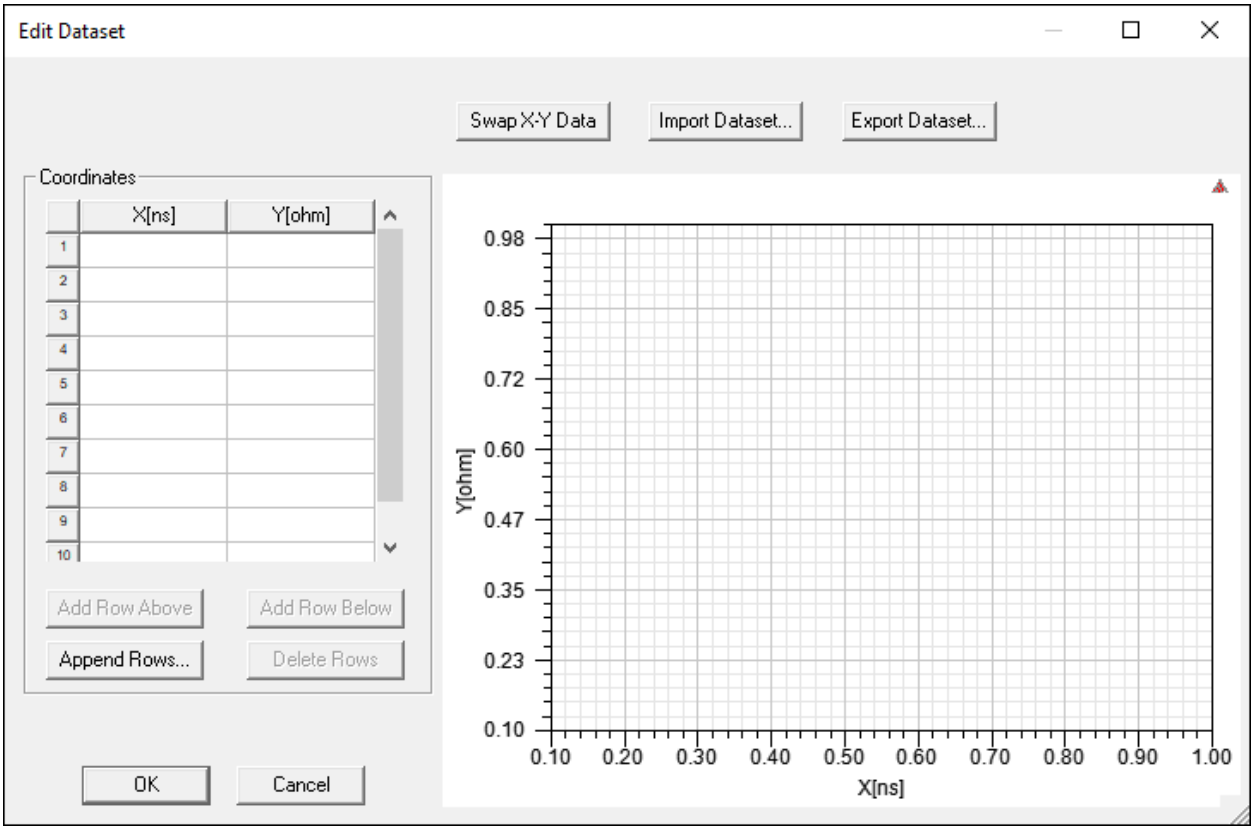
- Select **Specify Points** to open the **Edit Dataset** window to specify the points.



You can use the Edit Dataset window to enter EY values directly, import XY values from a *.tab file, or export the dataset to a file.

If you require additional data points, you can use the buttons to **Append Rows** to the Coordinates table. If you select a row in the **Coordinates** table, you can then use the buttons to **Add Row Above**, **Add Row Below** the selected rows, or **Delete Rows**.

Shift+click to select multiple adjacent rows, or **Ctrl+click** to select any rows for deletion.

> **Note:**
>
> Each limit line is associated with a particular Y axis (because it has to be scaled the same way as all the curves associated with the axis, follow its log/linear scale and so on). This Y axis association defaults to the first available Y axis when the limit line is created. However, if the plot contains multiple Y axes, it can be associated with a different Y axis later via its properties tab.

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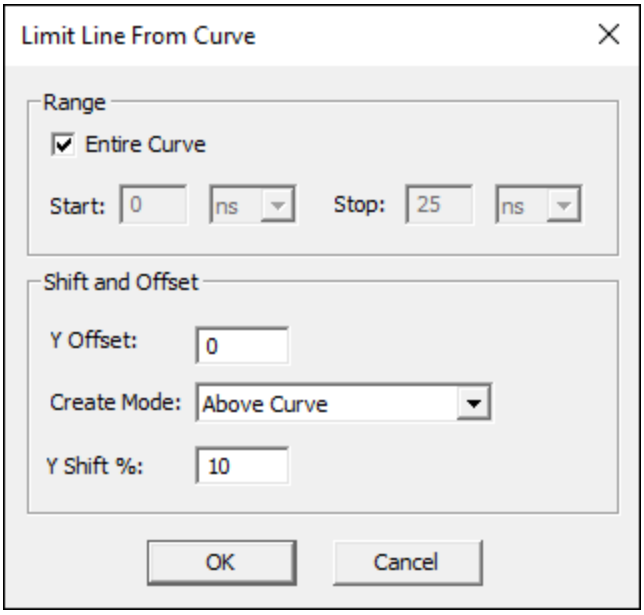
- Select **From Selected Curve** to open the **Limit Line From Curve** window.

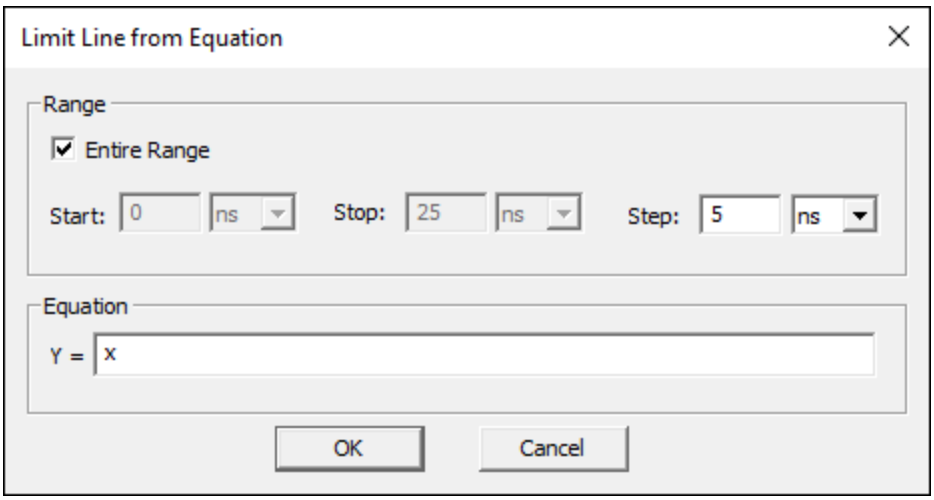


You can use the **Range** area to create a limit line with a range using either the **Entire Curve**, or a specified **Start** and **Stop**.

The **Shift and Offset** area allows you to select shift and offset relative to Y, either as a Y Offset value or as a Y Shift percentage.

Create Mode options are: **Above Curve**, **Below Curve**, or **Above and Below Curve**.

- Select **Specify Equation** to open the **Limit Line from Equation** window.



You can use the **Range** area to create a limit line with a range using either the **Entire Curve**, or a specified **Start** and **Stop**.

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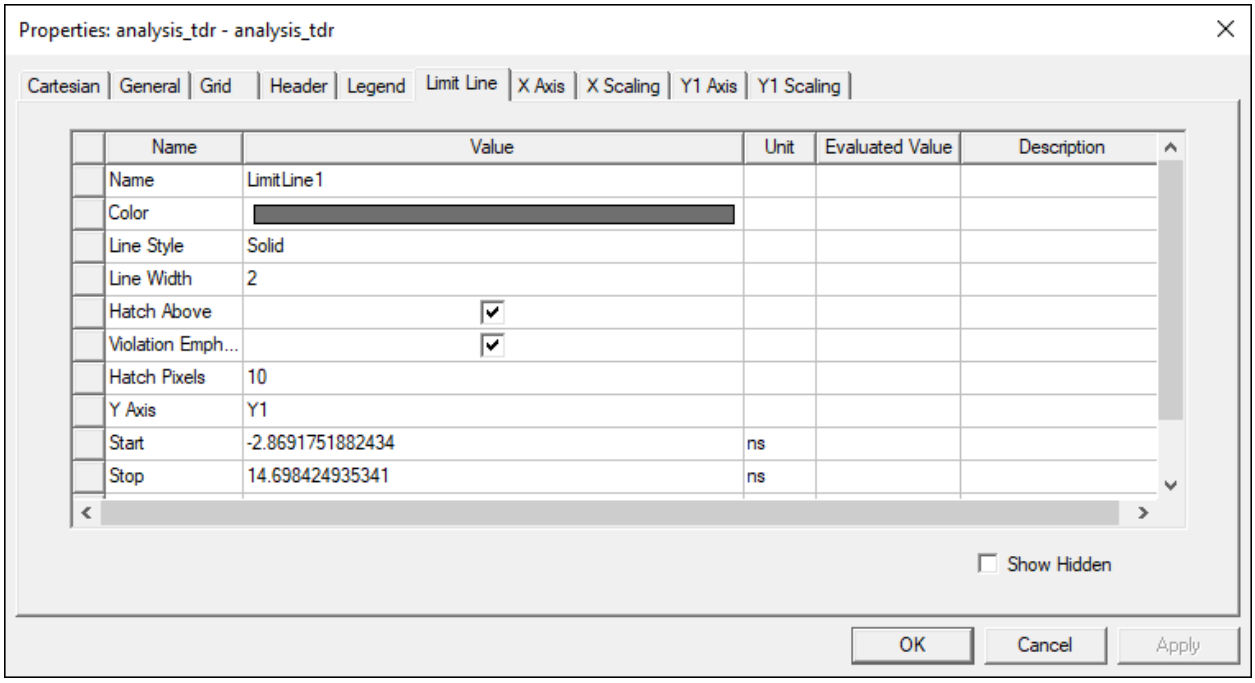
Use the **Equation** field to type the equation from which to create the limit line.

2. Click **OK**.

   The limit line is added to the plot and divides the plot into two regions within the context of its length. By default, the upper region is hatched to designate constraint violation.

3. You can select the limit line in the plot to edit its properties via the **Limit Line** tab.



See: Changing Report Display.

4. If you add a second limit line, you can designate it as hatch below by clearing **Hatch Above** to produce a tunnel marking upper and lower constraints.

   The following example shows the a limit line from curve plot, where the Hatch Above property for the lower limit line has been unchecked.

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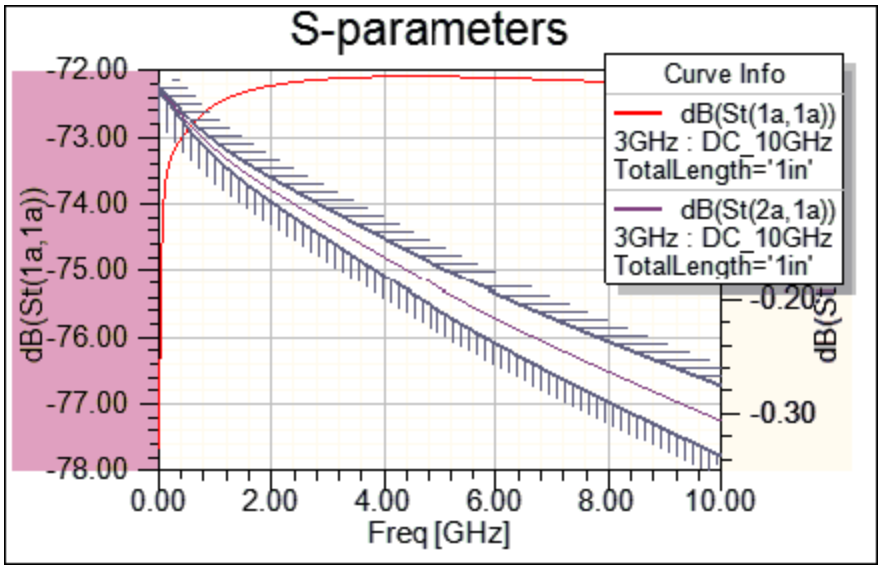
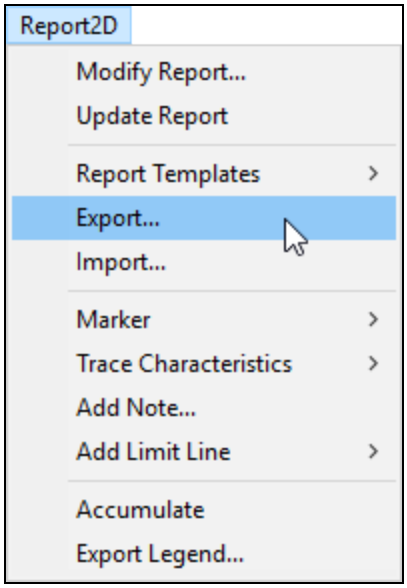


Exporting Reports

Reports can be exported from Ansys Electronics Desktop in a variety of data formats, and as graphics.

To export a report:

1. Click **Report2D** > **Export...**



The **Export Report** window appears.

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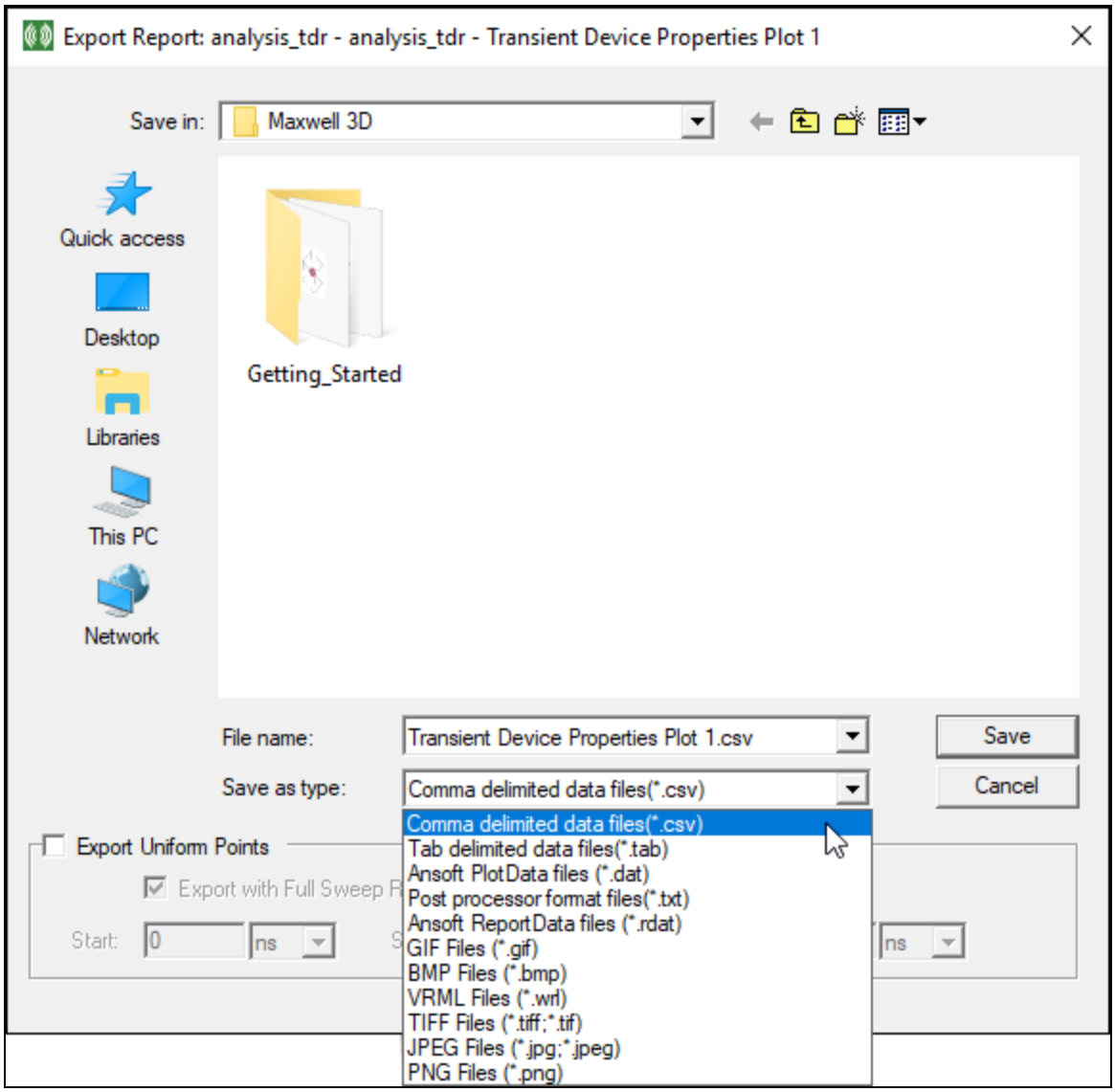

2. Use the **File Name** field to name your file for export.
3. Use the **Save as Type** field to select a file type.
4. Some formats display an **Export Uniform Points** check box. Selecting this will generate a file containing the points for the given start, stop, and step at the given frequencies.
5. Graphics formats display an **Image Export Options** area, where you can select the image size.

6. Click **Save** to export your report to the selected location.

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Sweeping a Variable in a Report

In SIwave, a swept variable is a variable that typically has more than one value. You can plot any calculated or derived quantity against one or more of the swept variable's values.

For large projects or projects with many variables, you may obtain faster post processing before generating a solution by selecting which variables function as Sweep variables. Only the variables with Sweep enabled are indexed for post processing.

To specify the swept variable values to plot a selected quantity against:

1. From the **Report** window , select the variable from the **X** (Primary Sweep) drop-down menu.
2. To modify the values that will be plotted for a variable:
   a. Click the **[...]** button on the **X** (Primary Sweep) line of the **Report** window to display a pop-up list of possible values.
   b. Select **All Values** or click the **Edit** button to display a window that lets you specify the sweeps to use.

   All of the selected variable's values will be plotted.

To sweep values across a distance:

1. If you are plotting a field quantity along a line, define a polyline in the problem region.
2. From the **Report** window, click the line geometry of interest in the **Geometry** list.
3. Specify the quantities you want to plot along the axes.
4. For the **X** (Primary Sweep), select the **Distance** variable.

   The values at which the selected quantity or quantities will be plotted are listed to the right.

   By default, a post-processing polyline object is divided into 100 equally spaced points.
5. For Near field, to plot the selected quantity or quantities at every point on the line, select **All Values**, or clear All Values and select the point values on which you want to plot.

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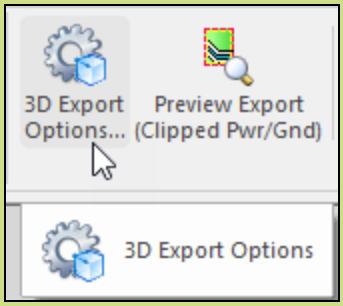
11 - Exporting 3D Models

To enable accurate analysis of the fields surrounding a complex design, SIwave can export a 3D geometric model to MCAD solvers such as HFSS for MCAD, Q3D, and Ansys Workbench.

Note:

Configure most options for solid models from the **Export Options** window. Refer to Setting Solid Model Options.



This section explains how to export a 3D model in various formats:

- Exporting a Solid Model
- Exporting a Parasolid Solid Model
- Exporting an HFSS Project
- Exporting an HFSS 3D Layout Project
- Exporting a Maxwell Project
- Exporting a Q3D Project

Export Options

Before exporting 3D models, you may want to change certain configuration settings.

In this section, you will learn about:

- Setting General Export Options
- Setting Solid Model Options

Setting General Export Options

You can set the number of facets for pads, antipads, solderballs, vias, and bondwires.

To set export options:

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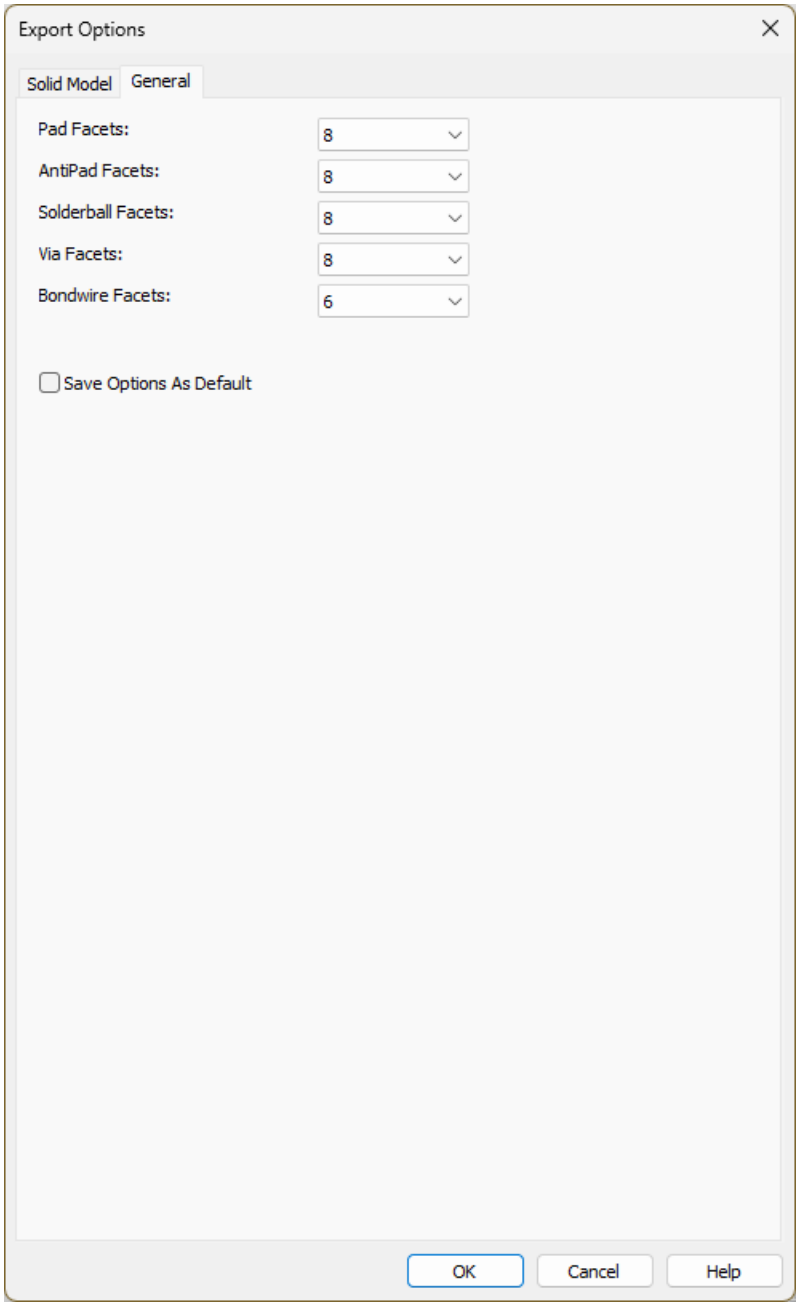
1. Click **Export**.
2. From the **3D Exports** area, click **3D Export Options** to open the **Export Options** window.
3. Click the **General** tab.



4. Use the **Facets** drop-down menus to select the number of facets for each component type (i.e., Pads, Antipads, Solderballs, Vias, and Bondwires).

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> **Note:**
>
> If **Set Ansys Mechanical Defaults** was checked in the **Solid Model** tab, all numerical values are set to **True Cylinder**.

5. If appropriate, check the **Save Options As Default** box.
6. Click **OK** to save configuration settings.

Setting Solid Model Options

To set solid model options:

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1. Click **Export**.

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2. From the **3D Exports** area, click **3D Export Options** to open the **Export Options** window.

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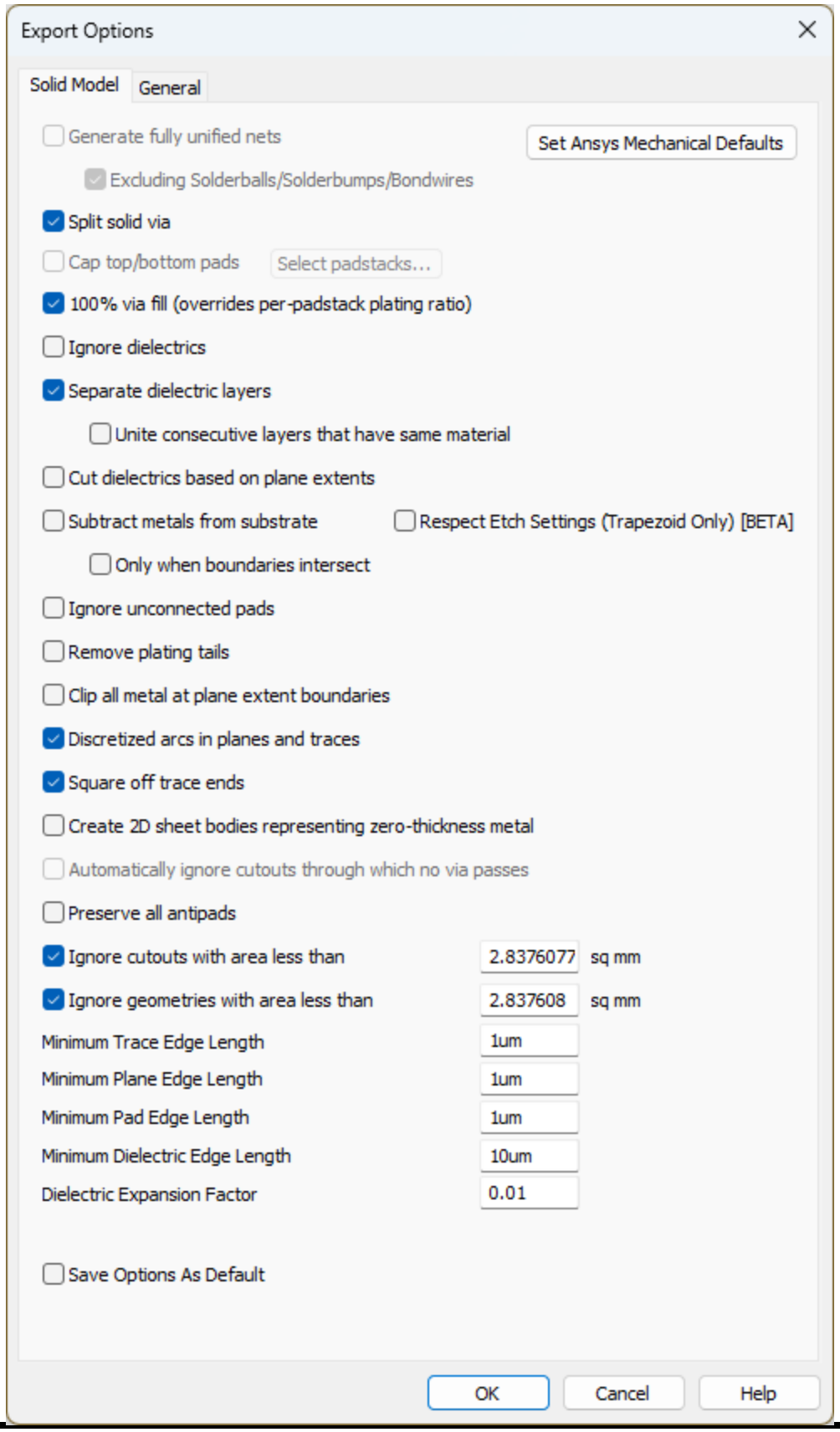

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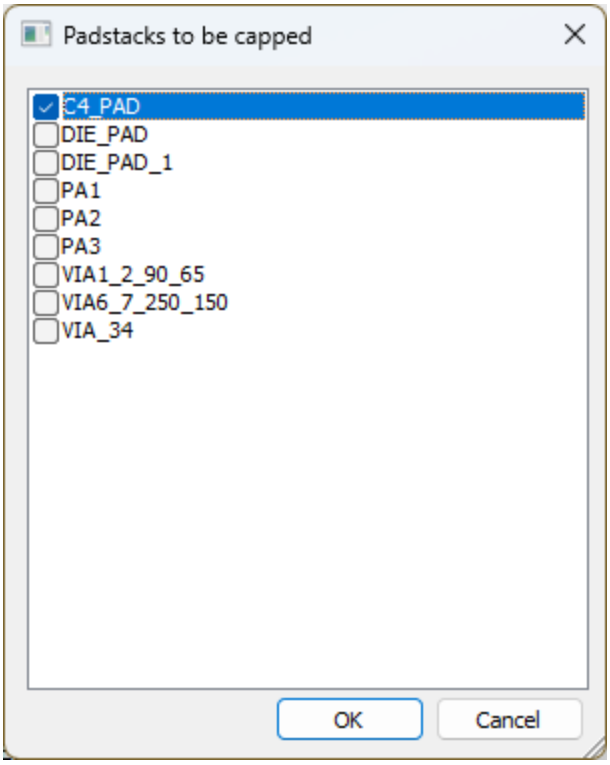
3. To set the optimal settings for Ansys Mechanical, click **Set Ansys Mechanical Defaults**, or check boxes and/or enter values in the adjacent fields from the following options:
   - **Generate fully united nets** — unites all solid objects in a net into a single solid object. If conductivities of the different metal layers are similar, this option reduces model complexity and solution time. ALinks sets the material of united nets to copper.
   - **Excluding Solderballs/Solderbumps/Bondwires** — unites all objects of each net, excluding solderballs, solderbumps and bondwires.

     Note:

     Check the **Generate fully united nets** box to activate **Excluding Solderballs/Solderbumps/Bondwires**, then check the **Excluding Solderballs/Solderbumps/Bondwires** box to select it.

   - **Split solid via** — cuts the top and bottom pads of all vias and hastens mesh generation.
   - **Cap/top bottom vias pads** — the top and bottom pads of all vias associated with the selected padstacks are capped for protection and to ensure a flat mounting surface. Click **Select padstacks** to open the **Padstacks to be capped** window, then check the box next to one or more padstacks, as necessary. Click **OK** to close the window.



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> **Note:**
>
> Uncheck the **Split solid via** box to activate **Cap/top bottom vias pads**, then check the **Cap/top bottom vias pads** box to select it.

- **100% via fill** — ignores the hole size and fills the via completely.
- **Ignore dielectrics** — omits dielectric layers from the exported 3D model. Check the **Ignore dielectrics** box to significantly reduce solution time if capacitance values are not required.
- **Separate dielectric layers** — creates a separate block for each dielectric layer. Do not check the **Separate dielectric layers** box if the dielectric constants of the dielectric layers in the stackup are similar.
- **Unite consecutive layers that have the same material** — unites consecutive layers of the same material.

> **Note:**
>
> Check the **Separate dielectric layers** box to activate **Unite consecutive layers that have the same material**, then check the **Unite consecutive layers that have the same material** box to select it.

- **Cut dielectrics based on plane extents** — if plane extents are defined, the resulting dielectric(s) in the solid model will have that shape. By default, the dielectric layers are exported as rectangular objects that encompass the metal.
- **Subtract metals from substrate** — explicitly subtracts the metal objects from the dielectric(s), as in the previous versions. If this option is unchecked, metals are not explicitly subtracted from the dielectric. This speeds up the solid model generation process.
- **Only when boundaries intersect** — adds this condition to **Subtract metals from substrate**.
- **Respect Etch Settings (Trapezoid Only)** — check this box to export solid models with the cross-section etching values set in the Trace Cross Section window.

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> **Note:**
>
> Users can create conformal dielectric coatings (i.e., modeling solder masks) that cover the top and bottom metal layers in the design stackup.
>
> To create and export a conformal coat, first create the environment variable `SIWAVE_3D_EXPORT_ENABLE_CONFORMAL_COAT_GENERATION` and enter the value `1`. The **Generate Conformal Layers** check box appears under the **Respect Etch Settings (Trapezoid Only)** check box. Checking the box creates the conformal coat, which can import into **Electronics Desktop**.
>
> *As of version 2024 R2, this feature is still experimental and results may be unexpected.*

- **Ignore unconnected pads** — omits any via pads that do not connect to a plane or trace.
- **Remove plating tails** — ignores traces that are outside the package and are removed during manufacturing.
- **Clip all metal at plane extent boundaries** — cuts the selected net that extends past the plane extent boundary. Only the portion within the specified plane extent is exported.
- **Discretized arcs in planes and traces** — creates chords and break the arcs into smaller fragments.
- **Square off trace ends** — allows the ends of the traces to not have rounded ends upon export. The round trace ends are chopped off.
- **Create 2D sheet bodies representing zero-thickness metal** — generates solid models containing 2D sheet bodies of zero thickness (instead of 3D bodies of finite thickness) representing geometry on metal layers. Set the layer thickness to zero for any geometry to be modeled as a 2D sheet (i.e., navigate to **Edit** > **Layer Stack**). Models containing only 2D sheet metal solve much faster than models containing full 3D metal.

> **Note:**
>
> Only available for HFSS and solid model exports.

- **Automatically ignore cutouts through which no via passes** — ignores the cutouts that do not have any via passing through them.
- **Preserve all antipads** — includes the antipads associated with unselected nets while exporting a 3D model. Sometimes they need to be preserved regardless of whether the associated nets are selected.
- **Ignore cutouts with area less than** — check this box and enter a value to ignore voids and/or cutouts smaller than specified.
- **Ignore geometries with area less than** — check this box and enter a value to omit any geometry from the solid model with an area smaller than specified.

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- **Minimum Edge Length (Trace Plane, Pad, and Dielectric)** — enter values in any/all of these four fields remove small, inappropriate faces from dielectric objects that may cause problems in the meshmaker or the solvers. Any face smaller than the specified value will be omitted from the solid model. Specify the units from the following: **um**, **mm**, **mil**, **cm**, and/or **in**.
- **Dielectric Expansion Factor**— enter a value that will increase the size of the resulting dielectric (e.g., enter **0** and the dielectric is exported exactly as the plane extent. Enter **0.1** and the dielectric shape is enlarged by 10% of the plane extent. A value of **0.2** enlarges the dielectric shape it by 20% of the plane extent.). The existence of a board outline will stop the dielectric from being expanded beyond that boundary.

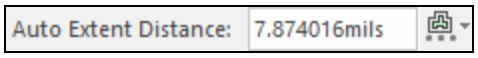
4. If appropriate, check **Save Options As Default**.
5. Click **OK** to save configuration settings.

> **Note:**
>
> If using a *.config file to set 3D export options, set environment variables to `1` to select check boxes and `0` to deselect them (e.g., the **100% Via Fill** check box is selected by placing `TOTAL_VIA_FILL = 1` in the *.config file).

Exporting a Solid Model

To export selected power and ground traces from the open model as a 3D Model geometry file:

1. Import the design (PCB, Package, or both).
2. Select the power or ground nets to be exported (see: Nets Workspace).
3. Click **Home**. From the Draw Geometry area, set the **Auto Extent Distance**.



4. Use **Auto Extent Distance** drop-down menu to apply an extent. The extent appears on the design.
5. Click **Export**. From the 3D Exports area, click Preview Export (Clipped Pwr/Gnd). The clipped region displays.
6. To return to the original view, click **Back to Unclipped Design**.
7. To export the 3D model, following the instructions for exporting HFSS, Q3D, or Parasolid Solid Model.

Exporting a Parasolid Solid Model

To export the model as a Parasolid Solid Model (*.x_b):

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1. Click **Export**.
2. From the 3D Exports area, click **Export Parasolid Solid Model**.

   A drop-down menu appears, listing version numbers.

3. Select the version you would like to export.

   The **Save As** window appears.

4. Browse to the directory where the project will be saved and enter a file name for the exported project.
5. Click **OK** to export the file.

Exporting ANF Files

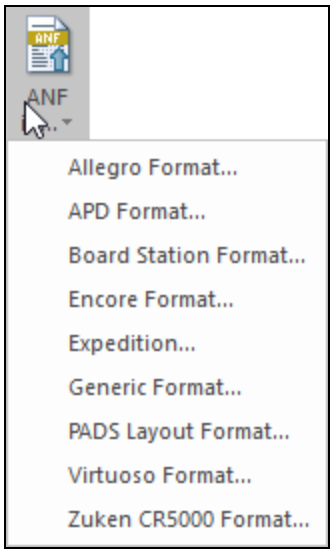
ANF files created in SIwave can be exported to other software that can read this format (e.g., Turbo Package Analyzer).

Options to export to other compatible software are available only if you have the required licenses. If you do not have valid licenses for these software packages, the options will be grayed out.

To export a file:

1. Click **Export**.
2. From the Ansys EDA Layouts area, click **ANF in**.

   A drop-down menu appears.



3. Select the format you want to export.

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The **Select Ansoft Neutral File name for export** window appears.

4. Browse to the directory where the project will be saved and enter a file name for the exported project.
5. Click **Save** to export the file.

   The ANF is exported in encrypted format.

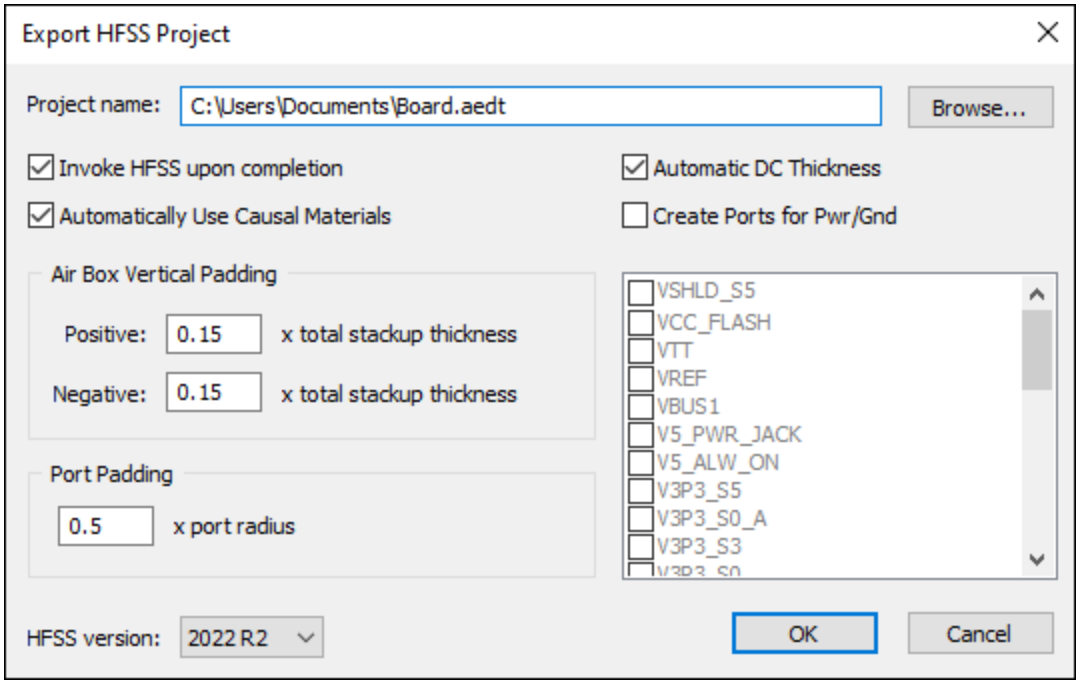
   If you choose Generic Format, the ANF is exported as a text file and is editable.

Exporting an HFSS Project

To export the model as an HFSS project (*.aedt):

1. Click **Export**.
2. From the 3D Exports area, click **Export to HFSS 3D**.

   The **Export HFSS Project** window appears.



3. From the **Project Name** field, enter a path and name for your project, or click **Browse** to select one.
4. Check options as appropriate:
   - **Invoke HFSS upon completion** – starts HFSS once the project has been exported.
   - **Automatically use Causal Materials** – enables HFSS to automatically use causal materials.

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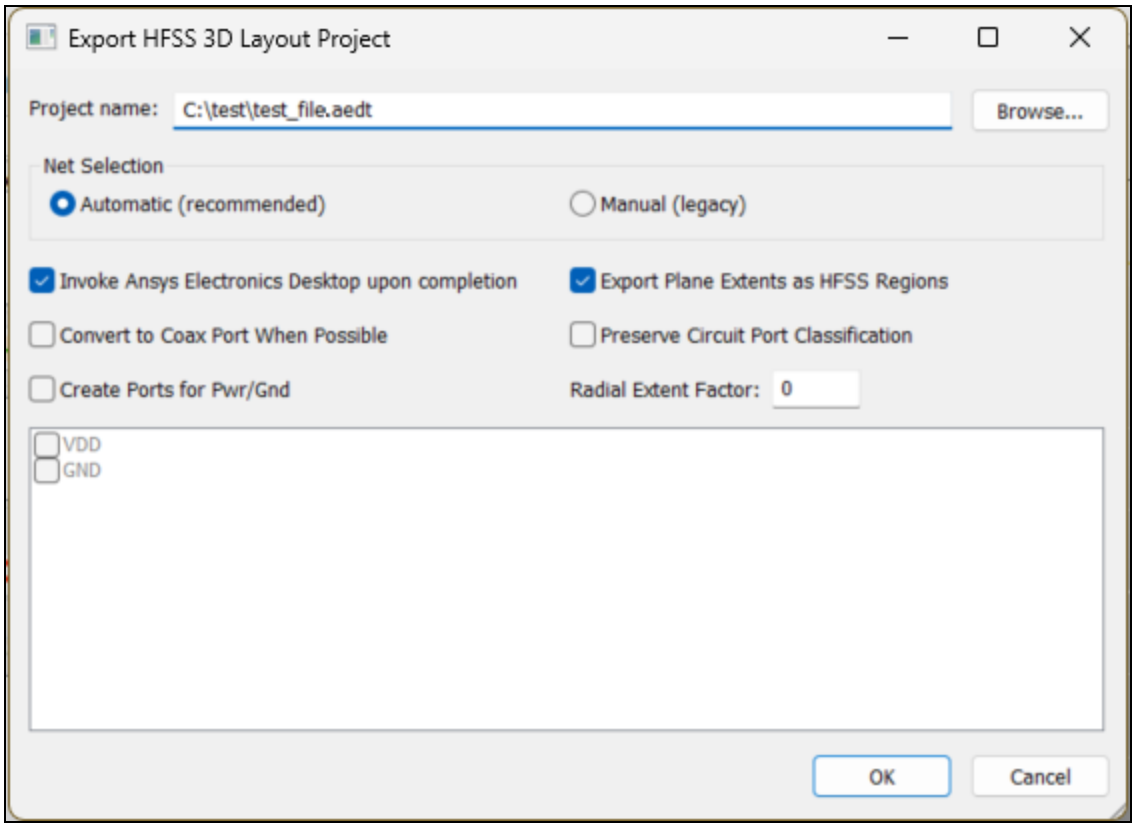
- **Automatic DC Thickness** – enables HFSS to automatically define DC thickness.
- **Create Ports for Pwr/Gnd** – when selected, you can use the check boxes below to select power/ground nets from which to create ports.

5. From the **Air Box Vertical Padding** area, specify the surrounding air box thickness. Air box thickness is given as a factor of the total layer thickness.
6. From the **Port Padding** area, specify the port padding.
7. Use the **HFSS version** drop-down menu to select the version of HFSS you wish to export.
8. Click **OK** to export the file.

Exporting an HFSS 3D Layout Project

To export the model as an HFSS 3D Layout project (*.aedt):

1. Click **Export** to open the **Export HFSS 3D Layout Project** window.



2. From the Ansys EDA Layouts area, click **HFSS 3D Layout**.
3. From the **Project Name** field, type a the destination folder and name for your file, or click **Browse** to select a directory.

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4. From the **Net Selection** area, select one of the two radio buttons:
   - **Automatic** – selects nets based on the same algorithm used for determining nets to include in an SIwave SYZ simulation (also includes any nets where coaxial ports are automatically generated).
   - **Manual** – selects nets using the same criteria used for HFSS 3D Layout simulations in release 2015 (uses the same logic as the MCAD exports).
5. If appropriate, check any/all of the following boxes:

- **Invoke Ansys Electronics Desktop upon completion** – after the **HFSS 3D Layout** project is exported, **Electronics Desktop** opens with the new project active
- **Convert to Coax Port When Possible** – circuit ports with a positive terminal connected to a pin and a negative terminal connected to a pin group on the same component are exported as coaxial ports
- **Create Ports for Pwr/Gnd** – creates ports on nets selected from the table following the check box.
- **Export Plane Extents as HFSS Regions** – export the design's plane extents as HFSS regions in the HFSS 3D Layout project
- **Preserve Circuit Port Classification** – all ports are exported as circuit ports, ignoring other selected options (e.g., **Convert to Coax Port When Possible**)

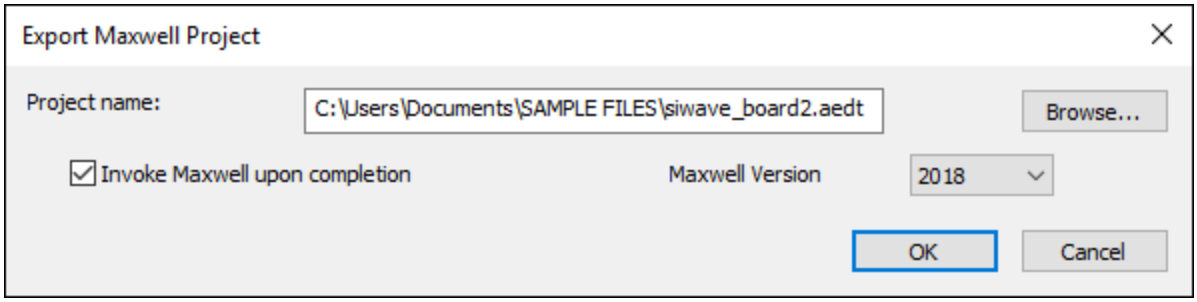
6. Enter a value in the **Radial Extent Factor** field. The radial extent factor sets the radius for the port geometry of coaxial ports. Entering **0** extends the radius of the pin as much as appropriate while creating port geometry, **1** creates port geometry that does not exceed the radius of the pin, and **2** creates port geometry twice the radius of the pin)
7. Click **OK** to create the project.

Exporting a Maxwell Project

To export the model as a Maxwell project (*.aedt):

1. Click **Export**.
2. From the 3D Exports area, click **Export to Maxwell 3D**.

   The **Export Maxwell Project** window appears.



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3. From the **Project Name** field, type the path and file name for export, or click **Browse** to select a location.
4. Use the **Maxwell Version** drop-down menu to select the version of Maxwell.
5. If appropriate, check the **Invoke Maxwell upon completion** check box to start Maxwell when the project has been exported.
6. Click **OK** to create the project.

Exporting a Q3D Project

Q3D Extractor projects may be immediately solvable, depending on how you set up the ALinks project. Keep the following in mind:

- Each conductor in the generated 3D model must have at least one source terminal and *exactly* one sink terminal.
- The IC die contact surfaces of wire bonds and flip-chip solder bumps are identified as current sink terminals by ALinks.
- The PCB contact surfaces of solderballs in BGA designs are identified as current source terminals.

If any conductor in the 3D model does not satisfy these criteria, and the **Mark floating objects as non-model** option is selected, all solid objects in this conductor are defined as non-model objects. Such objects are invisible by default and are not included in the solution process. They can, however, be changed into model objects using the 3D modeler.

> **Note:**
>
> Assign bondwire models to WIREBOND layers, and solderball models to appropriate padstacks, to allow ALinks to set up Q3D Extractor projects as completely as possible.

If a plane geometry is sliced in ALinks, there is a good chance that floating conductors will be present in the resulting 3D model. If the **Mark floating objects as non-model** option is selected, objects that make up floating conductors are identified as non-model objects; if they are required for a Q3D Extractor solution, you must change the floating objects to model objects using the 3D Modeler, and then assign boundaries appropriately.

To export a model as a Q3D Extractor project (*.aedt):

1. Click **Export**.
2. From the 3D Exports area, click **Export to Q3D Extractor**.

   The **Export Q3D Project** window appears.

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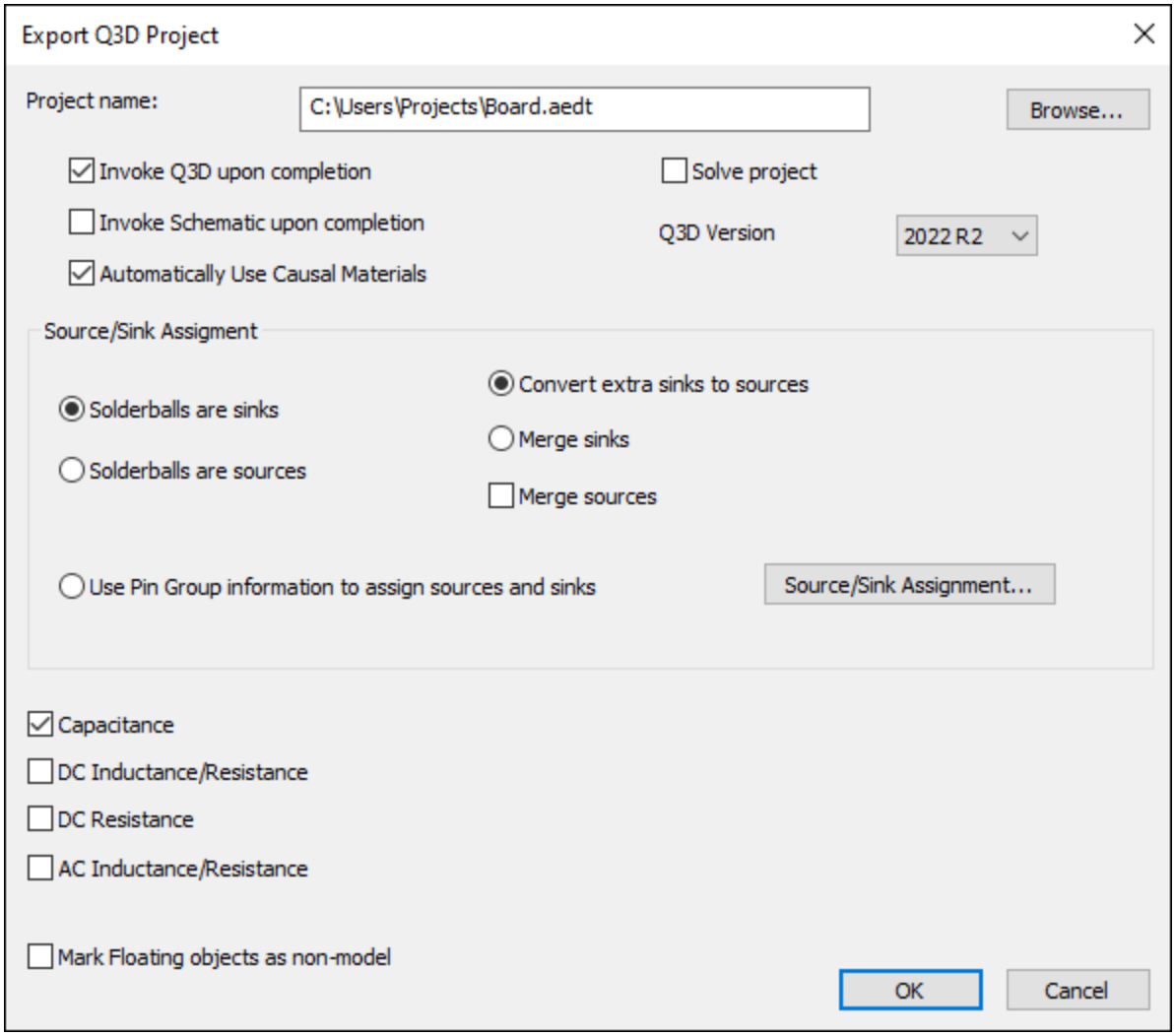

3. From the **Project Name** field, type the path and file name for the export, or click **Browse** to select a destination.
4. Use the **Q3D Version** drop-down menu to select the version for export.
5. Select an appropriate options:
   - **Invoke Q3D upon completion** – check this option to open Q3D Extractor after export.
   - **Invoke Schematic upon completion** – check this option to invoke Q3D Extractor as a Project Schematic. Note: This option requires checking **AC Inductance/Resistance**.
   - **Automatically Use Causal Materials** – check this option to enable Q3D Extractor to automatically use causal materials.
   - **Solve project** – check this option to start the solution process after Q3D Extractor is opened. Note: For UNIX machines, the **qp3d** executable must be in the path.
6. From the **Source/Sink Assignment** area, determine whether solderballs are sinks or sources.

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- If you wish to use pin groups to export the portion of the design that includes the pin group, select **User Pin Group information to assign sources and sinks**.

7. From the **Source/Sink Assignment** area, select whether to **Convert extra sinks to sources** or **Merge sinks**.
8. If you need to change terminal designations, click **Source/Sink Assignment**.

   The **Terminal Assignment** window appears. All bondwire and solderball terminals are displayed. To make an assignment, select an item in the list, select **Source**, **Sink**, or **Float**, and click **Apply**.

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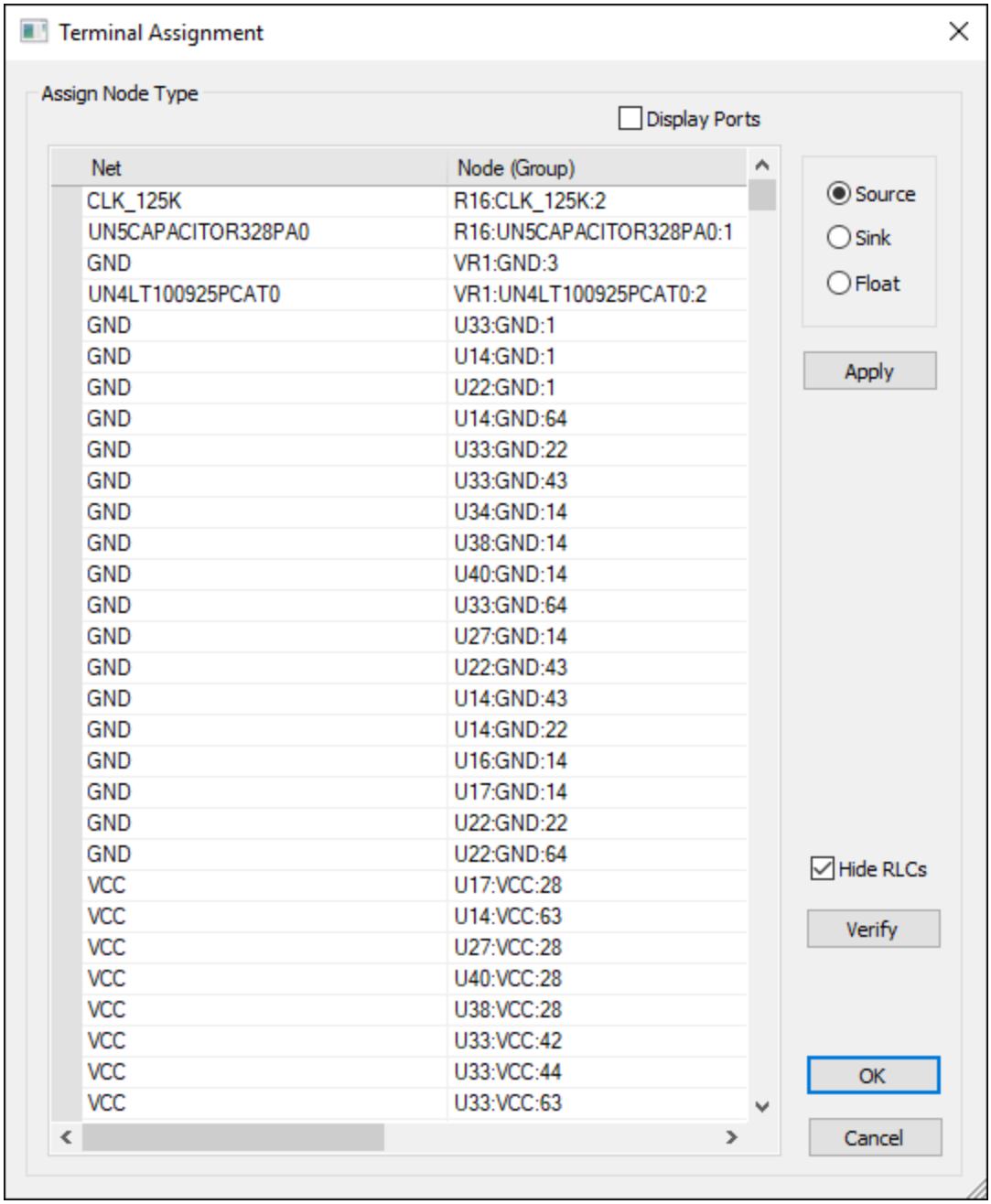

Click **OK** to save and return to the **Export Q3D Project** window.

9. Instruct Q3D Extractor to compute the selected matrices once the project is exported. Options include: **Capacitance**, **DC Inductance/Resistance**, **DC Resistance**, and **AC Inductance/Resistance**.
   - If you select **DC Inductance/Resistance**, the **DC Resistance** option becomes unavailable.

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10. If appropriate, select **Mark floating objects as non-model** to make the objects without sources and sinks as non-model. They are not included in the simulation.
11. Click **OK** to create the project.

Exporting Huray Roughness Models

To export a Huray Roughness Model:

1. Click **Export**.
2. From the **Ansys EDA Layouts** area, click **Huray Roughness Models**.

   The **Select file for Huray Roughness Model File** window appears.
3. Select the name and location for the Huray Roughness Model File (*.hrm).
4. Click **Save**.

PinToPin Export Automation

The PinToPin utility can quickly extract HFSS or SIwave models for specified nets of package and PCB geometries. It establishes a repeatable process for robust geometry extraction, port configuration, and passive model assignment. Process execution can be done via the user interface (Windows only) or in non-graphical mode (Windows or Linux).

Launching PinToPin Utility

To launch the PinToPin utility in non-graphical mode, type:

- **`PinToPinSetup`** `<workingDir> <path to XML control file> <path to appropriate EDB or XML output>`

To launch the PinToPin utility from within SIwave:

- Click **Tools**. From the **External Tools** area, click **PinToPin Setup**

The PinToPin utility launches in a window labeled **HFSS Setup**.

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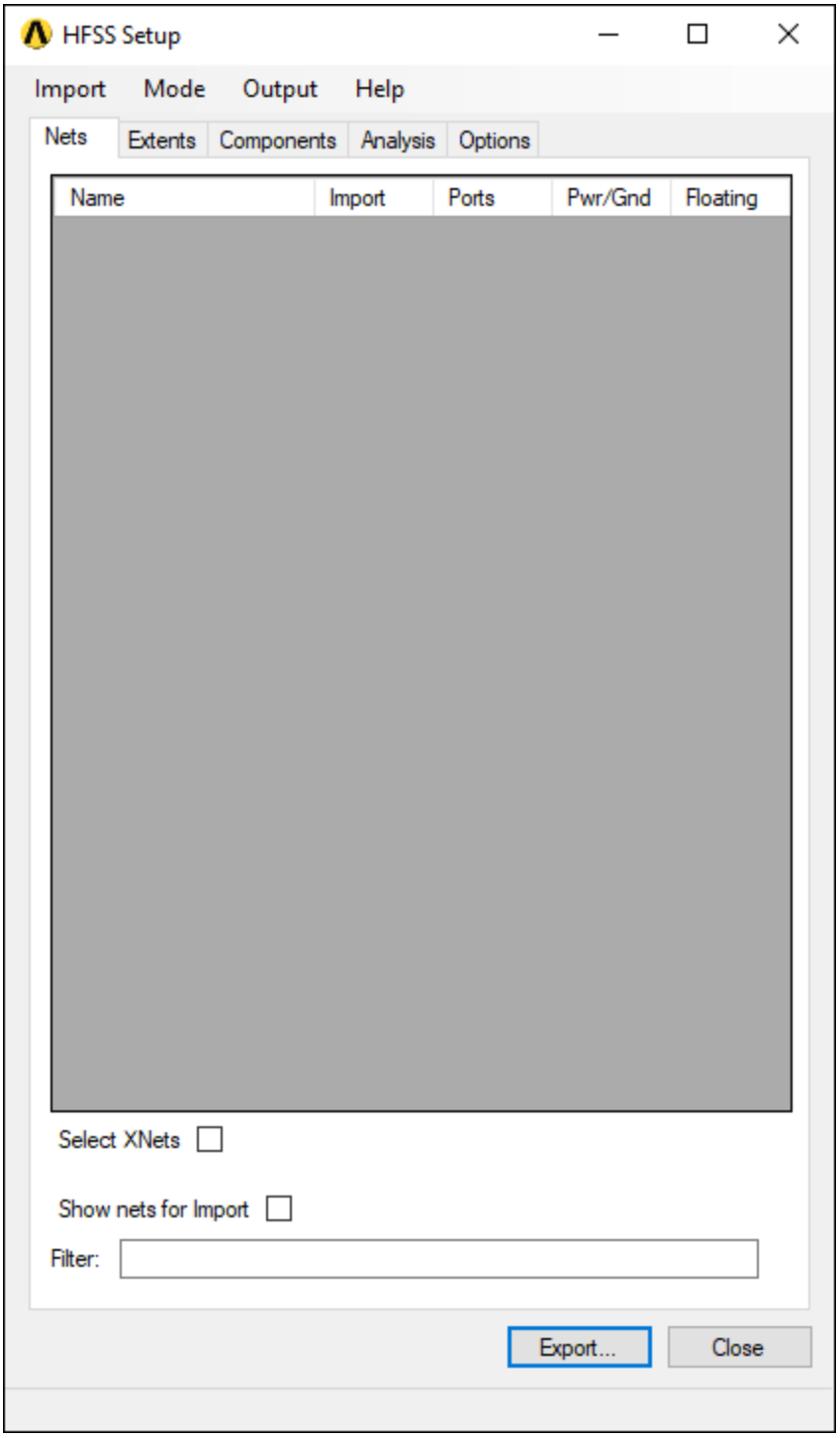

Importing a File

To import a file into PinToPin utility, click **Import** and select a file type.

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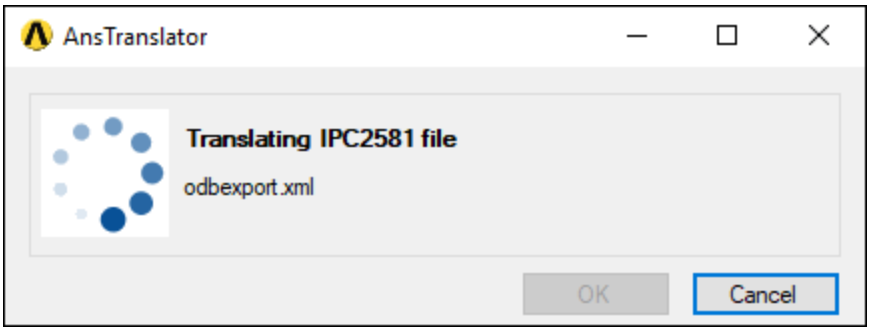
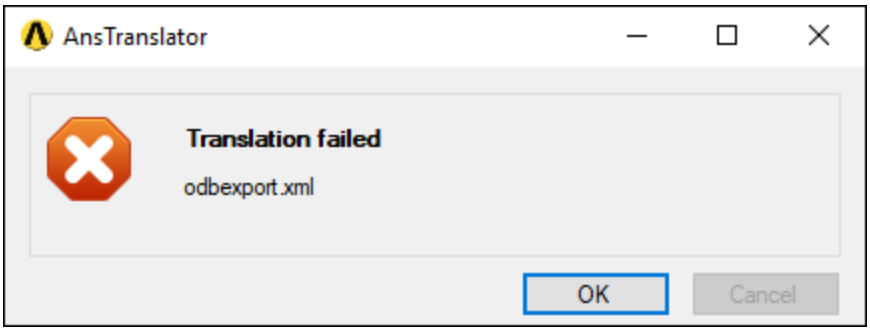
Supported file types are:

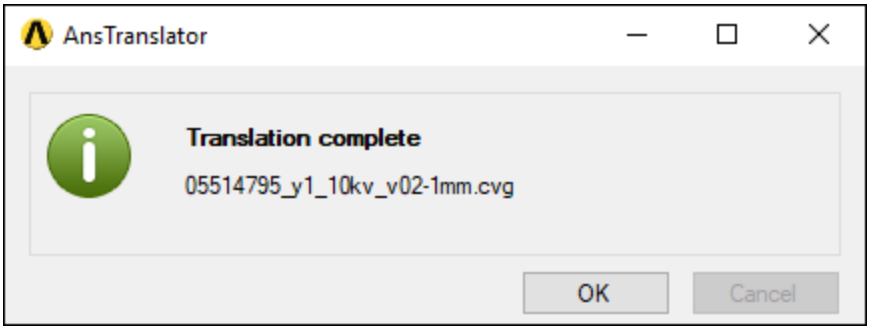
- Cadence Allegro/APD/SIP (*.brd, *.mcm, *.sip)
- ODB++ (*.tgz)
- IPC2581 (*.xml, *.cvg)
- Ansys EDB (*.def)
- XML configuration file (*.xml)

For Cadence, ODB++, and IPC2581 files, the **AnsTranslator** window will appear and alert you of translation progress:



It will then let you know whether translation has succeeded or failed.





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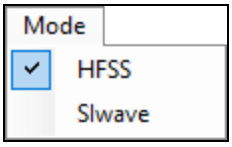
Once the file has been loaded, the window name changes to the file name.

Selecting a Simulation Mode

Click **Mode** and select either **HFSS** or **SIwave**.



The contents of the **Analysis** tab change based on this selection, and the **Extents** tab appears only for HFSS mode.

Changing PinToPin Settings

The PinToPin utility window contains up to five tabs:

- **Nets** – allows you to select nets for import, and to quickly denote ports, power/ground nets, and floating nets. You can also filter the nets using regular expressions.
- **Extents** (HFSS mode only) – allows you to specify cutout, airbox, and dielectrics settings.
- **Components** – allows you to change component part types, and to set model, solderball, die, and port properties.
- **Analysis** – allows you to set simulation and frequency sweep options.
- **Options** – allows you to alter the port naming convention or bondwire definitions.

For more information about these options, see PinToPin Settings.

To configure default settings, generate a `PinToPinSetup.xml` configuration file and place it in the same folder as `PinToPinSetup.exe`.

Exporting a File

Click **Output** and select one of the following:

- **HFSS 3D Layout** – *.aedb folder that can be imported into either Ansys Electronics Desktop or SIwave.
- **XML** – *.xml file that can be used in subsequent calls to PinToPin. This is a good way to save a configuration or create a template that can be called repeatedly to create multiple models from the same file.

Click **Export** to generate the selected file type.

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Troubleshooting PinToPin Utility

PinToPinSetup writes log files to the working directory. These log files may provide useful information about warnings or errors encountered during model generation.

PinToPin Settings

The PinToPin utility contains up to five tabs. Click a tab's name to learn more:

- **Nets**
- **Extents**
- **Components**
- **Analysis**
- **Options**

Nets Tab

The **Nets** tab allows you to select nets for import, and to quickly denote ports, power/ground nets, and floating nets. You can also filter the nets using regular expressions.

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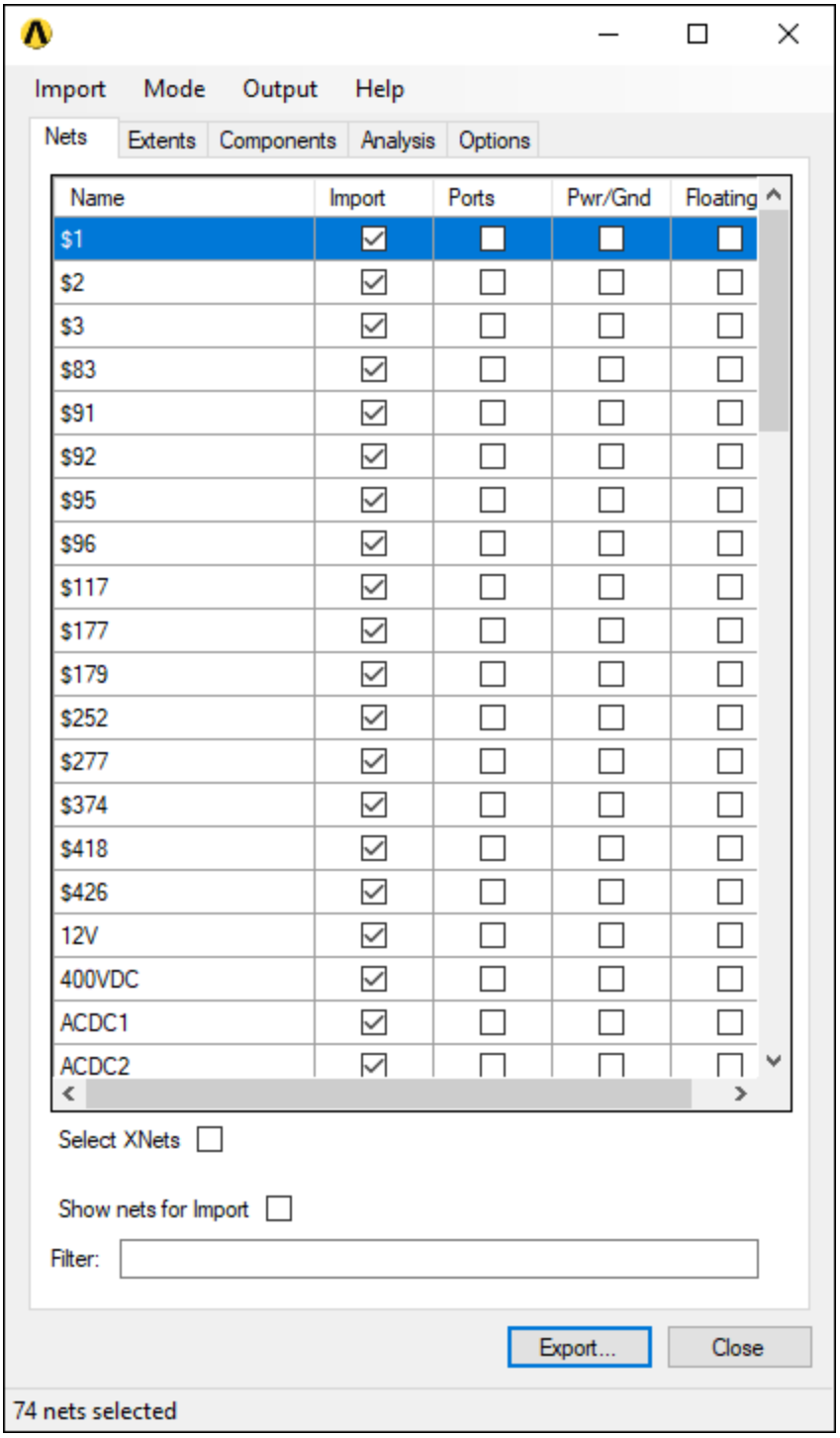

The bottom of this tab shows the number of nets currently selected.

Options include:

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- **Import** – use the check boxes to select nets for import.
- **Ports** – use the check boxes to identify nets for which ports will be created at component pins of class IO, IC, or Other.
- **Pwr/Gnd** – use the check boxes to identify power or ground nets. When clipping the model region, nets in this class will not be used to calculate the boundary. Nets included but not assigned Pwr/Gnd will be preserved by the clipping operation.
- **Floating** – use the check boxes to identify floating power or ground nets. Nets assigned as floating will not be tied into reference planes at component interfaces.
- **Select XNets** – when this option is enabled, selecting a net also includes any extended nets. Nets are in the same extended net if they have a serial connection through an R, L, or C component.
- **Show nets for Import** – when this option is enabled, the net list displays only nets selected for inclusion.
- **Filter** – enter regular expressions in this field to search for nets. Only those that satisfy the regular expression are shown.

Extents Tab

The **Extents** tab allows you to specify cutout, airbox, and dielectrics settings. It appears only in **HFSS** mode.

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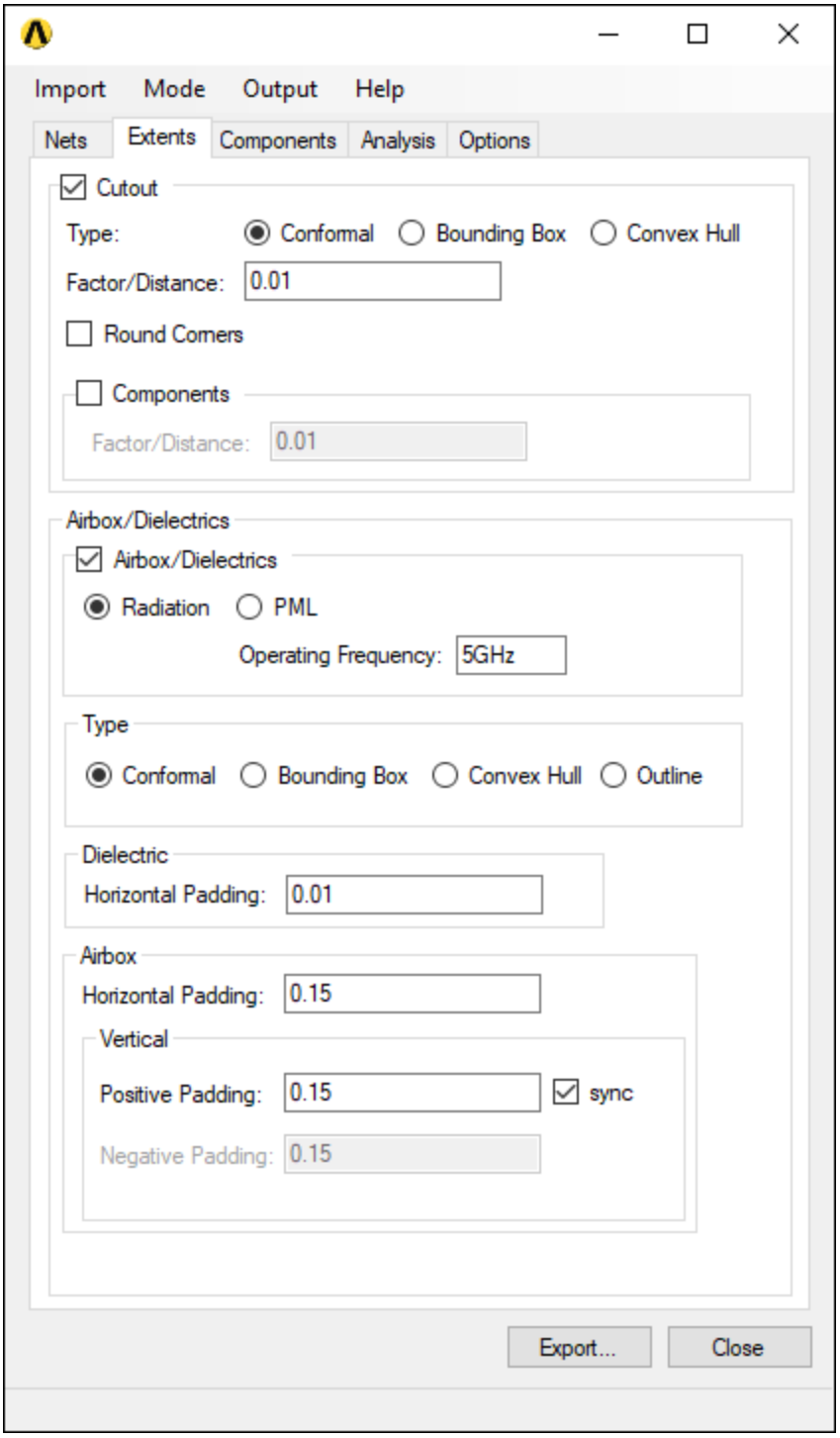

Consult the HFSS online help for detailed information about model extents.

Components Tab

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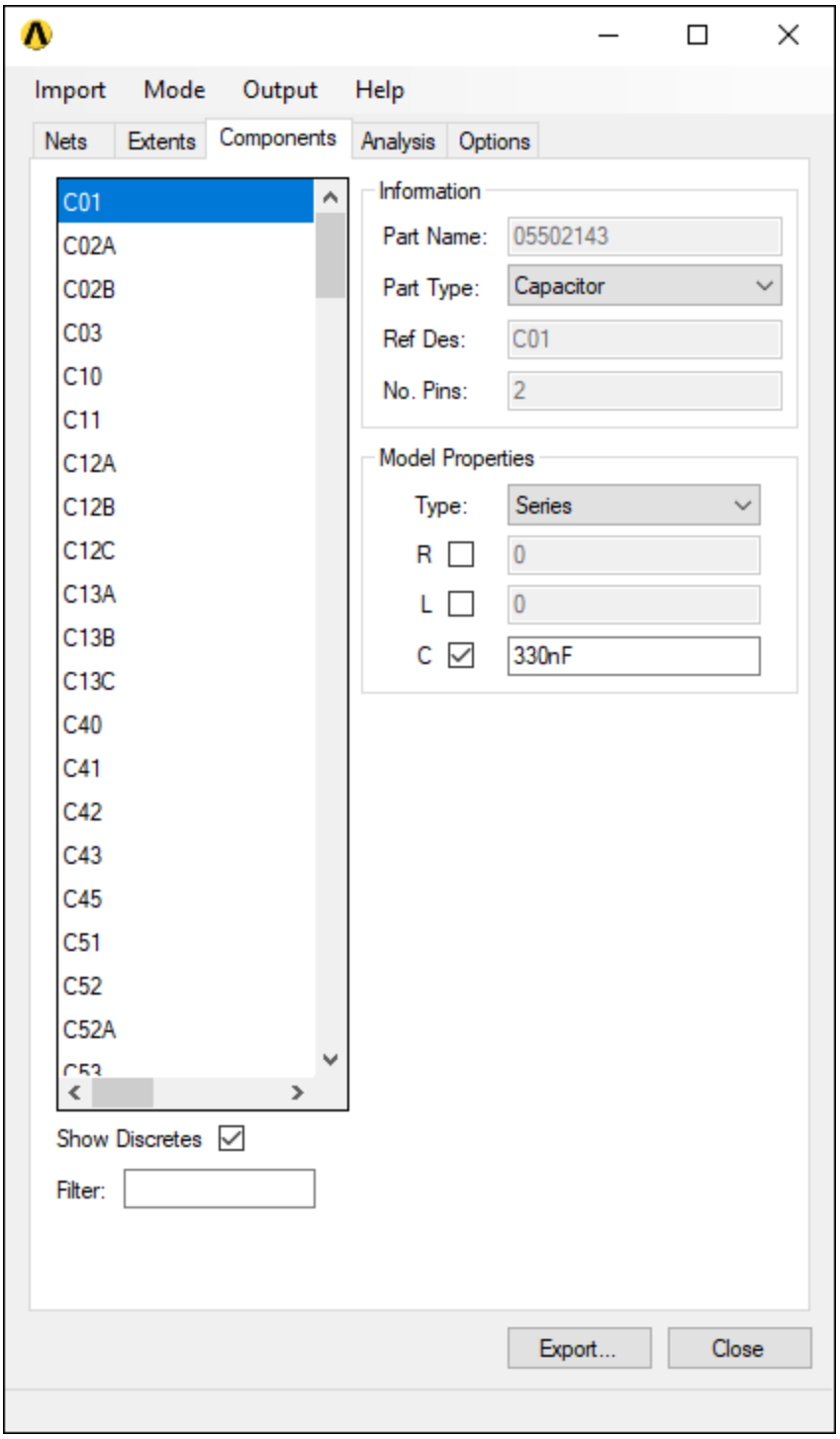
The **Components** tab allows you to change component part types, and to set model, solderball, die, and port properties.



Options include:

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- **Show Discretes** – enable to display resistor, capacitor, and inductor component types.
- **Filter** – enter regular expressions in this field to search for components. Only those that satisfy the regular expression are shown.

Select a component from the list at the left to view its **Information** and **Properties**. Options vary based on the **Part Type**, which you can change. Generally, you can alter model properties, die properties, solderball properties, and port properties.

Analysis Tab

The **Analysis** tab allows you to set simulation and frequency sweep options. Options vary based on whether you are in **HFSS** or **SIwave** mode.

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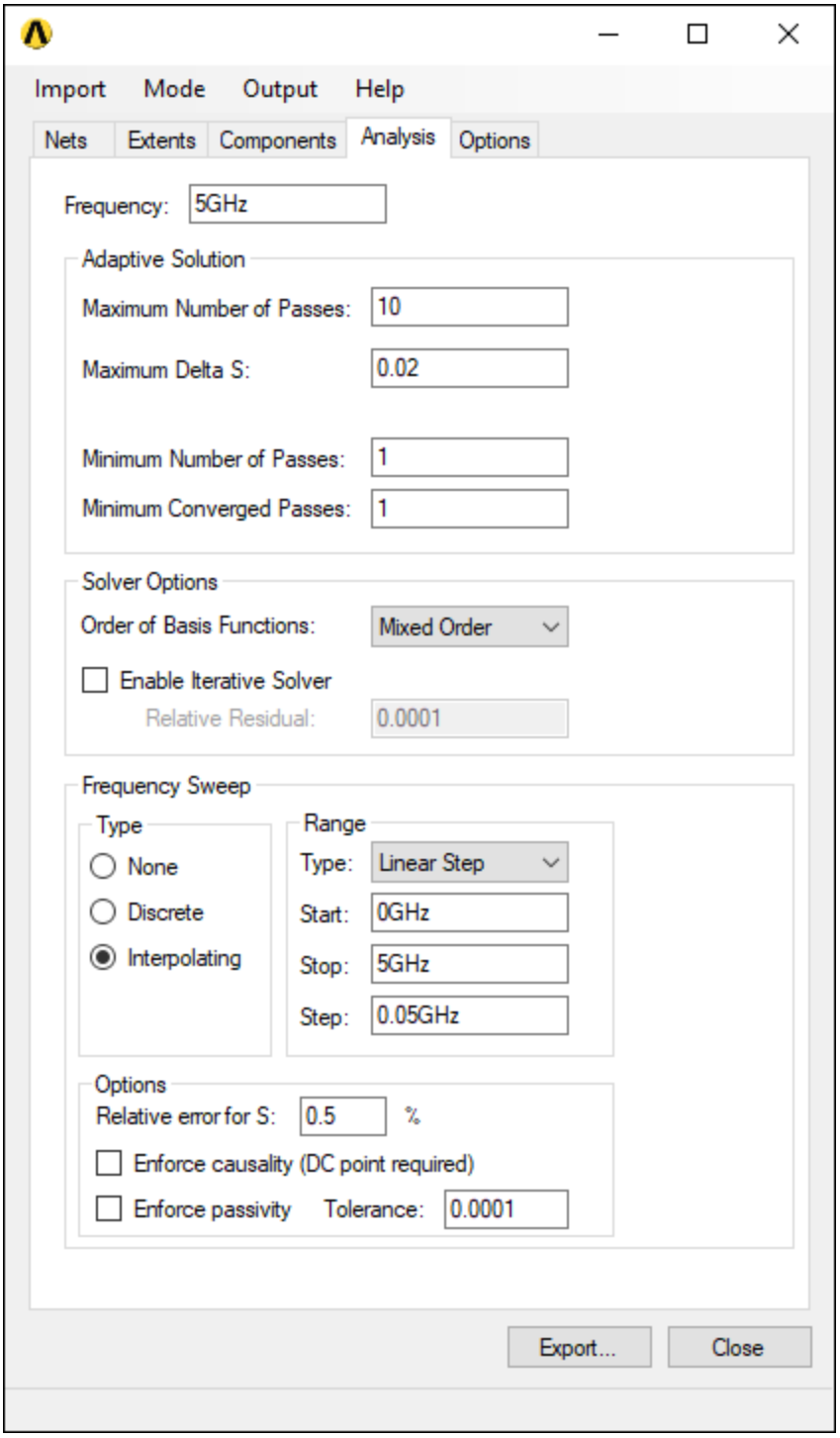

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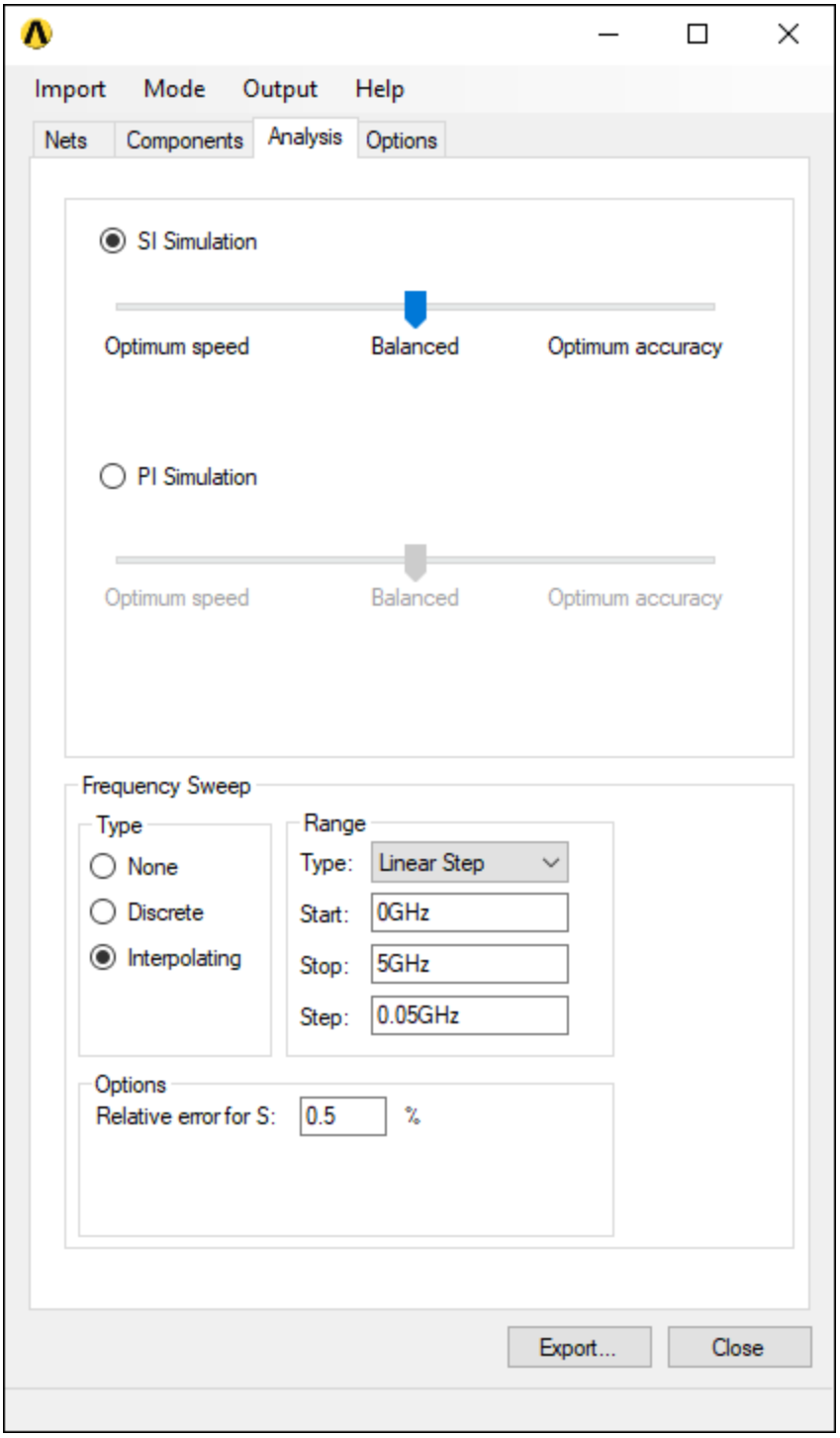

For information about setting up an HFSS simulation, consult the HFSS online help.

For information about setting up an SIwave simulation, see: Simulation Setup.

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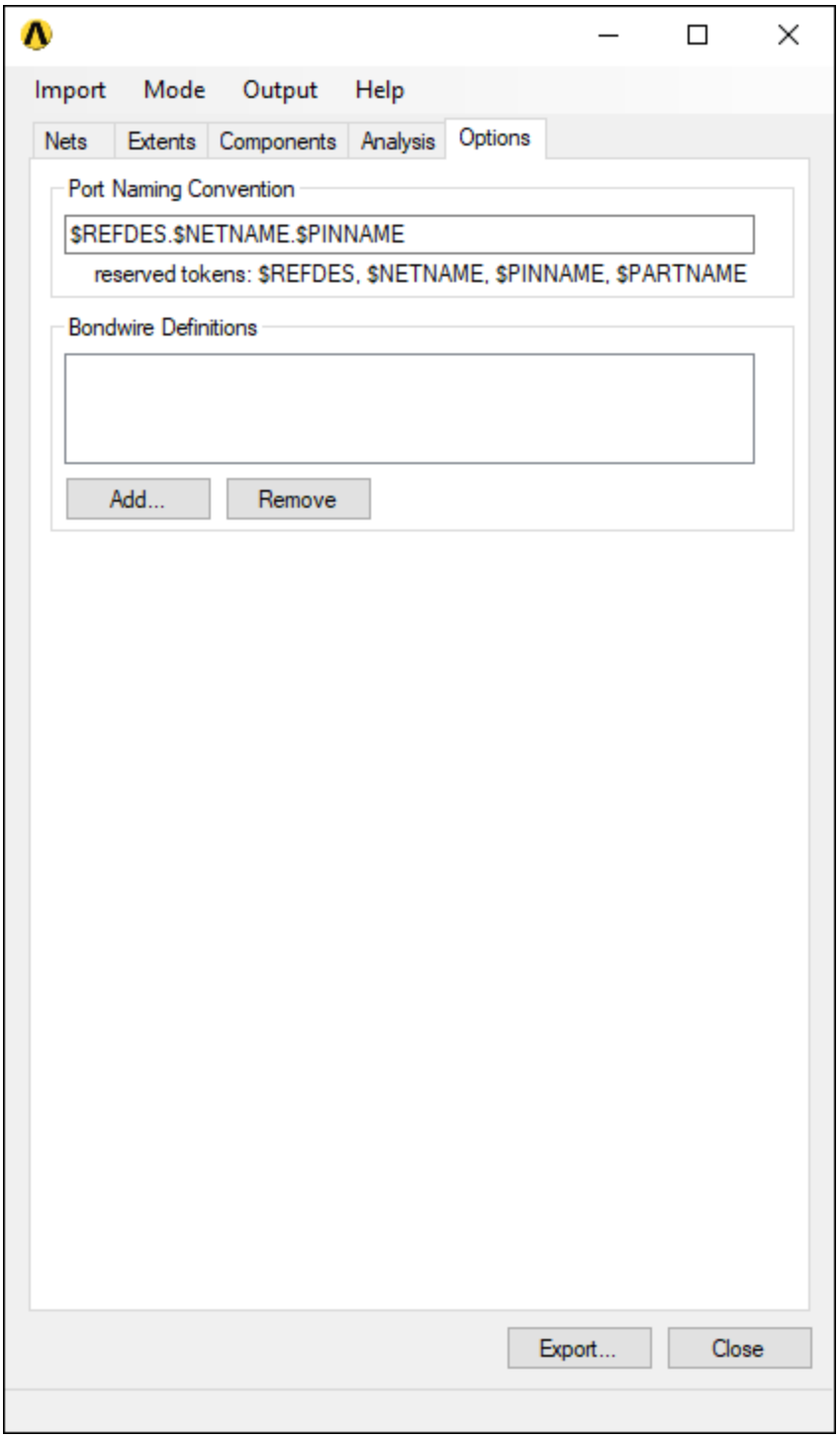
Options Tab

The **Options** tab allows you to alter the port naming convention or bondwire definitions.



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From the **Port Naming Convention** field, use the reserved tokens to designate a port naming convention (e.g., entering `$REFDES_$PINNAME_$NETNAME` would result in ports such as `U37_A10_DQ7`).

From the **Bondwire Definitions** area, click **Add** to upload an XML bondwire definition file.

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12 - Technical Notes

This section contains technical notes on the following topics:

- Assigning a Heat Sink
- Best Practices for SIwave-PSI Solver
- Best Practices for Q3D Model Export
- Circuit Elements
- Creating a Sample Pin Group
- DC IR Solution
- Djordjevic-Sarkar Model
- Frequency-Dependent Material Properties
- Full Wave Subcircuits
- Huray Surface Roughness Model
- Lumped Analysis
- Meshing
- Net Configuration File
- ODB++ Translator
- Resonant Frequencies
- RMS Surface Roughness and Conductivity
- Sensitivity Analysis
- S-Parameters
- Terminals and Extraction
- Using Environment Variables
- Window Functions and Time Domain Plotting

Assigning a Heat Sink

You can import an IDF file containing ECAD/MCAD into SIwave, and then display 3D components, including heat sinks.

ECAD/MCAD nodes appear in the component tree.

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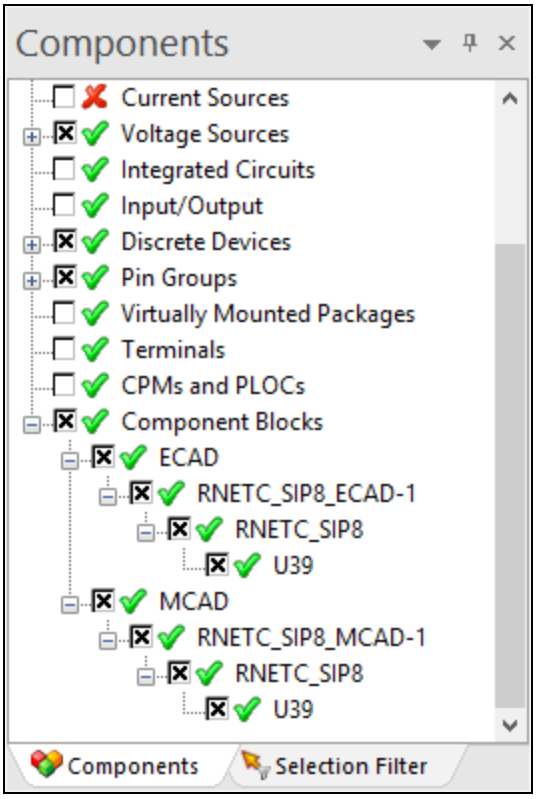

When you select a component block, its details appear in the **Properties** window.

To mount a heat sink:

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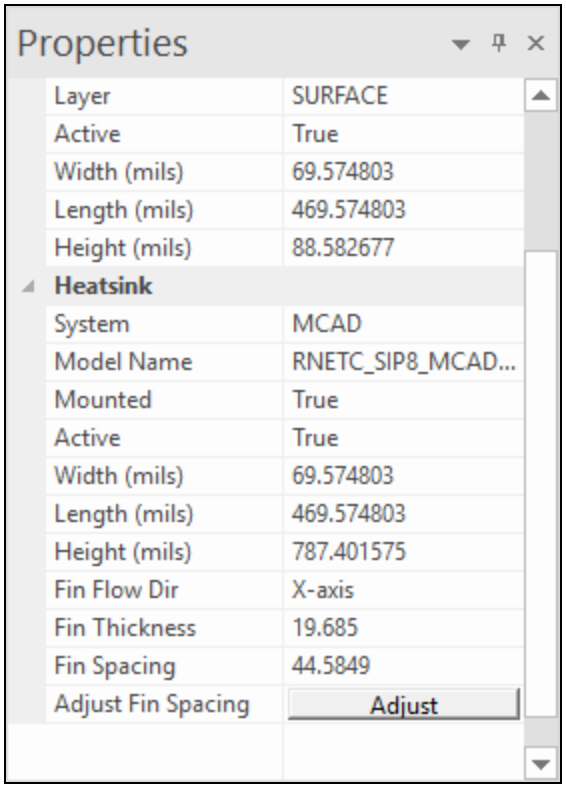
1. Change **Mounted** to **True**.



   The **Properties** window updates, and the component tree displays a new node for ECAD/MCAD objects.

   The heat sink is mounted on the top of ECAD object.

   The dimensions of the heat sink and the associated component block can be changed from the **Properties** window.

To assign a heat sink:

1. Click **Advanced** > **Heatsinks**.

   The **Assign Heatsinks** window appears, listing available components.

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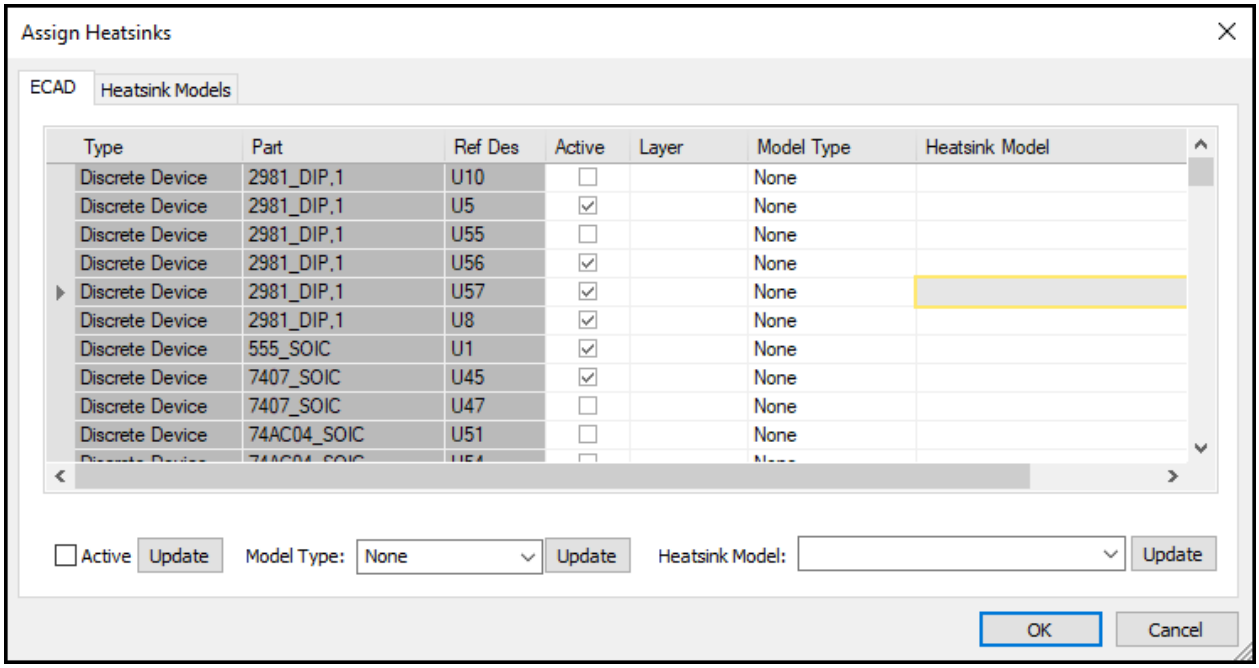


2. For an appropriate component, change the **Model Type** to **Heatsink** or **Component Block**.

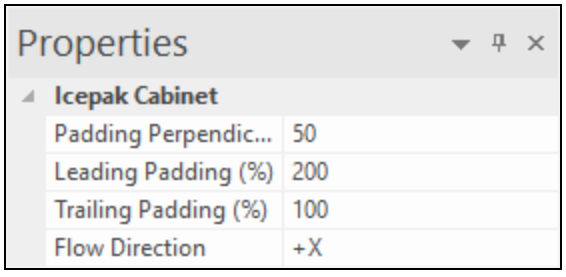
> **Note:**
>
> You can also remove a heat sink by changing its **Model Type** to **None**.

3. Click **OK** to apply changes.

To view the Icepak cabinet:

1. Click **View**.
2. From the **Show/Hide** area, click the **View Icepak Cabinet** icon ( ) to view the cabinet.

   The Modeling workspace displays the Icepak Cabinet and the **Properties** window displays Icepak Cabinet information.



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3. If appropriate, change the dimensions and flow direction.

Best Practices for SIwave-PSI Solver

SIwave-PSI (formerly PSI) is a 3D, full-wave, fast Finite Element Method (FEM) field solver customized for IC package and PCB analysis. This section provides key setup guidelines to get the best results out of the PSI solver:

- Model Type
- Number of Cores
- Solderballs and Bumps
- Net Classification
- Temporary Working Folder
- Port Setup
- Frequency Sweep

SIwave-PSI Best Practices: Model Type

For structures containing micron level routings, such as RDL structures, select the IC type.

Use PKG or PCB for all other layouts.

SIwave-PSI Best Practices: Number of Cores

Minimum: 8

Recommended: 12-16

All of the computationally intensive parts of the solver are shared memory multi-threaded, and performance is strongly dependent on the number of cores. Best performance is seen with 12 to 16 shared memory cores per node. Using fewer than 8 cores impacts performance negatively.

Distribution of frequency points over a large distributed compute cluster can drastically reduce overall simulation time since each frequency point can be solved independently of another. Frequency point solve time scales almost linearly; in other words, scaling up to 512, 1024, … cores is efficient as long as discrete frequency points are defined in the frequency sweep setup and more frequency points exist than cores.

SIwave-PSI Best Practices: Solderballs and Bumps

Set ball and bump dimensions using **Solderball Properties** on the **Home** tab.

This enables the solver to carry out meshing optimizations resulting in the highest accuracy.

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Important:

This is no longer possible if the balls/bumps are explicitly converted to physical vias and appear in the layer stackup.

SIwave-PSI Best Practices: Net Classification

It is essential to properly classify nets containing large planes as Power/Ground nets.

Signal nets containing microstrip and stripline routing need to be classified as Non Power/Ground nets. This enables the solver to judiciously choose the mesh refinement and optimization strategies for the signal and power/ground nets.

Warning:

Improperly classifying nets can lead to significant performance and accuracy degradation.

SIwave-PSI Best Practices: Temporary Working Folder

Locate the Temporary Working Folder on a local drive.

During the course of simulation, this folder is used to store temporary files created by PSI. In order to achieve the best performance, this folder must be located on a local hard drive where the simulation is running, with at least 20 to 30GB of available disk space. Using an NFS or remote drive could lead to a significant slowdown or even a simulation failure.

SIwave-PSI Best Practices: Port Setup

Broadband, 3D simulations require good definition and modeling of ports. Port concepts widely differ between simulation tools, even when called by the same name. To produce results that are true to physical reality, simulation models must account for the field distribution and the actual location of ports.

A port consists of a positive and a negative terminal, each generally identified by a pin or a group of pins. When analyzing a package, it is often convenient to locate internal ports at solder bumps and at solderballs. To produce realistic 3D analysis of such ports, PSI solver offers the following port types:

Port Type	Description	Recommendation
Undefined	Defaults to Coaxial-Open at solder ball and bumps. Defaults to Lumped for all others.	

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Port Type	Description	Recommendation
Coaxial-Open	A floating metal with antipads at positive and negative terminals is used (Fig. 1).	Recommended at solder bumps and balls, if ports do not share a common negative terminal.
Coaxial-Short	A floating metal with antipads at positive terminals is used. All of the negative terminals shorted to the metal (Fig. 2).	Recommended at solder bumps and balls, if ports share a common negative terminal.
Lumped	Excites the port as a line(s) connecting the pins (Fig. 3).	Recommended for ports defined directly on the metal pads or shapes, and when the port length is small (< 60um).
Gap	A port of finite width derived from its pad is enforced (Fig. 4).	Recommended for ports defined on rectangular pads, such as decaps, signal pads, etc.

Note:

Using **Coaxial** ports increases the computational complexity and the run time. In view of this, for situations where a large number (thousands) of solder bumps are grouped to define a port, it is recommended to use Lumped type. This setup gives good accuracy without compromising the run time as the presence of large pins groups doesn't warrant the Coaxial ports.

The following figure shows a Coaxial Open Port, with cutouts around negative terminals.

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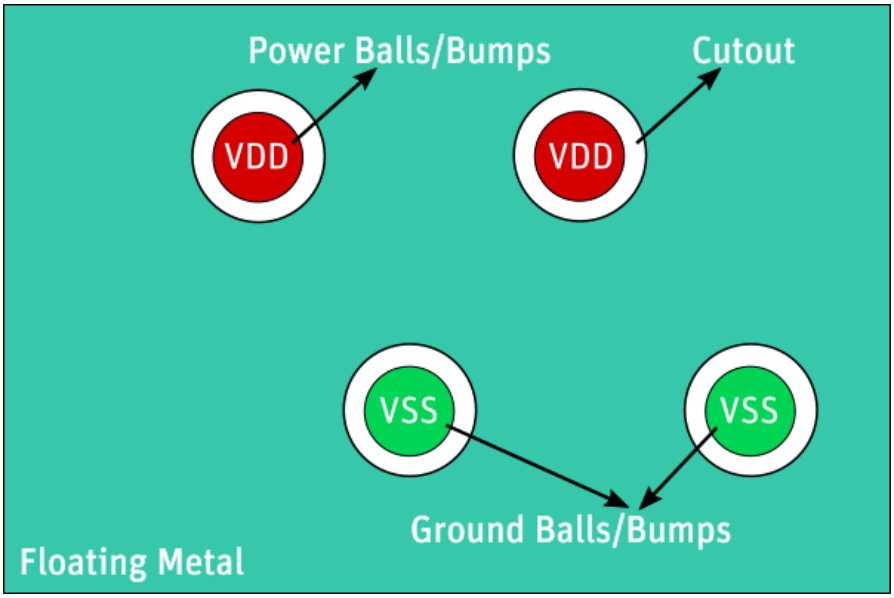
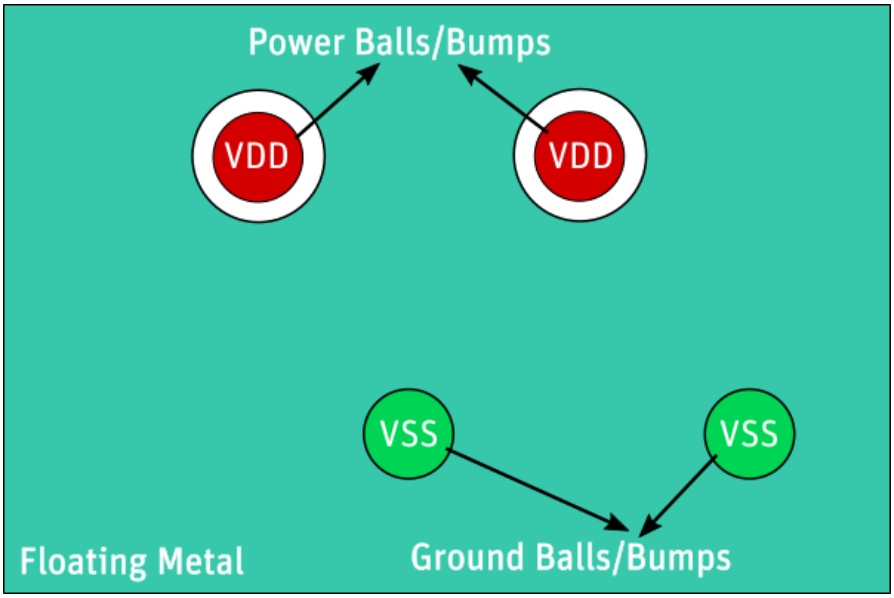


The following figure shows a Coaxial Short Port, with negative terminals shorted to the metal.



The following figure shows a Lumped port field excitation.

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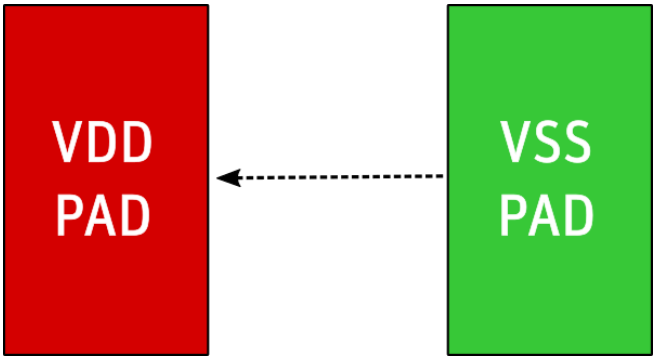
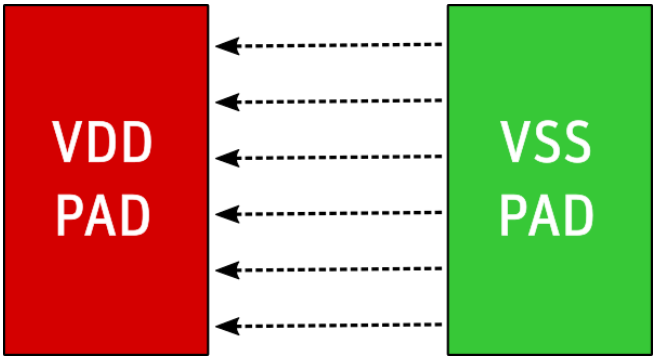


The following figure shows a Gap port, with field excitation spread over an area.



SIwave-PSI Best Practices: Frequency Sweep

Typically, 3D full-wave solvers have difficulty in solving the vector Helmholtz equation at low frequencies due to decoupling of electric and magnetic fields. This low frequency limit could be as high as 1 to 10MHz. But the PSI solver employs a tree-cotree splitting on the edge elements to overcome this instability, so that a simulation can be extended to extremely low frequencies (as low as 1Hz). Good accuracy is maintained in the S- and Y- parameters at such low frequencies. But the open-ended Z-parameters could exhibit non-monotonic behavior below the KHz range since the z-parameters try to capture open circuit responses coming from $1/\omega C$. To circumvent this behavior, select Enforce DC point and Causality, which enables the PSI solver to explicitly solve for the DC point and start simulation from a suitably higher frequency point.

Using the Interpolating Sweep is strongly recommended as it improves the performance significantly, with the same level of accuracy as Discrete sweep. Since the convergence of sweep requires more simulations at low frequencies, it is recommended to use a higher starting frequency in MHz region unless the application demands otherwise.

Heading	Description	Recommendation
Model Type	IC, Package or PCB	For RDL select IC.

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Heading	Description	Recommendation
		For all others - select Package or PCB.
Number of Cores	Shared Memory	12 – 16 cores is recommended. Do not use less than 8 cores for any simulation as simulation time greatly increases.
Number of Cores	Distributed Memory Cluster	Tremendous speed up can be achieved by adding a large number of cores. Essentially add 8-16 cores of shared memory for each frequency point to be solved. Clusters with core counts greater than 512, 1024 … can be utilized very efficiently.
Solderballs and Solder Bumps	Geometry and material characteristics	Define in the padstack editor to obtain optimal results.
Net Classification	Plane geometries must be classified as Power/Ground Nets. Signal Nets using Microstrip & Stripline geometries must be classified as Non-Power/Ground Nets.	Improves accuracy and speed of simulation.
Temporary Working Folder	Location & Size	Locate on a local drive (same as project) with at least

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Heading	Description	Recommendation
		20 – 30 GB of available space.
Ports	Port Setup	See: Port Setup.
Frequency Sweep	Discrete vs. Interpolating	Generally Interpolating sweep is recommended unless a large distributed compute cluster is available. With this arrangement use a Discrete sweep.

Best Practices for Q3D model export

Several options are available when exporting the layout to Q3D to ensure a fast and efficient solution. This section presents the recommended settings that could be applied to most SIwave exported Q3D projects.

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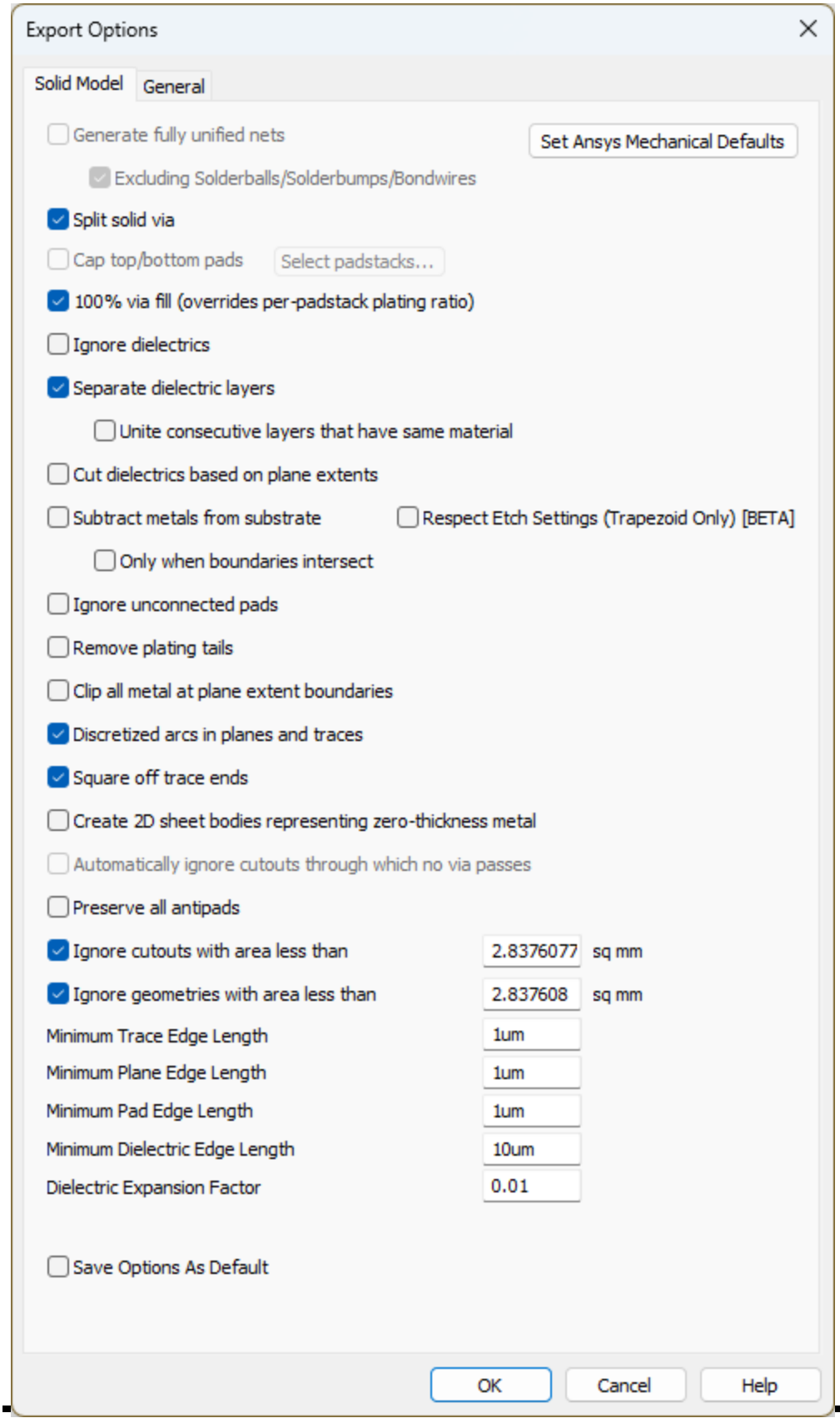

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Recommended settings in the **Export Options window**:

- **Generate fully unified nets** – Optional. This unites all solid objects of a net into a single one. If the conductivities of the metal layers are similar, this option can reduce the model complexity and save solution time. However, for most package projects, the vias and solder bumps/balls have different materials from the rest of the layout. Caution must be exercised before selecting this option.
- **Split Solid Via** – Recommended. This option cuts the top and bottom pads of the vias and hastens mesh generation.
- **100% via fill** – Recommended. This option removes the plating thickness and fills vias completely.
- **Separate dielectric layers** – Optional. This helps to create a separate object for each dielectric layer. If unchecked, it generates different layered dielectric layer into one layer substrate. If the dielectric layers have different materials, it is better to check this option to generate different layered dielectric substrate.
- **Cut dielectrics based on plane extents** – Optional. This ensures that the dielectric model has the same shape as the plane extents. The default will export a rectangular shape.
- **Subtract metals from substrate** – Not Recommended. This option subtracts the metal from dielectrics. Deselect it to reduce boolean processing time and speed up model generation.
- **Ignore unconnected pads** – Recommended. This option helps exclude via pads that are unconnected to metal planes. It is helpful to ignore the trace outside the package.
- **Clip all metal at layout extent boundaries** – Optional. This can cut the selected net that extends the plane extent boundary. It is helpful for defining the specified plane extent.
- **Discretized arcs in planes and traces** – Not Recommended. This option helps to avoid unconnected nets becoming connected in Q3D.
- **Square off trace ends** – Optional. This can chop off the rounded ends of the traces upon export. Some separated nets in SIwave project might overlap in Q3D if this option is not selected.
- **Ignore cutouts with area less than** – Recommended. This option removes small voids and cutouts and potentially speeds up the simulation.
- **Ignore planes with area less than** – Recommended. This option removes small planes and potentially speeds up the simulation.
- **Specify the Minimum Length for Traces, Planes, and Pads** – Recommended. This option removes small, inappropriate faces from these objects, which may cause problems in the meshing or in the EM solver. Any face smaller than the specified value will be omitted from the solid model.
- **Specify the Dielectric Expansion Factor** – Recommended. This option controls the size of the dielectric and stops it from being expanded beyond that boundary.

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> **Note:**
>
> A recommended setting in the **Export Q3D Project** window is to make sure that you have checked the **Merge sinks** and **Merge sources** options.

Additional tips for setup and export:

1. If solder bumps and solder balls exist in SIwave, check them for the exported Q3D project. For AC inductance and resistance analysis, solder balls and solder bumps are specially required on the package for adding source and sink terminals. However, overlapped pads could present issues in generating the solder bumps and balls in Q3D. In such situations, try to change the solder balls generated on the bottom-most layered pads, and the solder bumps generated on the top-most layered pads.
2. Clear the **Ignore unconnected pads** and **Discretized arcs in planes and traces** options. The generated Q3D projects might have different nets from the SIwave project due to overlapped nets in Q3D. Before simulation, auto identify the nets. If the proposed option is cleared, but the unmatched nets problem still exist, try to reduce the dimension of cutouts and planes.
3. User-defined materials might be missing in Q3D. In such cases, turn-on the option of separate dielectric layers in the **Export Options** window, which brings them in as air in Q3D. You can then redefine the air material appropriately.

Circuit Element Technical Notes

This set of technical notes provides details on the circuit elements.

Parasitic Elements

Capacitance

ESR and LI of a Capacitor

Inductance

Resistance

Parasitic Elements

Parasitic elements are electrical components that arise from the structuring of a circuit due to inherent electromagnetic effects. They produce an inappropriate and inefficient signal in an electric circuit, generally one that is higher or lower than an appropriate frequency.

Parasitic elements include:

- **Parasitic Capacitance** – the inherent capacitance of a component (e.g., the capacitance between windings in a transformer).

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- **Parasitic Inductance** – the inherent inductance in a component (e.g., the inductance of a wirewound resistor).
- **Parasitic Resistance** – the inherent resistance of a component (e.g., the finite resistance of the package leads in a capacitor).

Capacitance of a Capacitor

Capacitance is the ability of an object to store electric charge and is the amount of charge stored per unit voltage on a device. It is represented by C and is calculated as:

$$C = \frac{Q}{V}$$

Q is the magnitude of the charge distributed on either surface, in coulombs, and V is the potential difference between the surfaces, in volts.

The unit of capacitance is farad (F). One farad is equal to one coulomb per volt.

ESR and LI of a Capacitor

Every capacitor includes a parasitic series inductance, called the lead inductance (LI). LI is also referred to as package or mounting inductance, or sometimes as effective series inductance (ESL).

Every capacitor also includes a parasitic series resistance, called the equivalent series resistance (ESR). It acts to defeat the effectiveness of a capacitor. ESR is a real-valued impedance and is not a strong function of frequency. ESR acts like a resistor in series with a capacitor. Lead inductance acts like an inductor in series with the same capacitor.

The equation for capacitor impedance as a function of frequency is given by:

$$Z(f) = \left[\mathrm{ESR}^2 + \left[\frac{-1}{2\pi f C} + 2\pi f L\right]^2\right]^{\frac{1}{2}}$$

where:

ESR = Equivalent Series Resistance

C = capacitance, in farads

L = inductance, in henries

Z(f) =impedance magnitude, Ω at frequency *f*, in hertz

Inductance

Inductance is the property of a circuit element to oppose a change in current. The time-varying magnetic field produced by a change in current causes an induced voltage to oppose the original

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change in the magnetic field. Self-inductance is the property of a circuit whereby a change in current causes a change in voltage. It is represented by L and is calculated as:

$$V_L = L\frac{dI}{dt}$$

where:

V_L = the induced voltage, in volts

L = the value of self-inductance, in henries

$\frac{dI}{dt}$ = the rate of change in current, in amperes per second

The unit of inductance is henries (H). One henry is the amount of inductance that is required for generating one volt of induced voltage when the current is changing at the rate of one ampere per second. One henry is equal to one volt-sec per ampere.

Resistance

Resistance is the opposition to current flow. The resistance of an object depends on the width, length and the material of which the object is made. It is represented by R and is calculated as:

$$R = \rho\frac{L}{A}$$

where:

ρ is the resistivity of the material (in Ω)

L is the length

A is the cross-sectional area

The unit of resistance is ohms (Ω). One ohm is equal to one volt per ampere.

Creating a Sample Pin Group

This topic guides you through the process of creating pin groups from scratch.

It covers the following steps:

1. Create a simple project.
2. Create a component.
3. Create a pin group.
4. Create a port.

For additional information, see Grouping Pins.

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Creating a Sample Pin Group, Step 1: Create a Simple Project

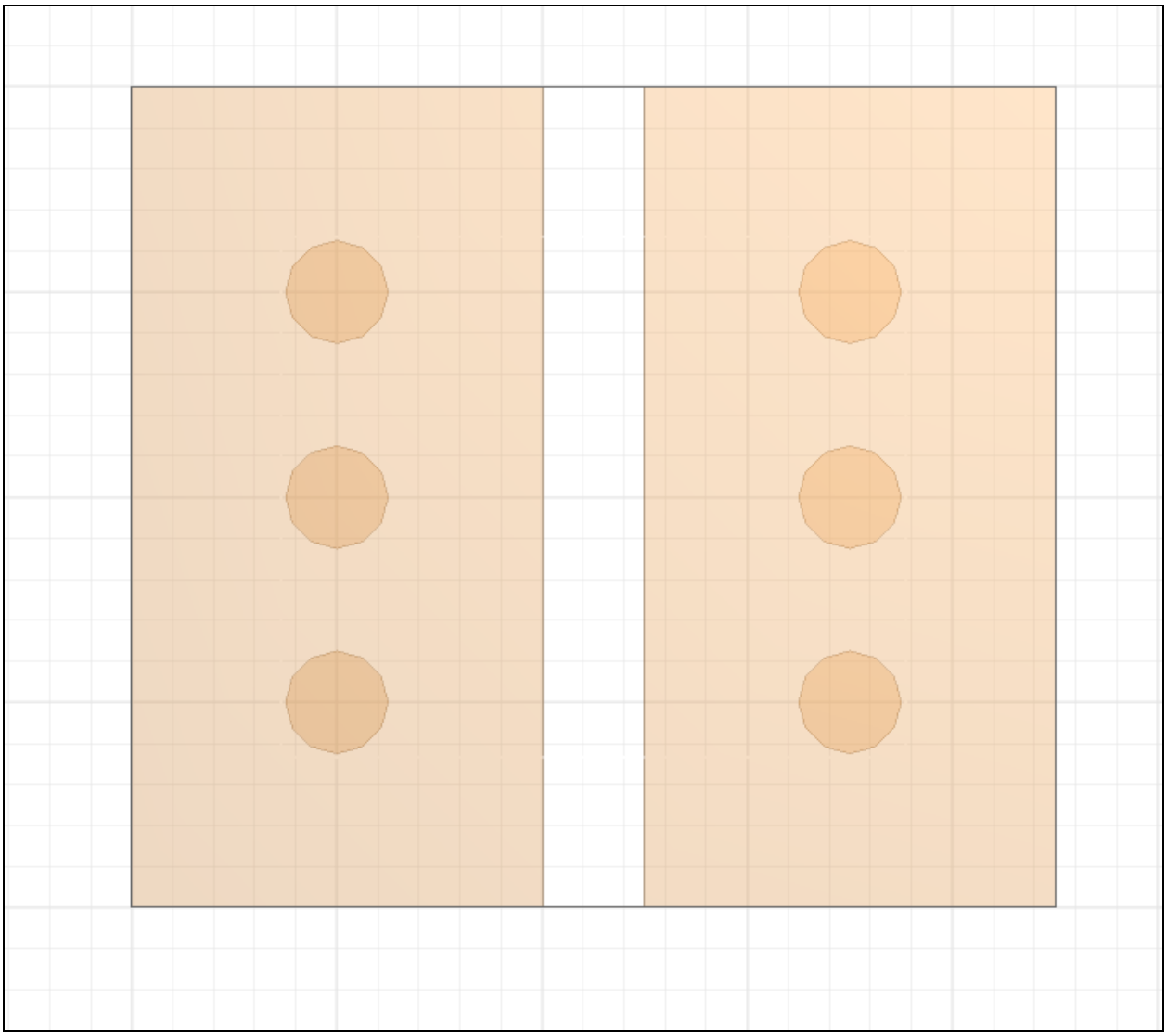
Perform the following steps:

1. Open SIwave, and click **New Project** in the welcome window.

   A default project opens up containing four layers.

2. From the **Layers** workspace, ensure that the **METAL_1** layer is selected.
3. Draw two adjacent 2x4mm planes, with a separation of 0.5mm.
4. Use the **Padstack Editor** to select **M1_PAD** and place three pads on each of the planes.

The model should look like the following:



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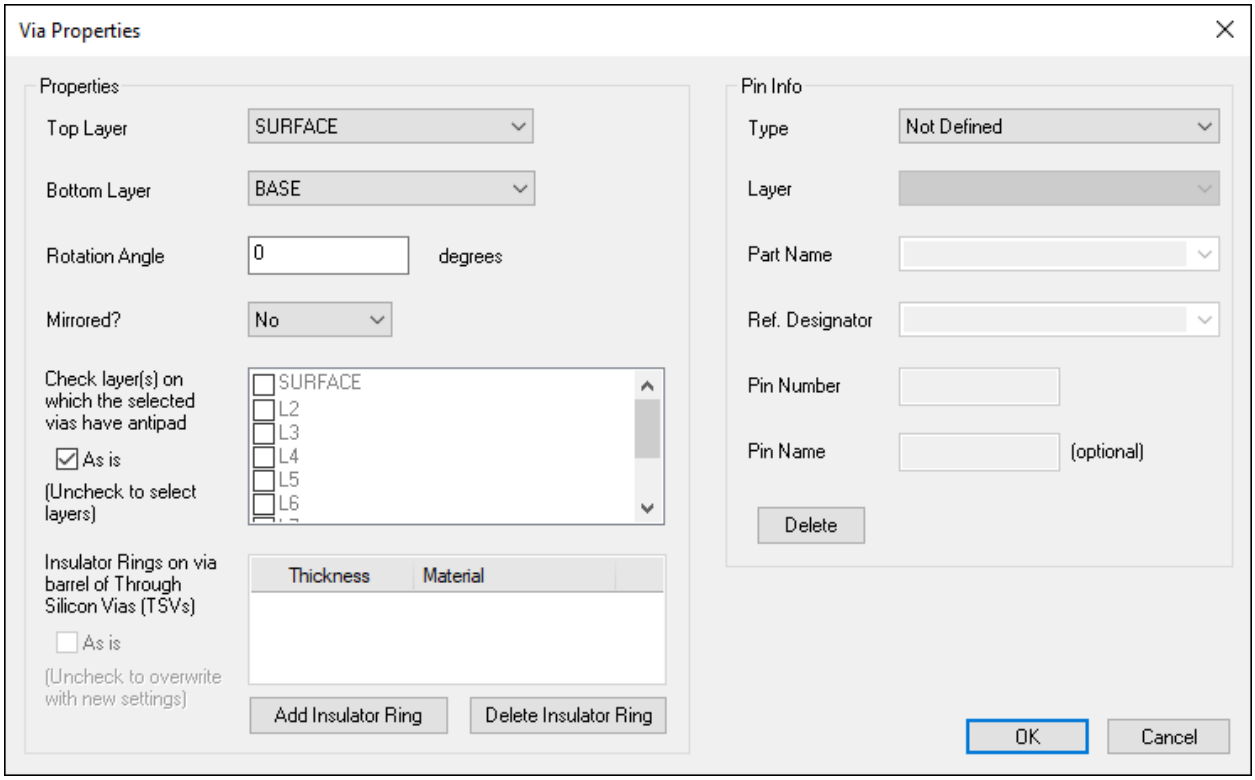
Creating a Sample Pin Group, Step 2: Create a Component

Perform the following steps:

1. **Ctrl+click** each pad to select all six pads.
2. Click **Advanced** > **Via**.

   The **Via Properties** window appears.



3. From the **Pin Info** area, specify the **Type**, **Part Name** and **Reference Designator**. The layer is already selected.
4. Click **OK**.

   The component displays as a black box in the Modeling workspace, and appears in the

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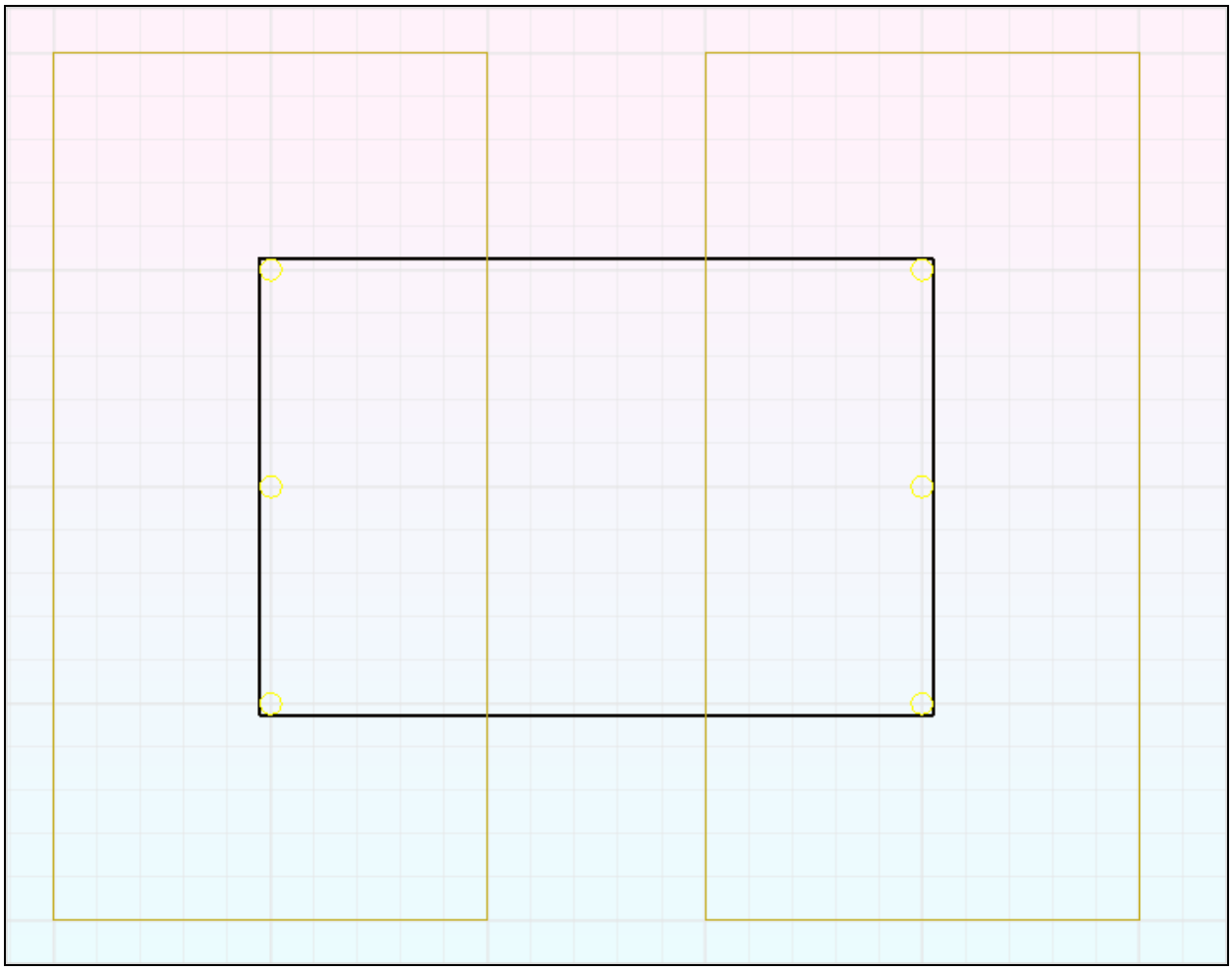
Components workspace under Integrated Circuits.



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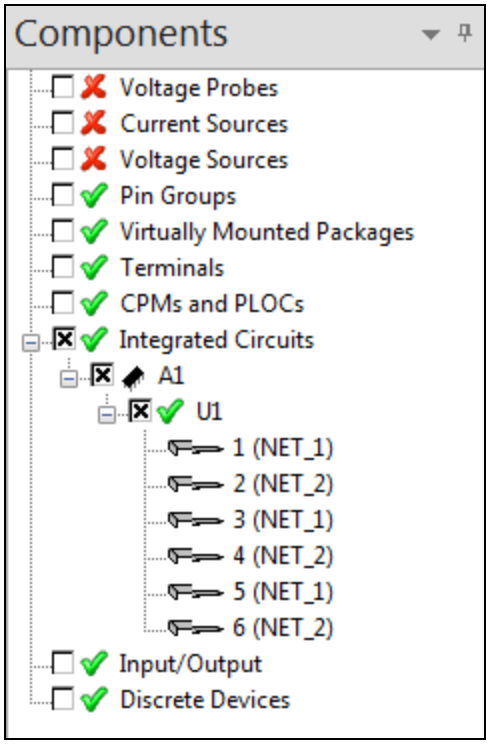

To move the component to another category in the Components workspace, drag it under an appropriate category.

Creating a Sample Pin Group, Step 3: Create a Pin Group

Perform the following steps:

1. From the **Modeling** workspace, select the component, right-click and select **Create/Manage Pin Groups** from the menu.

   The **Create/Manage Pin Groups** window appears.

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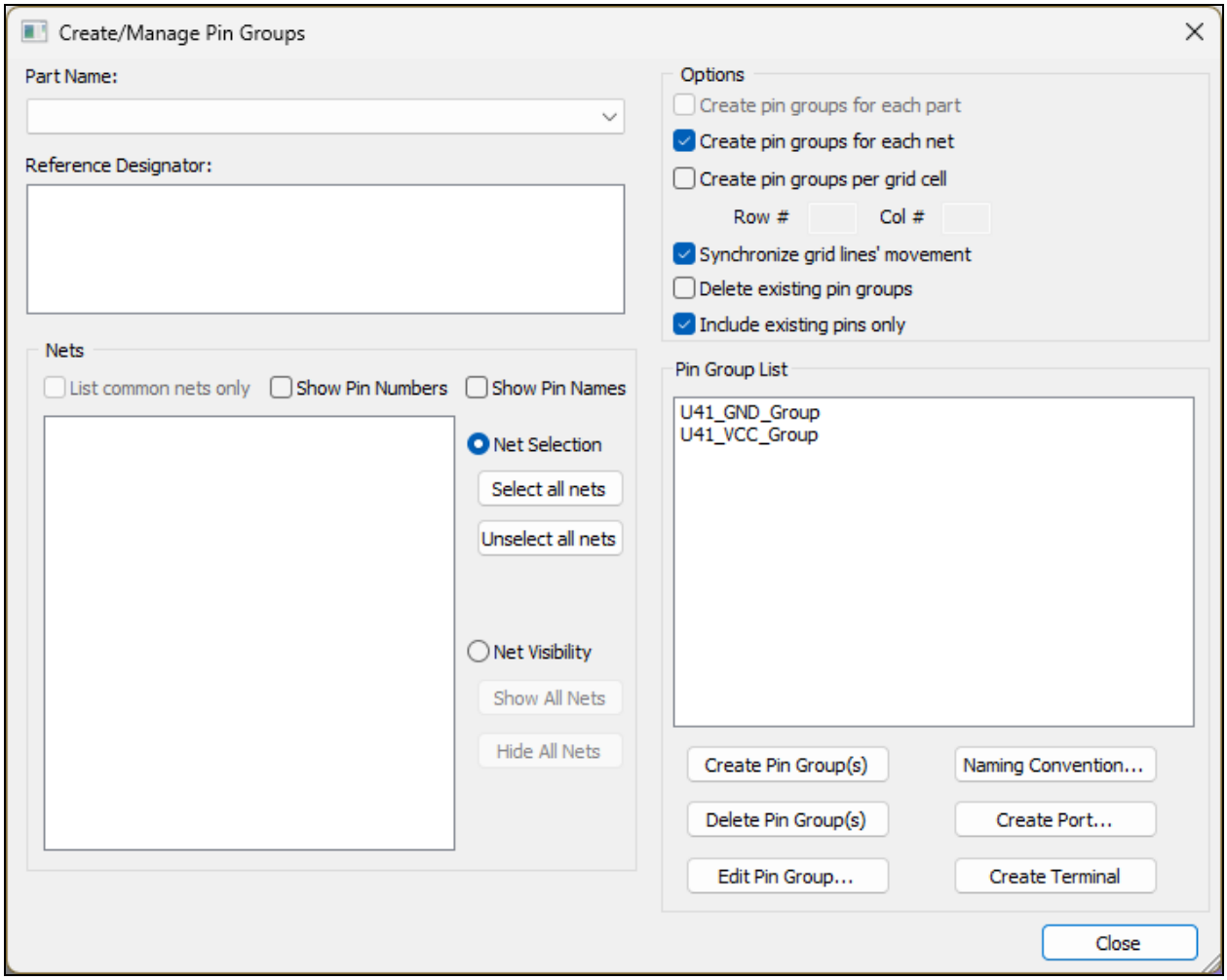

2. From the **Nets** area, use the check boxes to select the two nets.
3. From the **Options** area, ensure that **Create pin groups for each net** is checked.
4. Click **Create Pin Group**.

   Two pin groups are created: U1_NET_1_Group and U1_NET_2_Group.

   They appear in the **Components** workspace under **Pin Groups**.

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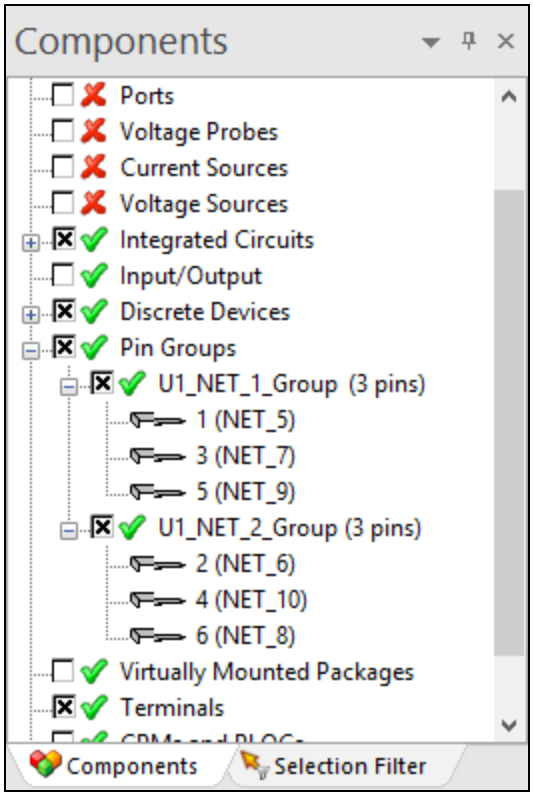

To edit pin groups:

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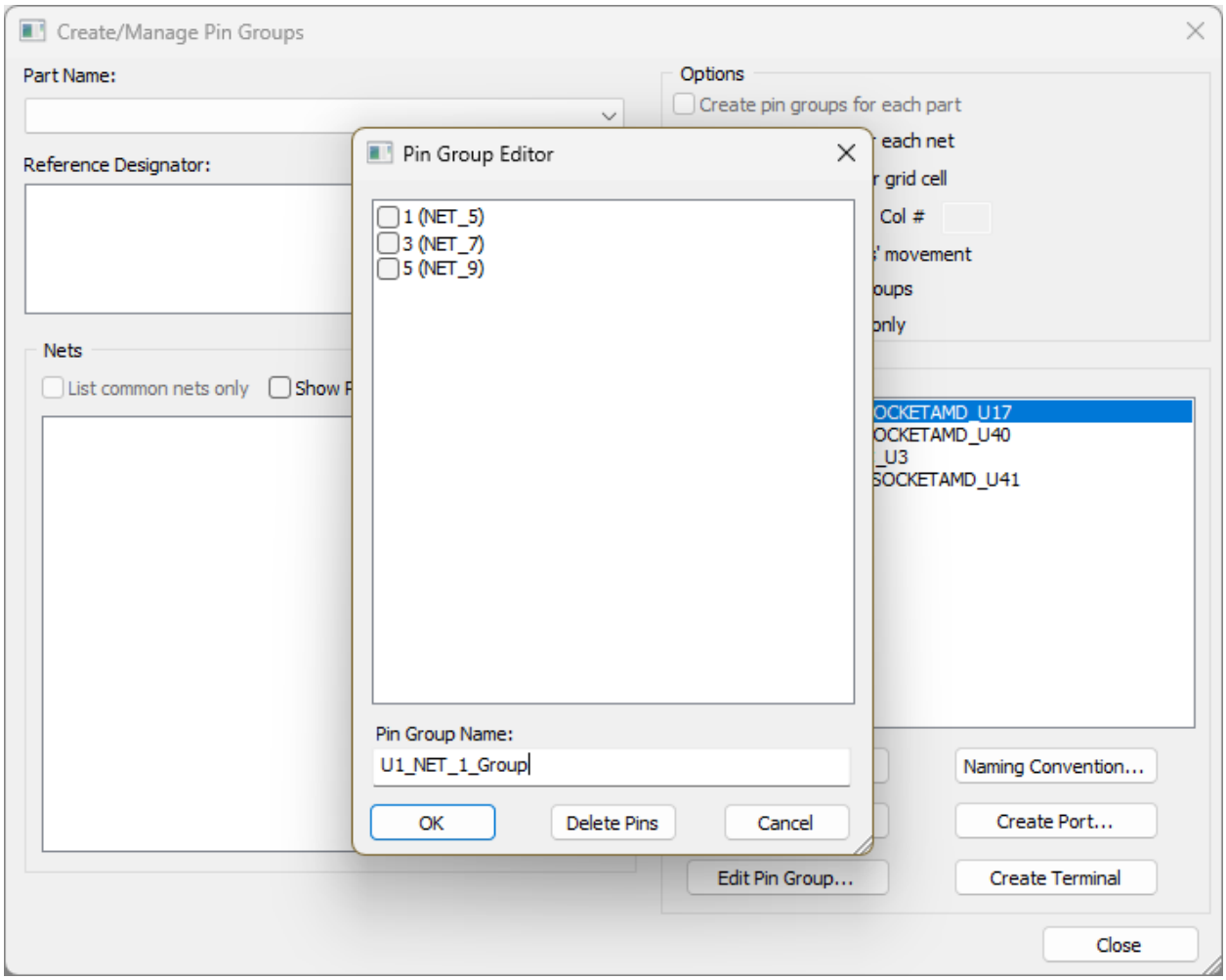
1. From the **Components** workspace, right-click a pin group and select **Edit Pin Group**.

   The **Pin Group Editor** window appears.



2. Select and delete pins or rename the pin group. Then click **OK**.

Creating a Sample Pin Group, Step 4: Create a Port

Create a port between the two pin groups:

1. From the **Modeling** workspace, select the two pin groups.
2. Click **Tools** > **Generate Circuit Element on Components**.

   The **Circuit Element Generation Dialog** appears.

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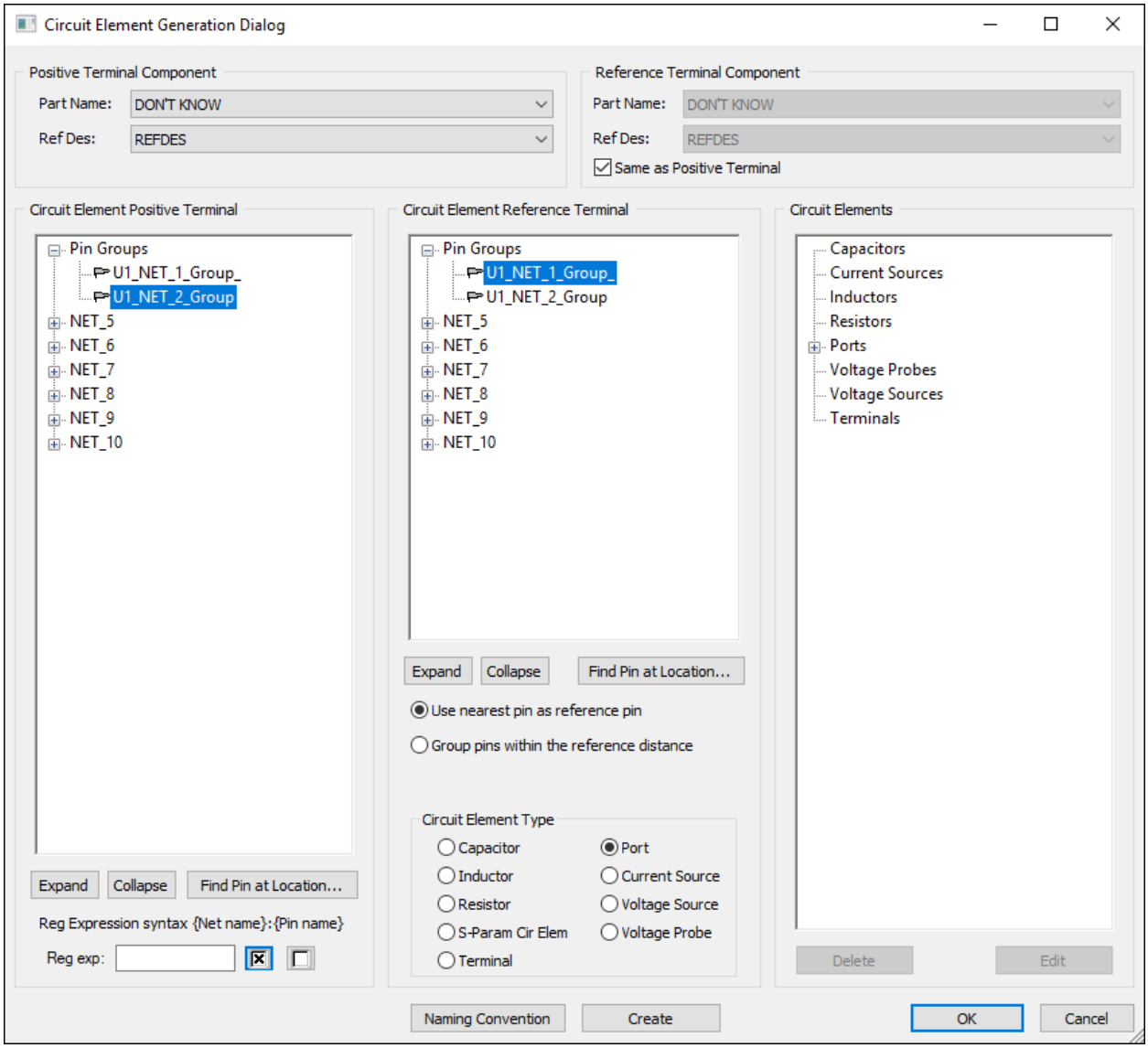

3. From the **Circuit Element Positive Terminal** area, select **U1_NET_2_Group** as the positive terminal.

   Note: If individual terminals need to be selected, the pin group must be deleted.

4. From the **Circuit Element Reference Terminal** area, select **U1_NET_1_Group** as the negative terminal.

   Note: If individual terminals need to be selected, the pin group must be deleted.

5. From the **Circuit Element Type** area, ensure that **Port** is selected.
6. Click **Create**.

   The **Port Properties** window appears.

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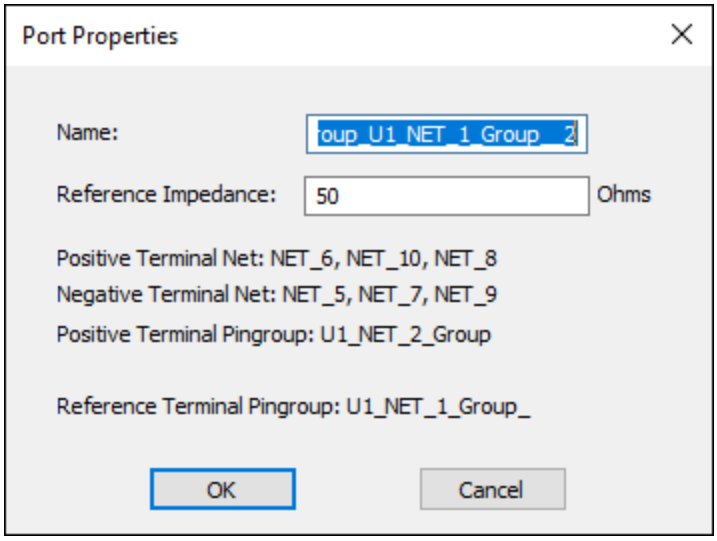

7. Leave the default **Name** and **Reference Impedance**.
8. Click **OK** to exit the **Port Properties** window.
9. Click **OK** to exit the **Circuit Element Generation Dialog**.

The port appears in the Modeling workspace, with positive terminals highlighted in red and negative terminals highlighted in green.

Click the port to display pin group names.

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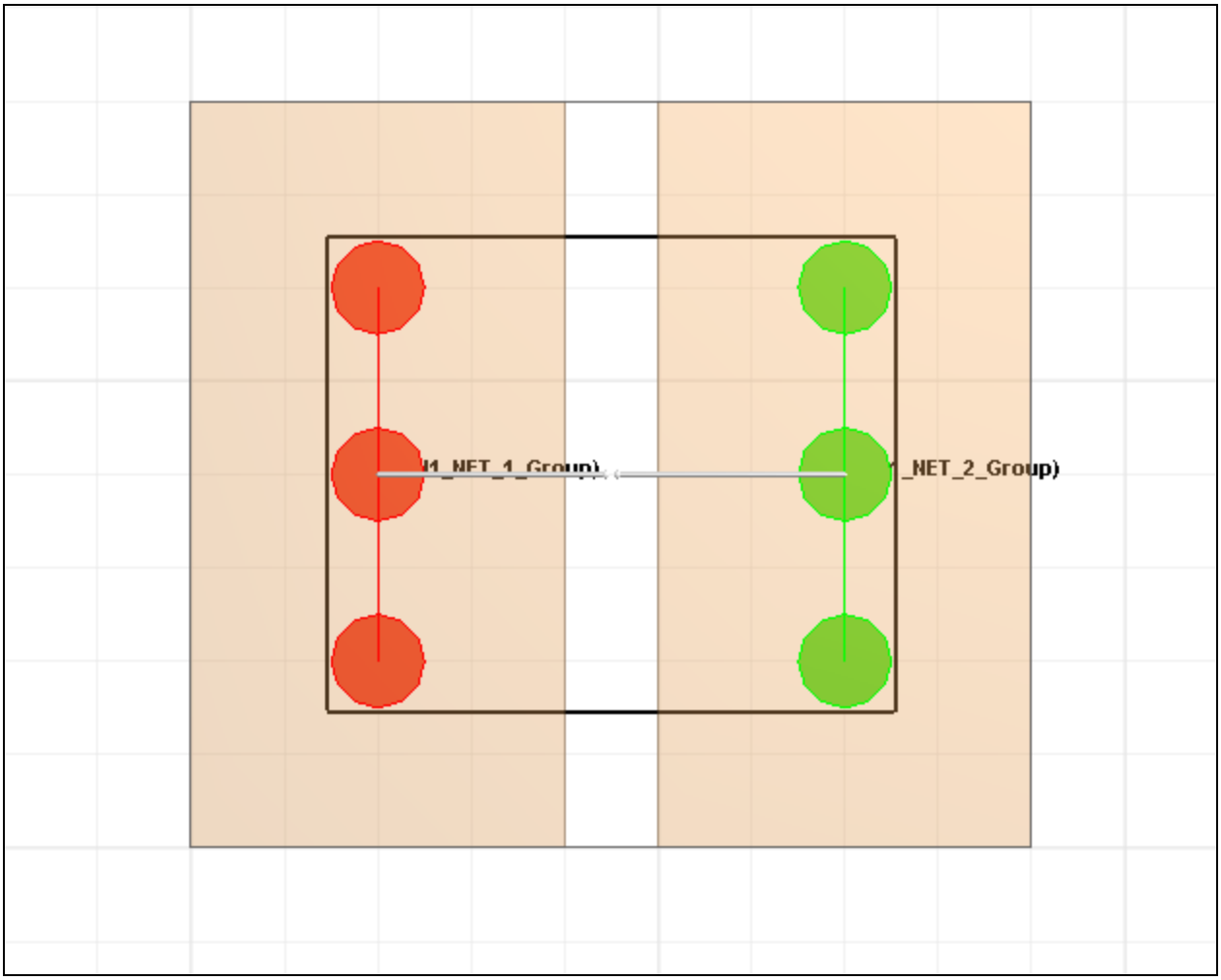

DC IR Solution Technical Notes

For a DC IR solution, the result is Pass if the total current is less than or equal to the current limit flowing through the element.

The current limit is defined as

$$I_{\text{limit}} = \tau A$$

Where:

- τ is a user-defined quantity, in $\frac{A}{m^2}$. You can edit its value in the **dc_coeff.txt** file stored under **<install_root>\SIwave**
- *A* is the cross-sectional area of conductor

For bondwires, *A* is defined as:

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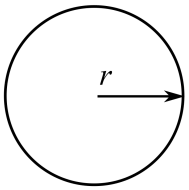
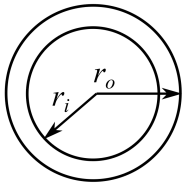
$$A = \pi r^2$$



For vias, *A* is defined as:

$$A = \pi \left({r_o}^2 - {r_i}^2 \right)$$



Djordjevic-Sarkar Model

The Djordjevic-Sarkar model is a causal, frequency-dependent dielectric model developed specifically to model the FR-4 epoxy resin material used commonly in printed circuit boards. It is also useful for many other low-loss insulator materials. The formula for the complex permittivity in this model is given by Formula One (1):

$$\varepsilon(\omega) = \varepsilon_\infty + \frac{\Delta\varepsilon}{\ln(\omega_B/\omega_A)} \ln\left(\frac{\omega_B + \mathrm{j}\omega}{\omega_A + \mathrm{j}\omega}\right) + \frac{\sigma_0}{\mathrm{j}\omega\varepsilon_0}$$

Here, ε_∞ denotes the high-frequency (or optical) limit of the relative permittivity and $\Delta\varepsilon$ is the difference between the low-frequency (DC limit) of the relative permittivity and ε_∞.

σ_0 is the DC conductivity (typically zero for low-loss dielectric materials). The model has lower and upper "corner frequencies" ω_A and ω_B respectively, which are described further below. All of these parameters are real-valued, and are computed for you from the material measurement data you provide.

The effective relative permittivity and conductivity for the Djordjevic-Sarkar model can be derived from the real and imaginary parts of Equation One (1) above.

Equation Two (2):

$$\varepsilon_r(\omega) = \varepsilon_\infty + \frac{\Delta\varepsilon}{2\ln(\omega_B/\omega_A)} \ln\left(\frac{{\omega_B}^2 + \omega^2}{{\omega_A}^2 + \omega^2}\right)$$

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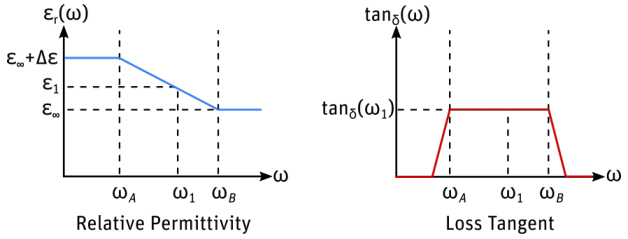
Equation Three (3):

$$\sigma(\omega) = \sigma_0 + \frac{\omega\varepsilon_0\Delta\varepsilon}{\ln(\omega_B/\omega_A)}\left[\operatorname{atan}\left(\frac{\omega}{\omega_A}\right) - \operatorname{atan}\left(\frac{\omega}{\omega_B}\right)\right]$$

The effective loss tangent is derived from the ratio of these:

$$\tan\delta(\omega) = \frac{\sigma(\omega)}{\omega\varepsilon_0\varepsilon_r(\omega)}$$

The frequency-dependent behavior of the relative permittivity and loss tangent are illustrated in the following figure. The frequency axis in this figure is shown on a *logarithmic* scale.



Some important points to note about these curves are:

- The low frequency relative permittivity is always higher than the optical permittivity.
- The relative permittivity decreases almost linearly (on a logarithmic frequency scale) between the two corner frequencies. Above and below this frequency range, it is essentially constant.
- The slope of the permittivity in the linear region is proportional to the loss tangent: a higher loss tangent results in a more rapid decrease of the permittivity.
- The loss tangent is nearly constant between the two corner frequencies. If the DC conductivity is zero, it rapidly decreases to zero outside this frequency range (If the DC conductivity is non-zero, then the loss tangent becomes infinite at DC).

Suppose that the relative permittivity ε_1 and loss tangent $\tan\delta(\omega_1)$ are given at a frequency ω_1 lying between the corner frequencies. Because the loss tangent determines the slope of the line, and the relative permittivity defines a point on the line, the line is completely determined by a single measurement. The only remaining parameters to be decided are the corner frequencies.

The upper corner frequency has not been observed in practice, and so it is set to a very high value ($10^{12}\,\mathrm{rad/s}$) The lower corner frequency will be determined by the DC permittivity, at the point where the flat DC part of the permittivity curve meets the linear part. If users do not provide the DC permittivity, the software will pick a value such that the lower corner frequency is on the order of 10 krad/s.

References

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A. R. Djordjevic, R. D. Biljic, V. D. Likar-Smiljanic and T. K. Sarkar, "Wideband Frequency-Domain Characterization of FR-4 and Time-Domain Causality," *IEEE Trans. on Electromagnetic Compatibility*, Nov. 2001, p. 662.

EMI Scanner Technical Notes

This section contains technical notes to aid in running EMI Scanner.

EMI Scanner Rule Setting Notes

Component Pin Grid Settings

Layout tools sometimes define a component's boundary box too large. For rules that check for whether a component falls inside the grid or outside the grid, this can lead to the rule thinking that a component is inside the grid when it is in fact outside the grid, although its boundary box still falls at least partially inside the grid. Users can change how EMI Scanner determines whether the component is inside or outside the grid in one of three ways:

1. Treat the component as inside the grid if any pin of the component is inside the grid. Use the following settings:

   " Require One Component/Capacitor Pin to be Inside Grid " = yes

   " Require ALL Component/Capacitor Pins to be Inside Grid " = no
2. Treat the component as inside the grid only if all the pins on the component are inside the grid. Use the following settings:

   " Require One Component/Capacitor Pin to be Inside Grid " = yes

   " Require ALL Component/Capacitor Pins to be Inside Grid " = yes
3. Treat the component as inside the grid if the component's boundary box intersects the grid. Use the following settings:

   " Require One Component/Capacitor Pin to be Inside Grid " = no

   " Require ALL Component/Capacitor Pins to be Inside Grid " = yes or no

Decoupling All Plane Combinations

When determining whether to select **Force All Plane Combinations to Be Decoupled**, consider the following stackup.

Assume the net references V02/V03 when on layer S02 and V04/V05 when on S04.

V02 --------------------

S02 ------+

V03 -----------|--------

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S03 |

V04 ----------|--------

S04 +-----

V05 ----------

For this case, you can have the tool either look for decaps connecting V02<->V04 and V03<->V05 or have it look for V02<->V04, V02<->V05, V03<->V04, and V03<->V05. By default, it will look for 1st ref layer to 1st ref layer and 2nd ref layer to 2nd ref layer (V02<->V04, V03<->V05). If you want the tool to decouple all ref plane combinations, set this value to YES.

I/O Net Classes

I/O net classes are as follows:

Class 1L – low speed intentional signals that leave the shielded enclosure.

Class 1H – high speed intentional signals that leave the shielded enclosure.

Class 2 – signals that leave the board on a cable and remain within the shielded enclosure.

Class 3 – signals that leave the board directly to another board and remain within the shielded enclosure.

Frequency Dependent Material Properties

The properties of some materials vary with the frequency of the field excitation. This frequency dependence is often linear within a certain frequency range and constant outside of the frequency range, as shown below:

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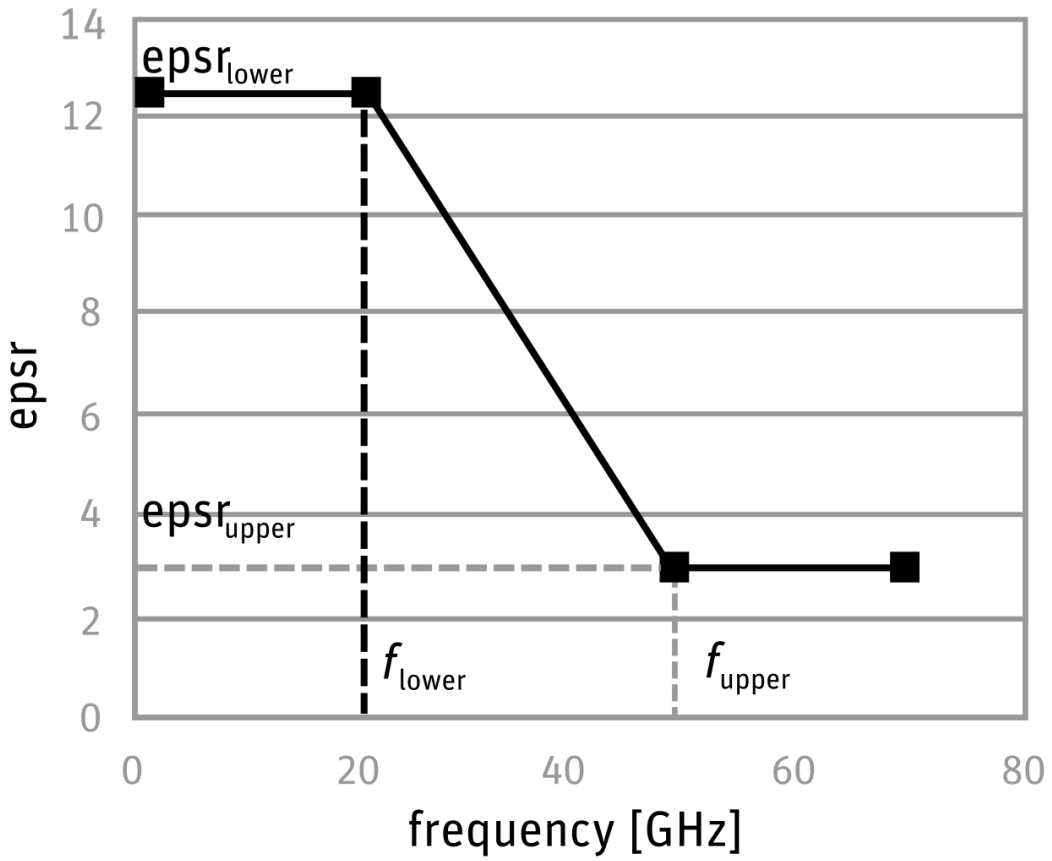

where

- $epsr_{lower}$ is the relative permittivity of a material below the frequency range 20 - 50 GHz.
- $epsr_{upper}$ is the relative permittivity of a material above the frequency range 20 - 50 GHz.
- f_{lower} is the lower frequency, below which the material property is constant.
- f_{upper} is the upper frequency, above which the material property is constant.

Frequency-dependent materials are appropriate for problems solved using a discrete or interpolating sweep.

Loss Tangent

Loss tangent is defined as the ratio of power loss in a dielectric material to the total power transmitted through the dielectric. It is equal to the tangent of the loss angle:

$$D_e = \frac{\varepsilon''}{\varepsilon'} = \tan\delta = \frac{1}{2\pi \mathrm{fC}_p R_p}$$

Where:

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f = frequency of applied voltage

C_p = equivalent parallel capacitance

R_p = equivalent parallel resistance

D = loss angle

Relative Permittivity

Relative permittivity is defined as the ratio of the permittivity of a material to the permittivity of a vacuum. The relative permittivity of all dielectrics is assumed to be complex:

$$\varepsilon = \varepsilon' + \mathrm{j}\varepsilon''$$

This can also be expressed as:

$$\varepsilon = \varepsilon' \left(1 - j\frac{\varepsilon''}{\varepsilon'}\right)$$

Where:

ε′ is the real portion of ε

$\frac{\varepsilon''}{\varepsilon'}$ is the dielectric loss tangent.

Full Wave Subcircuits

Four formats are available for a full wave subcircuit: Maxwell SPICE, HSPICE, Spectre, and Nexxim.

- **Maxwell SPICE**

  Full-wave SPICE models use a proprietary convolution-based technique to simulate high-speed structures. S-parameter matrices are computed at an evenly spaced set of frequency points (specified by **Num Points** and **Max Frequency**). This data is then written out in a form suitable for simulation in SPICE. The resulting model represents full-wave effects accurately. An added advantage is that it captures the frequency-dependence of the metal and dielectric losses.

- **HSPICE and Spectre**

  HSPICE models in SIwave employ a least squares fitting procedure to closely approximate the full-wave S-parameters with an HSPICE pole-zero model:

  $$S_{ij}(s) = c + \sum_{n=1}^{N} \left(k_n / (s - p_n)\right)$$

  Reduce the **appropriate Fitting Error** to obtain a closer approximation to the full-wave S-parameters.

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The minimum and maximum order parameters control the search for the number of poles *N*, when state-space fitting is by iterative rational function. The software attempts to find an approximation by first trying the minimum order and then checking the fitting errors. If it is too high, it raises the number of poles and tries again. The number of poles *per matrix entry* is never higher than the maximum order.

- **Nexxim**

  Nexxim also employs the least squares fitting procedure to closely approximate the full-wave S-parameters with an HSPICE pole-zero model. Nexxim provides time domain and frequency domain simulations from the same HSPICE compatible netlist or from the command line. SIwave allows a full wave parasitic extraction, and Nexxim allows the detailed verification.

Huray Surface Roughness Model

Surface roughness can increase conductor power losses by more than two times the loss associated with smooth conductors. In SIwave, a modification of the standard real-valued Huray surface roughness model is implemented to accurately account for these losses in both the frequency and time domains.

This modification fixes a causality problem with the original Huray model by adding some frequency-dependent reactance to the roughness-enhanced surface impedance. The purpose is to provide a complex-valued causal analytic model that exactly matches the loss results of the original model but is also suitable for time domain computations. The original Huray model was limited to calculations in the frequency domain and did not account for the effects of roughness on the phase of the transmitted signal. These limitations have been eliminated. The enhanced causal model provides accurate broad-band modeling of the losses in very rough copper foils (typically used in printed circuit board manufacturing), as did the original model, but also accurately predicts increased phase delay due to the surface roughness. because of its suitability for time domain computations.

Essentially, the smooth surface impedance (Z_{smooth}) is increased by a complex “Huray” factor (H_c), a function of frequency, given by the following formula:

$$H_c\left(j\omega\right) = 1 + \frac{K}{1+\left(\frac{j2\omega}{\omega_0}\right)^{-1/2}}$$

where:

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- ω is the frequency in radians/second
- ω_0 is a corner frequency:

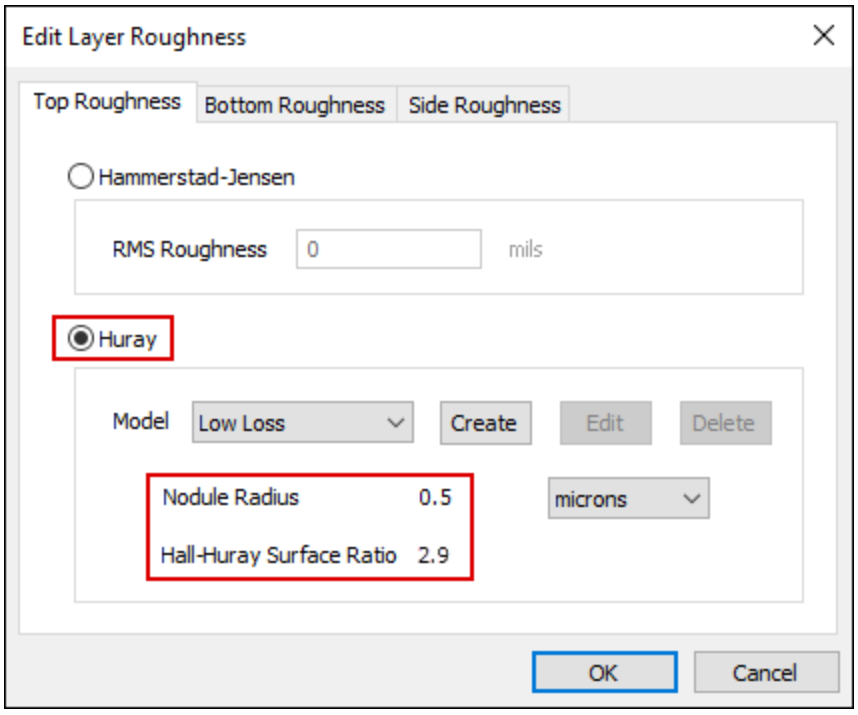
$$\omega_0 = \frac{2}{a^2 \mu \sigma}$$

- K is a derived constant used to simplify the equation:

$$K = \frac{3}{2} * SR = \frac{6\pi a^2 N}{A_f}$$

- a is the radius of a spherical nodule

> **Note:**
> a and SR are the two parameters you must enter in the *Edit Layer Roughness* dialog box when you select the *Huray* surface roughness model:



- μ is the permeability of free space = 4π * 1e-7 H/m
- σ is the electrical conductivity in Siemens/m
- N is the number of nodules

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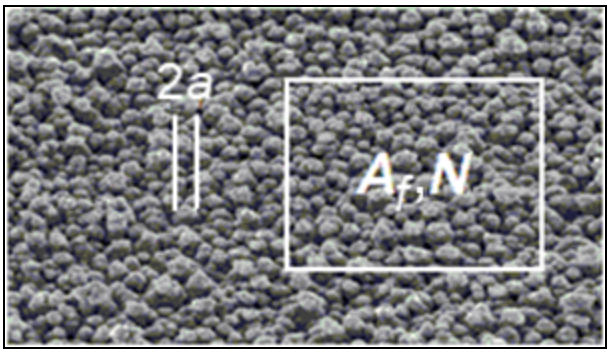
- A_f is a unit cell area

The following image of a magnified rough copper surface helps to clarify the a, A_f, and N parameters previously defined:



Note:

For more information about this complex causal Huray model – its necessity, background, derivation, proof of accuracy, and consistency with the original real-valued model – see the following article:

- J. Eric Bracken, ANSYS Inc., "*A Causal Huray Model for Surface Roughness*", DesignCon 2012, January 2012

This article is available from various online sources.

Once the Huray surface roughness factor is determined, the rough surface impedance (Z_{rough}) is determined as follows:

$$Z_{\text{rough}} = H_c * Z_{\text{smooth}}$$

References:

1. P.G Huray, S.G Pytel, S.H Hall, F. Oluwafemi, R.I. Mellitz, D. Hua, and P. Ye, "Fundamentals of a 3-D "Snowball" Model for Surface Roughness Power Losses", 11th Annual IEEE SPI Proceedings, May 13 – 16, 2007.
2. S.H Hall, S.G. Pytel, P.G Huray, D. Hua, A. Moonshiram, G. Brist, and E. Sijercic, "Multi-GHz, Causal Transmission Line Modeling Methodology with a Hemispherical Surface Roughness Approach", IEEE Transactions on Microwave Theory and Techniques, December 2007 pp 2614 – 2624.

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3. S.G Pytel, P.G Huray, A. Moonshiram, S.H Hall, R.I Mellitz, G. Brist, F. Oluwafemi, H.M Meyer, L. Walker, and M. Garland, "Analysis of Copper Treatments and the Effects on Signal Propagation", 58th Annual IEEE ECTC, May 26 – 30, 2008, pp 1144 – 1149.
4. S.G Pytel, "Multi-gigabit data signaling rates for PWBs including dielectric losses and effects of surface roughness", PhD. Dissertation, University of South Carolina, 2007.
5. P.G Huray, O. Oluwafemi, J. Loyer, E. Bogatin, and X. Ye; "Impact of Copper Surface Texture on Loss: A Model That Works", DesignCon 2010, February 1 - 4, 2010.
6. J. Eric Bracken, ANSYS, Inc., "A Causal Huray Model for Surface Roughness", DesignCon 2012, January 2012

Lumped Analysis

For applications such as IC packages with moderate signal speeds, it may be sufficient to characterize an entire conductor using only one section. This approximate model is referred to as a "lumped" model because all the distributed circuit elements have been collapsed into a single element. In this case, single-element lumped models may be constructed to model the time delay from one end of the conductor to the other. If crosstalk is considered, then a multiple conductor lumped model can be generated, which includes the inductive and capacitive couplings among the different conductors.

Meshing Technical Notes

To carry out a finite element analysis, the model is divided into a number of small discrete pieces. Meshing is the process of breaking up a physical domain into smaller sub-domains (elements) in order to facilitate the numerical solution of a partial differential equation.

From the *bottom-up approach* to mesh generation, vertices are meshed first, followed by curves, then surfaces and finally solids. Nodes are placed first at all vertices of the geometry and are then distributed along geometric curves. The result of the curve meshing process provides input to a surface meshing algorithm, where a set of curves define a closed set of surface loops. Decomposing the surface into well-shaped triangles or quadrilaterals is the next phase of the meshing process.

Technical Note Topics

Adaptive Mesh Refinement

Finite Element Method

Advanced Geometry Processing Options

Finite Element Method

The following are some of the characteristics of Finite Element Method (FEM):

FEM Discretization

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The starting point of the FEM is the subdivision of the domain into small subdomains called elements. An element is described by its vertices and one point on each edge. These points are called the nodes. The FEM mesh is constituted by the nodes and the elements.

Continuous Mesh

The mesh has to be continuous. If two elements touch, then the set of the common points has to be an edge or a vertex of each of the elements.

Structured & Unstructured Meshes

Structured meshes are characterized by regular connectivity. All interior chord nodes (on the extremities) of a structured mesh are connected to the same number of element edges. Unstructured meshes allow any number of elements to meet at a single chord node.

Mesh Requirements

FEM has certain requirements on a mesh:

- The mesh must be valid (no holes, self-intersections, or faces joined at two or more edges).
- The mesh must conform to the boundary of the domain.
- The density of the mesh must be controllable, to allow trade-off between accuracy and time.

Mesh Density

Choosing the correct mesh density required to solve a problem is an important factor. If the mesh is too coarse, then the element will not allow a correct solution to be obtained. Alternatively, if the mesh is too fine, the cost of analysis in computing time can be out of proportion to the results obtained.

A Good Mesh

A good or appropriate mesh is one that enables accurate resolution of the underlying physical phenomena, yet is coarse enough to allow a fast solution time.

Adaptive Mesh Refinement

DC current/voltage computation performs adaptive mesh refinement. An adaptive analysis is a solution process in which the mesh is refined iteratively in regions where the error is high, which increases the solution's precision. You set the criteria that control mesh refinement during an adaptive field solution. Many problems can be solved only by using adaptive refinement.

The general process followed during an adaptive analysis is:

1. SIwave generates an initial mesh.
2. Using the initial mesh, SIwave computes the current density that exist inside the structure when it is excited at the solution frequency.

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3. Based on the current finite element solution, SIwave estimates the regions of the problem domain where the exact solution has strong error. Triangles in these regions are refined.
4. SIwave generates another solution using the refined mesh.
5. SIwave recomputes the error, and the iterative process (solve, error analysis, refine) repeats until the convergence criteria are satisfied or the requested number of adaptive passes is completed.

Advanced Geometry Processing Options

SIwave requires at least one reference ground plane to build transmission line models for trace segments. The ground plane must be right above or below the center line of a trace section to act as a reference for trace segments. If no reference planes are found for a trace segment, the segment is considered unreferenced. No definite transmission line models can be built for unreferenced traces.

One common scenario that causes unreferenced traces is routing traces across voids in metal planes or via anti-pads. Sections of the trace routed over the voids become unreferenced trace sections. Unreferenced traces are processed specially within SIwave solver.

If the voids are small enough, omitting them and simulating the plane as solid may yield more accurate results and improved performance. From the **SI/PI Advanced** tab of the **SIwave Options** window, under **Geometry Processing**, the setting **Do not mesh voids smaller than** serves as a threshold for whether voids can be omitted (i.e., defeatured) from simulation, and is present in AC, DC, CPA, and PSI simulations.

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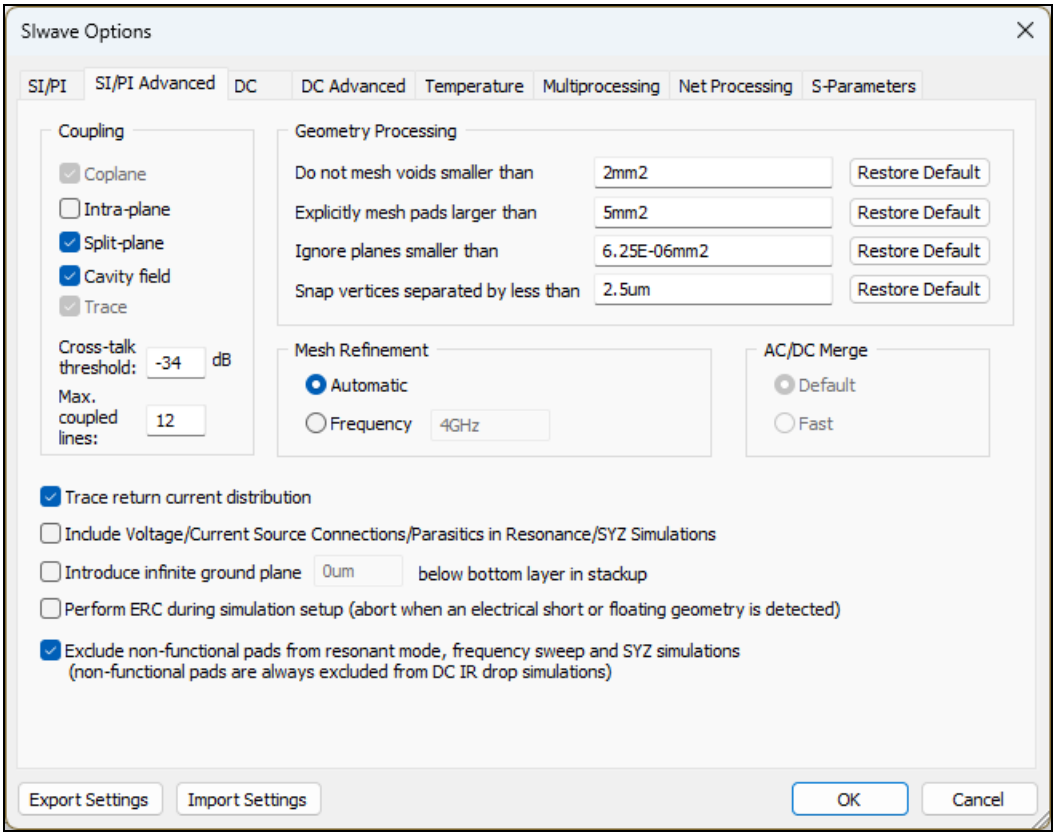

Note:

Since omitting small voids affects plane, via, and trace modeling, selecting a proper threshold is of the utmost importance. Since release 2020 R2, SIwave has implemented a more consistent approach for dealing with unreferenced sections of signal lines, thus eliminating any artificial effects that might creep into the results. This change could potentially affect SYZ results in cases where unreferenced trace effects are pronounced. Ansys recommends using SIwave default settings (in this case, $2mm^2$) to produce consistent results across versions.

Before or after simulation, users can view the voids set to be defeatured.

Viewing All Voids

Before or after simulation, users can complete the following steps to highlight the defeatured voids in the design. This will not affect the design in any way.

1. Click **View**.
2. Navigate to the **Preview Defeatured Voids** drop-down menu arrow.

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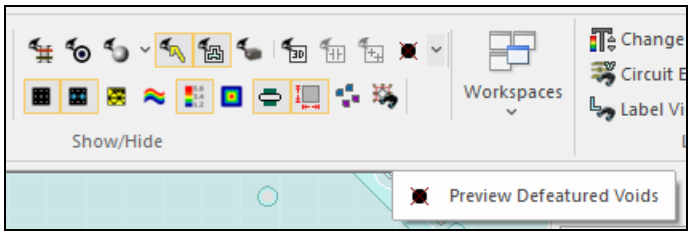
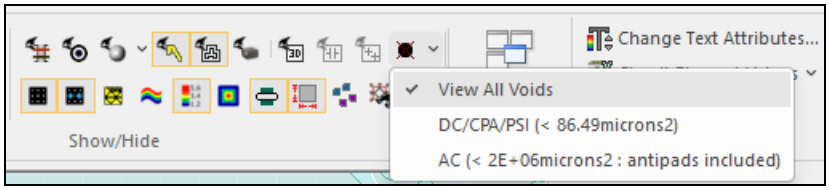
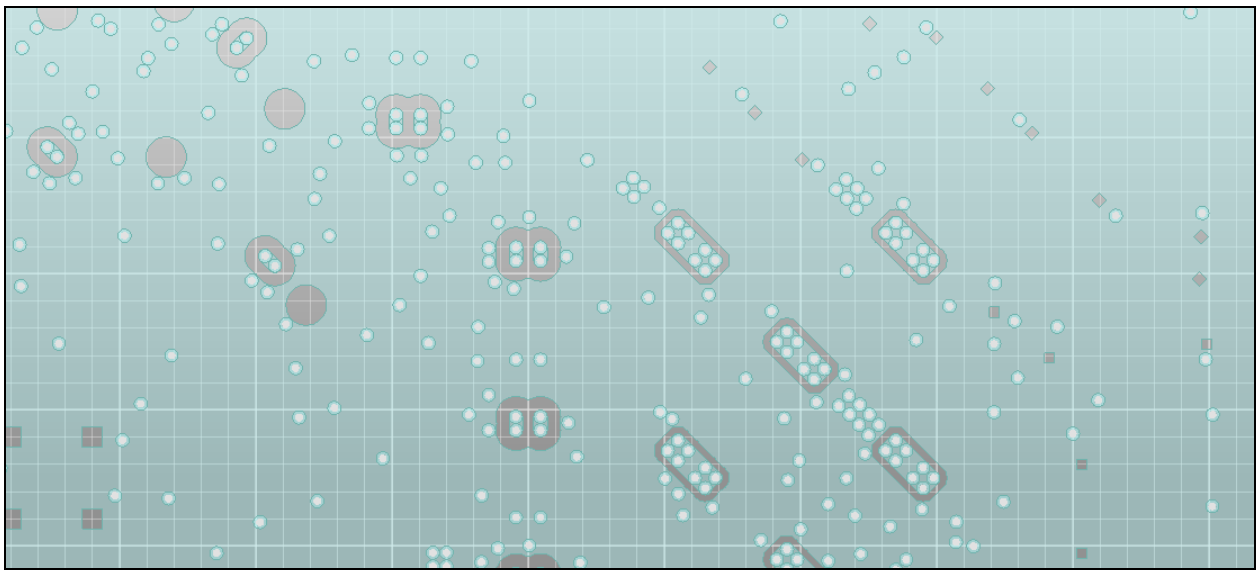


3. From the **Preview Defeatured Voids** drop-down menu arrow, select from the following:



- **View All Voids** — view all voids set by thresholds in DC, CPA, PSI, and AC simulation settings.
- **DC/CPA/PSI** (<value entered in the related options window>) — view all voids set by thresholds in DC, CPA, and PSI simulation settings.
- **AC** (<value entered in the related options window>) — view all voids set by thresholds in AC simulation settings.

4. Before selection, the **Modeling** workspace gives no indication of voids that will be ignored during simulation.



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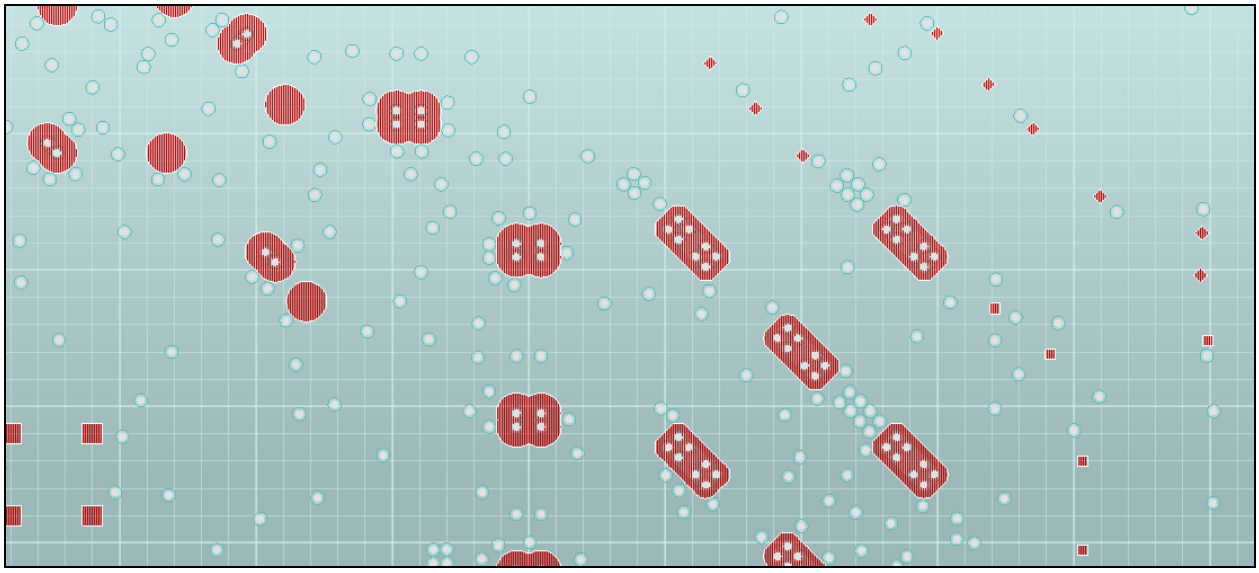
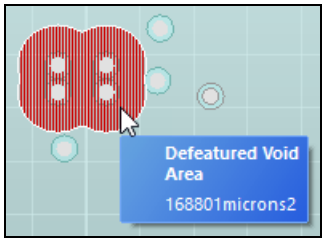
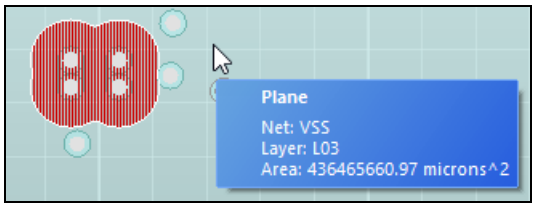
5. After selection, the **Modeling** workspace highlights voids that will be ignored during simulation in red cross-hatching.



6. Highlight a void to see its size (e.g., **168801microns^2**).



7. Highlight any featured area to see its location (i.e., **Net** and **Layer**) and size (i.e., **Area**).



Net Configuration File (*.ncf)

The ***.ncf** file is a simple text file containing a single line for each net.

Each line follows the format:

NET "Net Name" IMPORT=x CREATE_PORT=x REFNET="Reference Net Name"

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Each "x" should be replaced with a 0 or 1 to indicate whether the net should be imported and if ports should be created. The CREATE_PORT option is meaningless if IMPORT is 0.

ODB++ Translator

ODB++ is an ASCII open format developed by Mentor Graphics to capture CAD/EDA, assembly and PCB fabrication information. It has become the proprietary industry standard for formatting and transferring PC board data.

Ansys's ODB++ translator, **AnsTranslator**, allows you to utilize ODB++ and ANFv4 file formats to perform analyses of printed circuit boards in support of SIwave and PlanarEM. **AnsTranslator** takes as input an ODB++ v7.1 job structure and produces as output an ANFv4 or ANFv2 file and an SIwave component file (*.cmp).

- The input to **AnsTranslator** is an ODB++ v7.1 job structure—either as a compressed *.tgz file or an uncompressed top directory—and an optional control file (*.xml).
- The output from **AnsTranslator** is an ANFv4 file and a log file (*.log), or optionally an ANF v2 file and a component file (*.cmp).
- The information translated is a collection of geometric data that is sufficient to perform a useful analysis of the represented circuit for SIwave and PlanarEM designs (which support HFSS and Q3D as well).

> **Note:**
>
> The **AnsTranslator** process is subject to whatever limitations exist for the ANFv4 or ANF v2 format to represent ODB++ content.

Running AnsTranslator from the Command Line

The format for running **AnsTranslator** from the command line is:

`<AnsTranslator> <input> <output> <switches>`

Where:

- `AnsTranslator` is the complete path to AnsTranslator.exe
- `<input>` is the required path to the design to be translated
- `<output>` is the optional path to the edb directory. By default, the export type is edb. If no `<output>` is specified, the edb design is created in the same folder as the `<input>` file/folder.
- `<switches>` are any of the following options:
  - `-a(nfcmp)`

    Optionally used for ANFV2 import to specify a *.cmp file

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- `-c=controlFileName`

  Specifies the path to a control file (*.xml). If not specified, the control file is still used (*.xml) as long as it has the same name and path as the `<input>` file/folder.

- `-i=inputFormat`

  Specifies the file format for translator input. If not specified, the file type is deduced from the file extension. Gerber designs must be explicitly specified though this option.

  Options: AutoCAD, GDSII, Extracta, IPC2581, ODB++, Gerber, or anfv2

- `-l=logFilename`

  Specifies the path to log file (*.log). By default, the log file is created in the same folder as the `<output>` edb file.

- `-o=outputFormat`

  Specifies the output format. The default output is edb.

  Options: edb and ControlFile

- `-t=technologyFile`

  Specifies the path to a technology that defines a stack up. The file can be *.tech, *.layermap, *.ircx, *.vlc, *.tech, or *.itf. *.itf must have a mapping file specified with them. Use this switch when a technology file is provided. Do not specify a control file (-c) with this switch.

- `-f=filterfile.text`

  Use to specify all signal layers to import into the design as a list of layer names separated by end of lines. Via layers will only be imported if both the start and end layers are included in the list. The file can be *.ircx, *.itf, or *.vlc.tech. Requires a technology file (-t) switch.

- `-g=gdsMappingFile`

  Specifies the path to a GDS layer mapping file (*.map).

- `-a(nfcmp)`

  Optionally used for ANFV2 import to specify a *.cmp file

- `-v`

  Specifies verbose logging (without this option, only warnings and errors are logged).

- `-w=workingDirectoryName`

  Specifies the directory to use for any file manipulation needed by the translation. If not specified, the directory for the input is used as the working directory.

ODB++ Exporter Issues

The following known issues have been found regarding translated ODB++ directories. The problems occur when the contents of an ODB++ file do not completely conform to the Valor

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ODB++ specifications. The Ansys ODB++ Translator response varies depending on the nature of the problem, and an informative warning/error message is provided.

Extra text after the part-name of a CMP record in a components file

The one-word component part-name should be the final text before the terminating semi-colon in a CMP record (";"). Any extra text is ignored.

Example with the extra text in bold:

CMP 8 0.94074 0.3248 270.0 N J1 mPCIE **EDEGECONN** ;0=1,1=0.000010

Duplicate pin numbers in TOP records in a components file

Each toeprint record (TOP) for a component should have a distinct pin number. When a duplicate is found, the duplicate pin number is changed to an unused number and users are given a warning.

Example:

The bold pin numbers are duplicates.

...

TOP 14 -0.1284500 0.1181400 90.0000000 N 108 0 15

TOP 15 0.1284500 0.1181400 90.0000000 N 85 0 16

TOP 16 -0.1284500 0.1575100 90.0000000 N 109 0 17

TOP 17 0.1284500 0.1575100 90.0000000 N 7 0 18

TOP 18 0.0000000 0.3960000 90.0000000 N 1 0 G1

TOP **18** – 0.1140000 0.2820000 90.0000000 N 1 0 G1

TOP **18** 0.0790000 0.3530000 90.0000000 N 1 0 G1

TOP **18** – 0.0790000 0.3530000 90.0000000 N 1 0 G1

TOP **18** 0.1140000 0.2820000 90.0000000 N 1 0 G1

TOP 19 0.0000000 -0.3700000 90.0000000 N 1 0 G2

TOP **19** – 0.1140000 -0.2820000 90.0000000 N 1 0 G2

TOP **19** 0.1140000 -0.2820000 90.0000000 N 1 0 G2

TOP **19** 0.0790000 -0.3530000 90.0000000 N 1 0 G2

TOP **19** – 0.0790000 -0.3530000 90.0000000 N 1 0 G2

A NET record in an eda data file contains extra text

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The net name specified in the NET line of an eda data file should not contain spaces. If spaces are present, they are replaced with underscores. A warning is issued. This situation could happen when net names with spaces are exported without removing the spaces.

Example:

These NET lines from an edata/data file result in nets named JTG_ENA_TOP and JTG_ENA_PHY.

#NET 973

NET **JTG_ENA** TOP

...

#NET 974

NET **JTG_ENA** PHY

Duplicate pin names

Duplicate pin names within the same component — as defined by a PKG record in an eda data file. When a pin name is duplicated, the translator forces it to be unique by appending a number. A warning is issued.

Example with pin names 11 through 18 used twice in the PKG record:

PKG 2

PKG smnhda18.2_39_ni 0.03937 -0.4084999 -0.24 0.3825 0.24

RC -0.251 -0.24 0.502 0.48

PIN 1 S 0.15745 -0.1284499 0 U U

RC 0.14545 -0.1634499 0.024 0.07

PIN 2 S 0.15745 0.12845 0 U U

RC 0.14545 0.09345 0.024 0.07

PIN 3 S 0.11808 -0.1284499 0 U U

RC 0.10608 -0.1634499 0.024 0.07

PIN 4 S 0.11808 0.12845 0 U U

RC 0.10608 0.09345 0.024 0.07

PIN 5 S 0.07871 -0.1284499 0 U U

RC 0.06671 -0.1634499 0.024 0.07

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PIN 6 S 0.07871 0.12845 0 U U

RC 0.06671 0.09345 0.024 0.07

PIN 7 S 0.03934 -0.1284499 0 U U

RC 0.02734 -0.1634499 0.024 0.07

PIN 8 S 0.03934 0.12845 0 U U

RC 0.02734 0.09345 0.024 0.07

PIN 9 S -0.0000299 -0.1284499 0 U U

RC -0.0120299 -0.1634499 0.024 0.07

PIN 10 S -0.0000299 0.12845 0 U U

RC -0.0120299 0.09345 0.024 0.07

PIN 11 S -0.0393999 -0.1284499 0 U U

RC -0.0513999 -0.1634499 0.024 0.07

PIN 12 S -0.0393999 0.12845 0 U U

RC -0.0513999 0.09345 0.024 0.07

PIN 13 S -0.0787699 -0.1284499 0 U U

RC -0.0907699 -0.1634499 0.024 0.07

PIN 14 S -0.0787699 0.12845 0 U U

RC -0.0907699 0.09345 0.024 0.07

PIN 15 S -0.1181399 -0.1284499 0 U U

RC -0.1301399 -0.1634499 0.024 0.07

PIN 16 S -0.1181399 0.12845 0 U U

RC -0.1301399 0.09345 0.024 0.07

PIN 17 S -0.1575099 -0.1284499 0 U U

RC -0.1695099 -0.1634499 0.024 0.07

PIN 18 S -0.1575099 0.12845 0 U U

RC -0.1695099 0.09345 0.024 0.07

PIN G1 T -0.3959999 0 0 U U

CR -0.3959999 0 0.0125

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PIN G2 T 0.37 0 0 U U

CR 0.37 0 0.0125

PIN **11** S -0.0393999 -0.1284499 0 U U

RC -0.0513999 -0.1634499 0.024 0.07

PIN **12** S -0.0393999 0.12845 0 U U

RC -0.0513999 0.09345 0.024 0.07

PIN **13** S -0.0787699 -0.1284499 0 U U

RC -0.0907699 -0.1634499 0.024 0.07

PIN **14** S -0.0787699 0.12845 0 U U

RC -0.0907699 0.09345 0.024 0.07

PIN **15** S -0.1181399 -0.1284499 0 U U

RC -0.1301399 -0.1634499 0.024 0.07

PIN **16** S -0.1181399 0.12845 0 U U

RC -0.1301399 0.09345 0.024 0.07

PIN **17** S -0.1575099 -0.1284499 0 U U

RC -0.1695099 -0.1634499 0.024 0.07

PIN **18** S -0.1575099 0.12845 0 U U

RC -0.1695099 0.09345 0.024 0.07

Property line contains multiple words for property name

A property line (PRP) should contain a single-word property-name followed by a quoted string for the value. Some PRP lines have multiple words that precede the quoted value. In this case, it is assumed that the extra words are intended to be part of the property name and they are then concatenated together with underscores. A warning is issued.

Example:

PRP SIMULATION MODEL 'MAX2003'

Property line contains extra text after value

A property line (PRP) should contain a single-word property-name followed by a quoted string for the value. Some PRP lines have multiple-quoted values. The text after the first quoted value is ignored. A warning is issued.

Example:

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PRP PART LABEL 'RELE' TN2C'

Property line is missing value

A property line (PRP) should contain a single-word property-name followed by a quoted string for the value. Some PRP lines are missing the quoted value. When this occurs, the property is ignored. A warning is issued.

Example:

PRP Manufacturer

Discrepancy between component file and eda file

A correlation exists between the toeprints specified in the component file and those specified in the eda file. If the files are created incorrectly and their indexes do not match, the ODB++ Translator aborts translating the components file. Overall translation is continued, but components, padstacks, and nets are not translated. A warning is issued.

Negative net index specified in components file

Toeprints in a component file should have a positive net index. If the net index is negative, the ODB++ Translator aborts translating the components file. Overall translation is continued with padstacks and nets being translated, but components are not translated. A warning is issued.

Example with net index in bold:

TOP 1 6.31 7.9018001 0.0 N **-1** 0 2_3

The eda data file contains a trace subnet with a hole feature

Trace subnets (part of eda data file) should have only copper features as members. If holes are found as trace members, the hole feature is ignored. A warning is issued.

Example with hole feature in bold.

SNT TRC

FID H 6 4717

Features from multiple padstacks are listed in the same toeprint in the eda data file

The features listed for a toeprint in an eda data file are to be from the same padstack. When features from multiple padstacks are found in one toeprint warnings are issued. The first padstack is translated normally. Pads and hole from the other padstacks are merged into the first when possible.

Arc definition is incorrect

Arcs are specified in ODB++ directories with a start point, end point, and center point. The distance from the start point to the center should be the same as the distance from the end point

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to the center. If the two distances are different, an arc can not be created, and instead, the start and end points are used to create a segment (0 height arc). A warning message is issued.

Holes not specified in eda data file

Padstack via and pin holes are specified in the eda data file of the ODB++ directories. Following is an excerpt of an eda via specification. FID entries specify each part of a via: holes, pads, and antipads. Entries containing "C" are pads (copper), and entries containing "L" are antipads (laminate). Lines containing "H" specify holes, but there are no holes specified in this example because a known problem exists wherein hole features are not specified in the eda data file.

SNT VIA

FID C 2 8479

FID C 3 10992

FID L 4 1310

FID L 5 2414

FID L 8 1310

FID L 11 1310

FID L 14 2053

FID L 15 1310

FID C 16 5566

FID C 17 3399

If "H" lines were present they would be indicating which feature from which layer is to be used for the hole. Hole features are found on ODB drill layers. There is a drill layer defined in this ODB directory and it does have features. But because of a known problem, holes are not specified in the eda data file, so "H" lines are not present in the file.

A line in the feature file contains a non-numeric attribute value

The feature file contains lines that list numeric values which specify the setting of various attributes and options. The following feature line mistakenly contains an attribute with a string value instead of a numeric value.

P 3.6765000 2.4700000 0 P 0 0;0=0,**1=NO**,2=1

The attribute will not be used and a warning message is issued.

Non-numeric value for attribute on feature line in the features file

Feature lines may have attributes specified at the end of the line. The value for an attribute is omitted for boolean attributes. Otherwise it is an number representing either the numerical value

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for integer and float attributes, an option number for option attributes, or an integer referencing a string from the attribute text string section of the file. The feature line below has a value that is a string, rather than either being omitted or a number as is correct.

P 3.6765000 2.4700000 0 P 0 0;0=0,**1=NO**,2=1

The attribute will not be used and a warning message is issued.

Missing package name

The PKG record in the eda data file is missing the required package name. There should be a package name in the underlined space below.

PKG 0

PKG 0.1 -0.1275 -0.0275 0.9275 1.0275

Package contour hole before island in eda data file

A package contour specification for a footprint outline mistakenly specifies a **hole (H)** before it specifies the **island (I)** that could contain it. The hole is ignored and a warning is issued.

PKG 20

PKG T 0.03937 -0.2411574 -0.0492126 0.1688426 0.146504

CT

OB 0.0327165 0.040748 H

OS -0.068451 0.040748

OS -0.068451 0.040441

OS 0.0327165 0.040441

OS 0.0327165 0.040748

OE

OB -0.068451 0.0856299 I

OS 0.0327165 0.0856299

OS 0.0327165 0.1415828

...

Layout and ODB++ Control File

ODB++ directories do not contain certain information that is required by SIwave—in particular, material and layer characteristics (e.g., thickness). This information is often available in the original source program (e.g., Mentor Graphics). By specifying an input control file to the ODB++

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job that contains the materials and layer information, a usable design export can be obtained. The ODB++ Translator uses a control file that provides stackup information to Ansys Electronics Desktop and other related tools (Expedition from Version 7.9.4 on supports limited export of layer thickness).

The control file is in XML and can be created using standard third party text editors such as Notepad in Microsoft Windows or VI in Linux. The associated XML schema file, "stackup.xsd," is located in the parent installation directory. The schema file can be used with third-party editors or scripting tools that check XML syntax. Specific keywords that are valid to use in the control file can be found in the "stackup.xsd" schema. You are not required to use a control file when importing OBD++ files, however, stackup dimensions and material definitions will not be defined if you do not. If you do choose to use a control file when importing ODB++ files, you can later adjust the stackup either manually or by importing the control file into the design using the stackup window. If you import the control file, the stackup will be modified.

Following is a short example of a control file. The first three lines are heading lines that are required in all control files used with the ODB++ Translator. From the following example, after the heading lines, two other sections are present: one for materials and one for layers.

```
<?xml version="1.0" encoding="utf-8"?>

<Stackup xmlns="http://www.ansys.com/stackup"

         schemaVersion="1.0">

  <Materials>

   <Material Name="Solder_Mask">

      <Permittivity>

        <Double>1</Double>

     </Permittivity>

  <Materials>

    <Material Name="Dielectric_Material">

      <Permittivity>

        <Double>4.7</Double>

      </Permittivity>

  <Materials>

    <Material Name="Signal_Material">

      <Conductivity>
```


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```
        <Double>59880240</Double>
      </Conductivity>
     </Material>
    </Materials>
<Layers LengthUnit="mil">
      <Layer Name="DTOP" Type="dielectric" Material="Solder_Mask"
Thickness="3" />
      <Layer Name="LAYER_1" Type="conductor" Material="Signal_
Material" Thickness="0.7" />
      <Layer Name="D1-2" Type="dielectric" Material="Dielectric_
Material" Thickness="20" />
      <Layer Name="LAYER_2" Type="conductor" Material="Signal_
Material" Thickness="0.7" />
      <Layer Name="D2-3" Type="dielectric" Material="Dielectric_
Material" Thickness="20" />
      <Layer Name="LAYER_3" Type="conductor" Material="Signal_
Material" Thickness="0.7" />
      <Layer Name="D3-4" Type="dielectric" Material="Dielectric_
Material" Thickness="20" />
      <Layer Name="LAYER_4" Type="conductor" Material="Signal_
Material" Thickness="0.7" />
      <Layer Name="DBOT" Type="dielectric" Material="Solder_Mask"
Thickness="3" />
    </Layers>
</Stackup>
```

Using Excel to Generate an ODB++ Control File

It is possible to use XML schema functionality in Microsoft Excel to create stackup layer information that can then be exported to an ODB++ control file.

The schema is basically a set of rules (constraints) that define the structure and content (elements) of an XML file. Both XML and XML Schema documents (*.xml, *.xsd) are straightforward, user friendly text files, and Microsoft Excel offers an intuitive interface that "maps" elements in an XML schema to data cells in an ordinary worksheet. As such, and

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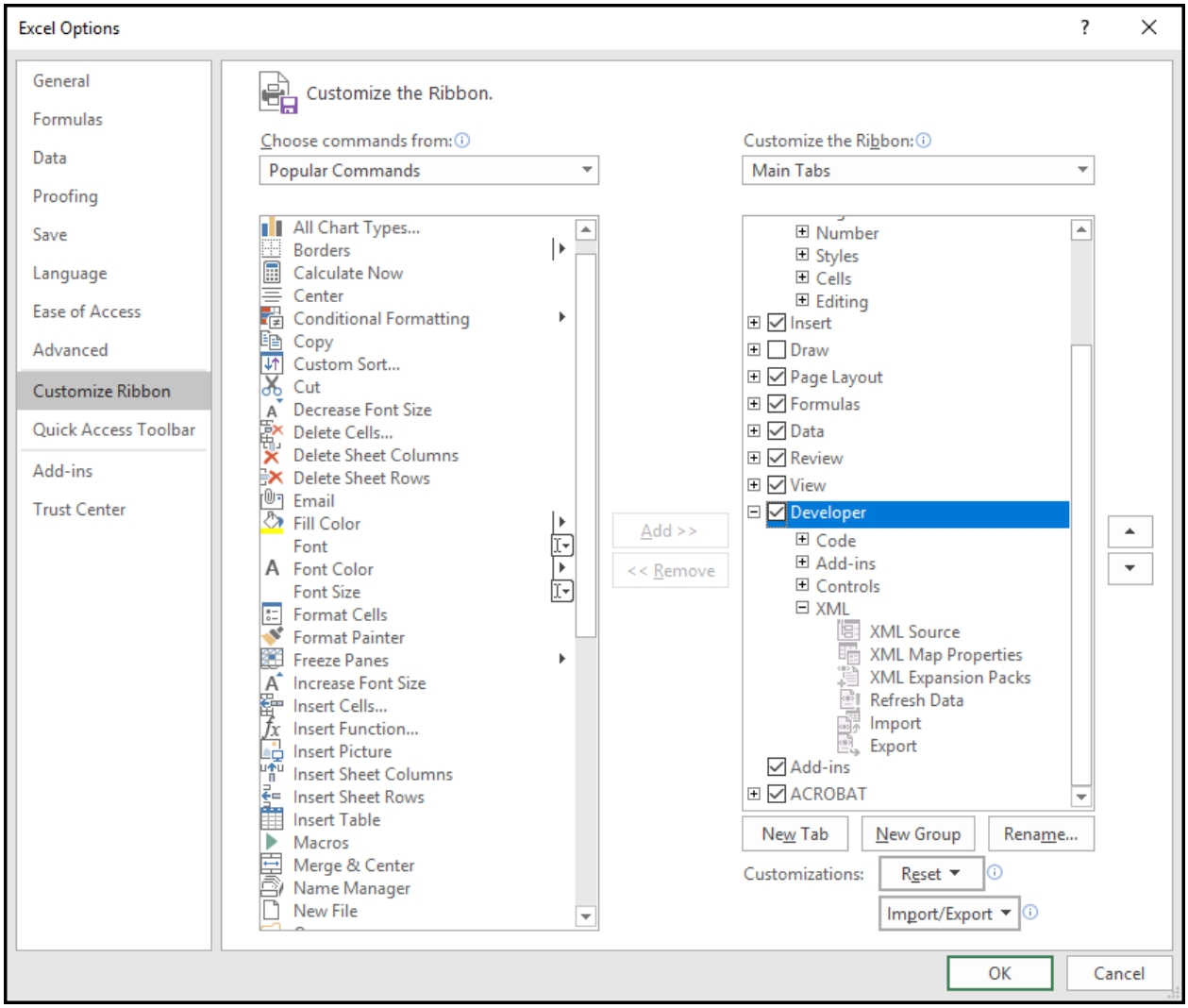
because the XML schema is quite simple, it is possible to use a plain-text XML editor in Microsoft Excel to create stackup layer controls that are suitable for Ansys electromagnetic tools. These controls can then be exported to an ODB++ Control File.

The schema used in the following example is shipped with SIwave and can be found at <*AnsysEM_installation_directory*>\Stackup.xsd.

This example uses Microsoft Excel 2016, but versions as early as Excel 2003 should be compatible:

1. To access the XML import/export functionality in Excel, you must first activate the **Developer** tab.

   If the Developer tab is not already visible, enable it in **Excel Options** > **Customize Ribbon**.



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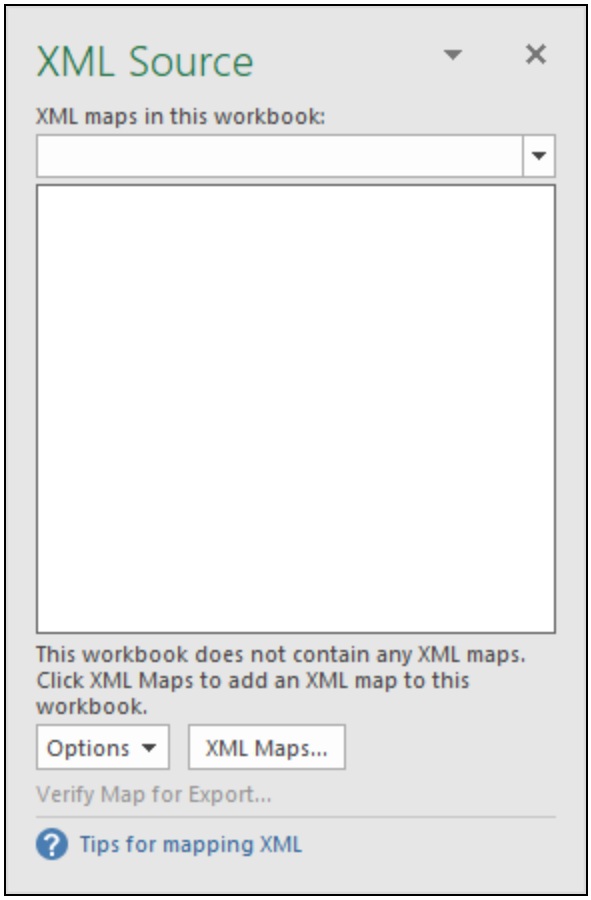
2. Open the spreadsheet file (*.xls or *.xlsx) that you wish to export to the control file.

   From the spreadsheet file, make sure there is at least one empty row preceding the cells you wish to export. If appropriate, delete any tags or headers.

3. On the **Developer** tab, click **Source** to open the **XML Source** task pane.



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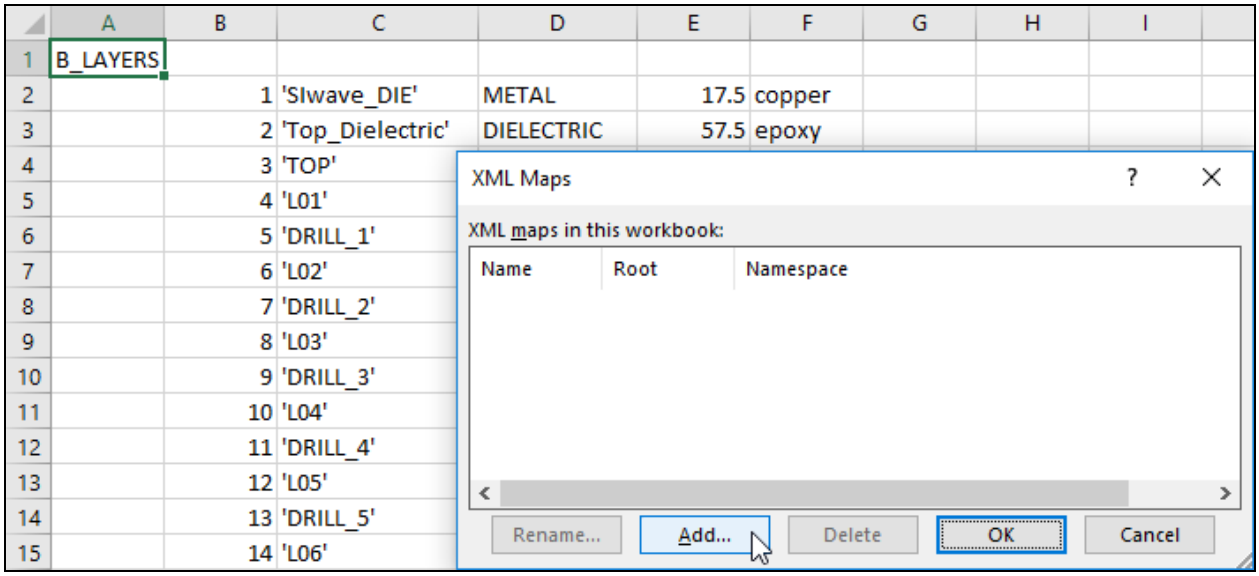
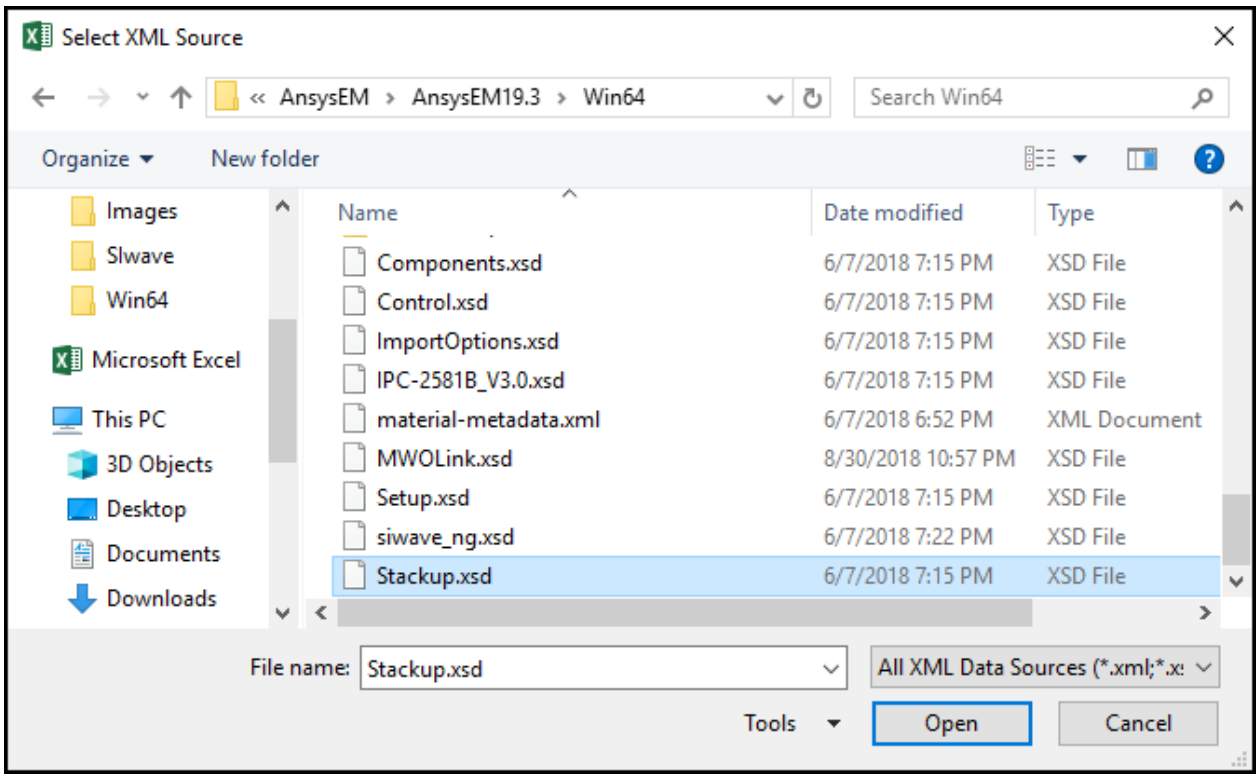
4. From the **XML Source** task pane, click **XML Maps** to open the **XML Maps** window.



5. Click **Add** to open the Select XML Source window. Browse to the Stackup.xsd file in the installation directory and click **Open**.



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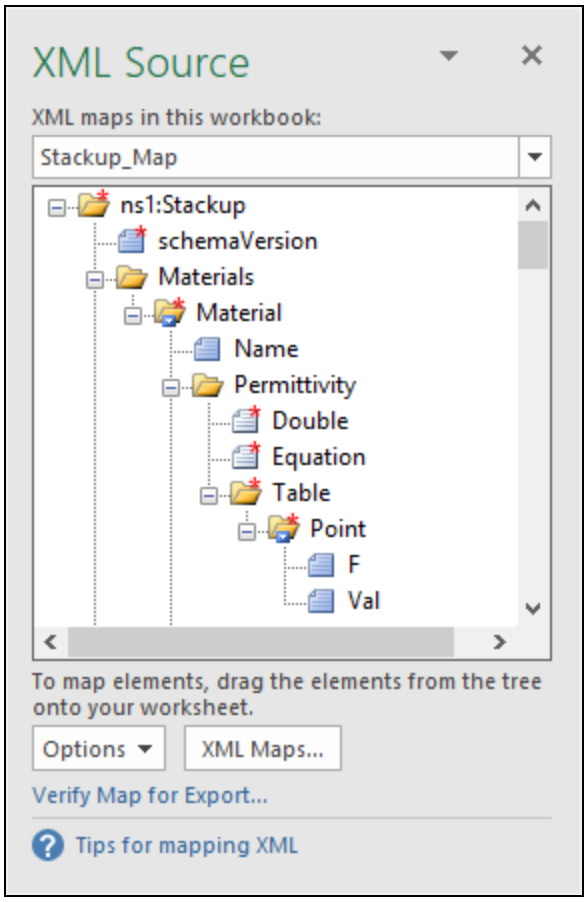
6. Click **OK** to close the **Source** window.

   The XML schema is loaded into the **XML Source** pane.



7. From the schema element list that appears in the task pane, elements with a red star are mandatory fields that you must map to cells in the worksheet. However, you do not need to map a starred element if its parent is not also starred.

   For most Excel files, you will need to add at least one cell in the worksheet that contains the schema version number — which is currently fixed at "1.0" — you can add it anywhere, but it must be formatted as "text", instead of the default format "number", so that the literal string will be exported. You may add additional fields to the worksheet, such as a layer-thickness unit, but this is not required. From the following image, the Schema Version and Layer Thickness Unit have been added to column H.

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	A	B	C	D	E	F	G	H
1	B_LAYERS							
2		1	'SIwave_DIE'	METAL	17.5	copper		1.0
3		2	'Top_Dielectric'	DIELECTRIC	57.5	epoxy		
4		3	'TOP'	DIELECTRIC	25	epoxy		mil
5		4	'L01'	METAL	15	copper		
6		5	'DRILL_1'	DIELECTRIC	30	epoxy		
7		6	'L02'	METAL	15	copper		
8		7	'DRILL_2'	DIELECTRIC	30	epoxy		
9		8	'L03'	METAL	15	copper		
10		9	'DRILL_3'	DIELECTRIC	30	epoxy		
11		10	'L04'	METAL	15	copper		
12		11	'DRILL_4'	DIELECTRIC	30	epoxy		
13		12	'L05'	METAL	15	copper		
14		13	'DRILL_5'	DIELECTRIC	30	epoxy		
15		14	'L06'	METAL	25	epoxy		

8. Many pre-existing layer stackup files may contain names or symbols that are different from those used by the XML Schema. These names will be flagged as errors, even if they represent the same entity. Because of this, these names must be replaced with valid entries before being exported to XML.

   For example, "METAL" is not a valid layer type, so it is replaced with "conductor."

   Additionally, XML is case-sensitive, so "DIELECTRIC" is replaced with "dielectric".

	A	B	C	D	E	F	G	H
1	B_LAYERS							
2		1	'SIwave_DIE'	conductor	17.5	copper		1.0
3		2	'Top_Dielectric'	dielectric	57.5	epoxy		
4		3	'TOP'	dielectric	25	epoxy		mil
5		4	'L01'	conductor	15	copper		
6		5	'DRILL_1'	dielectric	30	epoxy		
7		6	'L02'	conductor	15	copper		
8		7	'DRILL_2'	dielectric	30	epoxy		
9		8	'L03'	conductor	15	copper		
10		9	'DRILL_3'	dielectric	30	epoxy		
11		10	'L04'	conductor	15	copper		
12		11	'DRILL_4'	dielectric	30	epoxy		
13		12	'L05'	conductor	15	copper		
14		13	'DRILL_5'	dielectric	30	epoxy		
15		14	'L06'	conductor	25	epoxy		

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For a complete list of valid entries for each element, open the XML Schema document (*.xsd) in a text editor and search for the element name.

9. Map the XML schema to the workbook by dragging each element from the **XML Source** pane to the corresponding cell in the workbook. Mapped areas appear in blue nonprintable borders. Repeat this mapping operation for each element by dragging it into the workbook.

   For columns of data, drop the element on the cell directly above the top row in order to make it the header.

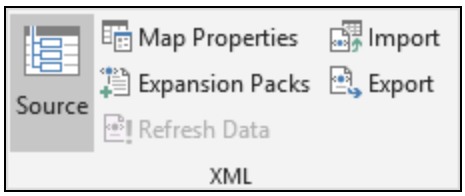
   For a single cell, simply drop the element on the cell itself.

	A	B	C	D	E	F	G	H
1	B_LAYERS	TargetLayer	Name	Type	Thickness	Material		
2		1	'SIwave_DIE'	conductor	17.5	copper		1.0
3		2	'Top_Dielectric'	dielectric	57.5	epoxy		
4		3	'TOP'	dielectric	25	epoxy		mil
5		4	'L01'	conductor	15	copper		
6		5	'DRILL_1'	dielectric	30	epoxy		
7		6	'L02'	conductor	15	copper		
8		7	'DRILL_2'	dielectric	30	epoxy		
9		8	'L03'	conductor	15	copper		
10		9	'DRILL_3'	dielectric	30	epoxy		
11		10	'L04'	conductor	15	copper		
12		11	'DRILL_4'	dielectric	30	epoxy		
13		12	'L05'	conductor	15	copper		
14		13	'DRILL_5'	dielectric	30	epoxy		
15		14	'L06'	conductor	25	epoxy		

10. To export to an XML file, use the **XML Source** pane to select the elements you wish to export. All corresponding mapped cells will be highlighted in the worksheet .

> **Note:**
>
> To select all, click ns1::Stackup.

11. On the **Developer** tab, click **Export**. From the **Export XML** window that opens, specify a name for the file. Click **Save** and the file is exported to XML.



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12. Review the XML File in a text editor or your software of choice.

```
<?xml version="1.0" encoding="UTF-8" standalone="yes" ?>

  <ns1:Stackup xmlns="http://www.ansys.com/stackup"
schemaVersion="1">

   <Layers LengthUnit='mil'>

    <Layer Name="'SIwave_DIE'" Type="conductor" TargetLayer="1"
Material="copper" Thickness="17.5" />

    <Layer Name="'Top_dielectric'" Type="dielectric"
TargetLayer="2" Material="epoxy" Thickness="57.5" />

    <Layer Name="'TOP'" Type="dielectric" TargetLayer="3"
Material="epoxy" Thickness="25" />

    <Layer Name="'L01'" Type="conductor" TargetLayer="4"
Material="copper" Thickness="15" />

    <Layer Name="'DRILL_1'" Type="dielectric" TargetLayer="5"
Material="epoxy" Thickness="30" />

    <Layer Name="'L02'" Type="conductor" TargetLayer="6"
Material="copper" Thickness="15" />

    <Layer Name="'DRILL_2'" Type="dielectric" TargetLayer="7"
Material="epoxy" Thickness="30" />

    <Layer Name="'L03'" Type="conductor" TargetLayer="8"
Material="copper" Thickness="15" />

    <Layer Name="'DRILL_3'" Type="dielectric" TargetLayer="9"
Material="epoxy" Thickness="30" />

    <Layer Name="'L04'" Type="conductor" TargetLayer="10"
Material="copper" Thickness="15" />

    <Layer Name="'DRILL_4'" Type="dielectric" TargetLayer="11"
Material="epoxy" Thickness="30" />

    <Layer Name="'L05'" Type="conductor" TargetLayer="12"
Material="copper" Thickness="15" />

    <Layer Name="'DRILL_5'" Type="dielectric" TargetLayer="13"
Material="epoxy" Thickness="30" />

    <Layer Name="'L06'" Type="conductor" TargetLayer="14"
Material="copper" Thickness="25" />

   </Layers>

  </nsl:Stackup>
```


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There are also free tools available online to validate an XML file against a given schema.

ODB++ Control File Part Mapping

During ODB++ translation, it is often appropriate to augment available data for purposes of simulation. One area where this is important is with component classification and value assignment. This supplementary information can be provided by using an XML Control file with a *Components/TypeMap* element.

The *TypeMap* element provides a sequence of either *Part* or *RefDes* elements. Each element specifies a Perl Regular Expression (http://perldoc.perl.org/perlre.html). A component's type and value are matched sequentially using the *TypeMap*, with *Part* elements evaluating against a part name and *RefDes* elements against the reference designator.

For example, a Control File mapping the type of components with reference designators beginning in 'L' to an inductor, 'R' to a resistor, and 'C' to a capacitor, is implemented as:

```
<?xml version="1.0" encoding="UTF-8"?>

<c:Control schemaVersion="1.0"
xmlns:c="http://www.ansys.com/control">

  <Components schemaVersion="1.0">

    <TypeMap>

     <RefDes Type="Inductor" RegEx="L.*"/>

     <RefDes Type="Resistor" RegEx="R.*"/>

     <RefDes Type="Capacitor" RegEx="C.*"/>

    </TypeMap>

  </Components>

</c:Control>
```

The regular expressions in the above example are mutually exclusive and, thus, do not rely on order for evaluation. A more complicated *TypeMap*, using part names, reference designators, and relying on order is:

```
<TypeMap>

  <RefDes RegEx="L.*" Type="Inductor"/>

  <RefDes RegEx="R.*" Type="Resistor" SR_Value="25ohm" />

  <Part RegEx="100nF" Type="Capacitor" SC_Value="100nF" SR_
Value="0.1ohm" />
```


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```
  <Part RegEx=".*nF" Type="Capacitor" SC_Value="0.1uF" SR_
Value="0.1ohm" SL_Value="0.1nH" />

  <RefDes RegEx="C.*" Type="Capacitor" SC_Value="1uF"/>

</TypeMap>
```

The following mappings should result:

Part Name	Refdes	Mapped To
AA-0.1nF	C21	Capacitor: (0.1uF,0.1ohm,0.1nH)
AB-1000nF-T	C22	Capacitor:(1uF)
100nF	C23	Capacitor: (100nF,0.1ohm)
100nF	L-C24	Inductor

Information regarding component type and values can be specified in the control file. If the component information is not in the control file, the translator looks for optional properties in the ODB++ component files if the component has 2 pins. If the component records in these files have property records TYPE and VALUE, the contents of these properties are used to determine component information. All comparisons are case independent.

The following table shows the type assigned to the component based on the TYPE property content:

TYPE property	Type assigned to the component
"resistor" or "embedded resistor"	resistor
"inductor"	inductor
"capacitor" or "embedded capacitor"	capacitor
Any other TYPE content 1. content does not begin with a number. 2. content begins with a number	**The content of VALUE is used to deduce the type** component is assumed to be discrete
without any following text	resistor

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TYPE property	Type assigned to the component
last letter is "h"	inductor
last letter is "f"	capacitor
following text includes "ohm"	resistor
last letter is a unit abbreviation ("p", "n", "u", "m", "k", "meg", "g", or "t")	resistor

Resonant Frequencies

Almost any PCB and chip package that contains power/ground plane structures has resonances at certain frequencies. Whether a resonance is excited depends on the location of a source and the frequency content of its signal.

The best way to view the natural resonances, and to what extent electromagnetic energy sources excite them, is to model the entire structure.

To model the structure:

1. Calculate the natural resonances/Eigen modes.

   Natural resonances are points at which the resonant frequencies are a function of the position of the PCB(s) and other components, and how/where the PCB ground plane bonds to the enclosure.

   SIwave employs a 2D Eigen solver to establish the natural resonant frequencies in the power-ground structure and the field distributions or *Eigenmodes* associated with them. The natural resonances are the resonances that may occur in the power/ground structure if there is an electromagnetic source that excites them. However, since the Eigen solver computes natural cavity resonances, no actual sources are involved.

2. Apply excitations.

   Modeling the application of one or more excitations establishes how they couple into the natural resonances. Excitations, over a range of frequencies, are applied at ports. At certain frequencies, typically the ones identified as Eigen frequencies earlier, little energy will be reflected back into the exciting port. The energy is trapped in an Eigen mode. Eventually, part of it will be dissipated in losses in the structure, and part of it will be accepted by ports. The fact that there is a dip in the return loss of a certain port at a certain frequency serves as a warning that an electromagnetic source at this location may excite a natural resonance at this frequency, usually leading to inappropriate behavior of the device. Based on this information, you can make changes, such as the insertion of decoupling capacitors, and then analyze the altered device.

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The resonant frequency analysis is typically followed by a frequency sweep of voltages and currents.

In Resonant Mode Analysis

The real part of the resonance frequency f_{res} is the frequency at which the mode oscillates. The imaginary part of the resonance frequency determines the rate at which the mode decays. The behavior of the mode vs. time in the absence of any excitation is calculated using:

$$A(t) = A_0 \cos\left(2\pi \cdot \mathrm{re}\left(f_{res}\right)t\right) \times e^{-2\pi \cdot \mathrm{im}\left(f_{res}\right)t}$$

Where A_0 is the initial amplitude at time t = 0, im() is the imaginary part, and k is the free space wave number, calculated as:

$$k = \mathrm{re}\left(f_{res}\right) \times 2\pi / c_0$$

Where c_0 is the speed of light in a vacuum and re() is the real part.

The free space wavelength is calculated as:

$$\mathrm{wavelength} = c_0 / \mathrm{re}\left(f_{res}\right)$$

Q is the quality factor, calculated as:

$$Q = \left|f_{res}\right| / 2 \times \mathrm{im}\left(f_{res}\right)$$

RMS Surface Roughness and Conductivity

Selecting the Hammerstad-Jensen model and specifying **Conductor Surface Roughness** options allows the PSI and SIwave solvers to use a more refined conductivity calculation. There are two types of conductor roughness models: Exponential (K_W) and Hammerstad (K_H). When you use one of these models, the user-specified **RMS surface roughness** value affects the calculation of metal conductivity, which changes according to the following equations:

$$K_H = 1 + \frac{2}{\pi}\tan^{-1}\left(1.4\left(\frac{h}{\delta}\right)^2\right)$$

$$K_w = 1 + \exp\left(-\left(\frac{s}{2h}\right)^{1.6}\right)$$

$$\sigma_c = \frac{\sigma}{K^2}$$

Where:

- K can be K_H or K_W, the loss coefficients in the two models.
- *s* and *h* are the surface RMS roughness parameters.

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Sensitivity Analysis

Sensitivity analysis is a way to compute derivatives of output quantities (like S, Y or Z parameters) with respect to a particular input quantity (like the impedance of a capacitor).

If you have a board containing one capacitor C1, and an output quantity S_{12}, then:

S_{12} is a function of C1's impedance: $S_{12} = F(Z_{C1})$

By computing the derivative dF/dZ_{C1}, we can determine how much S_{12} changes when the capacitor impedance changes.

Circuit elements with large derivatives are more important in determining the output response then elements with small derivatives.

Computing Sensitivity Analysis

Using perturbation analysis, start with a nominal impedance for C1, where:

$$S_{12} = F\left(Z_{C1}\right)$$

Now slightly perturb the impedance of C1 and solve again:

$$S_{12} + \Delta S_{12} = F\left(Z_{C1} + \Delta Z_{C1}\right)$$

Estimate the derivative from the difference formula:

$$\frac{dS_{12}}{dZ_{C1}} \cong \frac{\Delta S_{12}}{\Delta Z_{C1}} = \frac{F(Z_{C1}+\Delta Z_{C1}) - F(Z_{C1})}{\Delta Z_{C1}}$$

If the problem needs to be solved for *N* variable elements, the sensitivity of a small number of outputs can be computed automatically with respect to hundreds of variable circuit elements. This can be done with almost no increase in the CPU time required. Just a nominal analysis is needed. The results are not an estimate of the derivatives (like in perturbation analysis) but rather are the exact values.

Terminals and Extraction

All source and sink terminals are extracted either as a group or individually in accordance with the pin groups specified on the components. These pin groups can be overridden by selecting **Merge Sources** and **Merge Sinks** (e.g., you can leave the **Merge Sources** option unselected and use the pin groups to define multiple source groups for extraction on a component. See: Grouping Pins.). If every individual source needs to be extracted, remove all the pin groups for that component and clear the **Merge Sources** option.

When modeling power and ground planes, you can choose from the following different solution options:

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- Ground Pwr/Grnd Nets @ Terminals
- Active Mode

You may not be interested in detailed modeling of power and ground planes but may still want to include their effects on the inductance, capacitance and resistance of the signal traces. TPA then models the induced currents on the power and ground planes as it calculates the inductance, capacitance and resistance of the signal traces.

TPA allows you to treat the plane as being grounded at its terminals. In this case, the planes are suppressed in the resulting equivalent circuit model. For a more detailed analysis, you can treat the planes as "active" conductors. The different modeling options are described in more detail below.

Ground Pwr/Grnd Nets @ Terminals

TPA adds a ground connection to each terminal in the power and ground planes. This is equivalent to assuming that every solderball and bondwire connected to the plane is attached to a high-quality electrical ground. TPA then models the induced currents on the power and ground planes as it calculates the inductance of the signal traces.

Active Mode

The terminals in power and ground planes are exposed in the resulting Spice circuit model rather than just being grounded.

Active Mode generates the most accurate results, because it allows you to control how the plane terminals are actually connected. The drawback is the time it takes to analyze the additional terminals.

Use Active Mode when:

- You require a detailed modeling of non-ideal power and ground planes effects, such as ground bounce or simultaneous switching noise.
- You want to carefully model the current return paths for signal nets.

S-Parameter Technical Notes

This section contains the following topics:

S-parameters

Y-parameters

Z-parameters

Relationship between Y and Z Matrices

State-Space Method

Causality Checking

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Passivity Checking

S-Parameters

The S-Parameters (or scattering parameters) are a description of an N-port circuit based upon concepts of input (or incident) power and output (transmitted or reflected, collectively "scattered") power.

The S-parameter description makes use of a reference impedance, $Z_{0,n}$, for every port. This can be any positive number; often a value of 50 Ohms is used.

The normalized incident wave variable, A_n at a port is defined as:

$$A_n = \left(\frac{1}{2}\right)\left(\frac{1}{(\sqrt{Z_{0n}})}\right)(V_n + Z_{0n} \times I_n)$$

The normalized reflected wave variable, B_n, is defined as:

$$B_n = \left(\frac{1}{2}\right)\left(\frac{1}{(\sqrt{Z_{0n}})}\right)(V_n - Z_{0n} \times I_n)$$

The complex magnitude of A_n is denoted by $|A_n|$.

$|A_n|^2$ is interpreted as the incident power on the port, and $|B_n|^2$ is the reflected power. The total power on the port is $|A_n|^2 - |B_n|^2$.

The scattering matrix, S, relates these quantities:

$$\begin{bmatrix} B_1 \\ B_2 \\ B_3 \end{bmatrix} = S \begin{bmatrix} A_1 \\ A_2 \\ A_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ A_3 \end{bmatrix}$$

The entries S_{ij} of the scattering matrix are the individual scattering parameters. An S-parameter value of $S_{ij} = 0$ means no power is transmitted from port i to port j. A magnitude of 1 means that all available power is transmitted from port i to port j.

For example, S_{31} is used to compute the amount of power from the port 1 excitation that is transmitted to port 3. The phase of S_{31} specifies the phase shift that occurs from port 1 to port 3.

The S-parameters associated with a structure are a function of frequency. Therefore, separate solutions and S-matrices are generated for each frequency point of interest.

All voltage and current sources are ignored when the S-, Y-, and Z- parameters are computed.

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Y-parameters

It is usually possible to choose the port voltages, V_1, V_2, ... independently (Imagine connecting an independent voltage source across each port). A given set of port voltages determines the resulting port currents, I_1, I_2, ...

The relationship between port currents and port voltages is the admittance matrix Y:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = Y \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

The entries Y_{ij} of the admittance matrix are often called the Y-parameters.

Z-parameters

It is also possible to specify the port currents independently by attaching an independent current source across each port. This set of currents determines the resulting port voltages.

The relationship between port voltages and the port currents is the impedance matrix Z:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = Z \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}$$

The entries Z_{ij} of the impedance matrix are called Z-parameters.

Relationship between Y and Z matrices

The two matrices are not independent. In fact, $Y = Z^{-1}$.

Z-parameters are often used to evaluate the quality of a power distribution system. Generally, a low impedance is desirable because it indicates that the voltage will fluctuate little in response to a large current.

State-Space Method

S-parameters describe a system in terms of its frequency-dependent responses. The state-space model assumes a linear time-invariant (LTI) system with a vector of inputs **u(*t*)** of length *P* and a vector of outputs **y(*t*)** of length *Q:*

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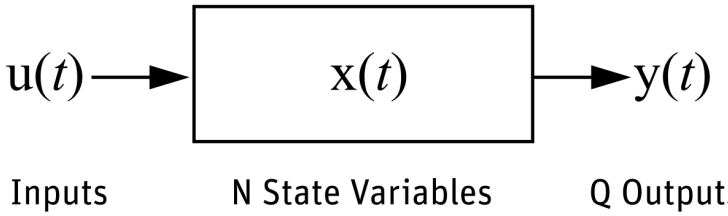
Model of Linear Time-Invariant System



The state-space model represents the data as a vector of N state variables **x(*t*)** representing the responses of the system for all inputs in the specified range, and four state-space matrices, **A**, **B**, **C**, and **D**.

State and Output Equations

Transfer Function

Impulse Response

Tsuk-White Algorithm (TWA) Fitting Method

State-Space Method: State Equations and Output Equations

The vector of state equations:

$$\mathbf{x}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t)$$

Where:

$$\mathbf{x} = \frac{\mathrm{d}}{\mathrm{d}t}\mathbf{x}(t)$$

This gives the rate of change of the state variables (responses), computed as a weighted sum of the current state vector and the input vector. Matrix **A**, the state matrix, contains the frequency-dependent poles of the system. Matrix **A** has dimension N by N. Matrix **B**, the input matrix, contains the weights applied to the input vector. Matrix **B** has dimension P by N.

From the time derivatives of the state variables ***x**(t)* one may calculate the values of ***x***$(t + \Delta t)$ using the vector of output equations:

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t)$$

The output vector is a weighted sum of the current state vector and the input vector. Matrix **C**, the output matrix, contains the weights applied to the state vector. Matrix **C** has dimension Q by N. Matrix **D**, the feedforward matrix, contains weights applied to the input vector. Matrix **D** has dimensions Q by P.

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State-Space Method: Transfer Function

The transfer function is the ratio of the output to the input. In Laplace space *s*, the transfer function can be expressed in terms of the state-space matrices:

$$H(s) = C(sI - A)^{-1}B + D$$

Where *sI* is an N by N matrix with *s* on the diagonal and zeros elsewhere.

H(s) is a matrix of frequency-dependent transfer functions with dimension Q by P, one output for every input.

State-Space Method: Impulse Response and Stability

The impulse response *h(t)* is the response of the system to the delta function, a pulse of vanishingly narrow width. The impulse response is the inverse Lagrangian of the transfer function, and can be expressed in terms of the poles of the system $\mathbf{p}_i$ (the entries of matrix **A**).

$$h(t) = \sum_{t>0} e^{p_i t} u(t)$$

Bounded-In, Bounded-Out (BIBO) stability specifies that as long as the input is bounded, the output must be bounded. For BIBO stability, the exponential factor e^{pt} must decay rather than increase. Thus, all the poles $\mathbf{p}_i$ must have negative real parts. For BIBO stability, the norm of the impulse response must always be finite:

$$||h(t)|| < \infty \quad \forall\, t$$

Tsuk-White Algorithm (TWA) Fitting Method

By default, SIwave uses a proprietary fitting method, the Tsuk-White Algorithm (TWA) for calculating the state-space matrices. The TWA algorithm for state-space fitting is an alternative to rational fitting. TWA generates the poles of the state-space fit from the singular value decomposition of Loewner matrices derived from the input data. Unlike rational fitting, TWA is not an iterative procedure and can produce high-quality state-space fits in much less time than rational fitting. The TWA algorithm may succeed where rational fitting produces a bad fit or a fit that is good but nonpassive on a problem too big for passivity enforcement.

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Note:

TWA cannot simultaneously enforce the exact DC point and enforce causality. When running SIwave in non-graphical batchmode, `ComputeExactDcPt` cannot be combined with `SIwaveSyzEnforceCausality`.

Causality Checking and Enforcement

A causal system is one that is non-anticipatory, that is, its impulse response $h(t)=0$ for all time $t<0$. With *primitive* causality, the response of a linear time-invariant system must never precede its excitation. SIwave can check and compensate for primitive causality problems. With *relativistic* causality, the S-parameter data must never imply a response that exceeds the speed of light in the medium. SIwave cannot determine the length of the device from its scattering parameters, and so cannot detect violations of relativistic causality.

SIwave can verify that the frequency response of data from a Touchstone file satisfies primitive causality. For a frequency-dependent complex transfer function to be causal, its real and imaginary parts must form Hilbert pairs (the Kramers-Kroning relation). Because of this relation, the imaginary part of the frequency response in a linear causal system can be obtained by the Hilbert transform of the real part. Thus, knowledge of the real part of the transfer function over all frequencies is sufficient to completely reconstruct the imaginary part and specify the system (the reverse is also true). Thus, a possible check for system causality is to compare the imaginary part of the frequency response with the Hilbert transform of the real part.

The causality checker does a frequency-by-frequency calculation of a causal reconstruction error based on numerical generalized Hilbert transform and compares that against a pre-calculated frequency-dependent threshold. If the causal reconstruction error exceeds the threshold at any frequency in the available range then the causality checker reports a causality violation and the relative worst error in percent. The causality check is performed for every port and at every frequency.

Two technical issues:

- Designers typically deal with sampled band-limited frequency responses. Triverio and Grivet –Talocia have proposed a technique for checking causality and self-consistency of band-limited sampled frequency responses based on the numerical implementation of the generalized Hilbert transform. They also propose to use a generalized version of the Hilbert transform instead of the standard Hilbert consistency test or Kramer-Kronig dispersion relation. Significantly, the Kramer-Kronig dispersion relation holds for the generalized Hilbert transform method.
- The basic causality check algorithm simply compares the frequency dependent error obtained from causal reconstruction against the truncation error used as a frequency-dependent threshold. In practice, the checker must also include error contributions from the numerical integration routines.

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Passivity Checking and Enforcement

A passive system does not contain any energy sources. Frequency-dependent data may nevertheless exhibit non-passive behavior. SIwave offers four methods for passivity checking and enforcement: an iterated fitting method, an iterated fitting method for better Z-fit at DC and low frequencies, a convex programming method, and a perturbation method.

- Convex Programming Method
- Perturbation Method
- Iterated Fitting of Passivity Violations (IFPV) Algorithm
- Iterated Fitting of Passivity Violations Low Frequency (IFPVLF) Algorithm

Passivity Checking: Convex Programming Method

By the Bounded Real Lemma, the state-space system ABCD is passive if a positive definite matrix **K**>0 exists such that:

$$\begin{bmatrix} -KA - A^T K & -KB & -C^T \\ -B^T K & I & -D^T \\ -C & -D & I \end{bmatrix} > 0$$

The convex programming method preserves the poles from the original state formulation (state matrix **A**). The formulation is such that the estimate of matrix **B** is not needed. For a fixed matrix **A**, the method recomputes matrices **C** and **D** to minimize errors while observing the Bounded Real Lemma.

The convex method of passivity enforcement is guaranteed to produce a passive state-space realization, but is very slow and memory-intensive. Convex optimization requires computing the Hessian or second derivative matrix, with dimension $(P+Q)^2$ by $(P+Q)^2$, where P+Q is the total number of input and output ports. The total memory requirement for the matrices is $(P+Q)^4$. The compute time to solve the matrices is $(P+Q)^6$. In practice, the exponential growth of the solution size limits the convex programming method to systems with the total number of ports (P+Q) less than or equal to 10.

Passivity Checking: Perturbation Method

With this method, passivity enforcement of scattering parameter data with larger numbers of ports is achieved by the perturbation of the singular values of the transfer function matrix.

The frequency-domain transfer function matrix **H**(jω):

$$H(j\omega) = C(j\omega I - A)^{-1} B + D$$

This is obtained from the transfer matrix fit to the S-parameter data *S(jω)*.

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The singular values of the transfer matrix σ [**H**(jω)] are the square roots of the eigenvalues of [$\mathbf{H}^H$(jω)**H**(jω], where $\mathbf{H}^H$(jω) denotes the complex conjugate transpose of **H**(jω).

For passivity, the singular values of the transfer matrix must be less than or equal to 1 for all frequencies.

$$\max\left(\sigma_i\left[H\left(j\omega\right)\right]\right) \leq 1 \quad \forall\omega$$

The perturbation method is derived from the eigenvalue (modal) perturbation of [$\mathbf{H}^H$(jω)**H**(jω)], equivalent to the perturbation of the singular values of **H**(jω). Higher order terms are ignored. As a first step, the **D** matrix is passified to guarantee asymptotic passivity. Next, linear perturbation is applied iteratively to the **C** matrix, minimizing the norm of the perturbation and the transfer matrix deviation at each iteration.

Generally, a nonpassive singular value exceeds the threshold only over a range of frequencies. The method uses the slope of the curve at the points where the singular value crosses the threshold to determine the direction of the perturbation to be applied.

The perturbation method generates matrices of approximate size *k* * N* (P+Q), where N is the number of states and *k* is the number of singular values that are greater than 1. Thus, this method is applicable to systems with large numbers of ports.

Passivity Checking: Iterated Fitting of Passivity Violations (IFPV)

Iterated Fitting of Passivity Violations (IFPV) is the default passivity enforcement algorithm provided by SIwave. IFPV requires relatively little memory to run, and runs significantly faster than either convex optimization or passivity by perturbation. However, IFPV does not guarantee goodness-of-fit as does the convex optimization method. The IFPV algorithm works by taking the results of the original state-space fit, selecting those areas that have passivity violations, and fitting just the excess values, with the original poles. The fitted residues are then subtracted from the original state-space fit. This step is iterated, balancing between goodness of fit and passivity, until a passive model is achieved.

Passivity Checking: Iterated Fitting of Passivity Violations Low Frequency (IFPVLF)

Iterated Fitting of Passivity Violations Low Frequency (IFPVLF) is the latest passivity enforcement algorithm. It builds upon the default passivity enforcement algorithm (Iterated Fitting of Passivity Violation) by providing a better fit to “Z” at DC and low frequencies.

In a dynamic link simulation, Circuit receives the calculated Scattering Parameter data (S-data) from the field solver. Circuit performs state-space fitting, which generates a macromodel that represents the input/output behavior of the structure modeled within the field solver, and performs time or frequency domain simulations. In many applications such as power delivery networks, Circuit must fit the S-data while also preserving its fit of the corresponding Z-data. This fitting process is called “Z-fitting”.

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Often, the generated macromodel is not passive. When passivity enforcement is invoked using the default Iterated Fitting of Passivity Violation (IFPV) method, there is no guarantee that the Z-fit to DC and low frequencies are preserved. Preserving the fit to Z-data at DC and low-frequency can be very important (e.g., due to inaccuracies of the fit to Z-data at DC and low frequencies, a DC-DC buck converter may not converge to a correct steady state voltage regulated value. To remedy this issue, Circuit offers a DC/low frequency Z-fitting passivity enforcement called Iterated Fitting of Passivity Violation at Low Frequency. IFPVLF enforces passivity while providing a better fit to Z-data at DC and low frequencies. Use IFPVLF for passivity enforcement when a better Z-fit at DC and low frequencies are appropriate).

Using Environment Variables with SIwave

The following table lists some commonly used environment variables.

Note:

- Configuration file settings take precedence over environment variables.

Environment Variable	Usage
ALINKS_CLUSTER_VIA	If you do not want to cluster vias, set the variable value to **No**. This setting only applies to via clusters found in IC geometries.
ALINKS_UNCONNECTED_PINS	Set the variable value to **No** if you do not want unconnected pins written to the ANF.
ANSOFT_DEBUG_MODE	Sets debugging level. Levels higher than 2 produce very large log files.
ANSOFT_DEBUG_LOG	Specify the log file directory and name. By default, this is the *.slog file in the SIwave working directory.
SIWAVE_BUFFER_LIB_DIR	Allows you to change the directory from which IBIS driver/receiver buffer models are loaded. This variable needs to point to the directory containing the "buflib" sub-dir. For example, if your buffer models are located at E:\SIwave\TXRX\buflib\IBIS\, set: SIWAVE_BUFFER_LIB_DIR=E:/SIwave/TXRX

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Environment Variable	Usage
SIWAVE_COMPLIB_DIR	Allows you to change the directory from which S-parameter models for capacitors and inductors are loaded. This variable should point to the directory containing the "complib" folder. For example, if your capacitors are located at E:\ansys\complib\Locked, set: SIWAVE_COMPLIB_DIR=E:/ansys.
SIWAVE_ENABLE_LEGACY_TPA	Set to variable value to **1** to expose legacy TPA functionality. Set to **0** to hide this functionality. TPA is no longer supported and has been replaced by CPA.
SIWAVE_INSTALL_DIR	Unix operating systems (Linux) must have this environment variable set for dynamic links and third-party layout imports to work correctly. Set the variable value to the directory where the Ansys EM Suite is installed. Example: /opt/ansys_inc/v251/AnsysEM
SIWAVE_MATERIAL_FILE	Points to the global .amat file; the contents of this file will be loaded in addition to any Designer/HFSS/Q3D material libraries.
SIWAVE_PROJECT_DIR	Set the variable value to the location where the project is saved after importing an ANF file. The PartMap.dat (RLC Part Values File) file can also be read from this location.
SIWAVE_REMOTE_SOLVE_DIR	When running remote solves, this environment variable allows you to specify the location (working directory) for intermediate simulation data files.
SIWAVE_SKIP_STACKUP_CHECK	Set the variable value to **1** to skip dielectric material validation, and allow SIwave to solve problems

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Environment Variable	Usage
	containing materials with large relative permittivity values (e.g., Er=1000).
SIWAVE_SUPRESS_GRAPHICS	Solve in non-GUI mode.
TEMP	Set the location of the temporary working directory.

Window Functions and Time Domain Plotting

SIwave allows for time-domain plotting of S-parameters. Often, this feature is used to calculate a step response or time-domain reflectometry (TDR) plot of the structure being simulated. Fourier analysis provides the mathematical mechanism for transforming frequency sweep data to a time-domain plot, but two approximations are involved. First, the transform is between two sets of discrete data points, as opposed to continuous waveforms. Second, the frequency sweep data cannot have infinite bandwidth, but must truncate at some upper limit. This section discusses the implications of these approximations, and provide information for successful time-domain plotting.

> **Note:**
>
> Frequency sweep data consists only of positive frequencies, but the negative frequencies are simply the complex conjugate of the positive: $S(-f) = S^*(f)$

This is true for any frequency-domain function when the corresponding time-domain waveform is real-valued.

Transforming Frequency To Time Domain

It is easier to make generalizations about the effect of finite bandwidth if we have continuous functions. Consequently, we will initially assume our frequency- and time- domain data is continuous, and defer discussion of the effects of discretization until later. With a continuous-time sweep over an infinite bandwidth, we could in principle calculate a time-domain response by multiplying our sweep data $S(f)$ with the spectrum of a time-domain excitation function and evaluating the inverse Fourier integral:

$$f(t) = \int_{-\infty}^{\infty} S(f) E(f) e^{2\pi j f t} df$$

In practice, however, sweep data does not extend to infinite frequencies and is restricted to a bandwidth b. If we simply assume that the spectrum is zero-valued outside of the bandwidth, we can interpret the data as an infinite sweep that has been multiplied by a rectangular "window" function $W(f)$, with a value of 1 within the bandwidth and a value of 0 otherwise.

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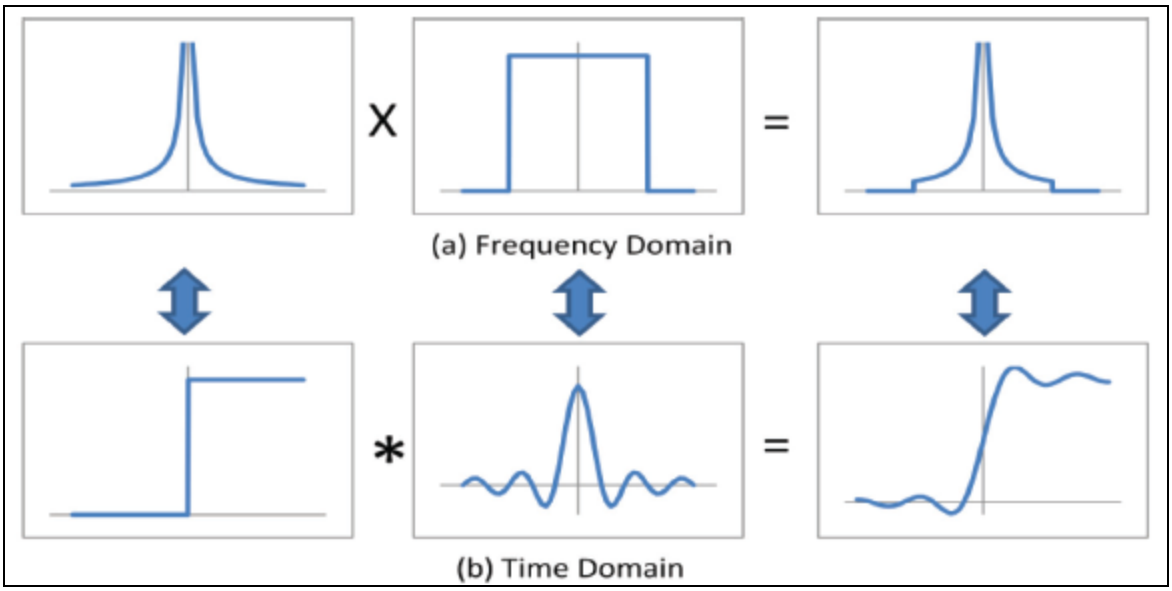
$$f(t) = \int_{-\infty}^{\infty} W(f)S(f)E(f)e^{2\pi jft}df = \int_{-b}^{b} S(f)E(f)e^{2\pi jft}df$$

This process is illustrated in the figure below, assuming that $S(f)$ $E(f)$ corresponds to an ideal unit step function in the time domain.The frequency spectrum (a) is truncated beyond a certain upper limit. Since multiplication in the frequency domain corresponds to convolution in the time domain, this has the effect of convolving the time-domain step with a sinc function – the inverse Fourier transform of the rectangle (b).

The final result is an edge with a finite rise time and some oscillation:



Multiplying the spectrum of a step function with a rectangular window produces a finite edge in the time domain.

If the sweep is extended to higher frequencies—making the window function wider—the corresponding sinc pulse more closely approaches an impulse, and the time-domain edge becomes sharper. However, the oscillation never disappears for any finite sweep. The figure below shows a step response for increasingly wider bandwidths:

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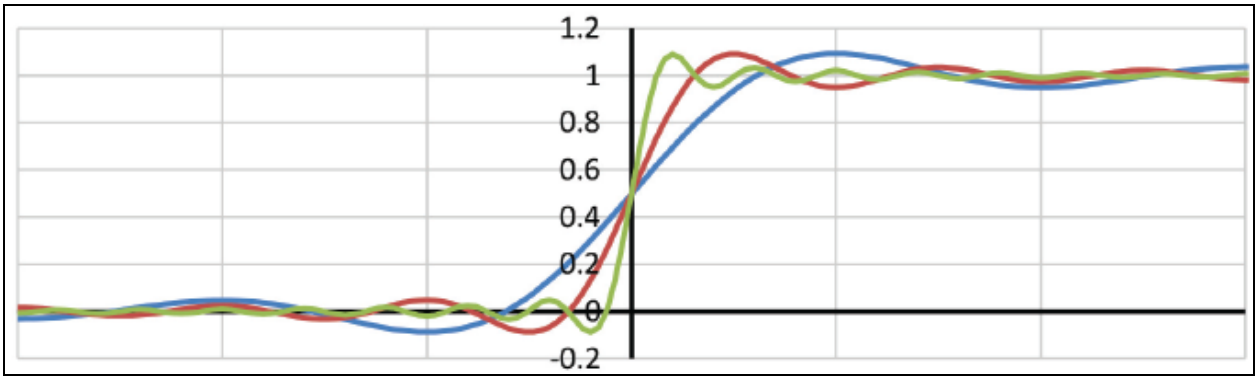

Increasing the width of the rectangular window makes the time-domain edge sharper, but does not eliminate the oscillation

Some distortion of the true time-domain waveform is unavoidable if the frequency sweep does not include the entire bandwidth of the signal, but there are other window functions besides the rectangle which distort the time waveform in ways which may be more desirable. In particular, it would be nice to reduce the spurious oscillation. The next sections will describe the window functions available and discuss their effects.

Window Functions

The window functions available are plotted in the two figures below, and their expressions are given in the Window Function Formulas table. All window functions have a spectral width *w* and are zero-valued for I*f* I > *w*/2. In addition to truncating the data outside of the bandwidth, the non-rectangular windows filter the spectrum inside. The windows differ from each other in how strongly they attenuate the spectrum as the frequency approaches the upper limit. The Kaiser window has a parameter, which controls how sharply it decays. For $\alpha = 0$, the Kaiser window is equivalent to the rectangular window; for $\alpha = 5.4414$, it is equivalent to the Hamming window; and for $\alpha = 8.885$, the Blackman window.

Although the TDR Options window allows for windows that are narrower than the bandwidth of the simulation, it is generally best to set the window width to 100% and take full advantage of the available bandwidth.

Window Functions with a width of *w*=2:

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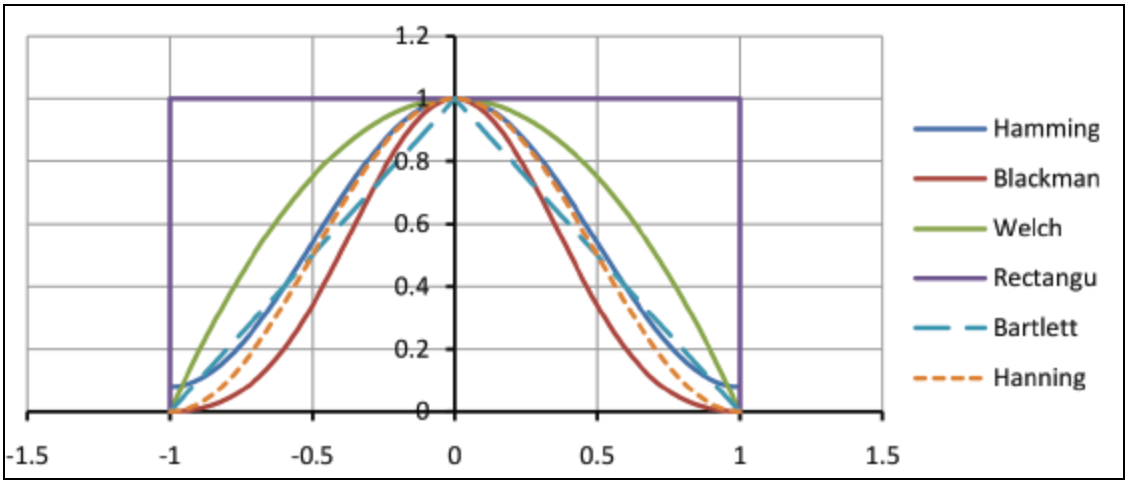
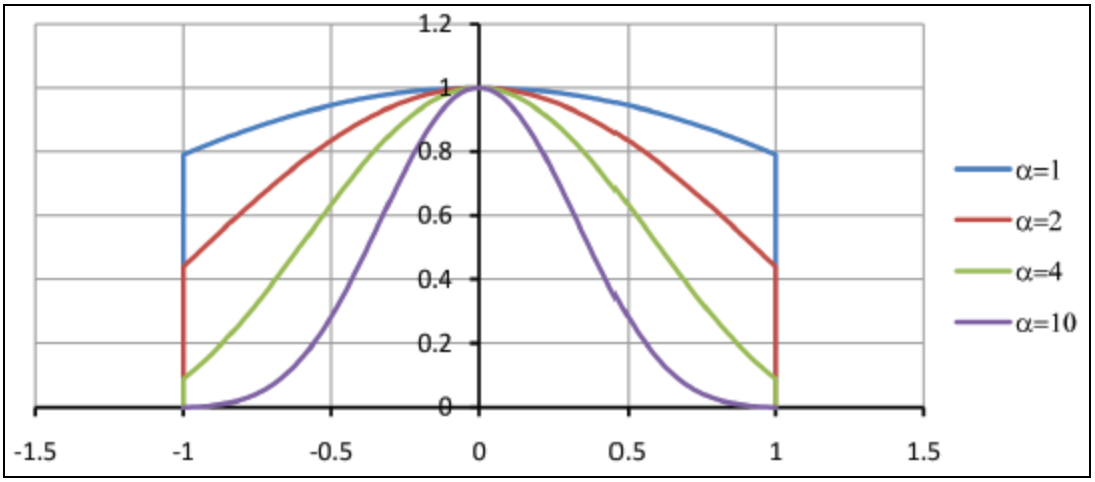


The Kaiser window for a width of *w*=2 and varying values:



Because the spectral width *w* includes both positive and negative frequencies, it is twice the bandwidth of the sweep, *b*, which is equal to the (positive) upper frequency limit.

Ideal Step Response

It is immaterial whether we think of the window as multiplying the frequency sweep data, with the spectrum of the time-domain excitation having infinite bandwidth, or if we instead imagine we have infinite sweep data and a windowed excitation spectrum. With the latter interpretation, we can examine the effects of different windows on an ideal step without concern for what the sweep data looks like.

We will apply different windows to an ideal step function, which is approximated in HFSS and SIwave by choosing an edge and setting the rise time to 0. We continue to assume that we have a continuous spectrum, and will defer a discussion of the effects of discretization until later.

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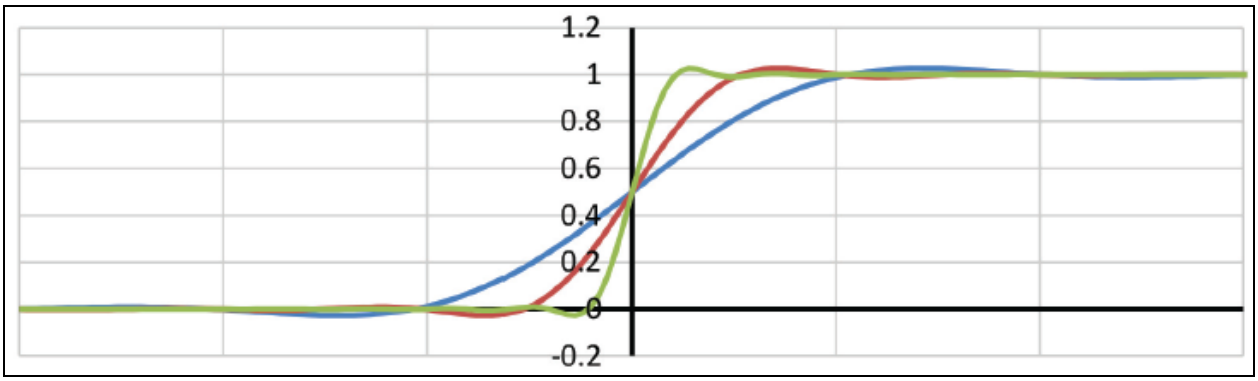
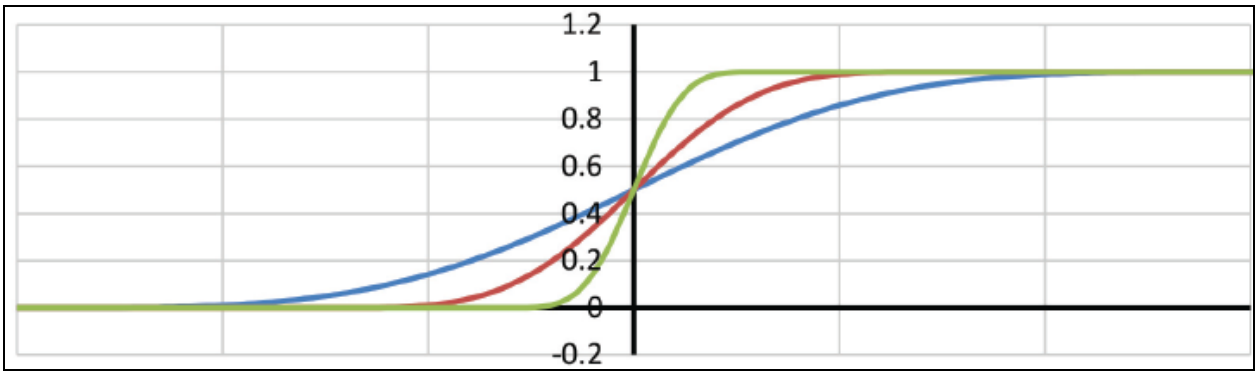
The figure below illustrates the effect of Welch windows of three different widths on an ideal step.



As you can see, the Welch window has substantially decreased the signal oscillation that was seen with the rectangular window.

The Blackman window results in almost no oscillation, as shown in the figure below.



When the effects of the rectangular, Welch, and Blackman windows are plotted together, each with the same bandwidth, it is clear that there is a tradeoff between edge rate and oscillation control. Windows with strong attenuation toward the frequency limits, such as the Blackman, result in minimal oscillation but slower edges. Windows with weak attenuation, such as rectangular, yield more oscillation but faster edges.

The figure below shows step response for three different windows, each with the same bandwidth:

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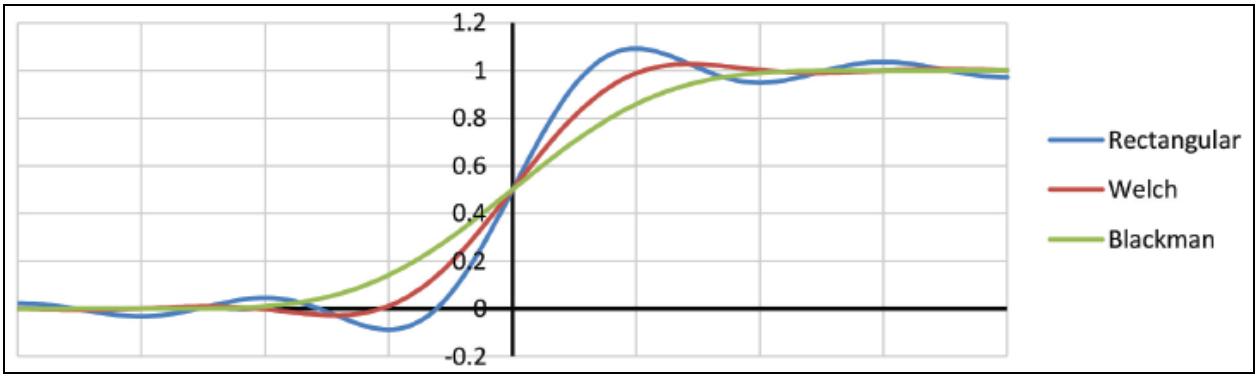
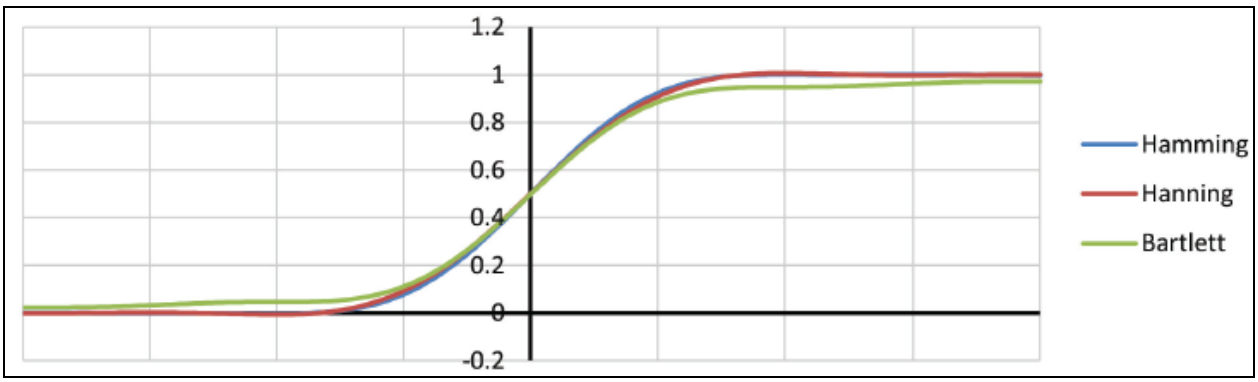


The effects of the Hamming, Hanning, and Bartlett windows are shown below:



As shown, the difference between Hamming and Hanning windows is usually quite small. The Bartlett window is generally not recommended, as it distorts the signal in the vicinity of the edge without providing any advantage over the Hamming and Hanning windows. The Kaiser window gives edges that are slower and less oscillatory with increasing α.

The rectangular, Welch, Hanning, and Blackman windows are sufficient to provide a good sampling of the edge-rate vs. oscillation tradeoff.

The table below quantifies the characteristics of these windows on an ideal step. With the exception of the Blackman window, it is possible to derive reasonably simple expressions for the step response. From the table, *b* is the bandwidth or upper frequency limit of the sweep and Si(χ) refers to the sine integral function:

$$\mathrm{Si}\,(x) = \int_0^{\mathbf{x}} \frac{\sin z}{z}\,dz$$

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Window	Step Response $f_S(t)$	10-90 Edge Rate	Max Overshoot
Rectangular	$\frac{1}{2} + \frac{\mathrm{Si}(2\pi bt)}{\pi}$	$\frac{0.45}{b}$	8.95%
Welch	$\frac{1}{2} + \frac{\cos(2\pi bt)}{2\pi^2 bt} - \frac{\sin(2\pi bt)}{4\pi^3 b^2 t^2} + \frac{\mathrm{Si}(2\pi b}{\pi}$	$\frac{0.70}{b}$	2.70%
Hanning	$\frac{2\pi+2\mathrm{Si}(2\pi bt)-\mathrm{Si}(\pi-2\pi bt)+\mathrm{Si}(\pi+2\pi bt)}{4\pi}$	$\frac{0.97}{b}$	0.64%
Blackman	--	$\frac{1.19}{b}$	0.02%

Note that in the expressions for the step response, the time variable is always multiplied by the bandwidth.

Changing the bandwidth scales the time response, but does not affect the shape of the edge.

Finite Edge Response

Finite edges can be simulated by providing a nonzero value for the rise time. For finite edges, the same edge rate vs. oscillation tradeoff applies. However, the spectrum of a finite edge declines with frequency at a faster rate than an ideal step. As a result, modest amounts of overshoot can be achieved even with a rectangular window. The continuous time finite edge response of a rectangular window is given by:

$$f_e(t) = \frac{1}{2} - \frac{\mathrm{Si}(2\pi b(r-t))}{\pi} + \frac{\cos(2\pi bt)-\cos(2\pi b(r-t))+2\pi bt(\mathrm{Si}(2\pi b(r-t)+\mathrm{Si}(2\pi bt)))}{2\pi^2 br}$$

The value of the edge response at $t = 0$ is given by:

$$f_e(\mathrm{O}) = \frac{1}{2} + \frac{1-\cos(2\pi br)}{2\pi^2 br} - \frac{\mathrm{Si}(2\pi br)}{\pi}$$

Along with the overshoot, f_e (O) is a useful metric for describing how closely the finite edge response approximates the ideal case, for which f_e (O) = O. The degree to which the windowed edge approximates an ideal finite edge depends only on *br*, the dimensionless product of the bandwidth and the rise time, as shown in the following figure:

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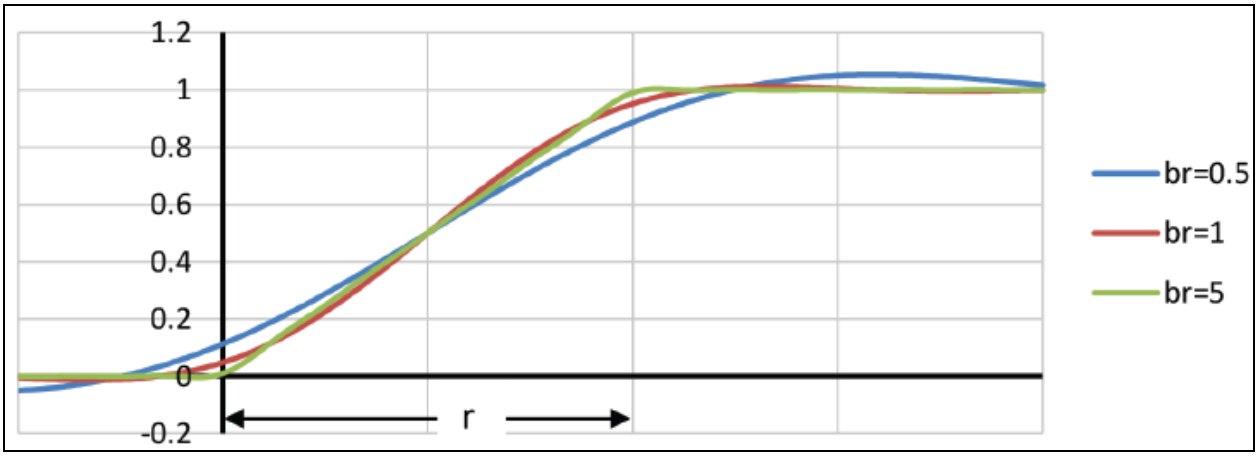

Note that the *y*-intercept and overshoot decline with increasing bandwidth *b*.

The table below quantifies these relationships, describing the finite edge response for rectangular windows over a continuous time.

Bandwidth*Risetime(br)	Edge Response at t = 0	Max Overshoot
0.5	0.113	5.34%
0.75	0.056	2.41%
1	0.049	1.19%
2	0.025	0.72%
3	0.017	0.51%
5	0.010	0.32%
10	0.005	0.17%

As shown, a fairly good finite edge can be achieved with a *br* of 1, but a *br* of around 5 is needed to give a very close approximation to the ideal finite edge.

Impulse Response

The principles behind the step and edge responses also apply to the calculation of impulse responses. Rectangular windows produce the sharpest impulses, but with the greatest amount of oscillation. Hanning and Blackman windows produce impulses that are more spread out, but with less oscillation.

The figure below shows impulse response for selected windows with a spectral width of 1:

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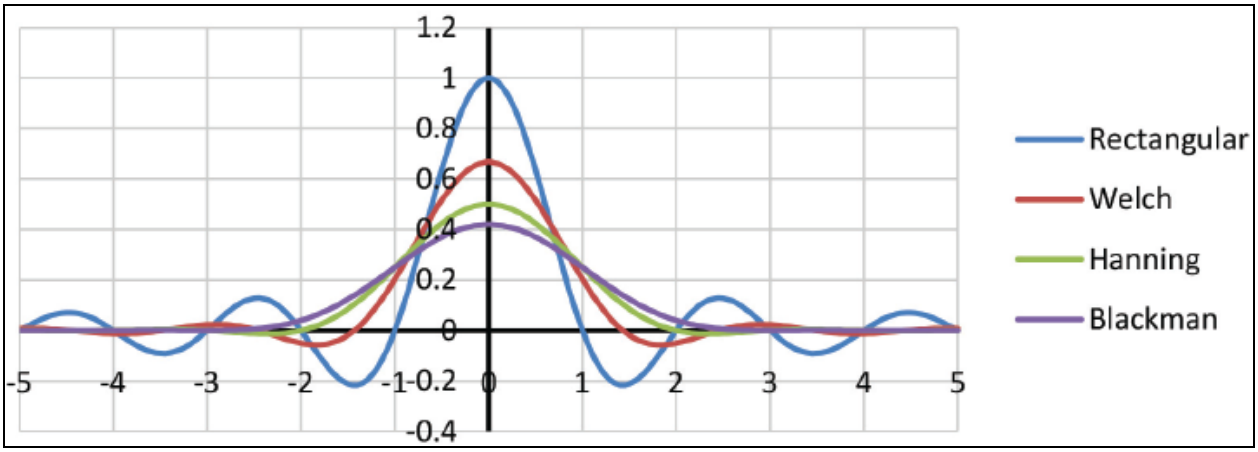

Discrete Time Domain Plotting

The preceding discussion treated frequency spectra as continuous functions, but in practice both the frequency and corresponding time data will be discrete. HFSS uses a discrete Fourier transform (DFT) to approximate a continuous time transform, with the frequency step size and upper limit determining the corresponding quantities in the time domain. The default time step and maximum time are given by:

$$t_{step} = \frac{1}{2f_{max}}$$

$$t_{max} = \frac{1}{2f_{step}}$$

Time resolution is controlled by the upper frequency in the sweep. The maximum time is controlled by the frequency resolution of the sweep. While t_{max} is fixed by the choice of frequency step and cannot be increased after the simulation, t_{step}, or the time delta, can be reduced from the default value within the **TDR Options** window. Decreasing the time delta does not increase the bandwidth of the frequency data, but it does more closely approximate the band-limited continuous time spectra we have so far discussed. Although decreasing the time delta will increase the time required to perform the DFT, the time required is rarely significant. Additionally, a smaller time delta has a significant benefit.

The figure below shows the step response of a matched, lossless transmission line for which the length is controlled by de-embedding the driving waveport, using rectangular window functions. The plots on the left are for a short transmission line length and those on the right correspond to a longer length. Time response using default values (a) shows some oscillation in the response, which is expected for a rectangular window, but the amplitude of the oscillation is different for the two length cases. This is problematic; since the line is matched and lossless, we expect that a length change will only affect the time delay of the response, not affect the shape or quality of the

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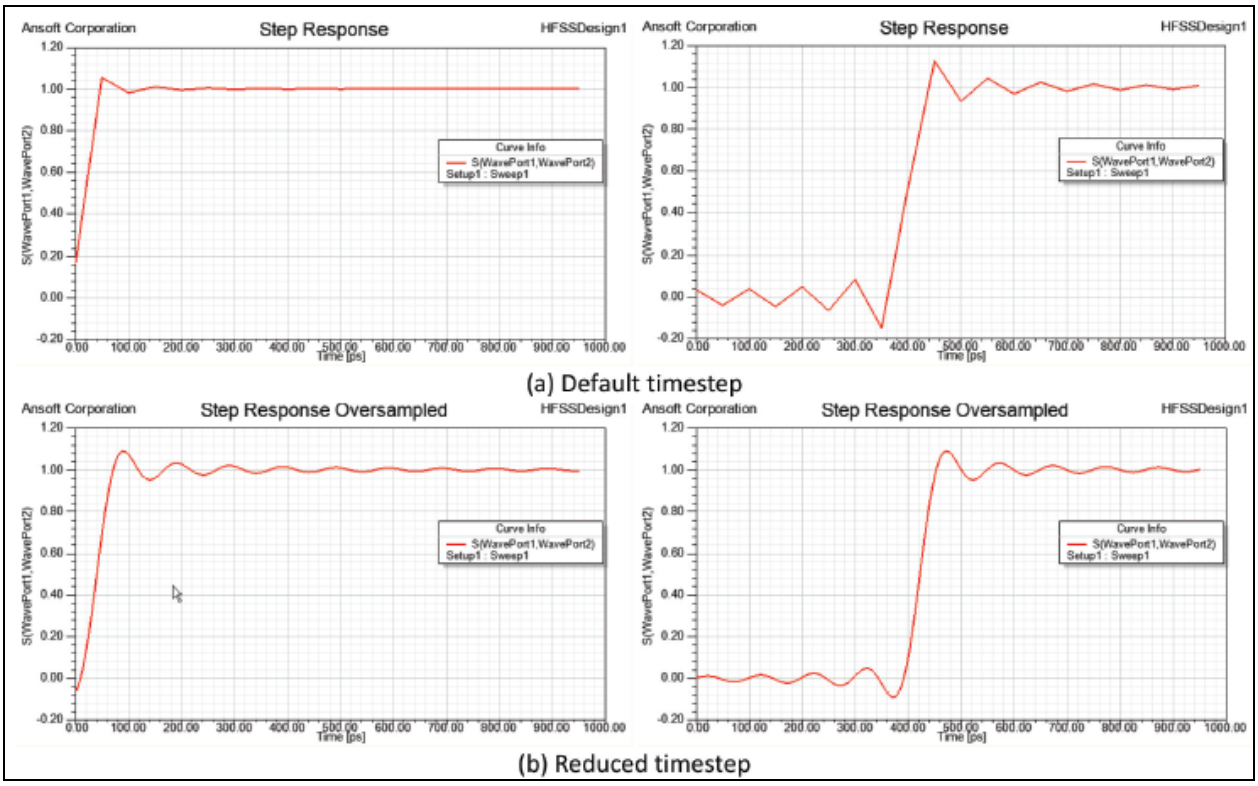
rising edge. The variation in the response is an undesirable artifact of the coarse time sampling. We can increase resolution by increasing the bandwidth of the sweep, but this requires additional simulation. With the time delta reduced using the TDR Options window (b), the same two cases show more intuitive results. The edge shape is the same for both line lengths and the only difference is the location of the edge. Setting the time delta to around 1/5 of the default value is generally sufficient, but finer time steps are needed for precise correlation to the tables.



The frequency step size governs the length of the time range generated. Although a coarse frequency sampling is often sufficient to generate enough time data for a TDR plot, it is important not to set f_{step} too high in the frequency sweep. Discrete frequency spectra necessarily correspond to periodic time-domain functions, so the calculated step is actually more like a repeating series of long pulses. The figure below shows the how the oscillation decays after the rising edge up to a point, but then begins increasing in anticipation of a falling edge.

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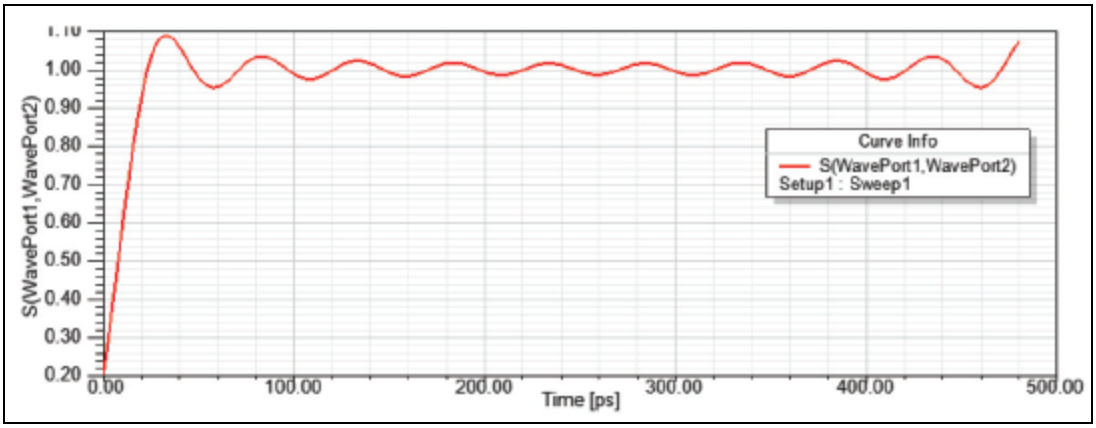

Setting f_{step} to a small value increases the length of the pulse, and minimizes the influence of the future falling edge. Additionally, a smaller f_{step} ensures that resonances and other sharp features in the frequency data are adequately captured. As t_{step} and f_{step} approach zero, the calculated results will converge on the continuous time descriptions given earlier.

Applications

When simulating a TDR plot, we want the fastest edge possible for the bandwidth of our simulation, subject to our preference for oscillation control. Therefore, an edge with a rise time of zero is a good choice. The following figure shows TDR plots of a transmission line with several impedance discontinuities. The results for a rectangular and Hanning window with a 20GHz bandwidth are compared with those for a Hanning window with a 50GHz bandwidth, which will necessarily be more accurate due to the higher bandwidth, and can be used as a reference. In all cases, the time step was set substantially lower than the default.

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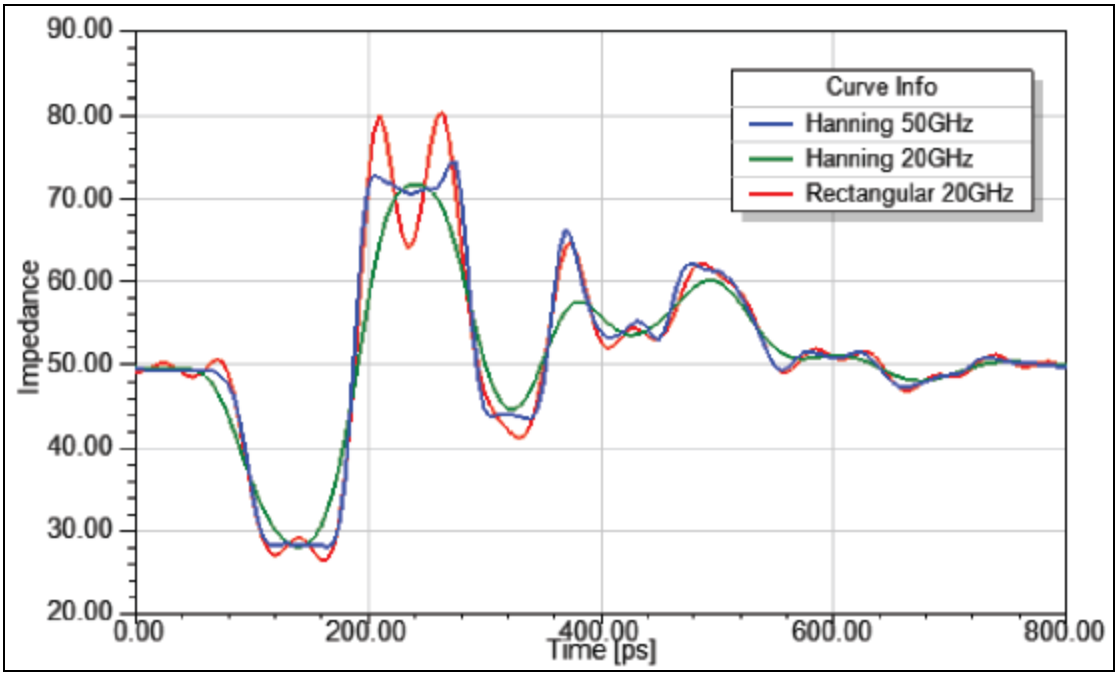

The rectangular window effectively captures the sharp impedance transitions, but also displays spurious oscillation. The 20GHz Hanning window does not suffer any oscillation, but gives less resolution on the sharp edges. These results are consistent with the step response characteristics of the different windows previously shown.

We can also use time-domain plotting to approximate how a structure would behave in a Nexxim Transient simulation. When comparing the results to a Transient simulation that uses a pulse or piecewise linear source, it makes sense to use a finite edge with a rectangular window. The figure below compares HFSS and Nexxim results for the transmission line, using a rise time of 50ps and a rectangular window with a 20GHz bandwidth *(br* = 1).

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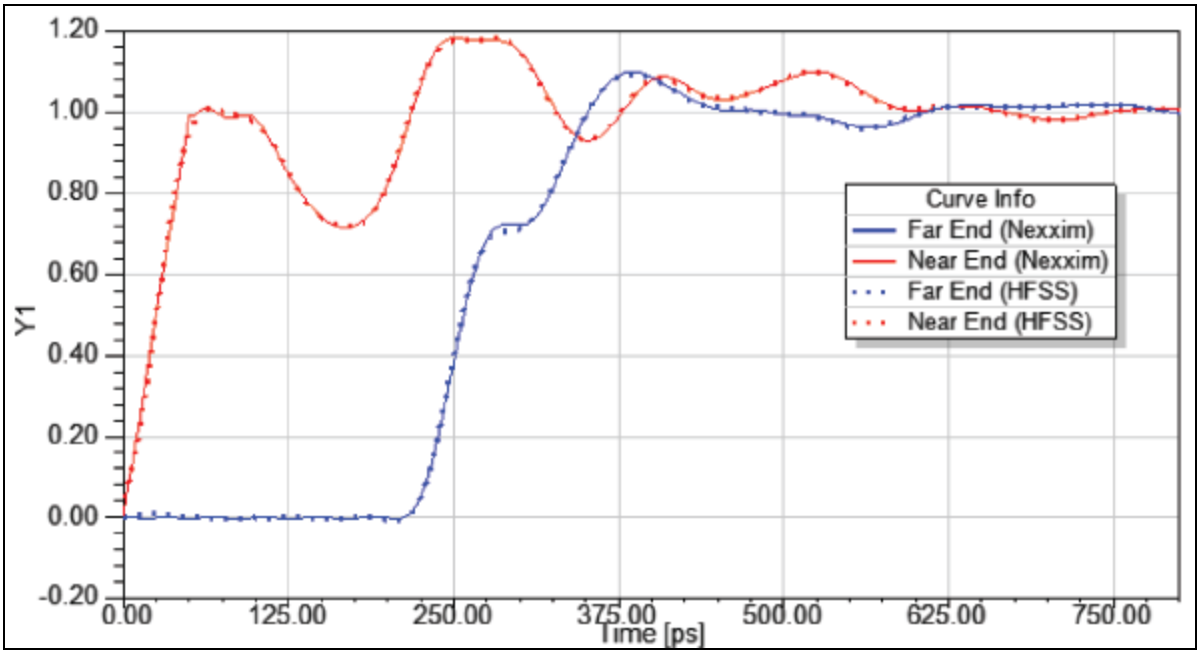

As shown, very good agreement between Nexxim and HFSS is possible when appropriate settings are used for time domain plotting.

Window Function Formulas

For context, see: Window Functions.

Rectangular	$\text{Rect}\left(\frac{f}{w}\right) \text{where } \text{Rect}\left(x\right) = \left\{ \begin{matrix} 1 & -\frac{1}{2} \le x \le \frac{1}{2} \\ 0 & \text{otherwise} \end{matrix} \right\}$
Bartlett	$1 - \left\lvert \frac{2f}{w} \right\rvert$
Blackman	$0.42 + 0.5\cos\left(\frac{2\pi f}{w}\right) + 0.08\cos\left(\frac{4\pi f}{w}\right)$
Hamming	$0.54 + 0.46\cos\left(\frac{2\pi f}{w}\right)$
Hanning	$0.5\left[1 + \cos\left(\frac{2\pi f}{w}\right)\right]$
Kaiser	$\frac{1}{I_0(a)} I_0\left(a\sqrt{1 - 4\left(\frac{f}{w}\right)^2}\right)$

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	where: $I_0\left(x\right)$ is a modified Bessel function of the first kind.
Welch	$1-\left(\frac{2f}{w}\right)^2$

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Glossary

Click a letter to view terms beginning with that letter.

A	B	C	D	E	F	G
H	I	J	K	L	M	N
O	P	Q	R	S	T	U
V	W	X	Y	Z		

A

Antipad – the area of copper etched away around a via or a plated through-hole on a power or negative signal plane that prevents electrical connection to that plane.

B

Backdrilling – the process of removing *stubs*.

Ball Grid Array (BGA) – a packaging technology similar to a *pad grid array*, in which a device's external connections are arranged as an array of conducting pads on the base of the package. However, in the case of a ball grid array, *solderballs* are attached to the conducting pads.

Bondwire – connects an integrated circuit to pads on the package.

C

Capacitance – the ability of an object to store electric charge.

Capacitor – an electronic component used to store charge.

Crosstalk – when PCB traces couple unintentionally, causing signal interference.

Current Sink – a *Current Source* fed from a negative voltage supply.

Current Source – an electronic circuit that delivers or absorbs an electric current which is independent of the voltage across it.

D

Die – An unpackaged integrated circuit.

Dielectric Layer – an insulating layer used to separate two signal layers.

E

Extents – the PCB design's work area. You can place components in this area.

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F

G

H

I

Inductance – the property of a circuit element to oppose a change in current.

Inductor – a passive electronic component that stores energy in the form of a magnetic field.

Integrated Circuit – a device in which components such as resistors, capacitors, diodes, and transistors are formed on the surface of a single piece of semiconductor.

J

K

L

Lead Frame – a metallic frame containing leads and a base to which a die is attached.

M

N

Net – a set of electrically connected *traces* and pins.

N-Port – network parameter data contained in spreadsheet form or by network parameter data contained in an external file. See: *Touchstone*.

O

P

Pad – a small copper surface that allows soldering components to the PCB; can be a through-hole or surface mount.

Pad Grid Array (PGA) – a packaging technology in which a device's external connections are arranged as an array of conducting pads on the base of the package.

Padstack – the stacking structure of shapes associated with pads and vias. Padstacks enable different shapes on different layers.

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Plane – a large copper area connected to the circuit's ground point (typically one terminal of the power supply).

Port – an external access point in the circuit.

Q

R

Resistance – the opposition to current flow.

Resistor – an electrical component that limits or regulates the flow of electrical current in an electronic circuit.

S

Signal Layer – layer carrying traces in a PCB.

Solderball – connects a *BGA* type package to the PCB at a designated reference designator location.

Stitching Via – the process of connecting multiple vias on different layers.

Stub – unused portion of a via that can result in signal disturbances.

T

Touchstone – a standard format for n-port S parameter data. It allows you to import the S-parameters into third-party simulation tools.

Trace – conducting line on a PCB.

U

V

Via – consists of a hole cut in the PCB to route a trace vertically from one layer to another, as well as the vertical pieces of conductor that make connections between layers.

Voltage Probe – specifies the two terminals across which a potential difference is computed; used in frequency sweeps.

Voltage Source – a two-terminal device which can maintain fixed voltage.

W

X

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Y

Z

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