Twin Builder Components: Transformations

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1 - Transformations Library

The components of the Transformations library provide allow quick and simple connection of nodes with different natures or data types. These components are particularly useful for VHDL-AMS simulation models, which oftern require data type conversions and connections between nodes with different natures.

The transformation components are available in the Tools>Transformations folder and are implemented as macros and C-models. The following types of components are available.

- Coordinate Transformations
- Mechanical Transformations
- Nature Transformations
- OmniCasters

Coordinate Transformations

- Clarke Transformation (CLARKE)
- Clarke & Park Transformation (CLARKE_PARK)
- Park Transformation (PARK)

Clarke Transformation

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

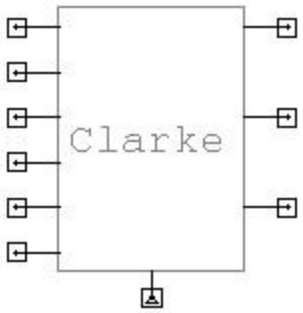

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Conservative Pins

• Parameters

• Input/Output Quantities

• Example

• References

Description

Clarke and Park transforms are used in high performance drive architectures related to permanent magnet synchronous and asynchronous machines.

Through the use of the Clarke transform, the α-component and β-component can be identified. The Park transform can be used to realize the transformation of the α-component and β-component from the stationary to the moving reference frame and control the spatial relationship between the stator current vector and the rotor flux vector.

The Clarke transform uses three phase currents (Ia, Ib, Ic) to calculate currents in the two phases orthogonal stator axis (Iα and Iβ). In many applications, the homopolar component (I0) is absent or less important.

You can transform voltage and current quantities. You can also specify a scaling factor. The pins A2, B2, and C2 can be connected with a node potential, usually the ground. You can also leave the pins open. The current flowing in the first pin is available at the respective second pin.

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Assumptions and Limitations

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Mathematical Description

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \cdot \frac{1}{FACT} \cdot \begin{bmatrix} I_\alpha \\ I_\beta \\ I_0 \end{bmatrix}$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{\sqrt{3}}{3} & -\frac{\sqrt{3}}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \cdot FACT \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

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Netlist Syntax

UMODEL CLARKE ?InstanceName(@InstanceName):(@(Refbase)@(ID)) A1:= %0, A2:= %1, B1:= %2, B2:= %3, C1:= %4, C2:= %5, ALPHA:= %6, BETA:= %7, ZERO:= %8 (FACT:= @FACT) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
A1/A2	Phase A	electrical
B1/B2	Phase B	electrical
C1/C2	Phase C	electrical
ALPHA	α-Component	electrical
BETA	β-Component	electrical
ZERO	Homopolar-Component	electrical

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
FACT	Scale Factor	real	1

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
VA/VB/VC	Line Voltage Phase A/B/C [V]	Output	real
VALPHA	α-Component of Line Voltage [V]	Output	real
VBETA	β-Component of Line Voltage [V]	Output	real
VZERO	Homopolar-Component of Line Voltage [V]	Output	real
IA/IB/IC	Line Current Phase A/B/C [A]	Output	real
IALPHA	α-Component of Line Current [A]	Output	real
IBETA	β-Component of Line Current [A]	Output	real
IZERO	Homopolar-Component of Line Current [A]	Output	real

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Example

See Example Clarke/Park Transformations

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References

Clarke & Park Transformation

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

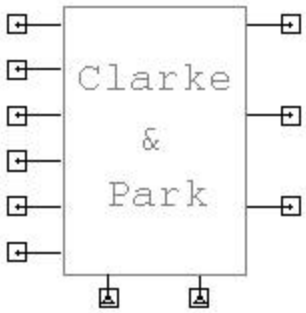

Figure 1. Component symbol

• Description

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• Mathematical Description

• Netlist Syntax

• Conservative Pins

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• Example

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Description

The Clarke-Park transform use three phase currents (Ia, Ib, Ic) to calculate currents in the moving reference frame (ID and IQ) over an angle φ in one step.

You can transform voltage and current quantities. Within the dialog you can specify a scaling factor for the Clarke transform as well as an angle φ and the transform type for the Park transform. The pins A2, B2, and C2 can be connected with a node potential, usually the ground. You can also leave the pins open. The current flowing in the first pin is available at the respective second pin.

See also Clarke Transformation

See also Park Transformation

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

MODEL CLARKE_PARK ?InstanceName(@InstanceName):(@(Refbase)@(ID)) A1:= %0, A2:= %1, B1:= %2, B2:= %3, C1:= %4, C2:= %5, D:= %6, Q:= %7, ZERO2:= %8 (TYPE:= @TYPE, FACT:= @FACT, PHI:= @PHI) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
D	Direct Component	electrical
Q	Quadrature Component	electrical
A1/A2	Phase A	electrical
B1/B2	Phase B	electrical
C1/C2	Phase C	electrical
ZERO2	Homopolar-Component (relating to D-Q)	electrical

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Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
TYPE	Type of Park Transform (Type 0 or 1)	real	0
FACT	Scale Factor	real	1

PHI	Angle	real	0 [rad]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
VA	Line Voltage Phase A [V]	Output	real
VB	Line Voltage Phase B [V]	Output	real
VC	Line Voltage Phase C [V]	Output	real
VALPHA	ALPHA-Component of Line Voltage [V]	Output	real
VBETA	BETA-Component of Line Voltage [V]	Output	real
VZERO	Homopolar-Component of Line Voltage [V]	Output	real
VD	Direct-Component of Line Voltage [V]	Output	real
VQ	Quadrature-Component of Line Voltage [V]	Output	real
IA	Line Current Phase A [A]	Output	real
IB	Line Current Phase B [A]	Output	real
IC	Line Current Phase C [A]	Output	real
IALPHA	ALPHA-Component of Line Current [A]	Output	real
IBETA	BETA-Component of Line Current [A]	Output	real
IZERO	Homopolar-Component of Line Current [A]	Output	real
ID	Direct-Component of Line Current [A]	Output	real
IQ	Quadrature-Component of Line Current [A]	Output	real

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Example

A permanently excited synchronous generator is simulated using the combined Park-Clarke Transformation model. The voltage induction depending on angular speed is modeled in the d-q equivalent circuit. The resistances and inductances of the stator winding and the load are summed up in the RL-combinations at the three-phase side. The schematic of the example is

shown in Figure 2, system parameters are listed in Table 4, and the simulation results are shown in Figure 3, 4, 5, and 6.

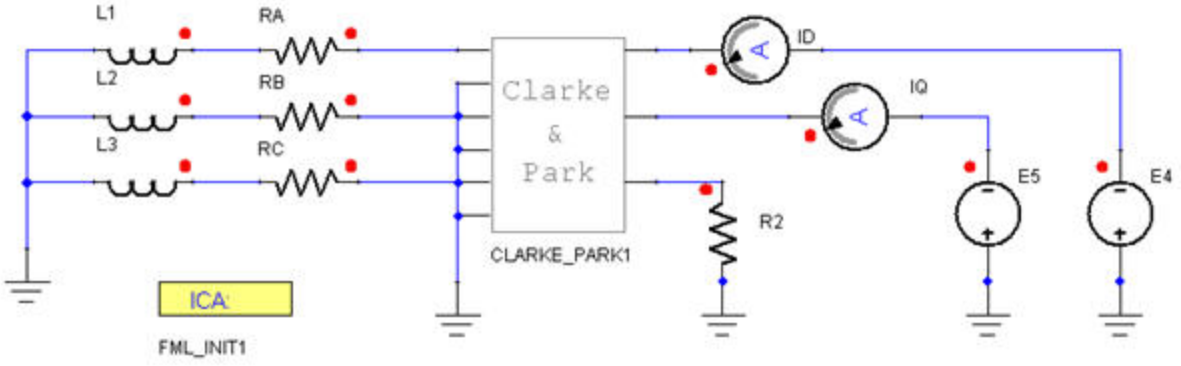

Figure 2. Application example of the Clarke & Park Transformation model

Table 4. System Parameters

Component	Parameter	Value [unit]
Voltage Source E4	EMF Value	(-OMEGA)*LSQ*IQ.I [V]
Voltage Source E5	EMF Value	OMEGA*(LSQ*ID.I-K) [V]
Resistor R2	R	1e12 [Ohm]
Resistor RA/RB/RC	R	R_0 [Ohm]
Inductor L1/L2/L3	L	L [H]
Clarke & Park Transformation CLARKE_PARK1	FACT	1
	TYPE	0
	PHI	OMEGA*Time
Initial Values FML_INIT1	EQU0	PolePairs:=2
	EQU1	N:=1800

	EQU2	OMEGA:=N/60*2*PI*PolePairs
	EQU3	R_0:=1
	EQU4	L:=0.0005
	EQU5	K:=30
	EQU6	LSD:=0.001
	EQU7	LSQ:=0.0001

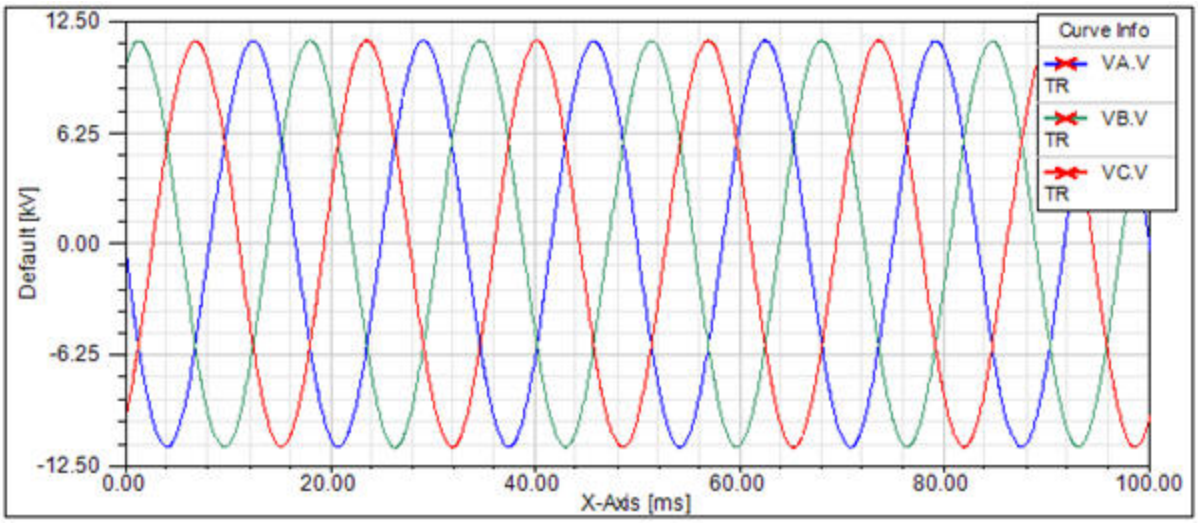

Figure 3. Simulation results-3 Phase line voltage output from CLARKE_PARK1

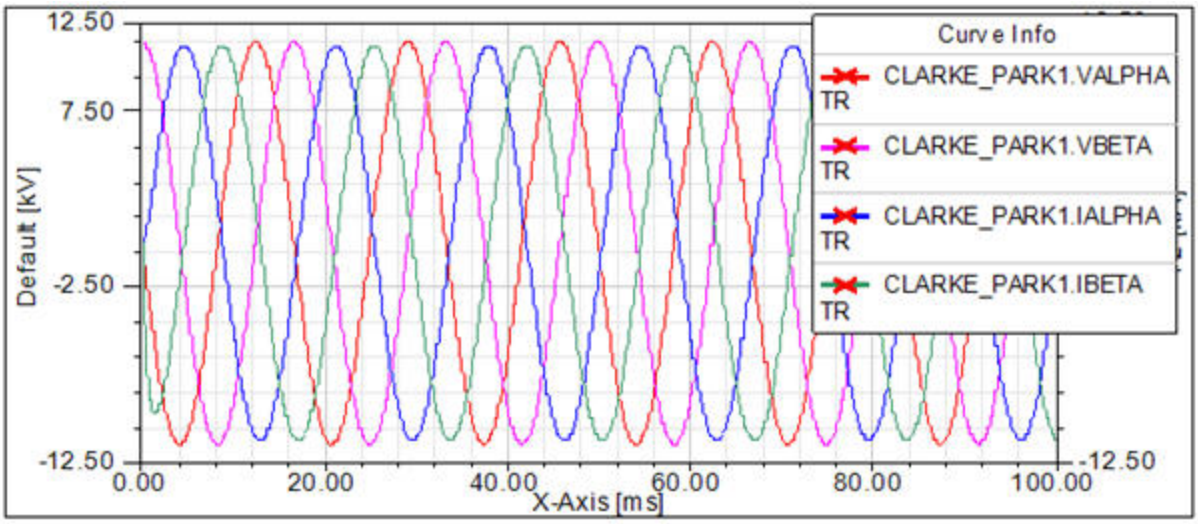

Figure 4. Simulation results-α and β component ouputs of CLARKE_PARK1

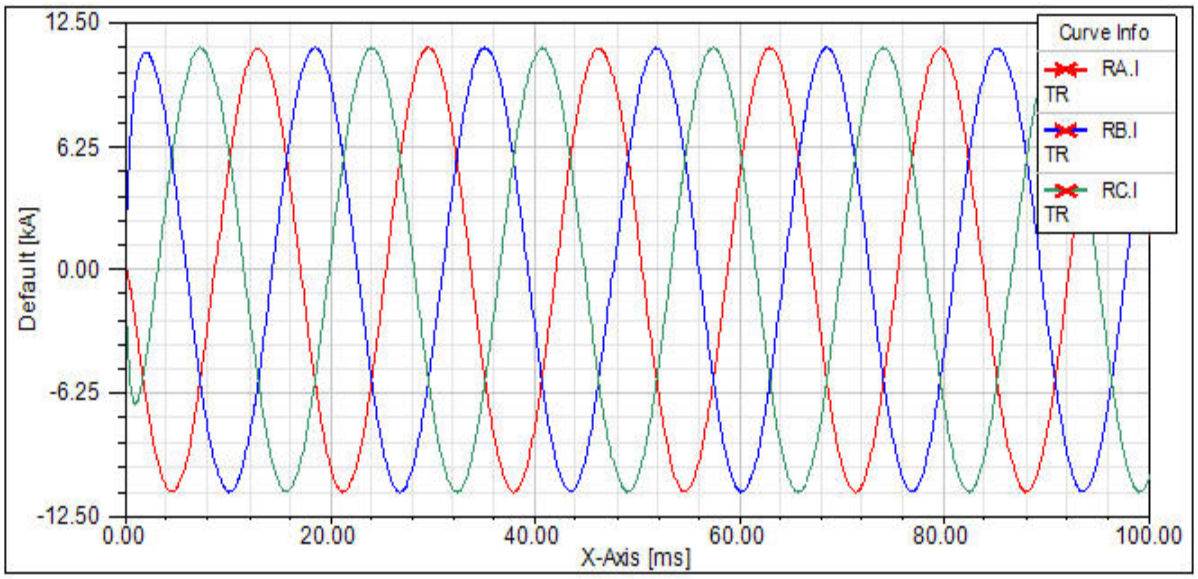

Figure 5. Simulation results-3 Phase current through resistors(RA/RB/RC)

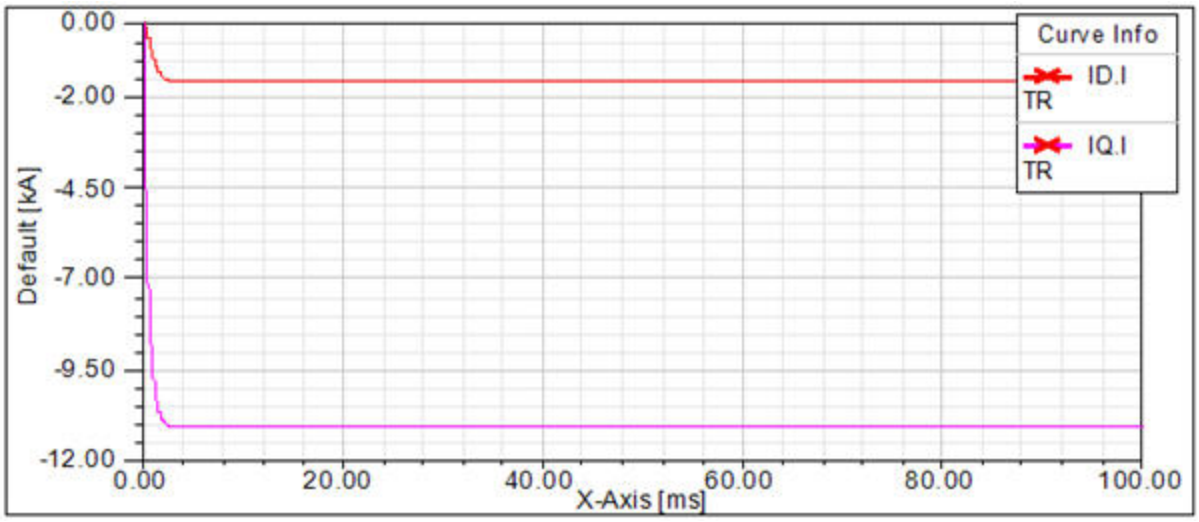

Figure 6. Simulation results-D and Q source currents measured with ammeters (ID and IQ)

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References

Park Transformation

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

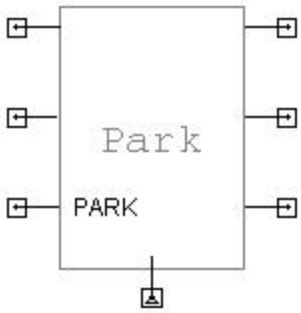

Figure 1. Component symbol

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Description

The Park transform uses currents in the two phases of the orthogonal stator axis (Iα and Iβ) to calculate currents in the moving reference frame (ID and IQ) over an angle φ.

You can transform voltage and current quantities. Within the dialog you can specify an angle φ and the transform type.

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Assumptions and Limitations

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Mathematical Description

Type 0

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_{01} \end{bmatrix} = \begin{bmatrix} cos\varphi & -sin\varphi & 0 \\ sin\varphi & cos\varphi & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_D \\ I_Q \\ I_{02} \end{bmatrix} \qquad \begin{bmatrix} V_D \\ V_Q \\ V_{02} \end{bmatrix} = \begin{bmatrix} cos\varphi & sin\varphi & 0 \\ -sin\varphi & cos\varphi & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \\ V_{01} \end{bmatrix}$$

Type 1

$$\begin{bmatrix} I_\alpha \\ I_\beta \\ I_{01} \end{bmatrix} = \begin{bmatrix} cos\varphi & sin\varphi & 0 \\ sin\varphi & -cos\varphi & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_D \\ I_Q \\ I_{02} \end{bmatrix} \qquad \begin{bmatrix} V_D \\ V_Q \\ V_{02} \end{bmatrix} = \begin{bmatrix} cos\varphi & sin\varphi & 0 \\ sin\varphi & -cos\varphi & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \\ V_{01} \end{bmatrix}$$

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Netlist Syntax

UMODEL PARK ?InstanceName(@InstanceName):(@(Refbase)@(ID)) ALPHA:= %0, BETA:= %1, ZERO1:= %2, D:= %3, Q:= %4, ZERO2:= %5 (TYPE:= @TYPE, PHI:= @PHI) SRC: DB (Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
D	Direct Component	electrical
Q	Quadrature Component	electrical
ALPHA	α-Component	electrical
BETA	β-Component	electrical
ZERO1	Homopolar-Component (relating to α-β)	electrical
ZERO2	Homopolar-Component (relating to D-	electrical

	Q)	

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
TYPE	Type of Park Transform (Type 0 or 1)	real	0
PHI	Angle	real	0 [rad]

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
VALPHA	ALPHA-Component of Line Voltage [V]	Output	real
VBETA	BETA-Component of Line Voltage [V]	Output	real
VZERO1	Homopolar-Component of Line Voltage 1 [V]	Output	real
VZERO2	Homopolar-Component of Line Voltage 2 [V]	Output	real
VD	Direct-Component of Line Voltage [V]	Output	real
VQ	Quadrature-Component of Line Voltage [V]	Output	real
IALPHA	ALPHA-Component of Line Current [A]	Output	real
IBETA	BETA-Component of Line Current [A]	Output	real
IZERO1	Homopolar-Component of Line Current 1[A]	Output	real
IZERO2	Homopolar-Component of Line Current 2[A]	Output	real
ID	Direct-Component of Line Current [A]	Output	real
IQ	Quadrature-Component of Line Current [A]	Output	real

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Example

See Example Clarke/Park Transformations

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References

Example Clarke/Park Transformations

In this example, an induction machine running at constant speed is simulated using the space-vector representation. Two identical equivalent circuits are used for the calculations of the alpha and beta components of the stator currents. An auxillary circuit using the Park transformation model was included in order to display the direct and quadrature components of the stator current. The schematic of the example is shown in Figure 2, system parameters are listed in Table 4, and the simulation results are shown in Figure 3, 4, 5, and 6.

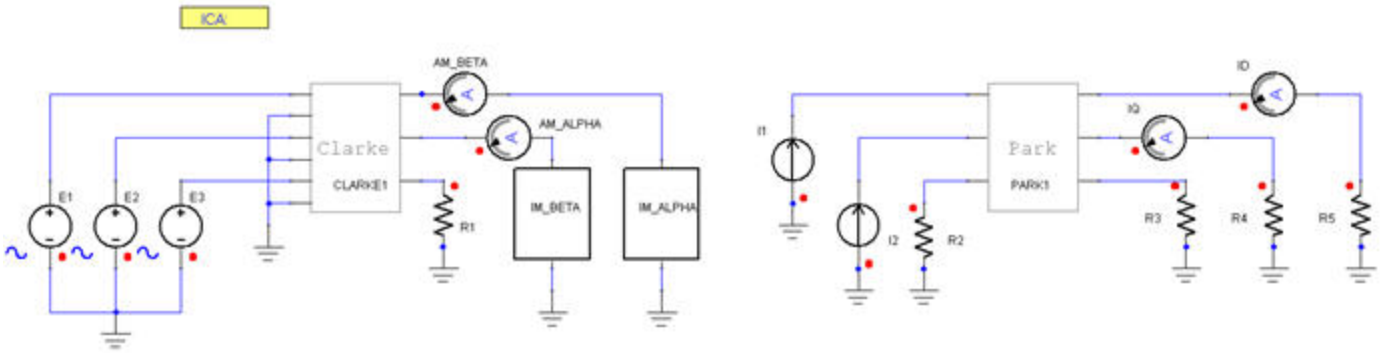

Figure 2. Application example of the Clarke and Park Transformation models

Table 4. System Parameters

Component	Parameter	Value [unit]
Voltage Source E1, E2, E3	AMPL	326 [V]
	FREQ	60 [Hz]
	Type	Sine
	Phase E1/E2/E3	0/120/240 [deg]
Resistor R1/R2/R3	R	1000 [Ohm]
Resistor R4/R5	R	1 [Ohm]
Current Source I1	IS	AM_ALPHA.I
Current Source I2	IS	AM_BETA.I

Induction Machine IM_ BETA	SLIP	SLIP
Induction Machine IM_ ALPHA	SLIP	SLIP
Clarke Transformation CLARKE1	FACT	1
Park Transformation PARK1	PHI	2*PI*60*Time
Initial Values FML_ INIT1	EQU0	PolePairs:=2
	EQU1	NSYNC:=3600/PolePairs
	EQU2	N:=1420
	EQU3	SLIP:=(NSYNC-N)/NSYNC

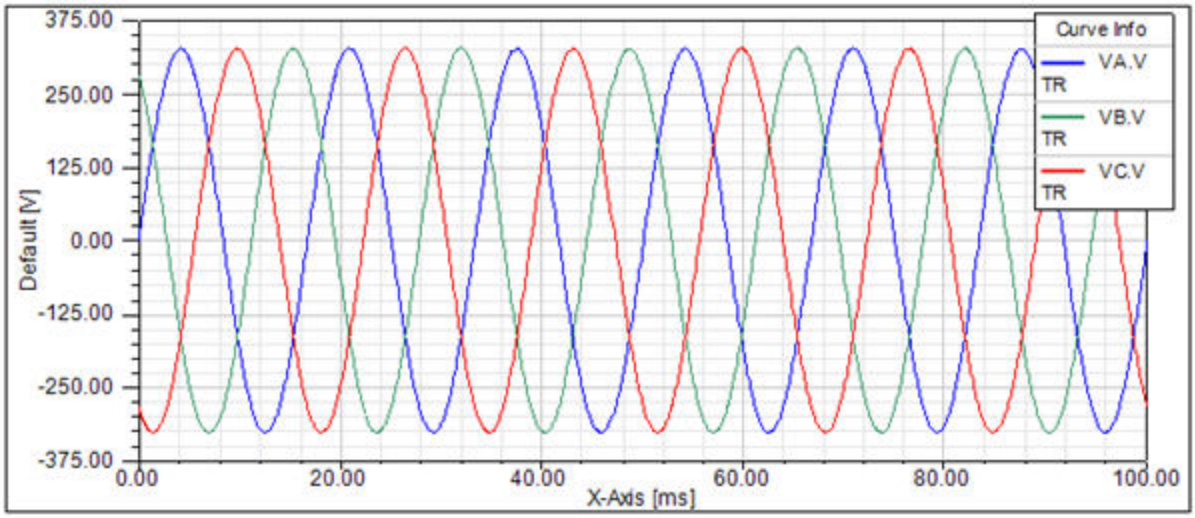

Figure 3. Simulation results-3 Phase line voltage output from CLARKE1

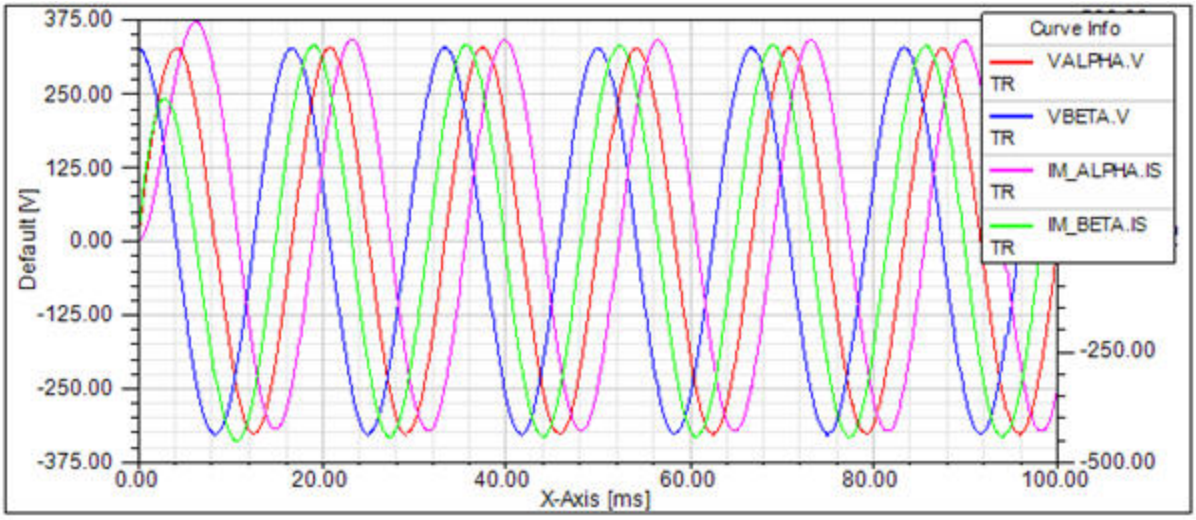

Figure 4. Simulation results-α and β component ouputs of CLARKE1 and Induction Motor Outputs (IM_ALPHA and IM_BETA)

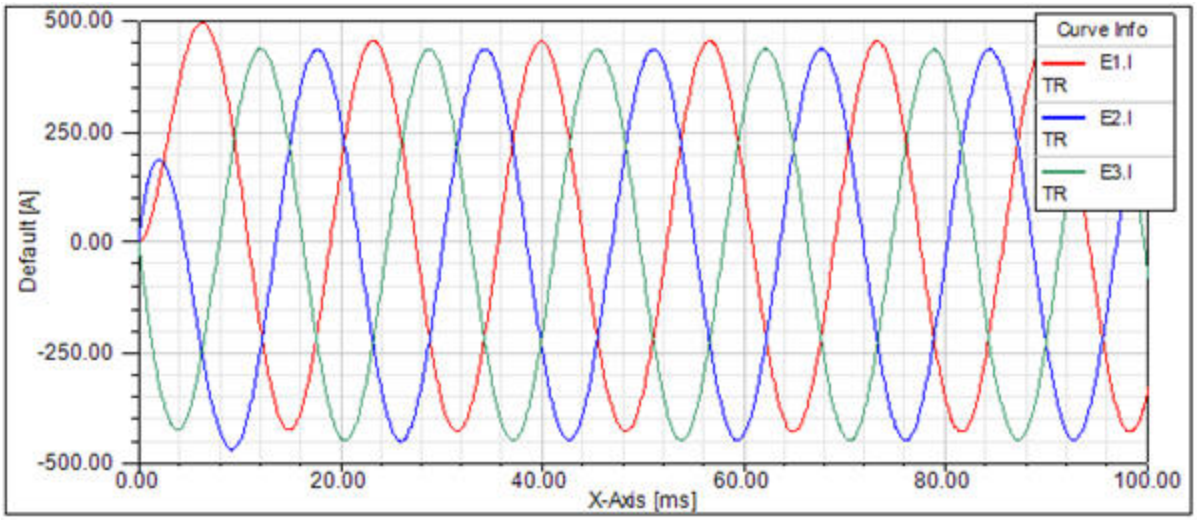

Figure 5. Simulation results-3 Phase source current output (E1/E2/E3)

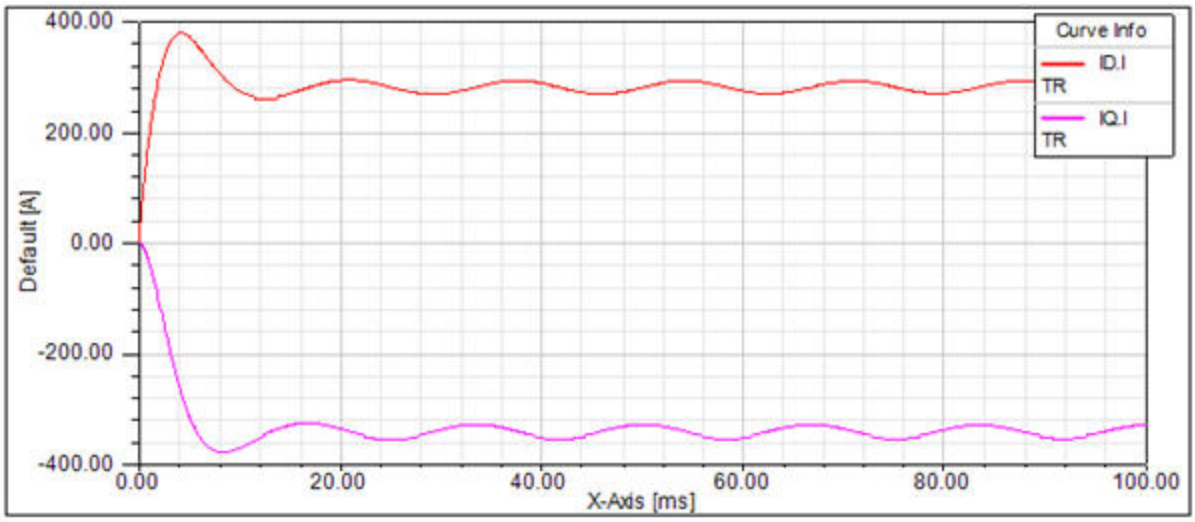

Figure 6. Simulation results-D and Q output currents from Park Transformation (Park1)

Mechanical Transformations

- Domain Transformation Rotational-Rotational_V (ROTB_ROT)
- Domain Transformation Translational-Translational_V (TRB_TR)

Domain Transformation Rotational-Rotational_V

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

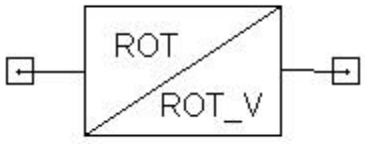

Figure 1. Component symbol

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• Mathematical Description
• Netlist Syntax
• Conservative Pins
• Input/Output Quantities
• Example
• References

Description

This component is used to connect two conservative nodes from different mechanical representations Displacement-Force and Velocity-Force. The Rotational-Rotational_V component works with rotational system components. The component has no user-defined parameters.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

UMODEL ROTB_ROT ?InstanceName(@InstanceName):(@(Refbase)@(ID)) ROTB1:= %0, ROT1:= %1 ( ) SRC: DB(Lib:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
ROTB1	Transformation Pin	Rotational
ROT1	Transformation Pin	Rotational_V

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Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
PHI	Angle [rad]	Output	real
TORQUE	Torque [Nm]	Output	real
OMEGA	Angular Velocity [rad/s]	Output	real

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Example

The transformation models for the mechanical domains allow the connection of models that use different representations. The ACROSS quantity can be either the position or the velocity at the considered network node. Please note that connecting translational and rotational models is not allowed. The schematic of the example is shown in Figure 2, system parameters are listed in Table 3, and the simulation results are shown in Figure 3, and 4.

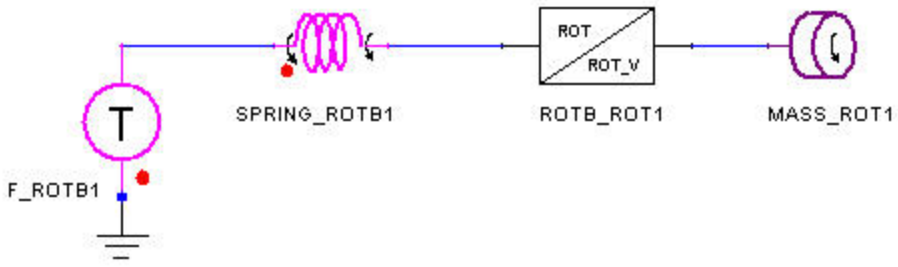

Figure 2. Application example of the rotational Mechanical Transformation model

Table 3. System Parameters

Component	Parameter	Value [unit]
Torque Source F_ROTB1	Value	1 [Nm]
Spring SPRING_ROTB1	C	1 [Nm/rad]
Transformation ROTB_ROT1	PHI	0 [rad]
	TORQUE	0 [Nm]
	OMEGA	0 [rad/s]
Mass MASS_ROT1	J	0.1 [Kg m^2]

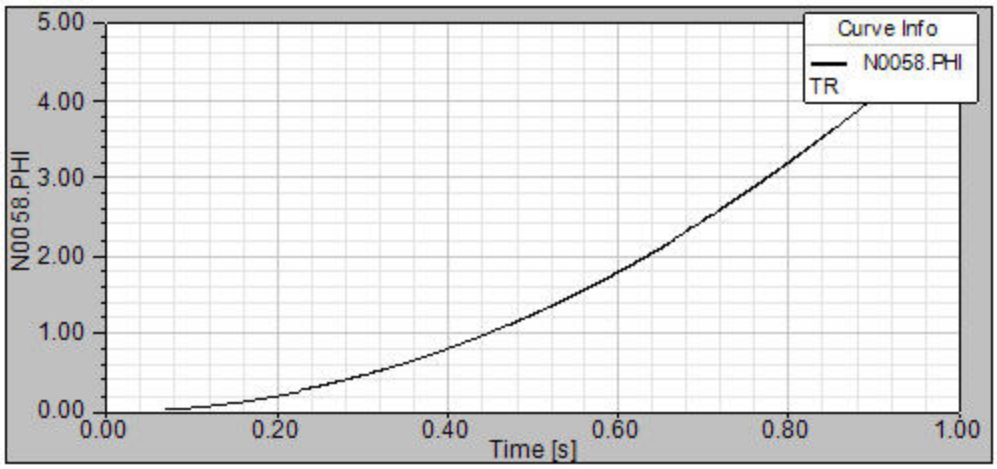

Figure 3. Simulation results-Angle ouput of transformation ROTB_ROT1

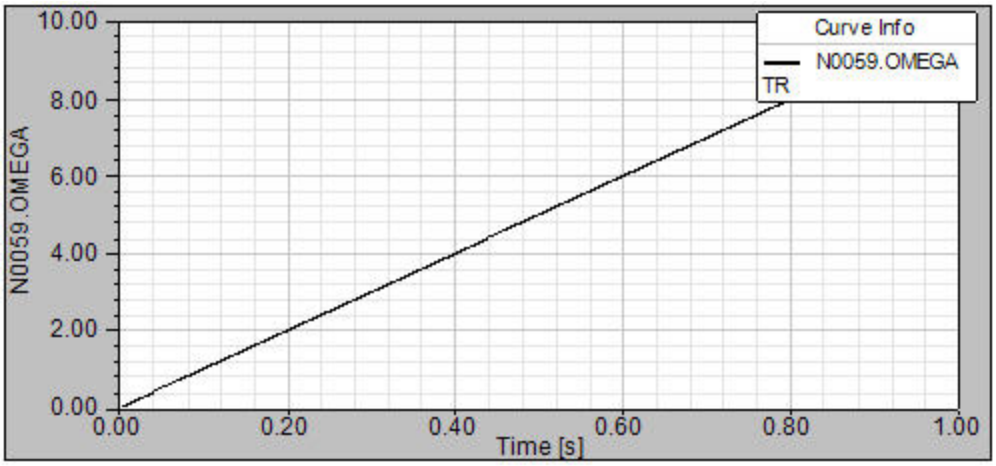

Figure 4. Simulation results-Angular velocity ouput of transformation ROTB_ROT1

Top

References

Domain Transformation Translational-Translational_V

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

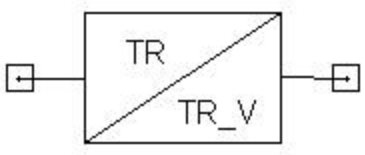

Figure 1. Component symbol

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This component is used to connect two conservative nodes from different mechanical representations Displacement-Force and Velocity-Force. The Translational-Translational_V component works with translational system components. The component has no user-defined parameters.

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Assumptions and Limitations

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Mathematical Description

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Netlist Syntax

UMODEL TRB_TR ?InstanceName(@InstanceName):(@(Refbase)@(ID)) TRB1:= %0, TR1:= %1 ( ) SRC: DB(Lib:=@ModelLibraryName) ;

Top

Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
TRB1	Transformation Pin	Translational
TR1	Transformation Pin	Translational_V

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
S	Displacement [m]	Output	real
F	Force [N]	Output	real
V	Velocity [m/s]	Output	real

Top

Example

The transformation models for the mechanical domains allow the connection of models that use different representations. The ACROSS quantity can be either the position or the velocity at the considered network node. Please note that connecting translational and rotational models is not allowed. The schematic of the example is shown in Figure 2, system parameters are listed in Table 3, and the simulation results are shown in Figure 3, and 4.

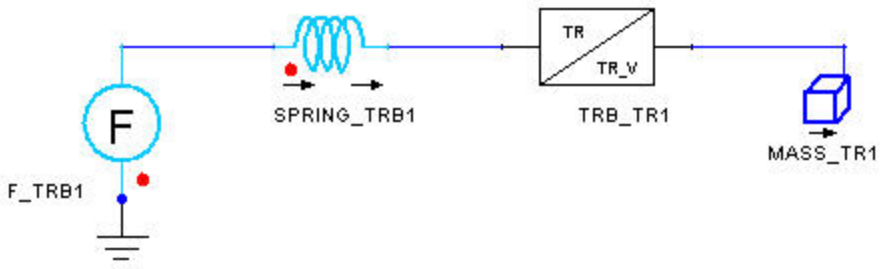

Figure 2. Application example of the translational Mechanical Transformation model

Table 3. System Parameters

Component	Parameter	Value [unit]
Force Source F_TRB1	Value	10 [N]
Spring SPRING_TRB1	C	10000 [N/m]
Transformation TRB_TR1	S	0 [m]
	F	0 [N]
	V	0 [m/s]
Mass MASS_TR1	M	1 [Kg]

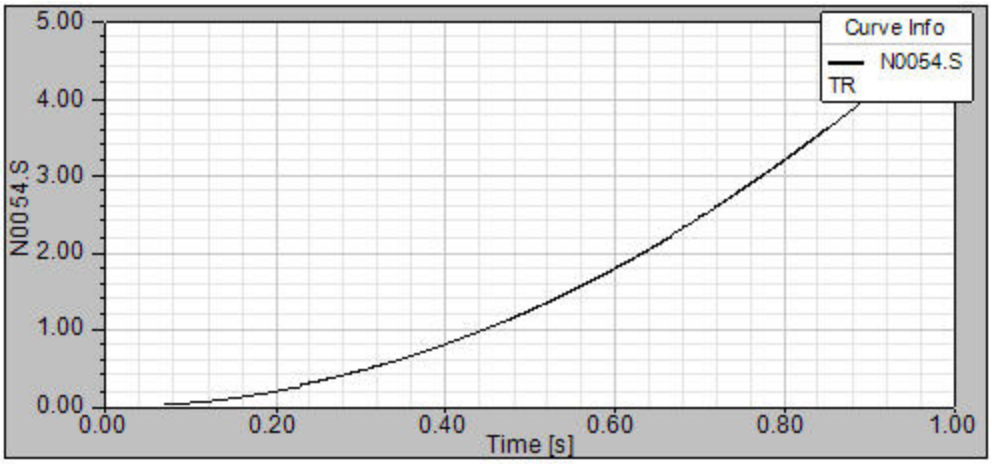

Figure 3. Simulation results-Position ouput of transformation TRB_TR1

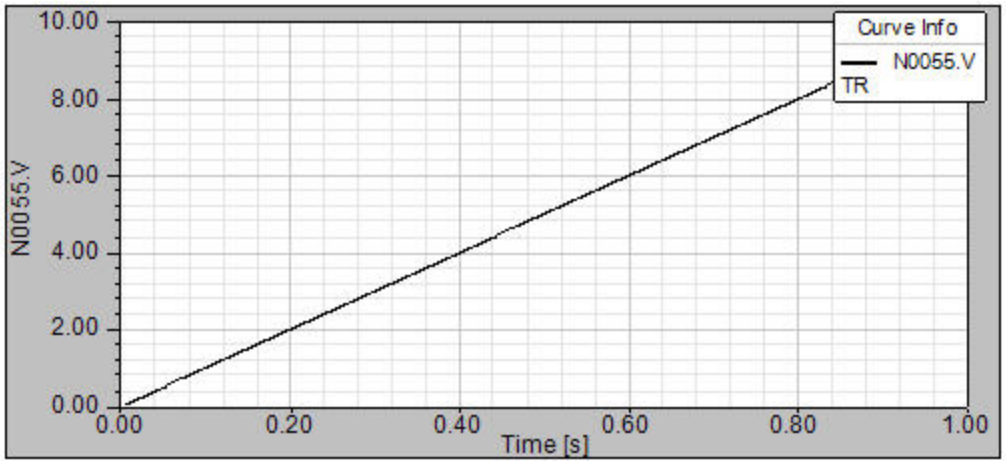

Figure 4. Simulation results-Velocity ouput of transformation TRB_TR1

Top

References

Nature Transformations

- Node Across Quantity Access (C2NC)
- General Domain Transformation (D2D)

Node Across Quantity Access

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Conservative Pins

• Input/Output Quantities

• Example

• References

Description

The C2NC connection model allows you to easily access across quantities of conservative systems and pass them to a block diagram. C2NC components are inserted automatically, when wiring a conservative node to a non-conservative input node of a block.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

INTERN C2NC ?InstanceName(@InstanceName):(@(Refbase)@(ID)) N1 := %0 (&($:= # ,)^ (InstanceName,CompDlg));

Top

Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
N1	Transformation Pin	Electrical

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
OUT	Output Signal	Output	real

Top

Example

The C2NC component is automatically inserted to transform the convservative output for use as the input to an Integrator Block. The schematic of the example is shown in Figure 2, system parameters are listed in Table 3, and the simulation results are shown in Figure 3.

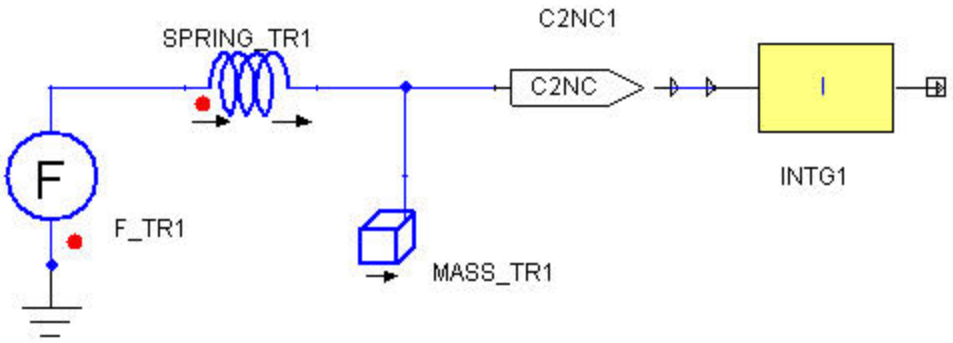

Figure 2. Application example of the Conservative node to Non-Conservative node transformation

Table 3. System Parameters

Component	Parameter	Value [unit]
Force Source F_TR1	VALUE	1 [N]
Spring SPRING_TR1	C	100 [N/m]
Mass MASS_TR1	M	1 [Kg]
Node Across Quantity Access C2NC1	OUT	0
Integrator Block INTG1	INPUT	N0073.V
	Integration_ Method	Forward Euler

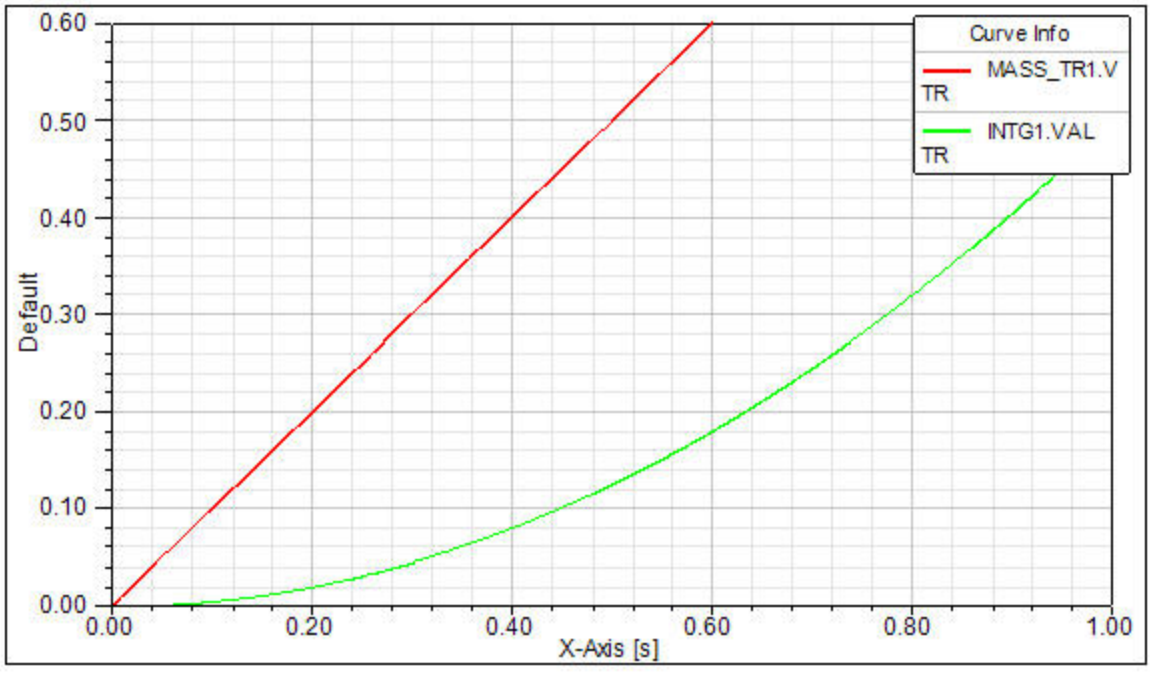

Figure 3. Simulation results-transformed mass velocity into Integrator INTG1 and integrated velocity out of INTG1

Top

References

General Domain Transformation

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Conservative Pins

• Parameters

• Example

• References

Description

The component is used to connect two conservative nodes with different nature types. The component has no user-defined parameters. The two natures are defined from the connected types. Except for mechanical natures, you can connect all types with each other. To connect different translational and rotational natures use the TRB_TR or ROTB_ROT component. The following table shows all possible connections available in the Domain to Domain transformation.

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Assumptions and Limitations

	Electrical	Fluidic	Magnetic	Translational	Trans_V	Rotational	Rot_V	Thermal
Electrical	X	√	√	√	√	√	√	√
Fluidic	√	X	√	√	√	√	√	√
Magnetic	√	√	X	√	√	√	√	√
Trans-	√	√	√	X	TRB_			√

lational					TR			
Trans_V	√	√	√	TRB_TR	X			√
Rotational	√	√	√			X	ROT-B_ROT	√
Rot_V	√	√	√			ROTB_ROT	X	√
Thermal	√	√	√	√	√	√	√	X

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Mathematical Description

Top

Netlist Syntax

UMODEL D2D ?InstanceName(@InstanceName):(@(Refbase)@(ID)) N1:= %0, N2:= %1 (NATURE_1:= @NATURE_1, NATURE_2:= @NATURE_2) SRC: DB(Lib:-:=@ModelLibraryName) ;

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Conservative Pins

Table 1

Name	Port/Terminal Description	Nature/Data Type
N1	Transformation Pin	Electrical
N2	Transformation Pin	Electrical

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
Nature_1	Nature Type of Pin 1	real	0
Nature_2	Nature Type of Pin 2	real	0

Top

Example

The Domain-to-Domain transformation model allows the connection of models from different domains. One can use it if one is sure about the analogies used. In this example a diode is used as a valve in a hydraulic circuit. The schematic of the example is shown in Figure 2, system parameters are listed in Table 3, and the simulation results are shown in Figure 3.

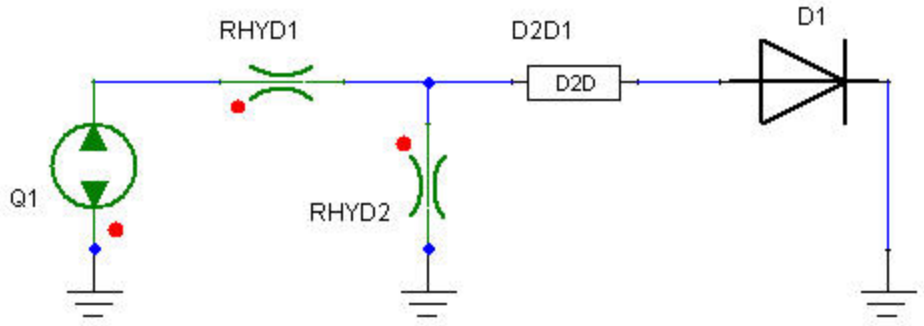

Figure 2. Application example of the General Domain Transformation model

Table 3. System Parameters

Component	Parameter	Value [unit]
Flow Source Q1	AMPL	0.0002 [m^3/sec]
	Type	Sine
	FREQ	1 [Hz]
	OFF	0 [Pas]
Linear Orifice RHYD1/RHYD2	K	1e-7 [m^3/Pas]
Domain Transformation D2D1	Nature_1	Fluidic
	Nature_2	Electrical
Diode D1	TYPE	Equivalent Line
	VF	0 [V]
	RB	1e-9 [Ohm]

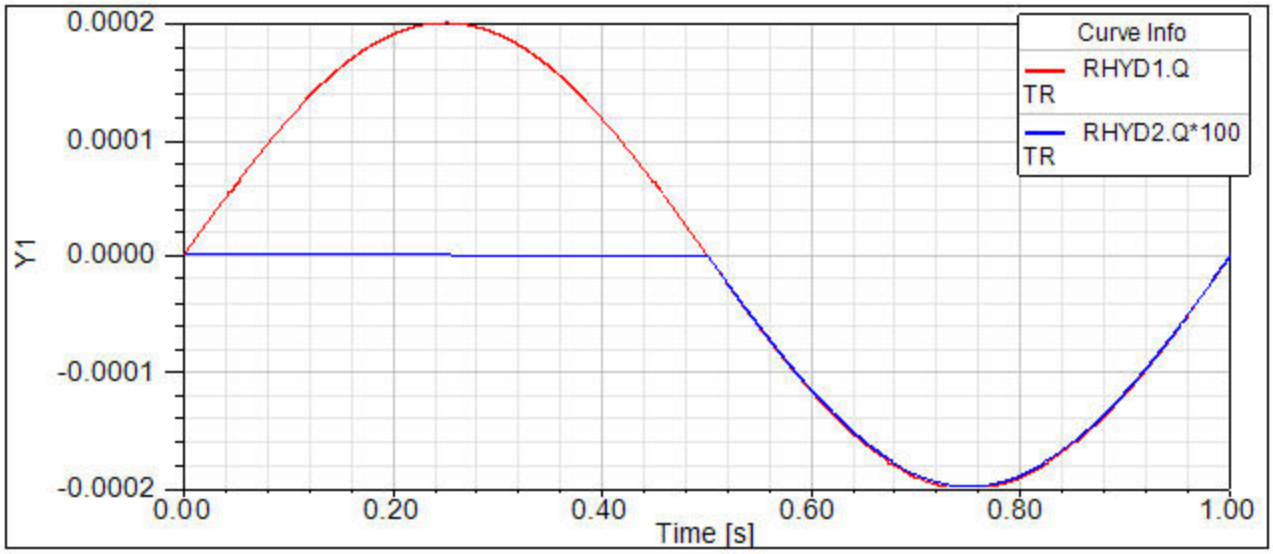

Figure 3. Simulation results-Flow through linear orifices RYHD1 and RHYD2

Top

References

OmniCasters

Omnicasters are interface models that perform conservative-to-signal, signal-to_conservative, quantity-to-signal, signal-to-quantity, and signal-to-signal conversions.

• Conservative-Signal Transformation

• Quantity-Signal Transformation

• Signal-Conservative Transformation

• Signal-Quantity Transformation

• Signal-Signal Transformation

Conservative-Signal Transformations

- Electrical Voltage to Bit Signal Caster (voltage_bitsig)

Electrical Voltage to Bit Signal Caster

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

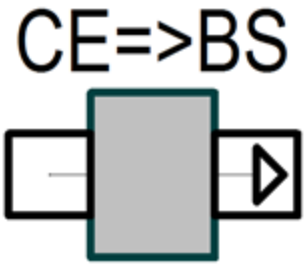

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Conservative Pins

• Parameters

• Input/Output Quantities

• Example

• References

Description

The voltage_bitsig caster provided the ability to connect electrical conservative pins to binary signal ports. The transformation from voltage to binary signal depends on user given threshold value.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data Type
v_in	Electrical port v_in	electrical

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
threshold	Threshold value.	real	2.5

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
bs_out	Bit signal output.	Output	bit

Top

Example

Top

References

Quantity-Signal Transformations

- Real Quantity-Bit Signal Caster (realqty_bitsig)
- Real Quantity-BitVector Signal Caster (realqty_bitvectorsig)
- Real Quantity-Boolean Signal Caster (realqty_booleansig)
- Real Quantity-Integer Signal Caster (realqty_integersig)
- Real Quantity-Real Signal Caster (realqty_realsig)
- Real Quantity-StdLogic Signal Caster (realqty_stdlogicsig)
- Real Quantity-StdLogicVector Signal Caster (realqty_stdlogicvecsig)

Real Quantity-Bit Signal Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

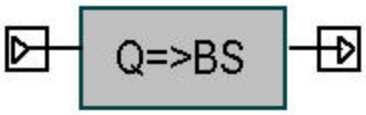

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into a bit signal.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL realqty_bitsig ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (thres := @thres , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
thres	Real Threshold Value	real	1

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
inp	Real Quantity Input	Input	real

Top

Example

Top

References

Real Quantity-BitVector Signal Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

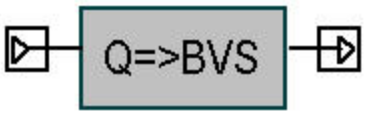

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into a bit vector.

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Assumptions and Limitations

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Mathematical Description

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Netlist Syntax

COUPL realqty_bitvectorsig ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (ts := @ts , length := @length , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
ts	Sample Time	real	0.001
length	Length of BitVector	real	8

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
inp	Real Quantity Input	Input	real

Top

Example

Top

References

Real Quantity-Boolean Signal Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

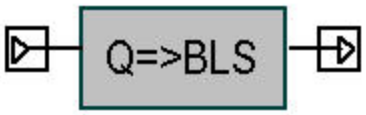

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into a boolean signal.

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Assumptions and Limitations

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Mathematical Description

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Netlist Syntax

COUPL realqty_booleansig ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (thres := @thres , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
thres	Real Threshold Value	real	1

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
inp	Real Quantity Input	Input	real

Top

Example

Top

References

Real Quantity-Integer Signal Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

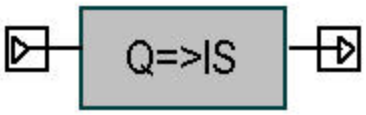

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into an integer signal.

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Assumptions and Limitations

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Mathematical Description

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Netlist Syntax

COUPL realqty_integersig ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (ts := @ts , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
ts	Sample Time	real	0.001

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
inp	Real Quantity Input	Input	real

Top

Example

Top

References

Real Quantity-Real Signal Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

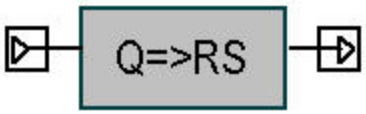

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into an real signal.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

COUPL realqty_realsig ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (ts := @ts , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
ts	Sample Time	real	0.001

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
inp	Real Quantity Input	Input	real

Top

Example

Top

References

Real Quantity-Stdlogic Signal Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

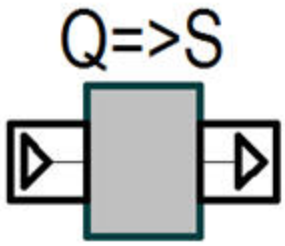

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into a stdlogic signal.

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Assumptions and Limitations

Top

Mathematical Description

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Netlist Syntax

COUPL realqty_stdlogicsig ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (thres:= @thres, inp:= @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\");

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
thres	Real Threshold Value	real	1

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
inp	Real Quantity Input	Input	real

Top

Example

Top

References

Real Quantity-StdLogicVector Signal Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

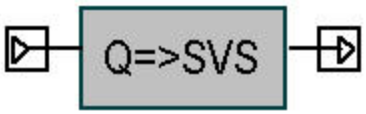

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into a logic vector.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL realqty_stdlogicvecsig ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (ts := @ts , length := @length , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
ts	Sample Time	real	0.001
length	Length of StdLogic Vector	real	8

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
inp	Real Quantity Input	Input	real

Top

Example

Top

References

Signal-Conservative Transformations

- Bit Signal to Electrical Voltage Caster (bitsig_voltage)

Bit Signal to Electrical Voltage Caster

Library: Transformations	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

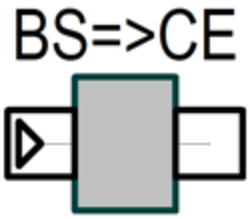

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Conservative Pins

• Parameters

• Input/Output Quantities

• Example

• References

Description

The bitsig_voltage caster provides the ability to connect binary signal ports to electrical conservative pins. The transformation from binary signal to voltage depends on the user-provided nominal voltage values.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

Top

Conservative Pins

Table 1

Name	Port/Terminal description	Nature/Data Type
v_out	Electrical port v_out	electrical

Top

Parameters

Table 2

Name	Description	Data Type	Default Value [Unit]
nominal_ voltage_ zero	The nominal voltage value used when input bit signal is “0” [V].	real	0
nominal_ voltage_ one	The nominal voltage value used when input bit signal is “1” [V].	real	5
t_rise	Rising time when the signal value changed. [sec]	real	0
t_fall	Falling time when the signal value changed [sec]	real	0

Top

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
bs_in	Bit signal input.	Input	bit

Top

Example

Top

References

Signal-Quantity Transformations

- Bit Signal-Real Quantity Caster (bitsig_realqty)
- BitVector Signal-Real Quantity Caster (bitvecsig_realqty)
- Boolean Signal-Real Quantity Caster (booleansig_realqty)
- Integer Signal-Real Quantity Caster (integersig_realqty)
- Real Signal-Real Quantity Caster (realsig_realqty)
- StdLogic Signal-Real Quantity Caster (stdlogicsig_realqty)
- StdLogicVector Signal-Real Quantity Caster (stdlogicvectorsig_realqty)

Bit Signal-Real Quantity Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

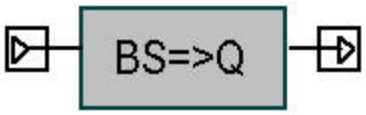

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a bit signal into a real signal quantity.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

COUPL bitsig_realqty ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_rise := @t_rise , t_fall := @t_fall , zero_val := @zero_val , one_val := @one_val , inp := @inp) DST: SIM(Type:-:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_rise	Rise Time	real	0
t_fall	Fall Time	real	0
zero_val	Real Value for 0	real	0
one_val	Real Value for 1	real	1

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
val	Real Quantity Output	Output	real

Top

Example

Top

References

BitVector Signal-Real Quantity Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

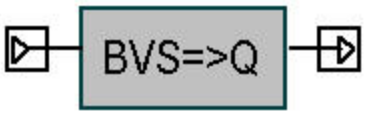

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a bit-vector signal into a real signal quantity.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

COUPL bitvecsig_realqty ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_rise := @t_rise , t_fall := @t_fall , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB (File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_rise	Rise Time	real	0
t_fall	Fall Time	real	0
length	Length of Bitvector	real	8

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Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
val	Real Quantity Output	Output	real

Top

Example

Top

References

Boolean Signal-Real Quantity Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

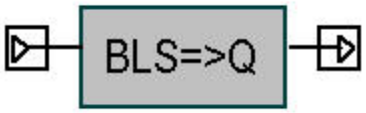

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a boolean signal into a real signal quantity.

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Mathematical Description

Top

Netlist Syntax

COUPL booleansig_realqty ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_rise := @t_rise , t_fall := @t_fall , false_val := @false_val , true_val := @true_val , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:-:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_rise	Rise Time	real	0
t_fall	Fall Time	real	0
false_val	Real Value for FALSE	real	0
true_val	Real Value for TRUE	real	1

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
val	Real Quantity Output	Output	real

Top

Example

Top

References

Integer Signal-Real Quantity Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

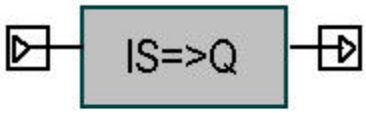

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a integer signal into a real signal quantity.

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Mathematical Description

Top

Netlist Syntax

COUPL integersig_realqty ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_rise := @t_rise , t_fall := @t_fall , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_rise	Rise Time	real	0
t_fall	Fall Time	real	0

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
val	Real Quantity Output	Output	real

Top

Example

Top

References

Real Signal-Real Quantity Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

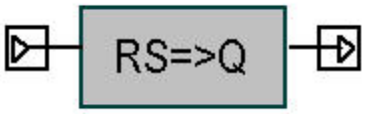

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a real signal into a real quantity.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL realsig_realqty ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_rise := @t_rise , t_fall := @t_fall , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_rise	Rise Time	real	0
t_fall	Fall Time	real	0

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
val	Real Quantity Output	Output	real

Top

Example

Top

References

Stdlogic Signal-Real Quantity Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

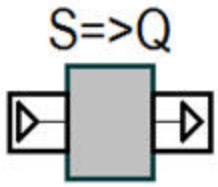

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a stdlogic signal into a real signal quantity.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL stdlogic_realqty ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_rise:= @t_rise, t_fall:= @t_fall, zero_val:= @zero_val, one_val:= @one_val, inp:= @inp) DST: SIM(Type:-:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\");

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_rise	Rise Time	real	0
t_fall	Fall Time	real	0
zero_val	Real Value for 0	real	0
one_val	Real Value for 1	real	1

Top

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
val	Real Quantity Output	Output	real

Top

Example

Top

References

StdLogicVector Signal-Real Quantity Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

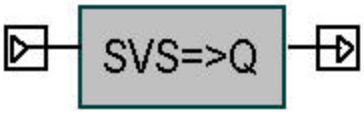

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Input/Output Quantities

• Example

• References

Description

This omnicaster converts a StdLogicVector signal into a real quantity.

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Mathematical Description

Top

Netlist Syntax

COUPL stdlogicvectorsig_realqty ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_rise := @t_rise , t_fall := @t_fall , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_rise	Rise Time	real	0
t_fall	Fall Time	real	0
length	Length of Stdlogic Vector	real	8

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Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
val	Real Quantity Output	Output	real

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Example

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References

Signal-Signal Transformation

- Bit-Boolean Caster (bit_boolean)
- Bit-Integer Caster (bit_integer)
- Bit-Real Caster (bit_real)
- Bit-Stdlogic Caster (bit_stdlogic)
- BitVector-Integer Caster (bitvector_integer)
- BitVector-Real Caster (bitvector_real)
- BitVector-StdLogicVector Caster (bitvector_stdlogicvector)
- Boolean-Bit Caster (boolean_bit)
- Boolean-Integer Caster (boolean_integer)
- Boolean-Real Caster (boolean_real)
- Boolean-Stdlogic Caster (boolean_stdlogic)
- Integer-Bit Caster (integer_bit)
- Integer-BitVector Caster (integer_bitvector)
- Integer-Boolean Caster (integer_boolean)
- Integer-Real Caster (integer_real)
- Integer-StdLogicVector Caster (integer_stdlogicvector)
- Real-Bit Caster (real_bit)
- Real-BitVector Caster (real_bitvector)
- Real-Boolean Caster (real_boolean)
- Real-Integer Caster (real_integer)
- Real-StdLogicVector Caster (real_stdlogicvector)
- Stdlogic-Bit Caster (stdlogic_bit)
- Stdlogic-Boolean Caster (stdlogic_boolean)
- StdLogicVector-BitVector Caster (stdlogicvector_bitvector)
- StdLogicVector-Integer Caster (stdlogicvector_integer)
- StdLogicVector-Real Caster (stdlogicvector_real)

Bit-Boolean Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

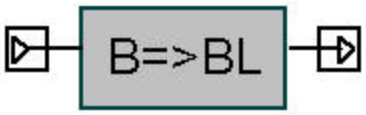

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a bit signal into a boolean quantity.

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Mathematical Description

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Netlist Syntax

COUPL bit_boolean ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0

Top

Example

Top

References

Bit-Integer Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

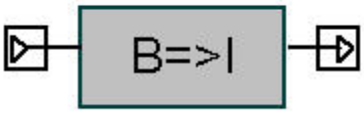

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a bit signal into a integer quantity.

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Mathematical Description

Top

Netlist Syntax

COUPL bit_integer ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , zero_val := @zero_val , one_val := @one_val , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
zero_val	Integer Value for Bit 0	real	0
one_val	Integer Value for Bit 1	real	1

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Example

Top

References

Bit-Real Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

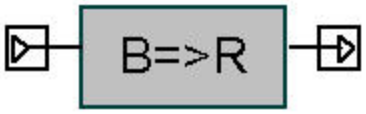

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a bit signal into a real quantity.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL bit_real ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , zero_val := @zero_val , one_val := @one_val , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
zero_val	Integer Value for Bit 0	real	0
one_val	Integer Value for Bit 1	real	1

Top

Example

Top

References

Bit-Stdlogic Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

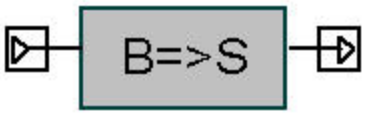

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a bit signal into a STDlogic quantity.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL bit_stdlogic ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0

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Example

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References

BitVector-Integer Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a bit vector signal into an integer quantity.

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Mathematical Description

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Netlist Syntax

COUPL bitvector_integer ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of Bit Vector	real	8

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Example

Top

References

BitVector-Real Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

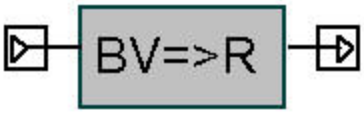

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a bit vector signal into an real quantity.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL bitvector_real ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of Bit Vector	real	8

Top

Example

Top

References

BitVector-StdLogicVector Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

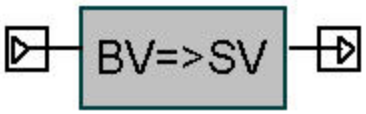

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

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• Example

• References

Description

This omnicaster converts a bit vector into a Stdlogic vector.

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Mathematical Description

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Netlist Syntax

COUPL bitvector_stdlogicvector ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_ prop := @t_prop , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of Bit Vector	real	8

Top

Example

Top

References

Boolean-Bit Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

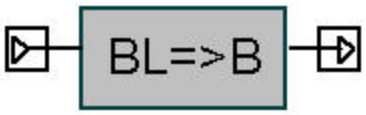

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a Boolean into a bit signal.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL boolean_bit ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0

Top

Example

Top

References

Boolean-Integer Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

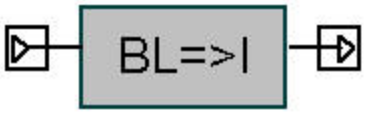

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a Boolean into an integer.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL boolean_integer ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , false_val := @false_val , true_val := @true_val , inp := @inp) DST: SIM(Type:-:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
false_ val	Integer Value for FALSE	real	0
true_val	Integer Value for TRUE	real	1

Top

Example

Top

References

Boolean-Real Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

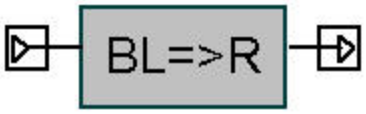

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a Boolean into an real value.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL boolean_real ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , false_val := @false_val , true_val := @true_val , inp := @inp) DST: SIM(Type:-:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
false_val	Real Value for FALSE	real	0
true_val	Real Value for TRUE	real	1

Top

Example

Top

References

Boolean-Stdlogic Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

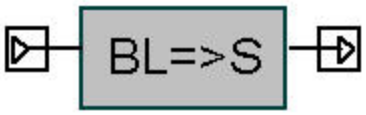

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts a Boolean into a Stdlogic value.

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Assumptions and Limitations

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Mathematical Description

Top

Netlist Syntax

COUPL boolean_stdlogic ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0

Top

Example

Top

References

Integer-Bit Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

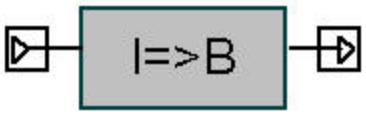

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts an integer into a bit signal.

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Assumptions and Limitations

Top

Mathematical Description

Top

Netlist Syntax

COUPL integer_bit ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , thres := @thres , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

Top

Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
thres	Integer Threshold Value	real	1

Top

Example

Top

References

Integer-BitVector Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

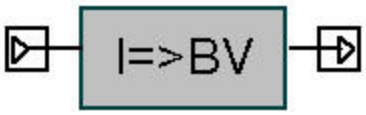

Figure 1. Component symbol

• Description

• Assumptions and Limitations

• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts an integer into a bit vector signal.

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Assumptions and Limitations

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Mathematical Description

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Netlist Syntax

COUPL integer_bitvector ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of Bit Vector	real	8

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References

Integer-Boolean Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

• Description

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• Mathematical Description

• Netlist Syntax

• Parameters

• Example

• References

Description

This omnicaster converts an integer into a boolean.

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Netlist Syntax

COUPL integer_boolean ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , thres := @thres , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
thres	Integer Threshold Value	real	1

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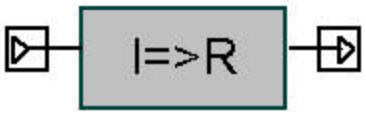
References

Integer-Real Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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This omnicaster converts an integer into a real value.

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Netlist Syntax

COUPL integer_real ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0

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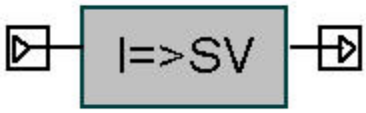
Integer-StdLogicVector Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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This omnicaster converts an integer into a Stdlogic vector.

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Netlist Syntax

COUPL integer_stdlogicvector ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of StdLogic Vector	real	8

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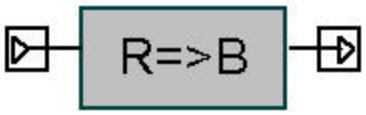
References

Real-Bit Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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This omnicaster converts an real value into a bit value.

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Netlist Syntax

COUPL real_bit ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , thres := @thres , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Parameters

Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
thres	Real Threshold Value	real	1

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Real-BitVector Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

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This omnicaster converts an real value into a bit vector.

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Netlist Syntax

COUPL real_bitvector ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of Bit Vector	real	8

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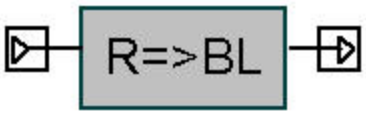
Real-Boolean Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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Description

This omnicaster converts an real value into a boolean value.

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Netlist Syntax

COUPL real_boolean ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , thres := @thres , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
thres	Real Threshold Value	real	1

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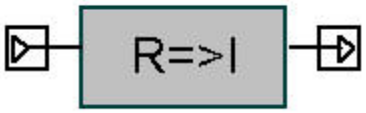
References

Real-Integer Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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This omnicaster converts an real value into a integer value.

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Netlist Syntax

COUPL real_integer ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0

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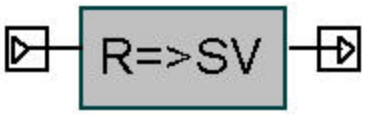
Real-StdLogicVector Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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This omnicaster converts an real value into a Stdlogic vector.

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Netlist Syntax

COUPL real_stdlogicvector ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of StdLogic Vector	real	8

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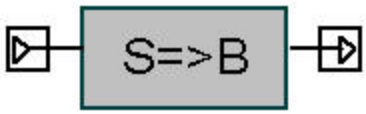
Stdlogic-Bit Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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Netlist Syntax

COUPL stdlogic_bit ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:-:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
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Stdlogic-Boolean Caster

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This omnicaster converts an Stdlogic value into a boolean.

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Netlist Syntax

COUPL stdlogic_boolean ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , inp := @inp) DST: SIM(Type:=SimVHDL) SRC: DB(File:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0

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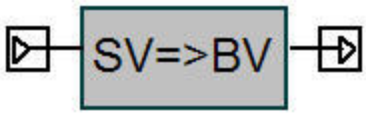
StdLogicVector-BitVector Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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This omnicaster converts a Stdlogic vector value into a bit vector.

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Netlist Syntax

COUPL stdlogicvector_bitvector ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of StdLogic Vector	real	8

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StdLogicVector-Integer Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

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This omnicaster converts a Stdlogic vector value into an integer value.

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Netlist Syntax

COUPL stdlogicvector_integer ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of StdLogic Vector	real	8

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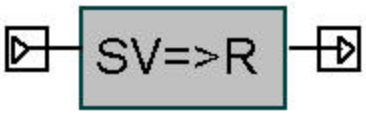
StdLogicVector-Real Caster

Library: Transformation	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2



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Description

This omnicaster converts a Stdlogic vector value into an real value.

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Netlist Syntax

COUPL stdlogicvector_real ?InstanceName(@InstanceName):(@(Refbase)@(ID)) (t_prop := @t_prop , length := @length , &inp($:=#,)) DST: SIM(Type:=SimVHDL) SRC: DB(File:-:=@ModelLibraryName, Lang:=VHDLA, Lvl:=\"@Architecture\"); ;

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Table 1

Name	Description	Data Type	Default Value [Unit]
t_prop	Propagation Time	real	0
length	Length of StdLogic Vector	real	8

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