Getting Started with SI Xplorer

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Conventions Used in this Guide

Please take a moment to review how instructions and other useful information are presented in this documentation.

- Procedures are presented as numbered lists. A single bullet indicates that the procedure has only one step.
- Command font is used for:
  - Command line prompts that should be typed exactly as written.
  - Script examples.
- Bold type is used for the following:
  - Names of windows, workspaces, menu commands, and options.
    - Menu commands are often separated by angle brackets (e.g., **File** > **Open**).
  - Labeled keys on the computer keyboard (e.g., **Enter**).
- Italic type is used for the following:
  - Emphasis.
  - Publication titles.
- The plus sign (+) is used between keyboard keys to indicate that you should press the keys at the same time (e.g., “Press **Shift**+**F1**” means to press the **Shift** key and, while holding it down, press the **F1** key). You should always depress the modifier key or keys first (e.g., **Shift**, **Ctrl**, **Alt**, or **Ctrl**+**Shift**), continue to hold it/them down, and then press the last key in the instruction.

Getting Help: Ansys Technical Support

For information about Ansys Technical Support, go to the Ansys corporate Support website, http://www.ansys.com/Support. You can also contact your Ansys account manager in order to obtain this information.

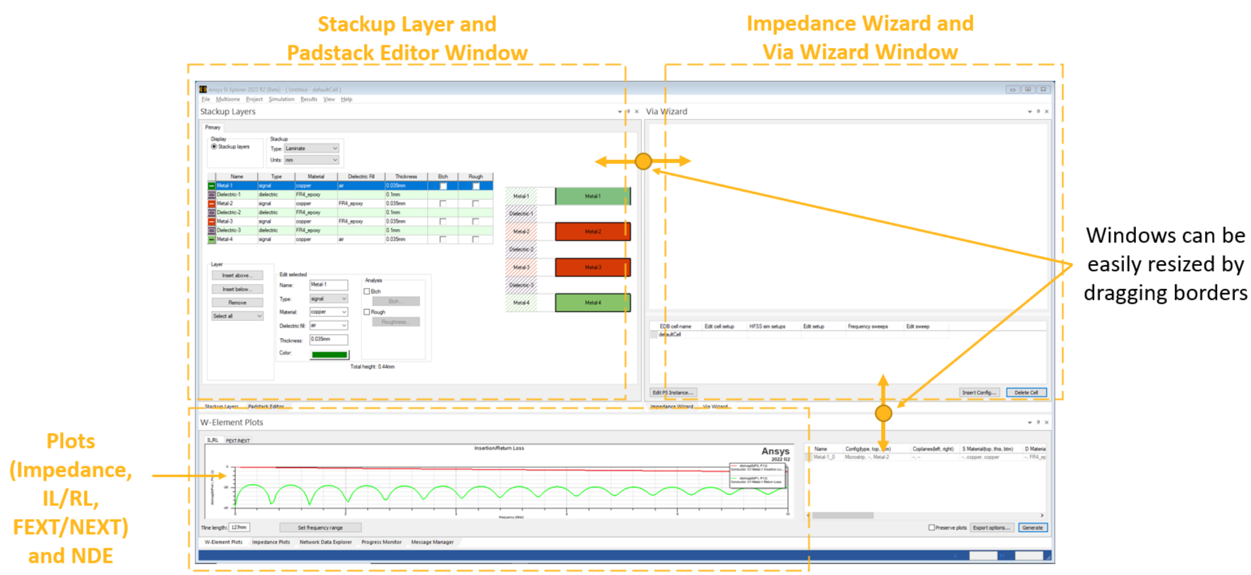
All Ansys software files are ASCII text and can be sent conveniently by e-mail. When reporting difficulties, it is extremely helpful to include very specific information about what steps were taken or what stages the simulation reached, including software files as applicable. This allows more rapid and effective debugging.

Table of Contents

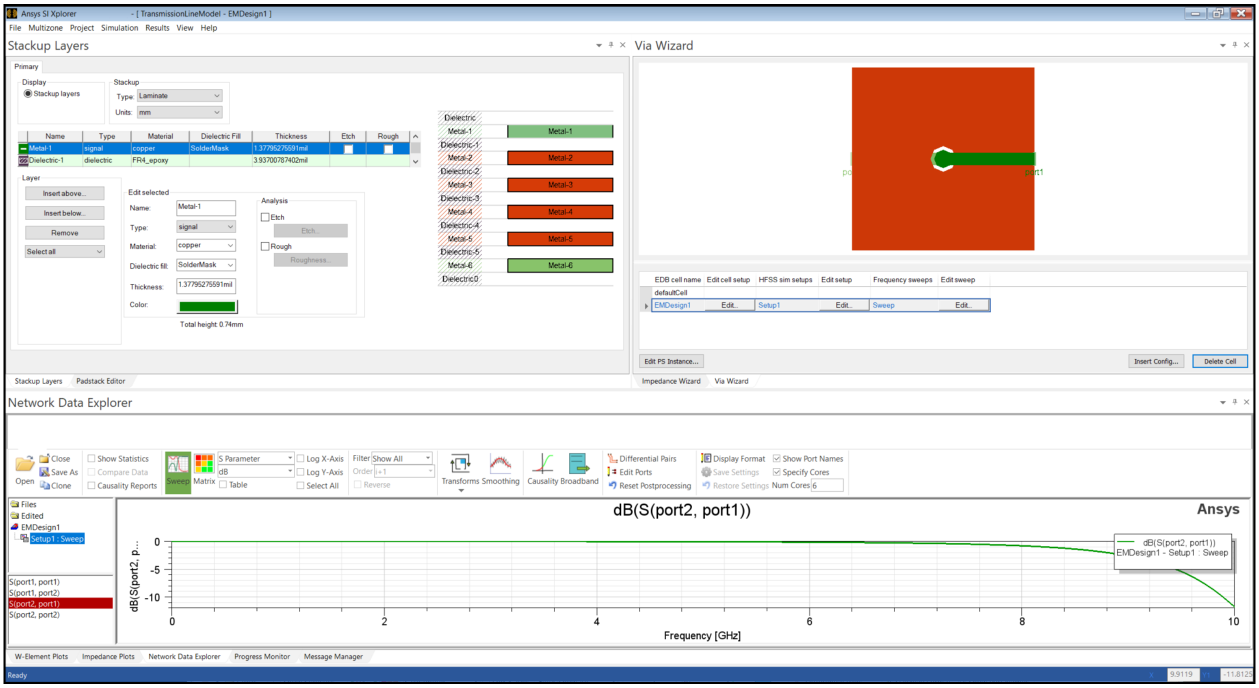
1 - Introduction

This Getting Started Guide is intended to quickly familiarize users with the capabilities of SI Xplorer. SI Xplorer is useful for pre-layout model generation and consists of several tools, including the following:

- Stackup Layers Editor
- Padstack Editor
- Network Data Explorer
- Impedance Wizard (i.e., 2D MoM solver)
- Via Wizard

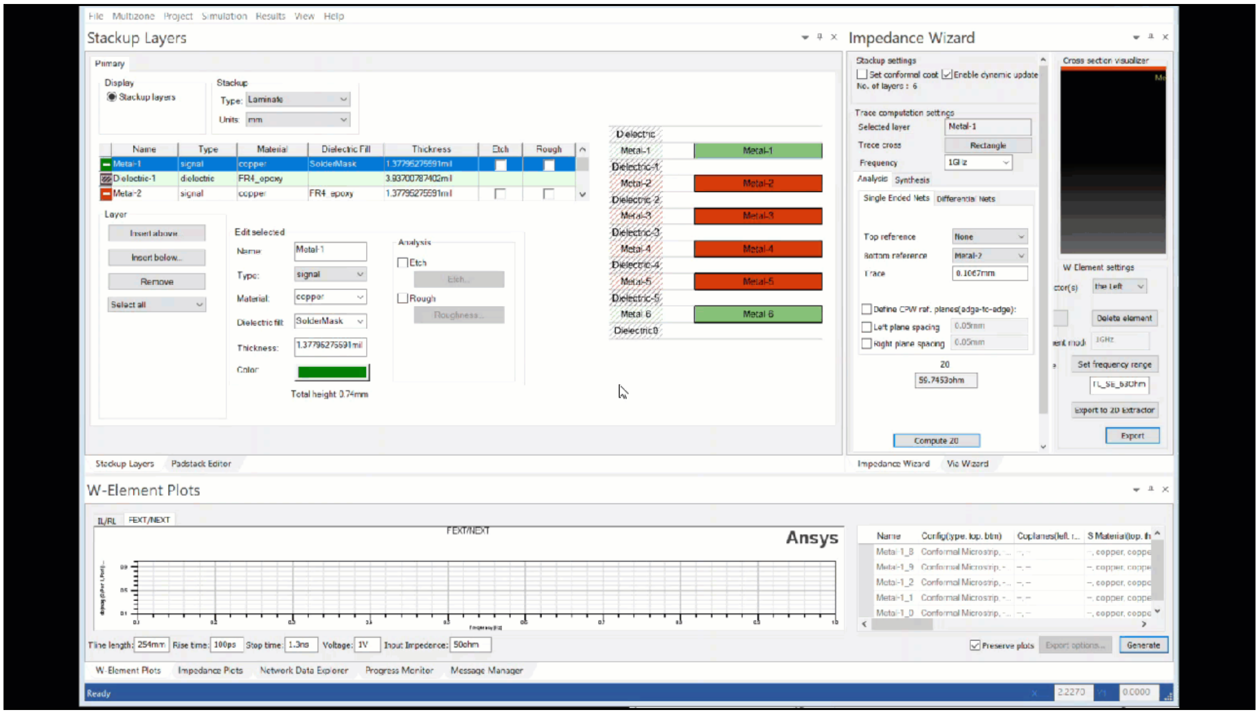


This guide leads you step-by-step through adding and editing a stackup, editing the padstack, defining a transmission line, generating W-element plots, configuring vias, modifying and analyzing the subsequent design, viewing the results, then exporting various elements to Circuit (e.g., W-element, Touchstone, and Broadband SPICE models) for further design and analysis.



Resizing SI Xplorer

Every window within SI Xplorer can be resized, as appropriate, to more easily interact with the active project or enter values in tables and fields. While following the instructions in the Getting Started Guide, resize windows as appropriate. Reset the workspace at any time by navigating to **View** > **Toolbars and Docking Windows** > **Reset Workspaces**.



Continue to Editing the Stackup and Padstacks.

2 - Editing the Stackup and Padstacks

This section explains how to perform the following tasks:

- Start SI Xplorer and Import a Stackup
- Create a Stackup
- Edit the Padstacks

Starting SI Xplorer and Importing a Stackup

Complete the steps in the following subsections to start **SI Xplorer** and, if appropriate, import a stackup.

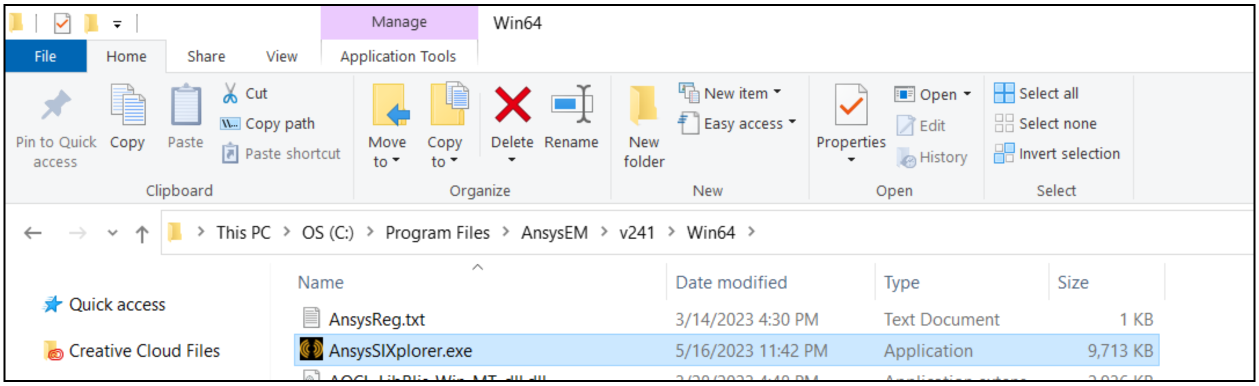
> **Note:**
>
> Stackups created in **SIwave** and **HFSS 3D Layout** can be imported directly into **SI Xplorer**.

Starting SI Xplorer

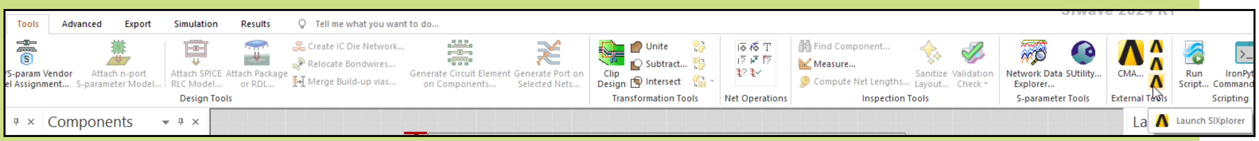
1. Depending on the user's operating system, navigate to one of the following locations:
   - Windows: **\Program Files\AnsysEM\[*version*]\Win64**
   - Linux: **/Program Files/AnsysEM/[*version*]/Linx64/**

   > **Note:**
   >
   > Where **[*version*]** is the current Ansys software version installed (e.g., if version 24.1 is installed, then enter ***v241***).

2. Double-click the file **AnsysSIXplorer.exe**.

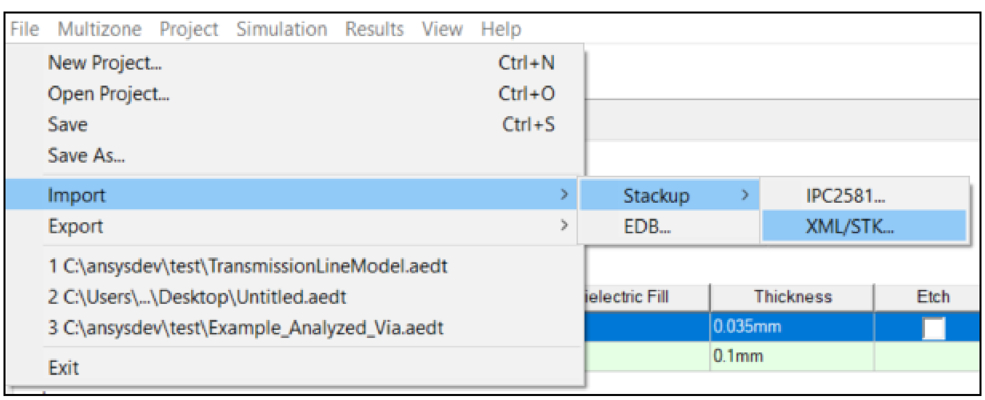


3. Wait for **SI Xplorer** to start.

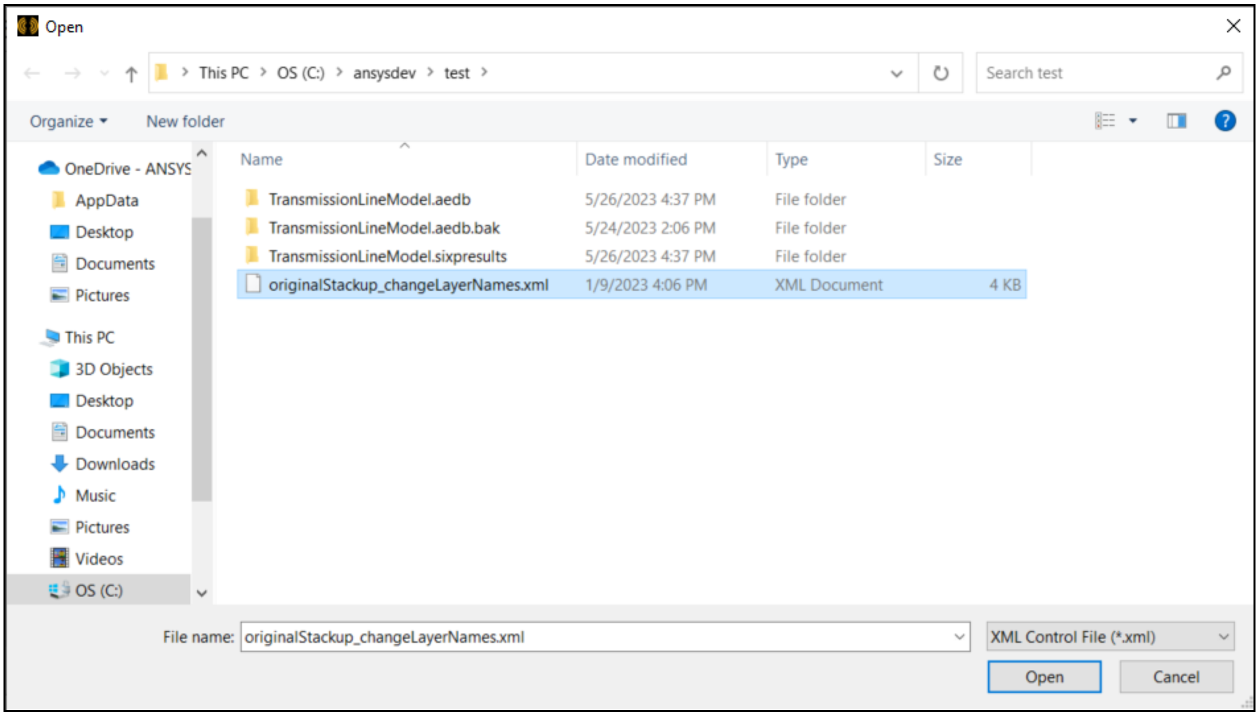
> **Note:**
>
> **SI Xplorer** can also be started from **SIwave** (i.e., from the **SIwave Tools** tab, navigate to the **External Tools** area. Then click **Launch SI Xplorer** and wait for **SI Xplorer** to start.
>
> 
>

Importing a Project

1. From **File**, select **Import** > **Stackup** > **XML/STK**.

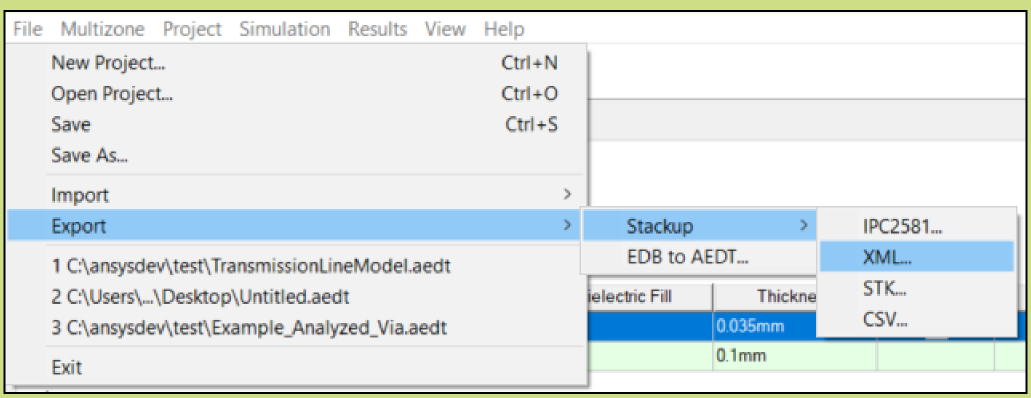


2. Navigate to an appropriate stackup *.*xml* file. Then select the file and click **Open** to populate **SI Xplorer** with the stackup's parameters.



Note:

Export a stackup by navigating to **File** > **Export** > **Stackup** > **XML**.

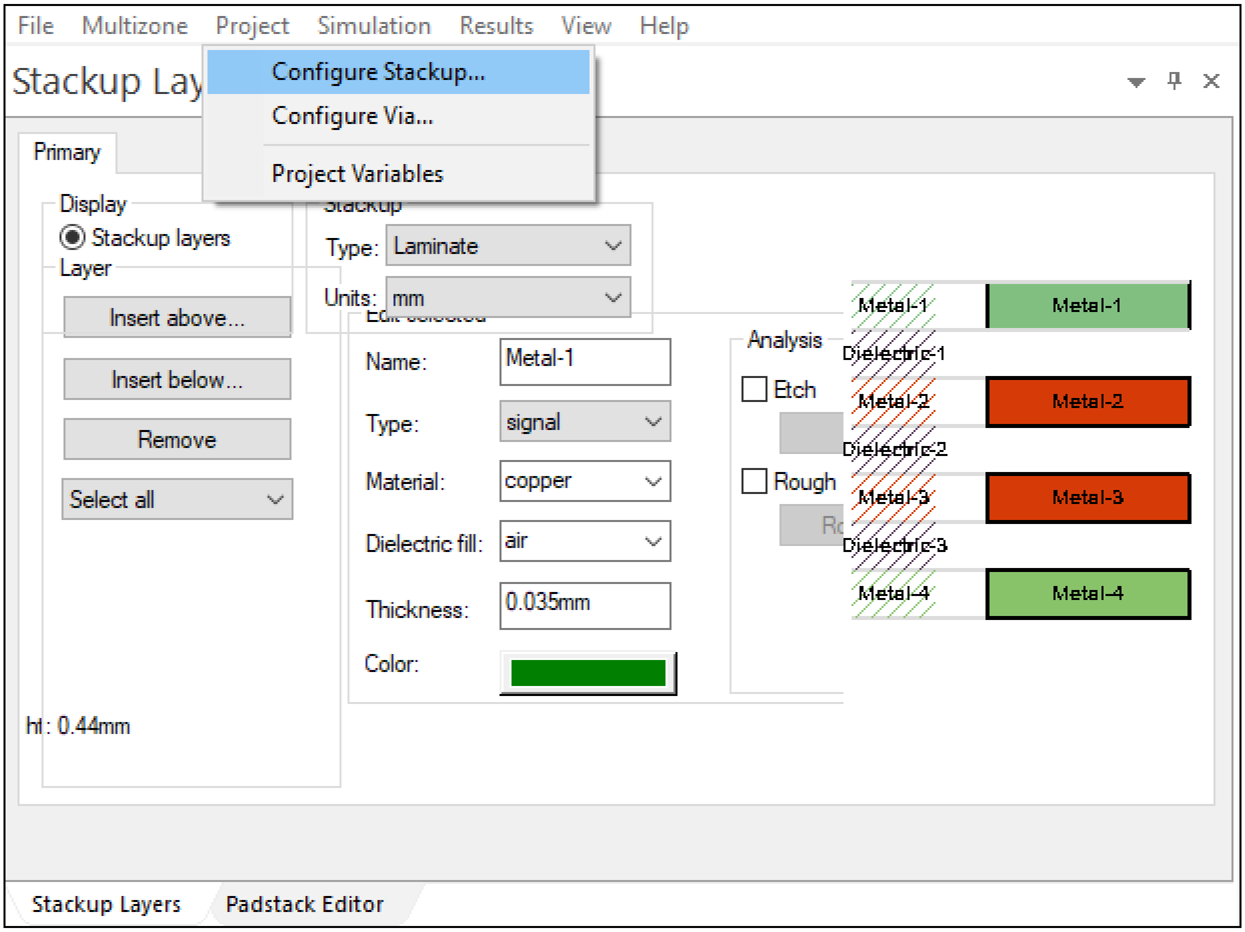


Continue to Creating a Stackup.

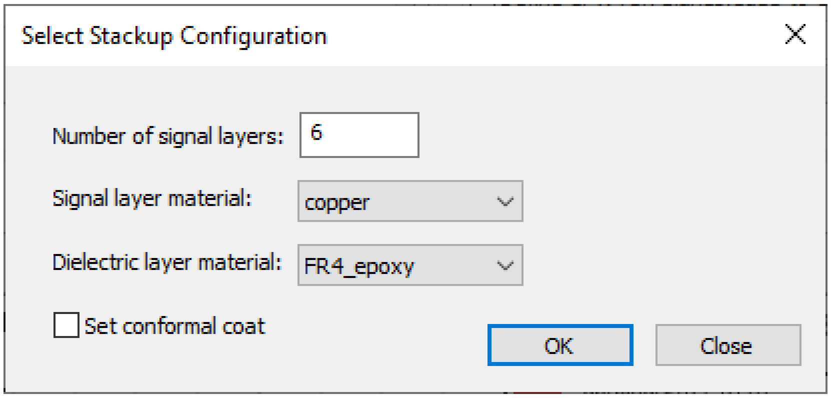
Creating a Stackup

Complete the following steps to create a six-layer stackup.

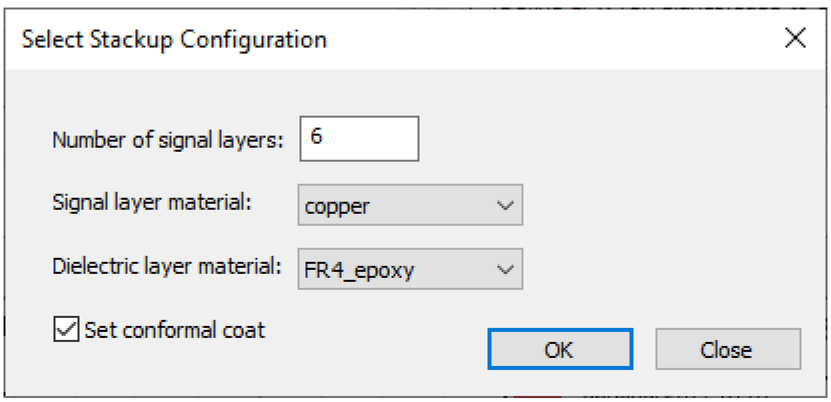
1. From **Project**, select **Configure Stackup** to open the **Select Stackup Configuration** window.



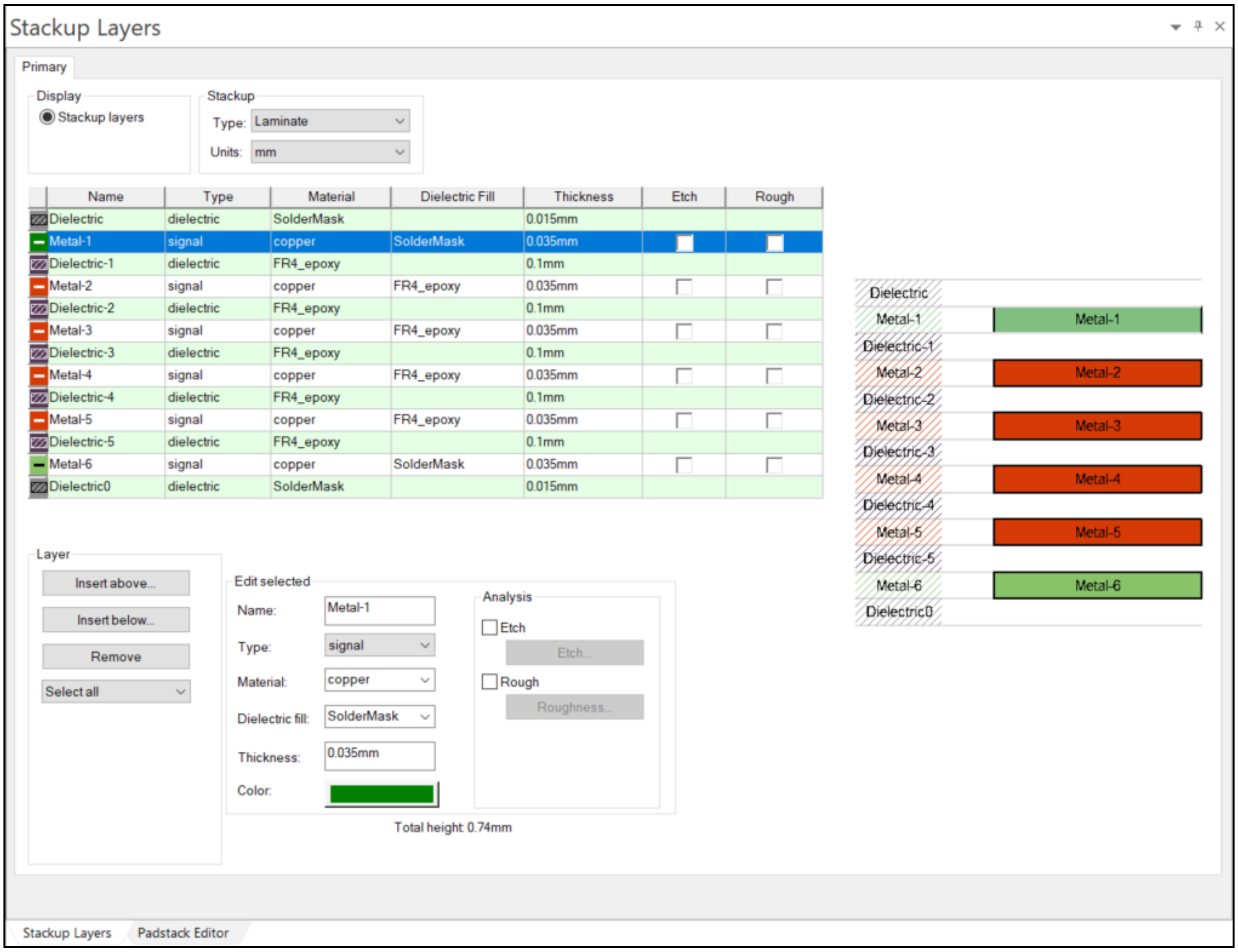
2. Ensure the **Number of signal layers** is **6** (i.e., default value).



3. Check the **Set conformal coat** box.



4. Click **OK** to close the **Select Stackup Configuration** window and add the new stackup to the **Stackup Layers** window.

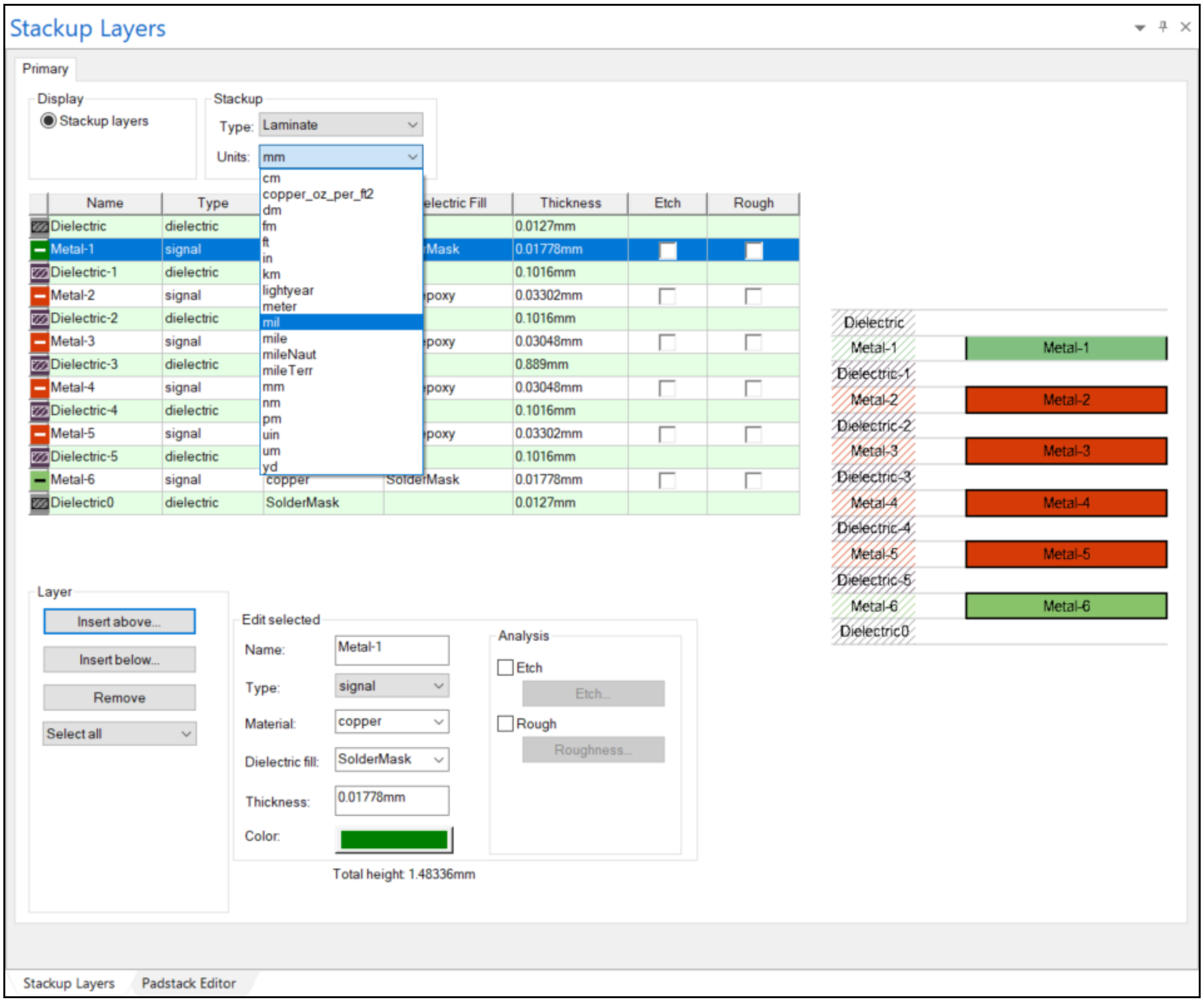


Note:

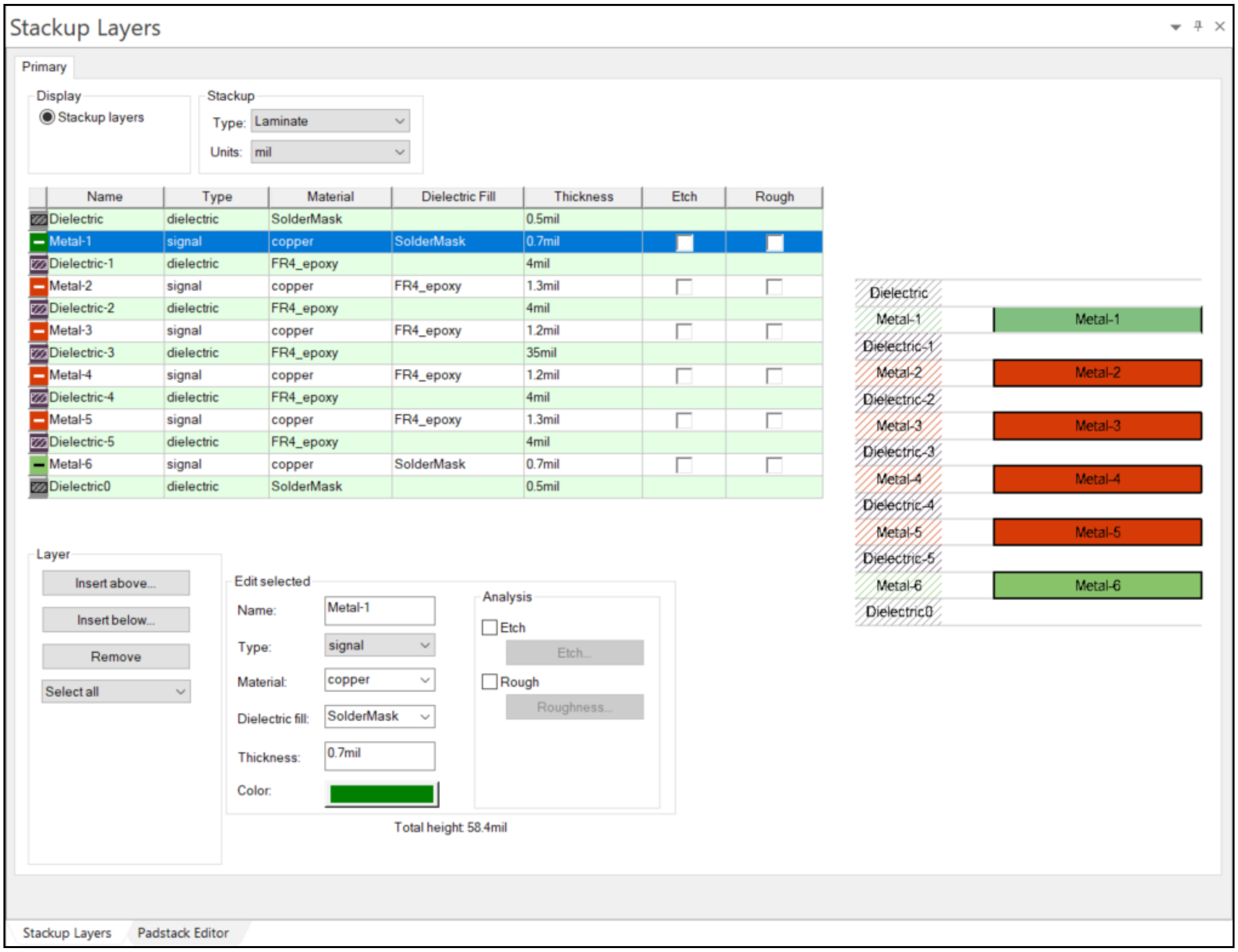
Resize the **Stackup Layers** window so the layers table is visible. Refer to the [Resizing SI Xplorer subsection in the Introduction](#).

5. From the **Stackup Layers** window, do the following:

   a. From the **Stackup** area, select **mil** from the **Units** pull-down menu.



b. Edit the contents of the **Thickness** column to match the following example:



Note:

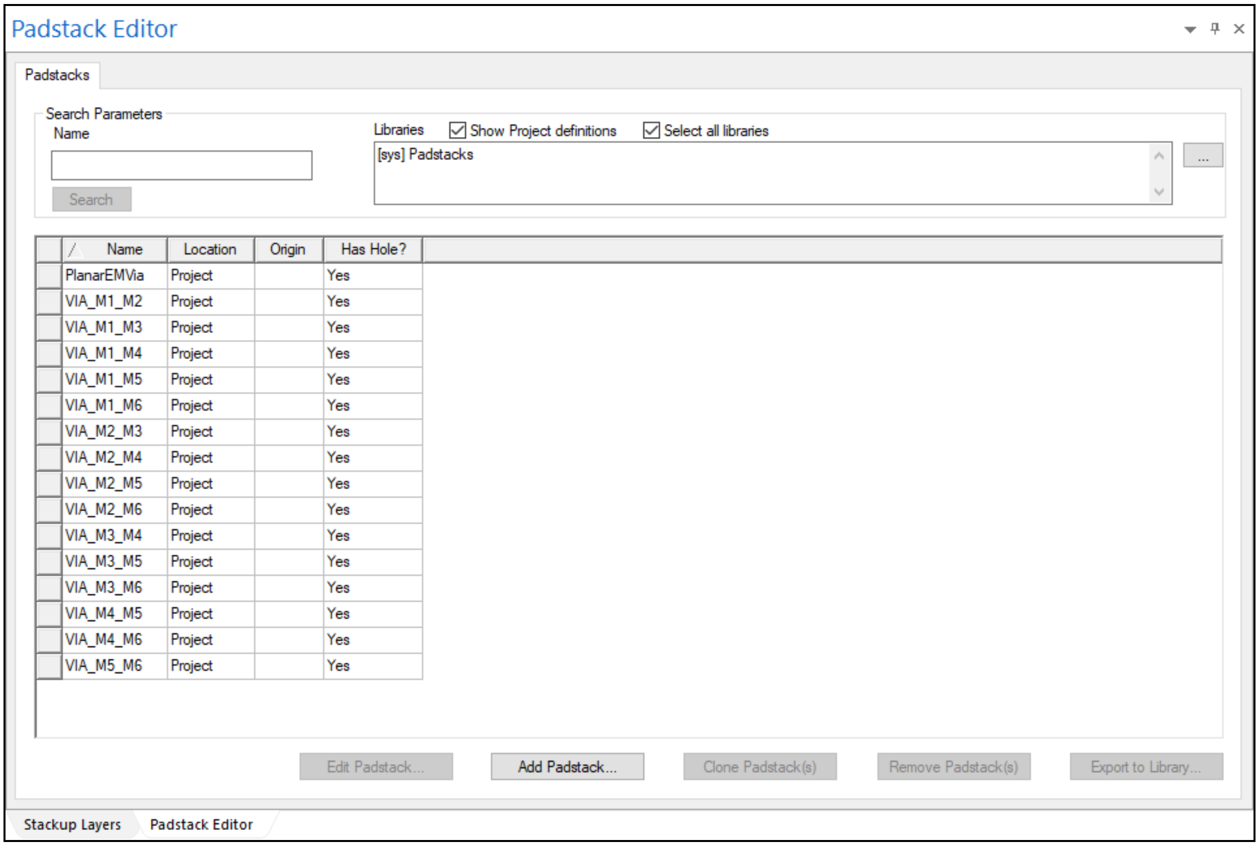
Material definitions (i.e., dielectrics) can be edited from the **Stackup Layers** window, but there is no need to modify the definitions now.

Continue to Editing the Padstack.

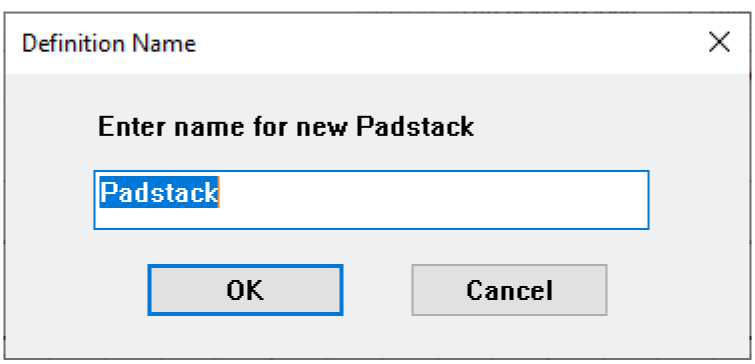
Editing the Padstacks

Complete the following steps to edit the padstacks (i.e., vias).

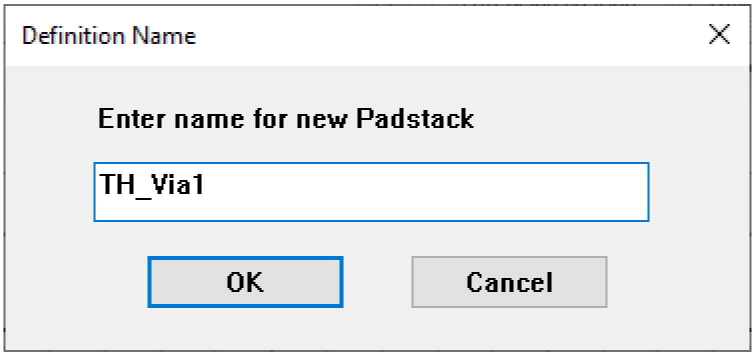
1. Navigate to the bottom of the **Stackup Layers** window and select the **Padstack Editor** tab.



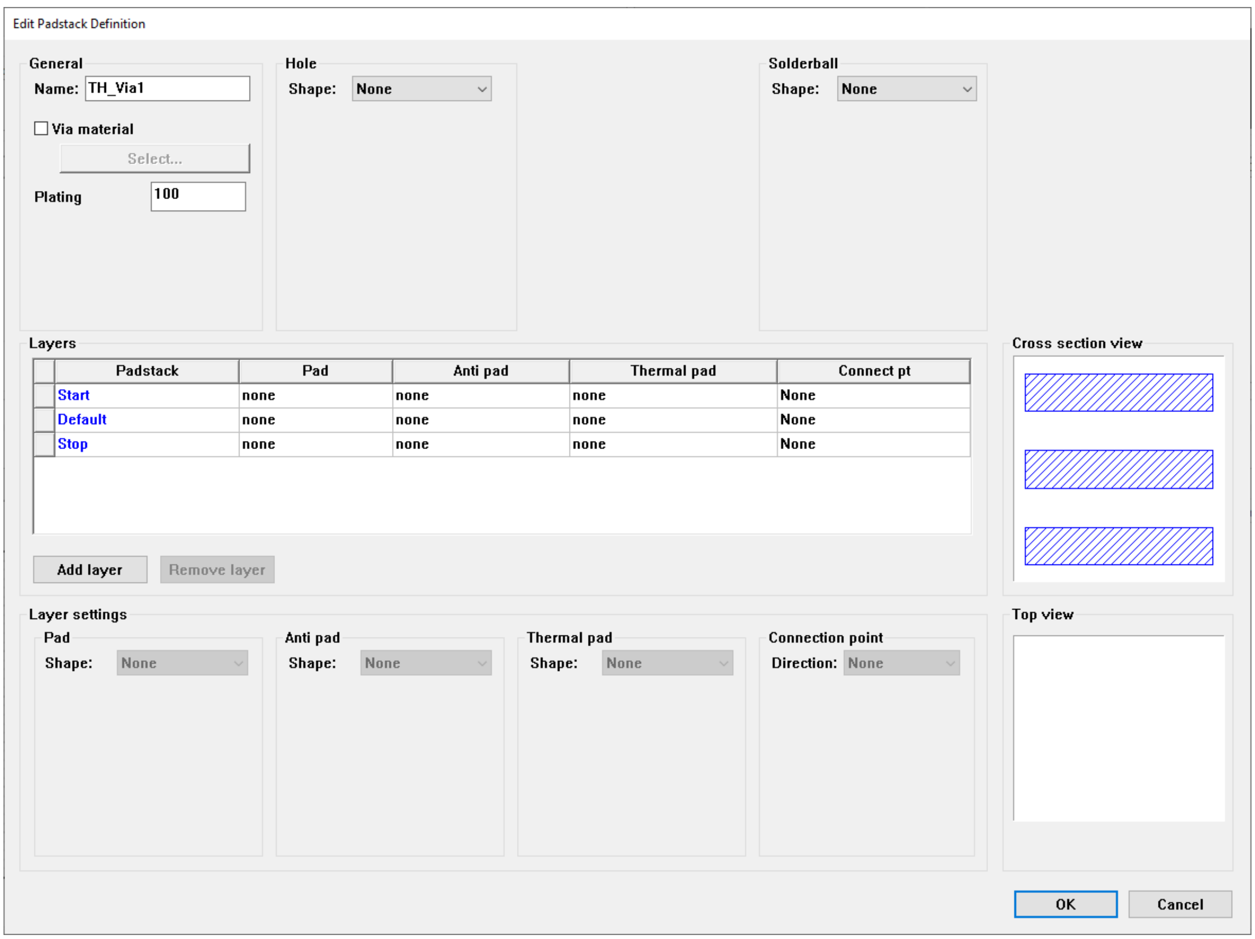
2. From the **Padstack Editor** window, define a new via by doing the following:
   a. Click **Add Padstack** to open the **Definition Name** window.



b. From the field, enter a new name for the padstack (e.g., **TH_Via1**).

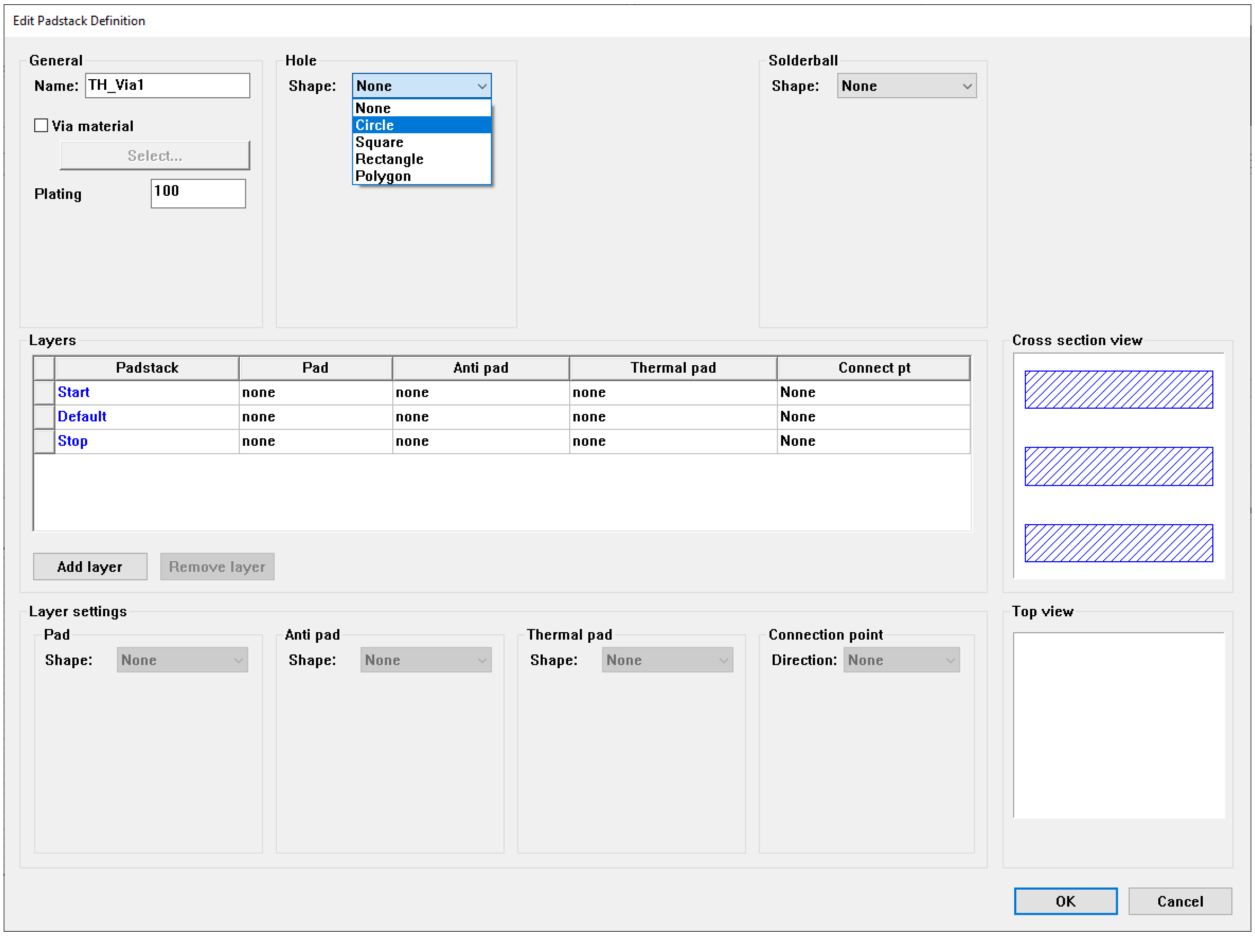


c. Click **OK** to close the **Definition Name** window and open the **Edit Padstack Definition** window.

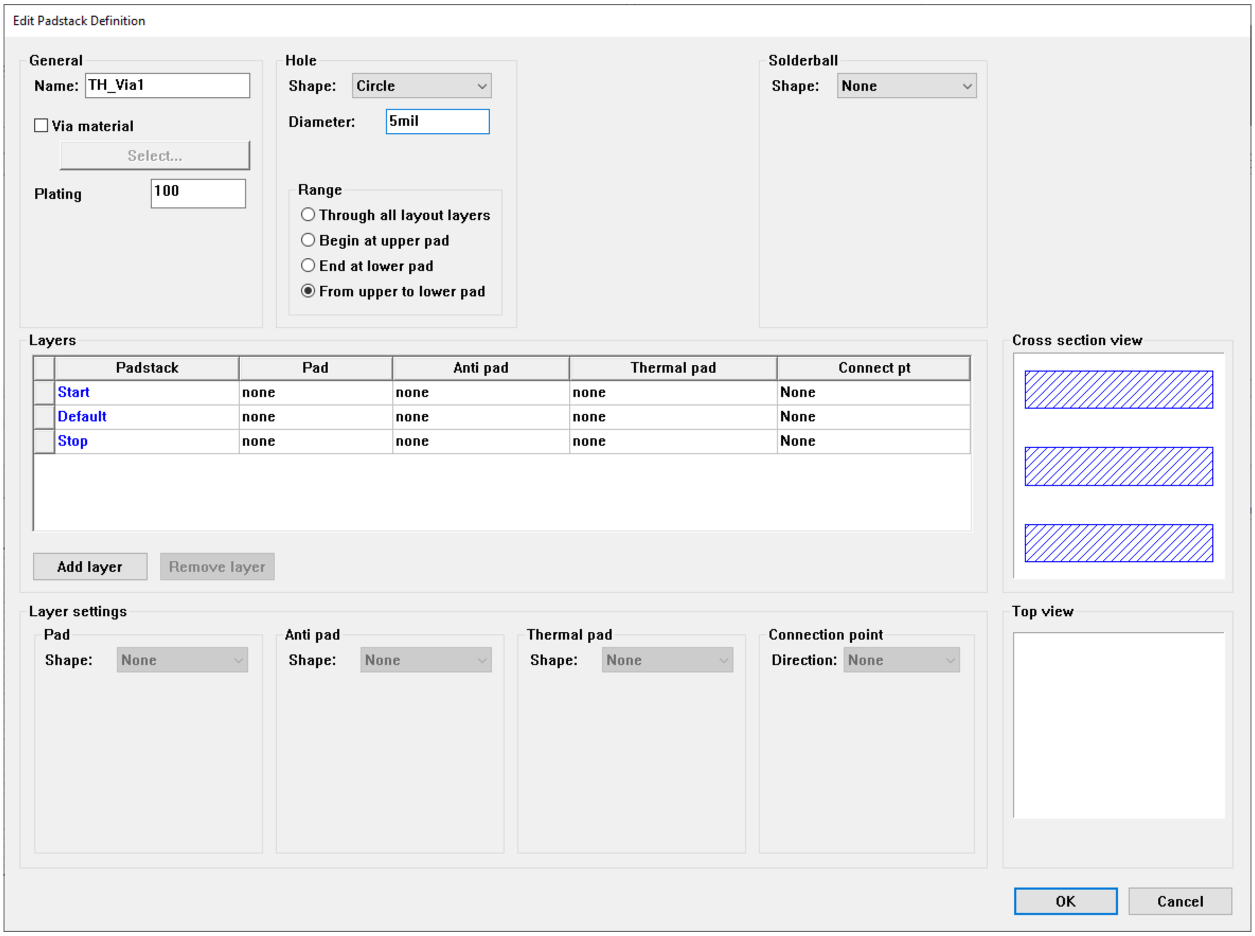


3. From the **Edit Padstack Definition** window, define the via barrel by doing the following:

a. Select **Circle** from the **Shape** drop-down menu.

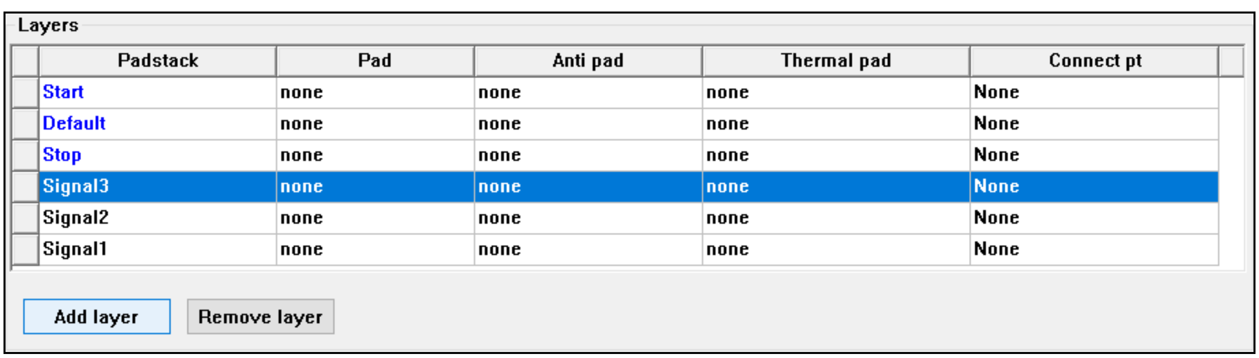


b. Enter **5mil** in the **Diameter** field.

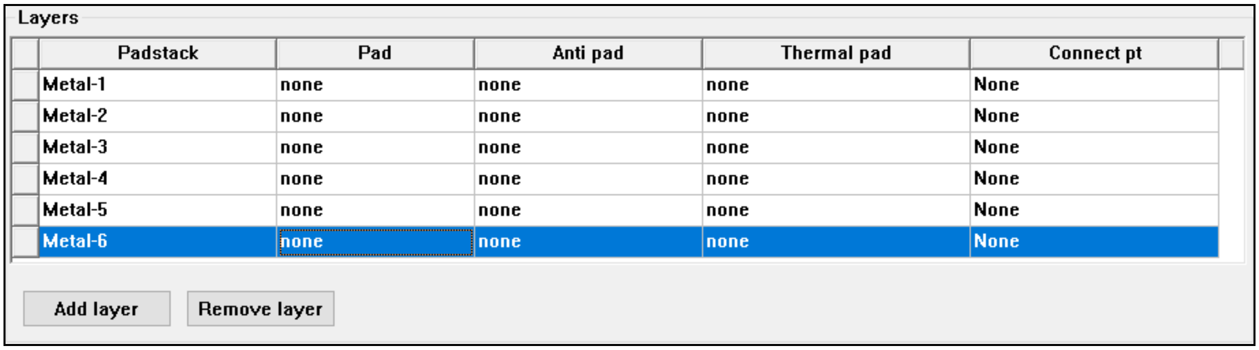


c. From the **Layers** table, create a six-layer through-hole via by doing the following:

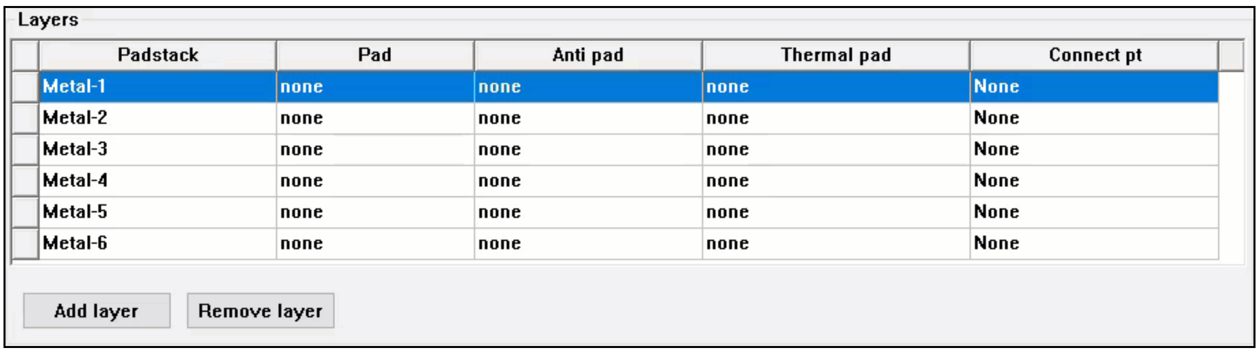
i. Click **Add layer** three times.



ii. Enter new names for each layer in the **Padstack** column. Ensure the new names match the names of the stackup signal layers (i.e., **Metal-1** through **Metal-6**. Refer to Creating a Stackup).

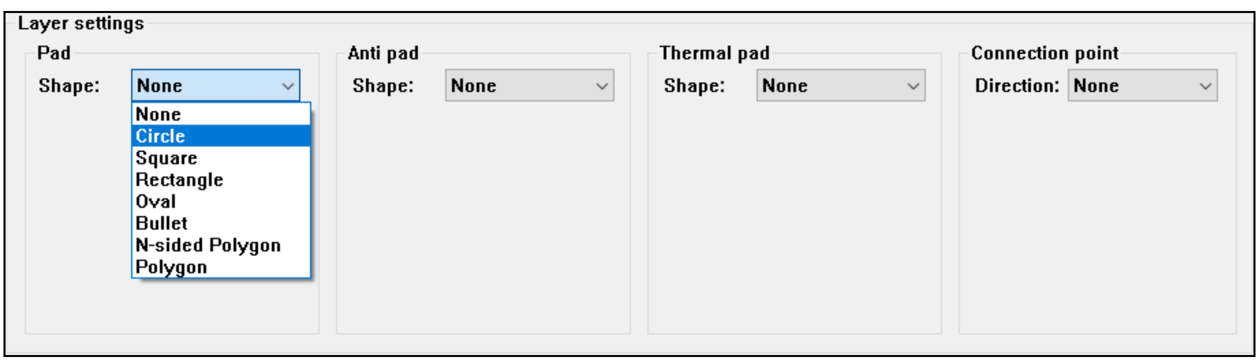


iii. Hold **Shift** and select the empty box adjacent to the first layer (e.g., **Metal-1**). Then click the box adjacent to the sixth layer (e.g., **Metal-6**) to highlight all six layers.

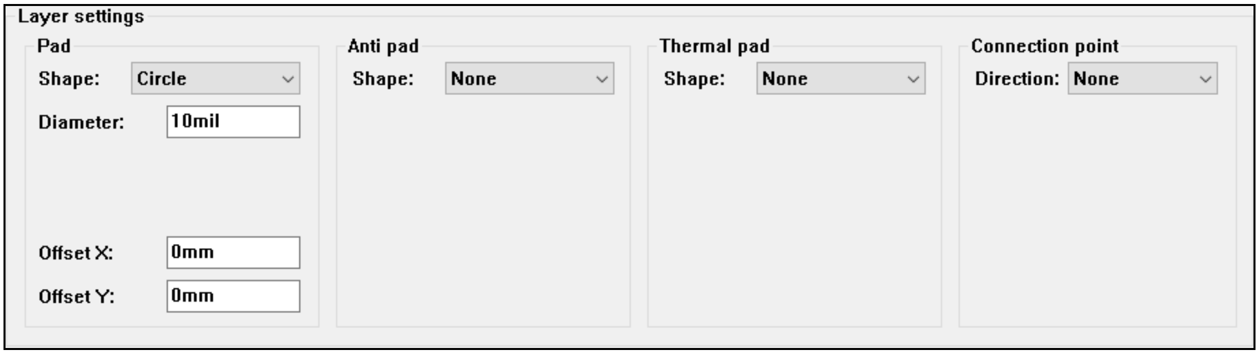


d. From the **Layer settings** > **Pad** area, do the following:

i. Select **Circle** from the **Shape** drop-down menu.

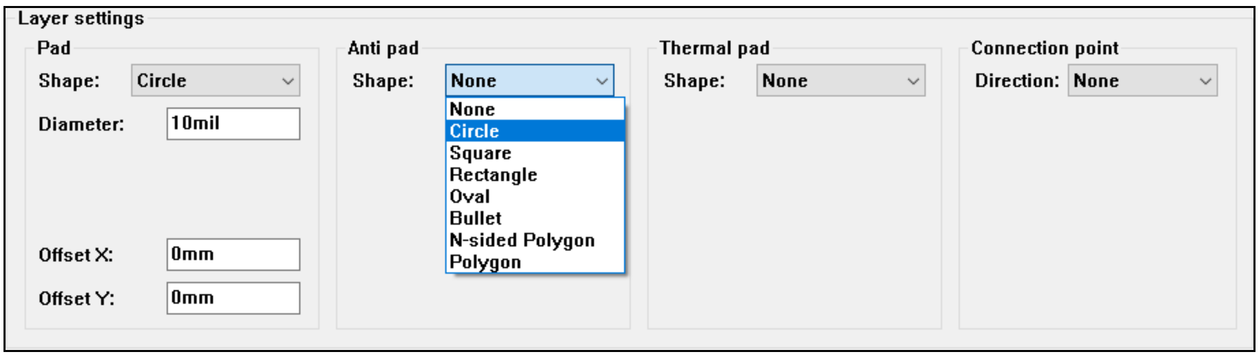


ii. Enter **10mil** in the **Diameter** field.

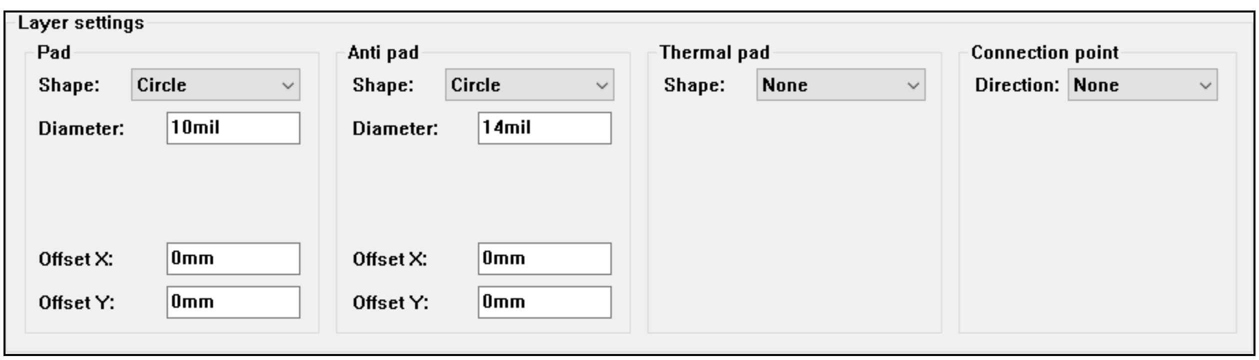


e. From the **Anti pad** area, do the following:

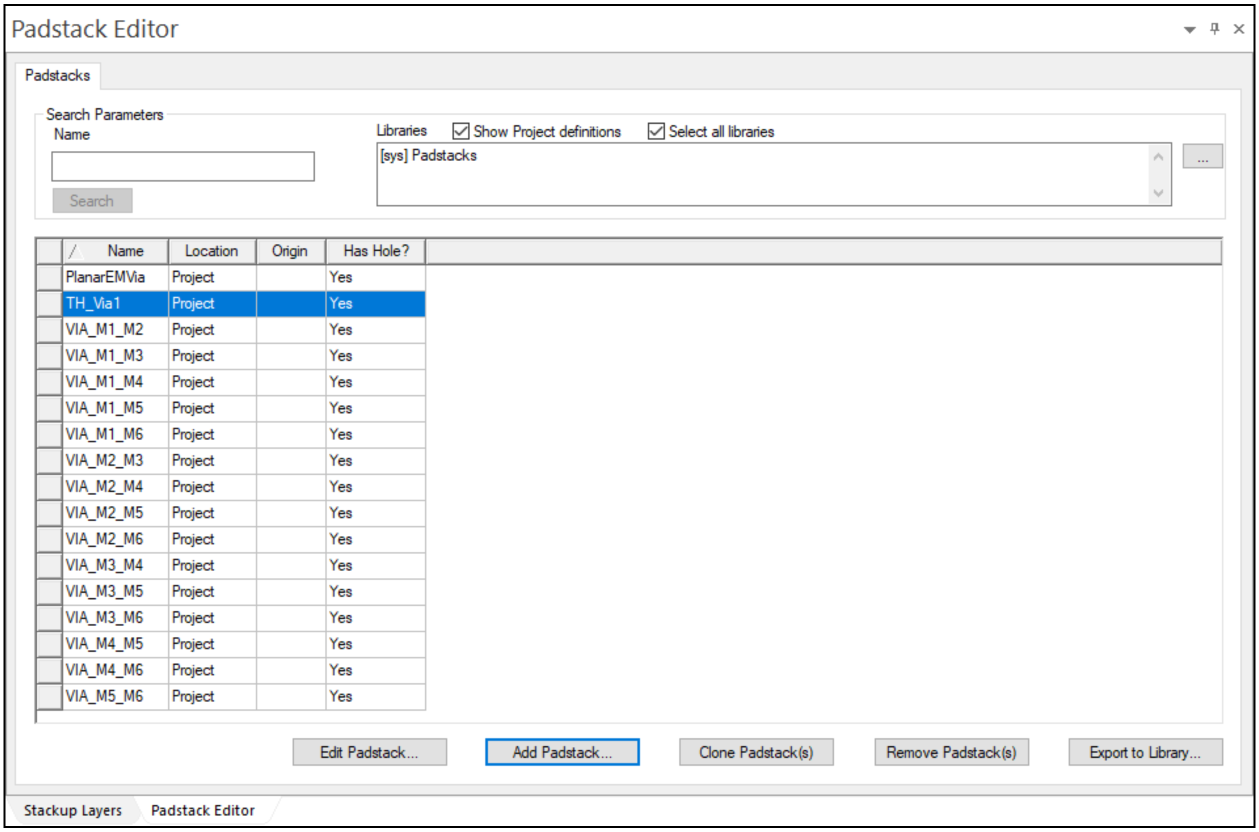
i. Select **Circle** from the **Shape** drop-down menu.



ii. Enter **14mil** in the **Diameter** field.



4. Click **OK** to close the **Edit Padstack Definition** window and add the new padstack to the **Padstack Editor** table.



Continue to Modeling a Transmission Line.

3 - Modeling a Transmission Line

Note:

Complete the Editing the Stackup and Padstacks section before continuing.

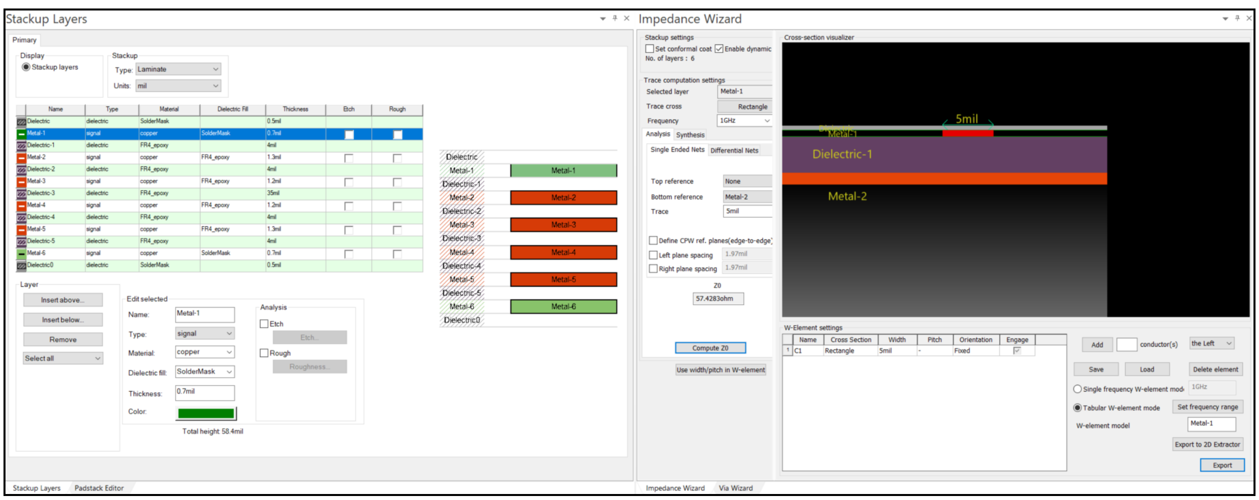
This section explains how to perform the following tasks:

- Define a Transmission Line
- Generate W-element Plots
- Generate Impedance Plots
- Export a W-element Model

Defining a Transmission Line

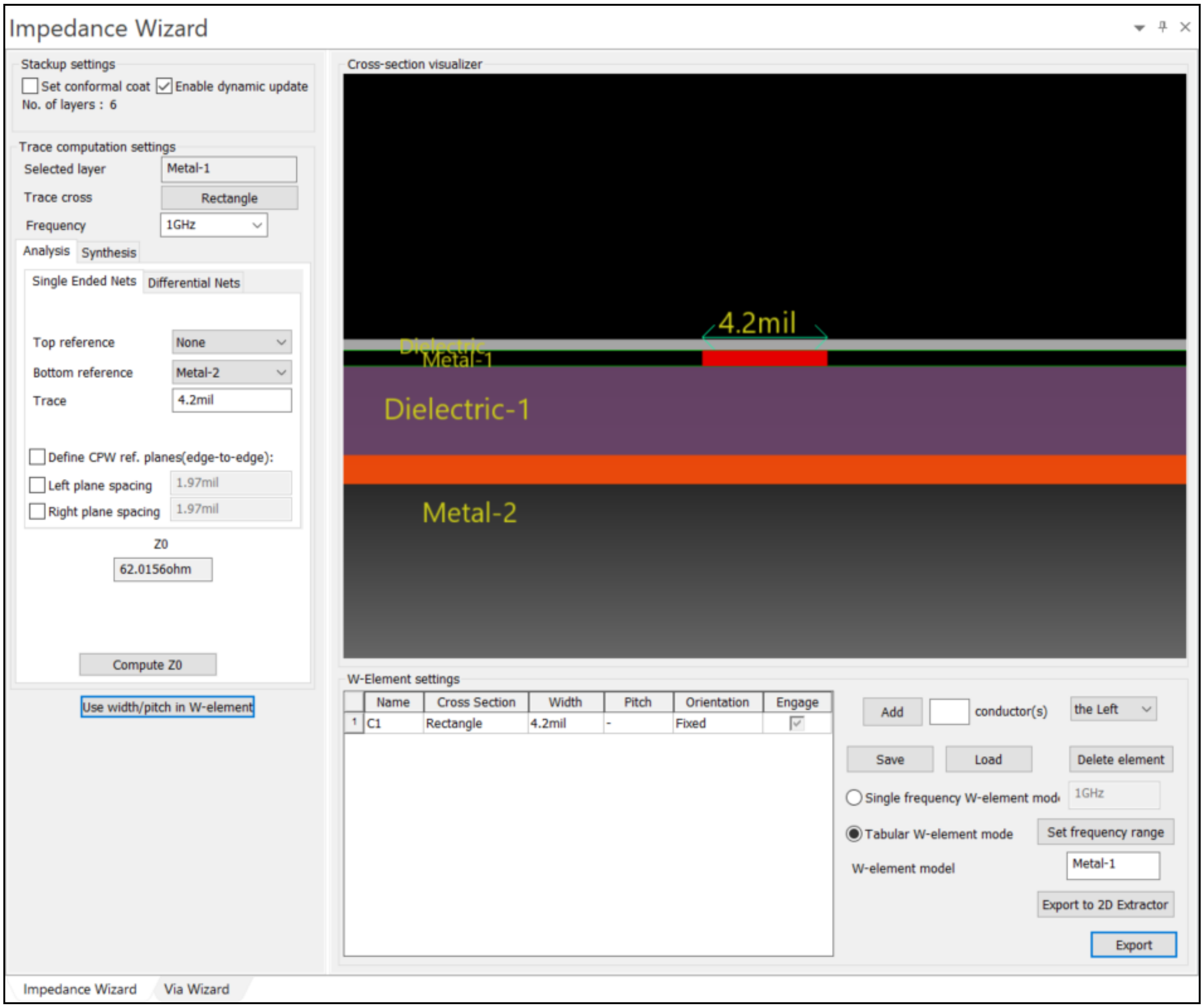
Complete the following steps to define a transmission line.

1. From the **Stackup Layers** window, select the second row in the table (i.e., **Metal-1**) to place a transmission line on **Metal-1**, as shown in the **Impedance Wizard**.



2. From the **Trace computation settings** in the **Impedance Wizard**, do the following:
   a. Ensure **Metal-2** is selected from the **Bottom reference** drop-down menu.
   b. Enter **4.2mil** in the **Trace** width field.
   c. Click **Compute Z0** to display the impedance in the **Z0** field (i.e., **62.0156 ohm**).

3. Click **Use width/pitch in W-element** to refresh the **Cross-section visualizer**.



Note:

From the **Trace computation settings** area, users can perform **Analysis** (i.e., determine impedance based on trace width) or **Synthesis** (i.e., determine trace width for a selected impedance). There are several additional settings that are not used in this Getting Started Guide but are documented in the Help.

Continue to Generating W-element Plots.

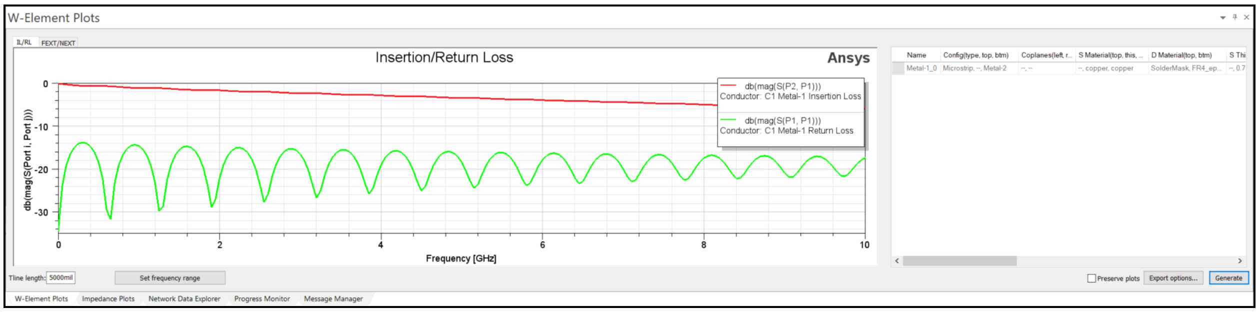
Generating W-Element Plots

Complete the following steps to generate W-element plots.

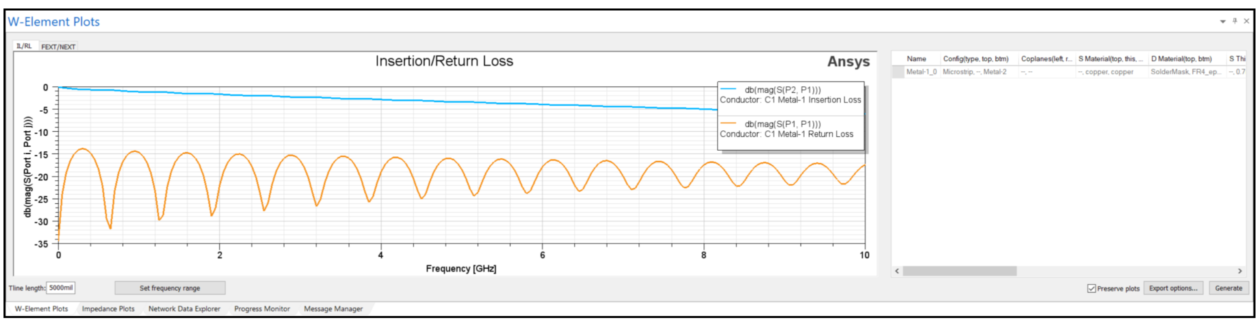
Note:

Resize the **W-Element Plots window** window so the plots are visible. Refer to the [Resizing SI Xplorer subsection in the Introduction](#).

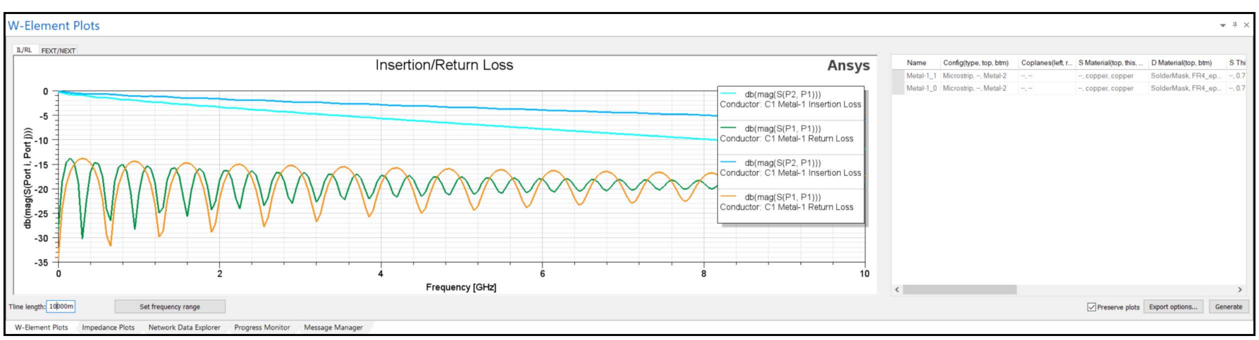
1. Navigate to the **W-Element Plots** window. If appropriate, select the **IL/RL** tab (i.e., Insertion Loss/Return Loss). Then click **Generate** to create an **Insertion/Return Loss** plot.



Check the **Preserve plots** box to save the current **5000mil** plot.



2. Enter **10000mil** in the **Time length** field and the plot will automatically update for 10000 mils.



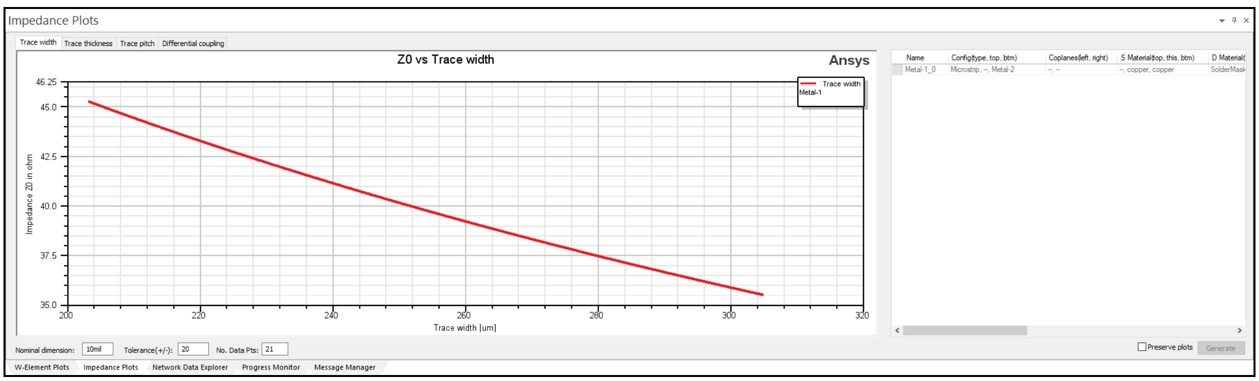
Continue to [Generating Impedance Plots](#).

Generating Impedance Plots

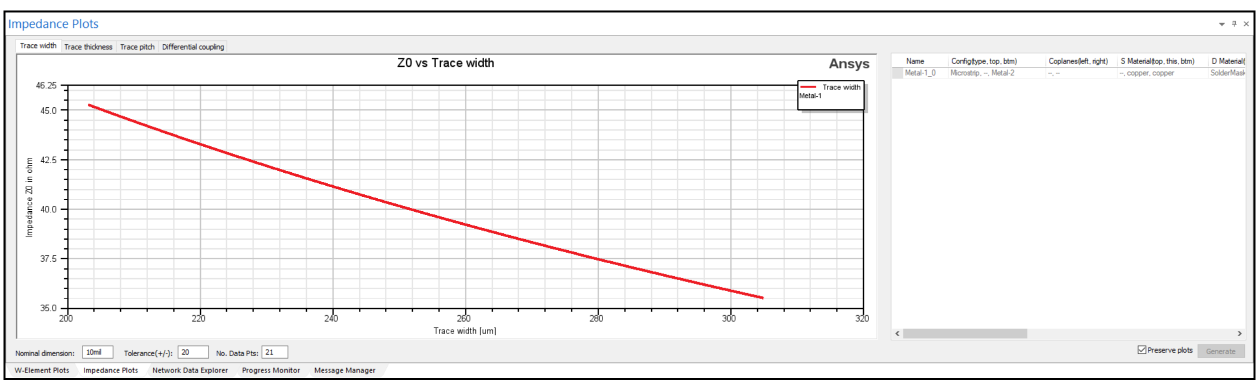
Complete the following steps to generate impedance plots.

1. Click the **Impedance Plots** tab. Then click **Generate** to create a **Z0 vs Trace width** plot (i.e., impedance vs trace width).

> **Note:**
>
> The following **Impedance Plots** are also generated: **Z0 vs Trace thickness** (i.e., impedance vs trace thickness), **Zdiff vs Trace pitch** (i.e., impedance vs trace pitch), and **Zdiff/Z0 vs Dielectric thickness** (i.e., differential coupling). Trace pitch and differential coupling plots are only generated for differential traces.

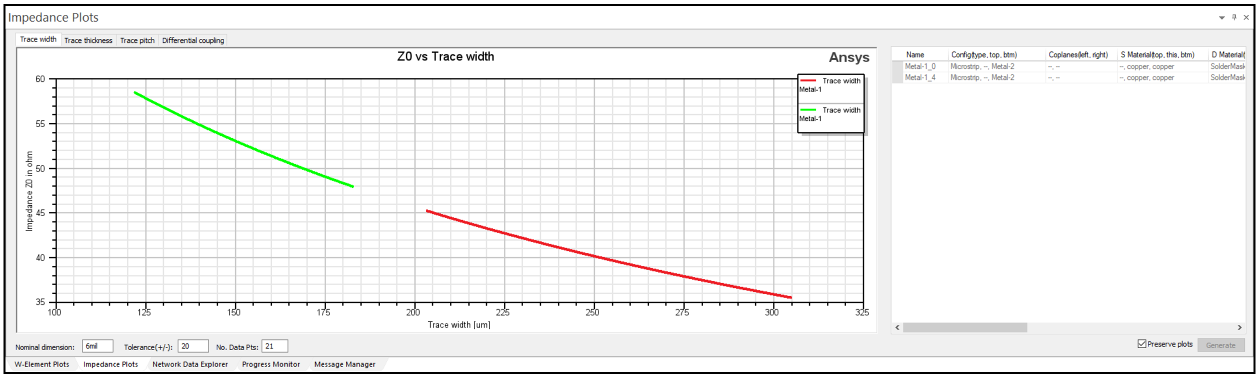


2. Check the **Preserve plots** box to save the current **10mil** plot.



3. Enter **6mil** in the **Nominal dimension** field. Then click **Generate** to see the updated **Z0 vs Trace width** plot. According to the following example, to achieve 50 ohms, approximately

175um (i.e., 6.9mil) trace width is appropriate.

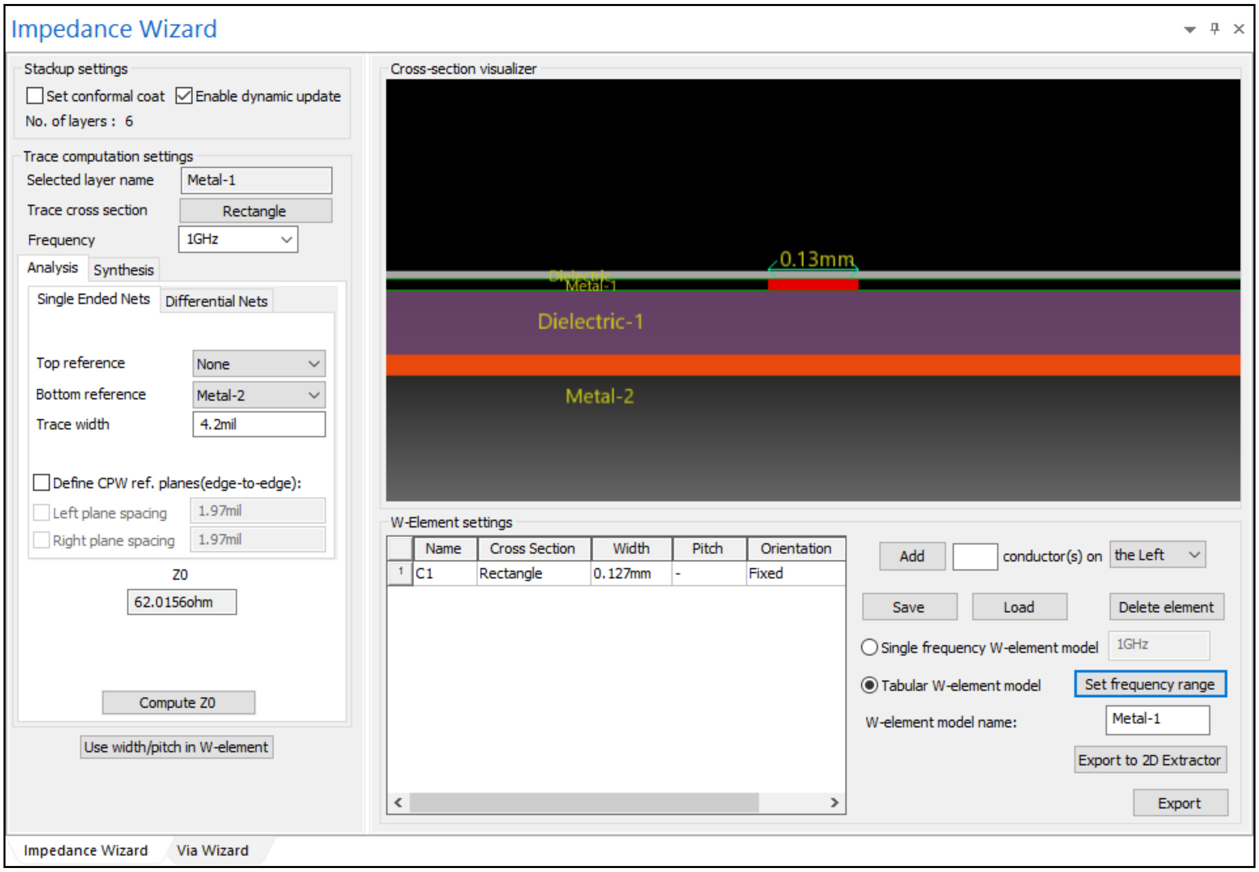


Continue to Exporting a W-element Model.

Exporting a W-Element Model

Complete these steps to export a transmission line W-element model.

1. From the **Impedance Wizard**, click **Set frequency range** to open the **Frequency Setup Dialog** window.

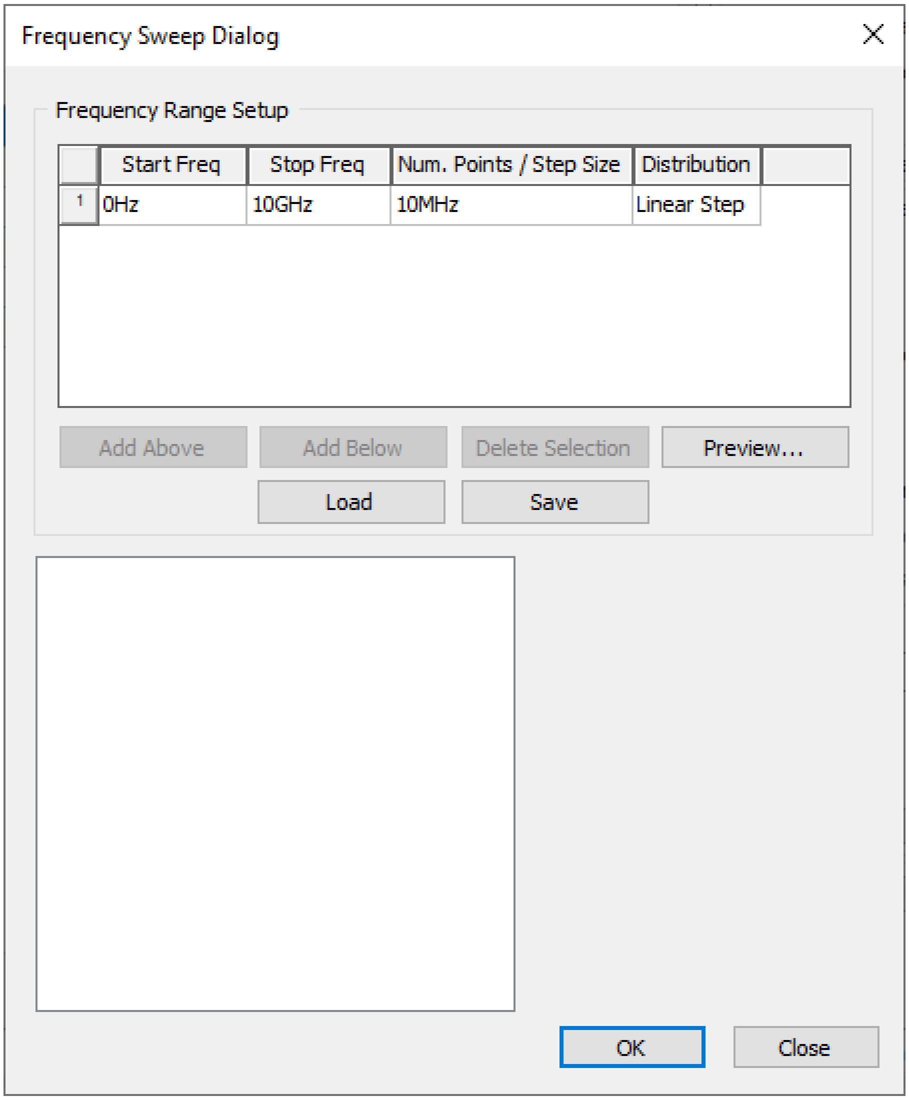


2. From the **Frequency Setup Dialog** window, enter the following parameters in the existing row:

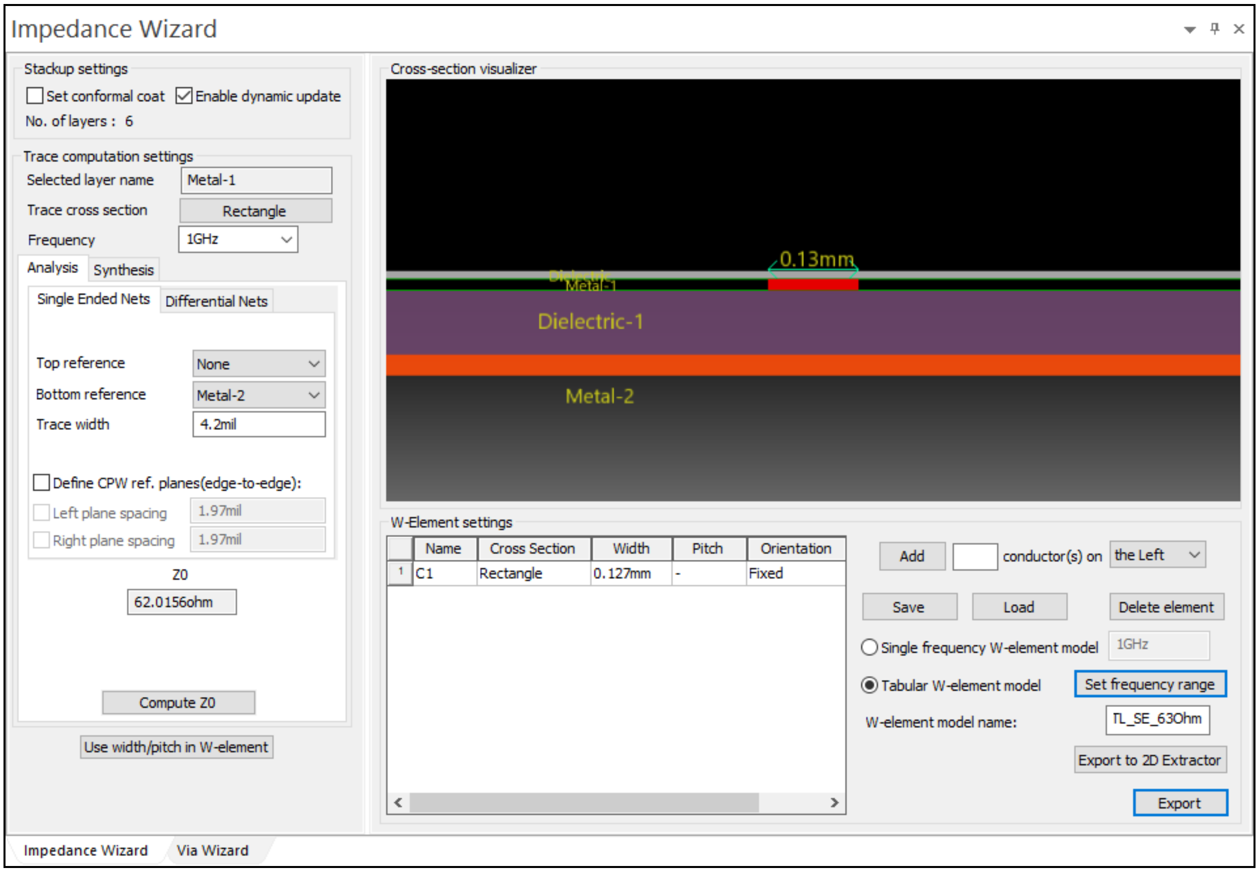
   a. Enter **0Hz** in the **Start Freq** field.

   b. Enter **10GHz** in the **Stop Freq** field.

   c. Enter **10MHz** in the **Num. Points / Step Size** field.



3. Click **OK** to close the **Frequency Setup Dialog** window and save the sweep settings.
4. Enter a new name for the model in the **W-element model name** field (e.g., **TL_SE_ 63Ohm**).

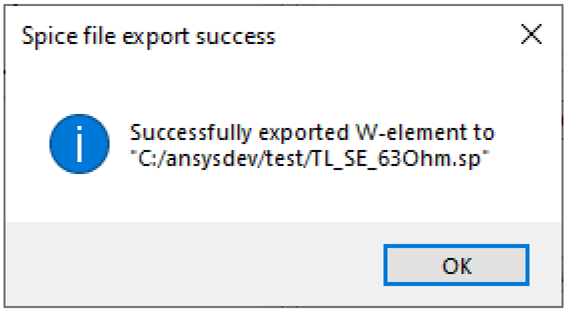


Note:

If more than one W-element model is imported to Circuit, a unique name is required for each model to prevent duplicate SPICE submodel names.

5. Click **Export** to open an explorer window. Then navigate to an appropriate directory and enter a **File name** for the model (e.g., **TL_SE_63Ohm**).
6. Click **Save** to export the W-element model. If the export is successful, the following dialog

box will appear, listing the directory and file name of the new *.*sp* (i.e., Spice) file.



Continue to Modeling a Via.

4 - Modeling a Via

Note:

Complete the Modeling a Transmission Line section before continuing.

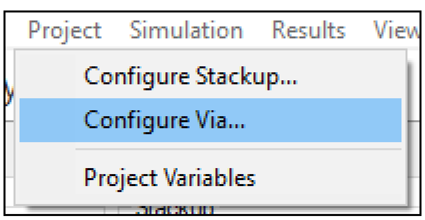
This section explains how to perform the following tasks:

- Add a Via
- Modify Simulation Settings
- Analyze a Via
- View Analysis Results
- Export Via S-Parameters

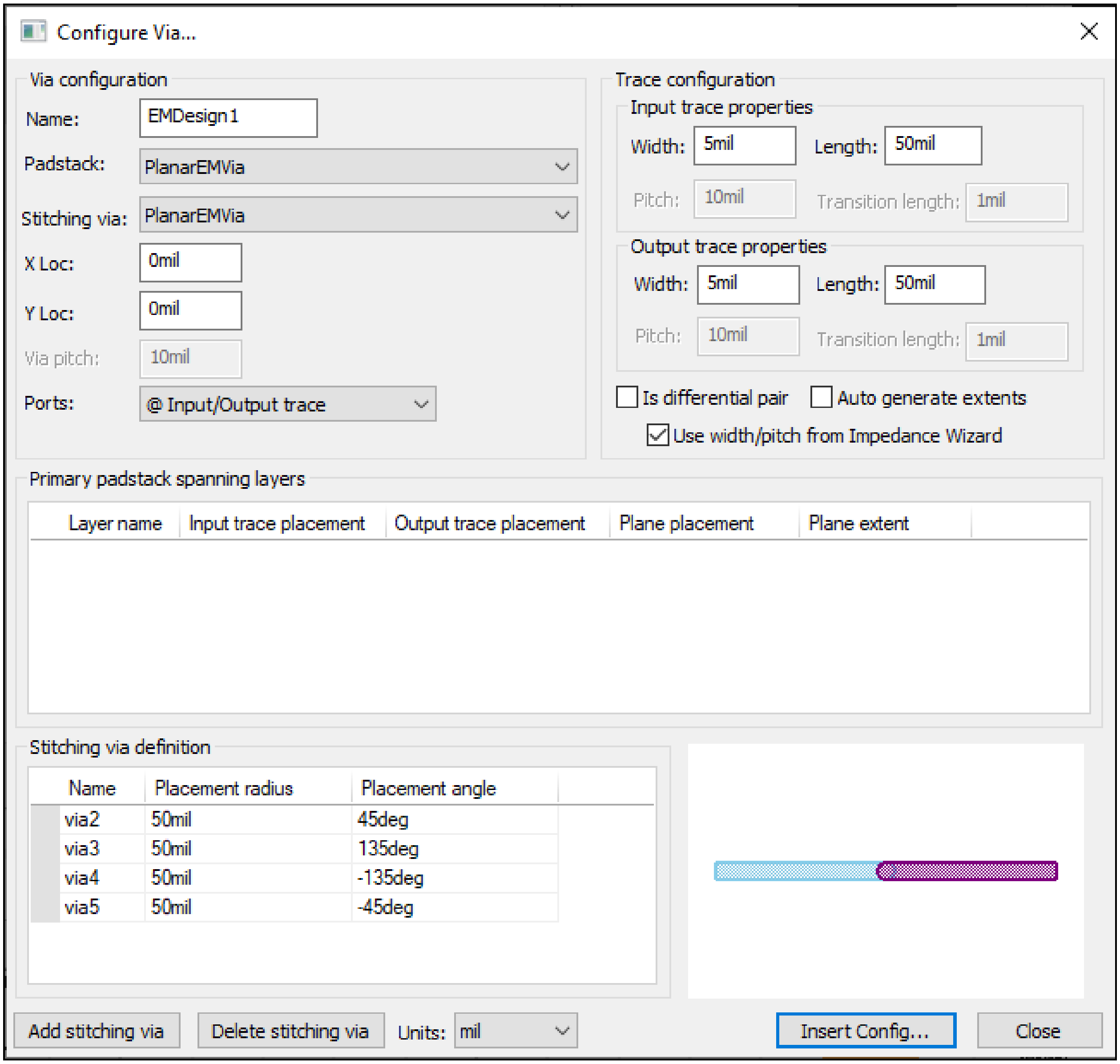
Adding a Via

Complete these steps to add a through-hole via to the design.

1. From **Project**, select **Configure Via**.

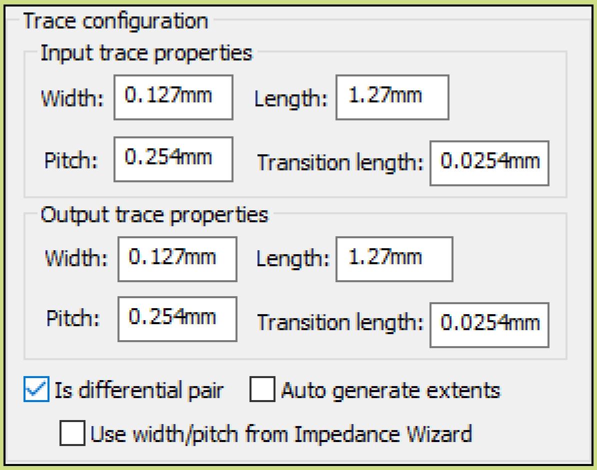


The **Configure Via** window opens.



2. From the **Configure Via** window, enter the following parameters:
   a. From the **Via configuration** area, select **TH_Via1** from the **Padstack** drop-down menu.
   b. Select **VIA_M2_M5** from the **Stitching via** drop-down menu (i.e., starting from layer **Metal-2**, stopping at layer **Metal-5**).
   c. From the **Trace configuration** area, enter **6.9mil** into both **Width** fields (i.e., **Input trace properties** and **Output trace properties**).
   d. Ensure **50mil** is entered in both **Length** fields.

e. Remove the check from the **Use width/pitch from Impedance Wizard** box.

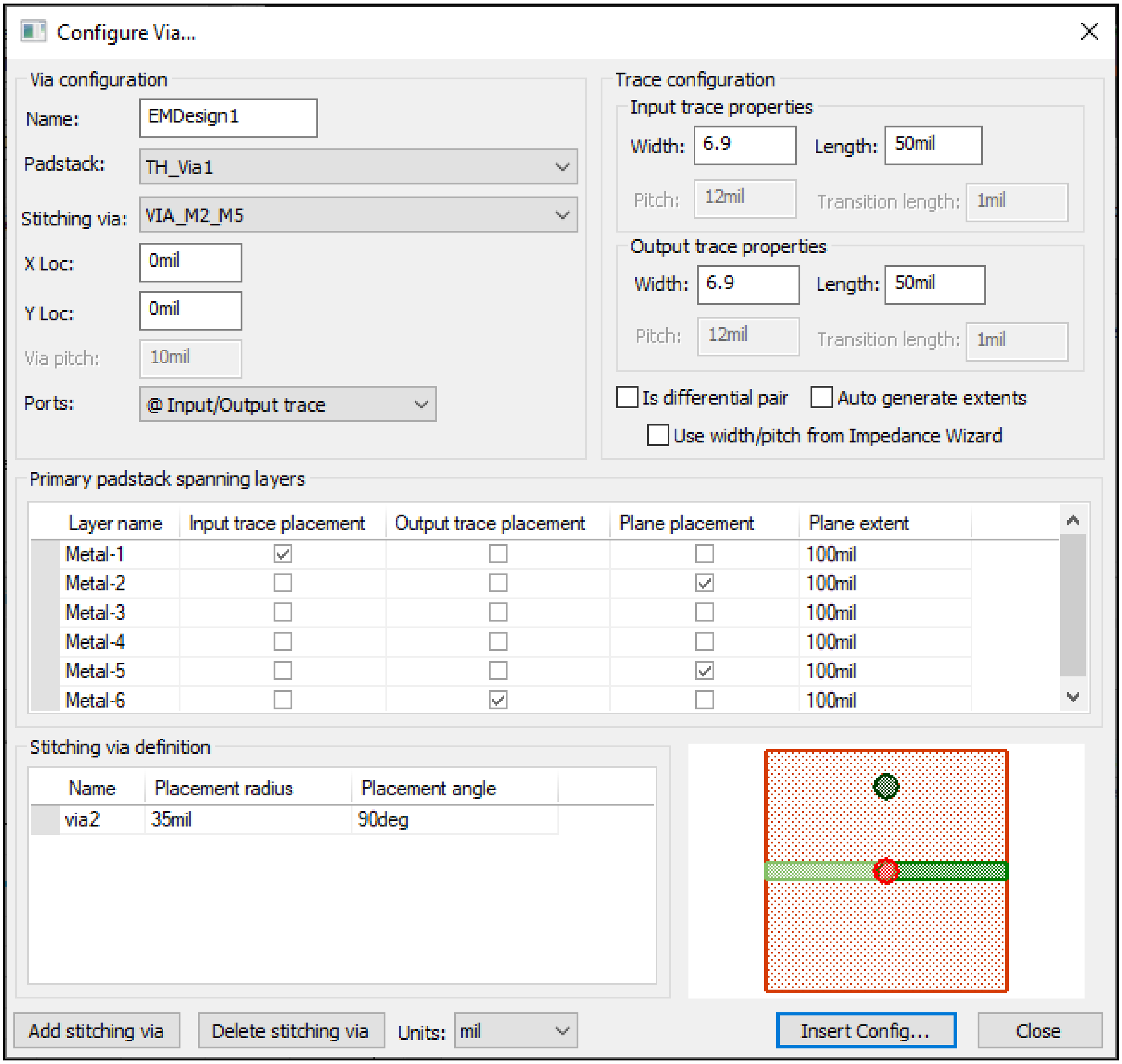
> **Note:**
>
> Define a differential via by checking the **Is differential pair** box.
>
> 
>

f. From the **Primary padstack spanning layers** area, remove the checks from the **Plane placement** column boxes in the **Metal-3** and **Metal-4**. There are no planes on the **Metal-3** and **Metal-4** layers.

g. From the **Stitching via definition** area, delete all but one stitching via (i.e., **via2**) by highlighting one or more stitching via rows and click **Delete stitching via**.

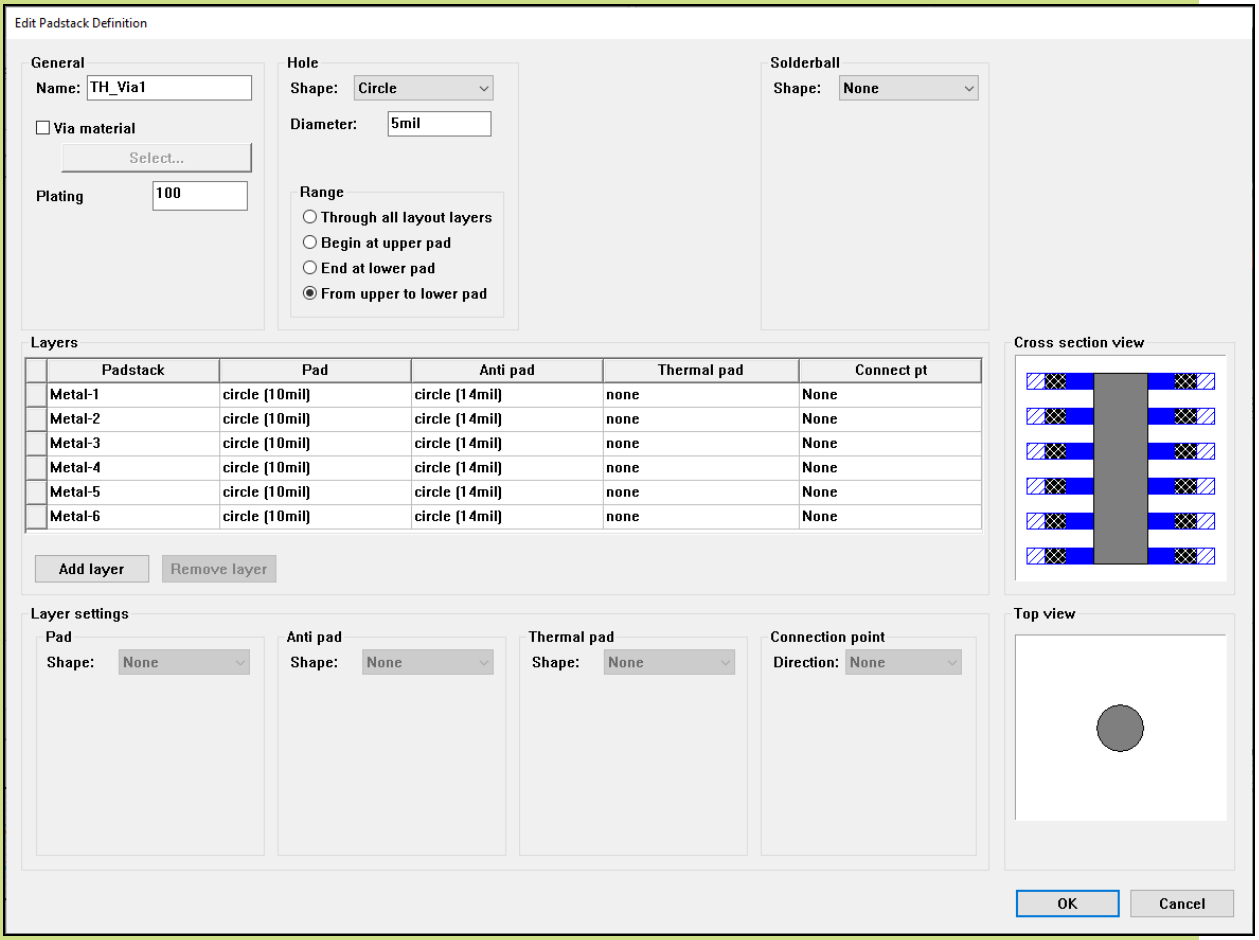
h. From the **via2** row, enter **35mil** in the **Placement radius** column and **90deg** in the **Placement angle** column.

i. Select **Insert Config** to close the **Configure Via** window and create the instance.


Configure Via...
Via configuration
Name: EMDesign1
Padstack: TH_Via1
Stitching via: VIA_M2_M5
X Loc: 0mil
Y Loc: 0mil
Via pitch: 10mil
Ports: @ Input/Output trace
Trace configuration
Input trace properties
Width: 6.9 Length: 50mil
Pitch: 12mil Transition length: 1mil
Output trace properties
Width: 6.9 Length: 50mil
Pitch: 12mil Transition length: 1mil
Is differential pair
Auto generate extents
Use width/pitch from Impedance Wizard
Primary padstack spanning layers
Layer name | Input trace placement | Output trace placement | Plane placement | Plane extent
Metal-1 100mil
Metal-2 100mil
Metal-3 100mil
Metal-4 100mil
Metal-5 100mil
Metal-6 100mil
Stitching via definition
Name | Placement radius | Placement angle
via2 35mil 90deg
Add stitching via
Delete stitching via
Units: mil
Insert Config...
Close

Note:

Via dimensions (e.g., barrel, pad, anti-pad size, et cetera) can be viewed and/or modified from the **Padstack Editor** window (i.e., click the **Padstack Editor** tab).



Continue to Modifying Simulation Settings.

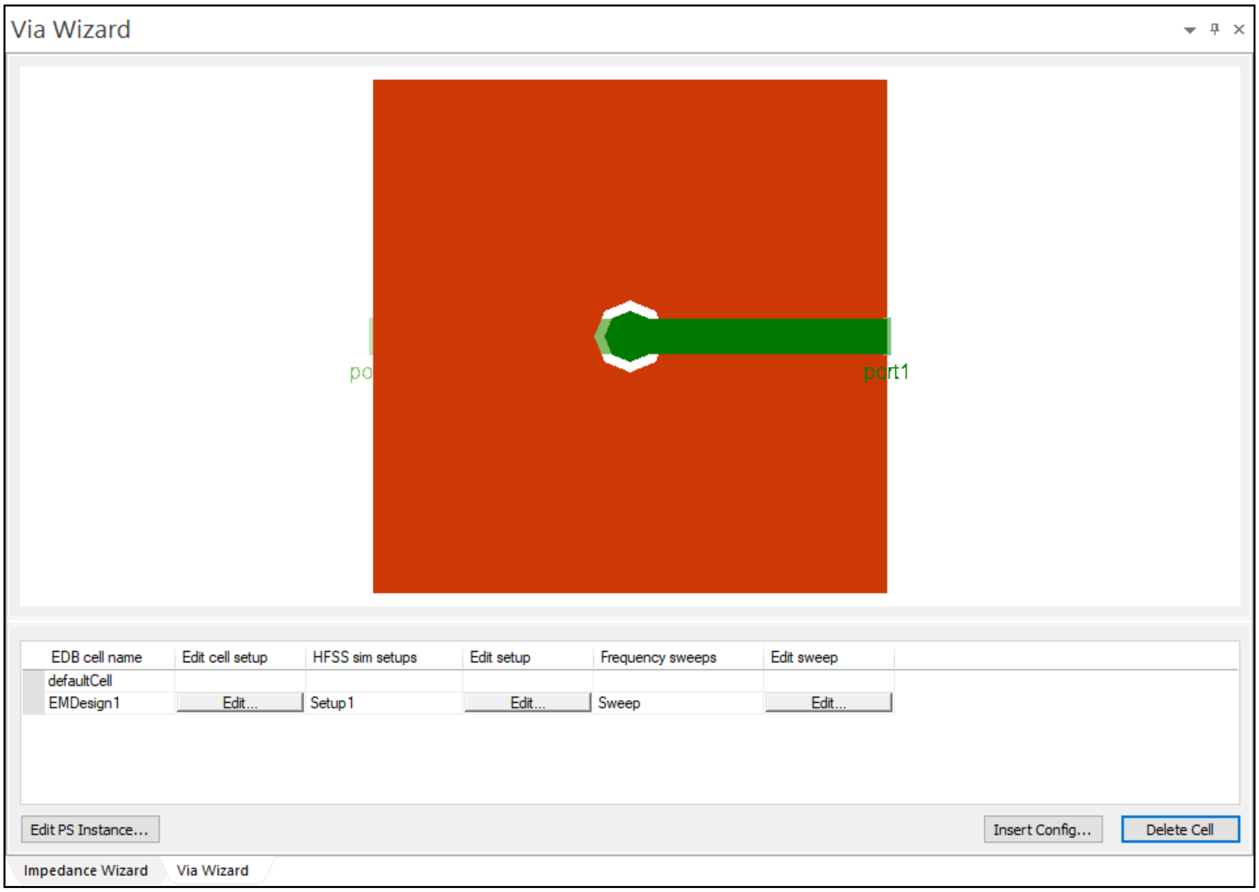
Modifying Simulation Settings

Complete these steps to configure an HFSS simulation and modify the default frequency sweep parameters.

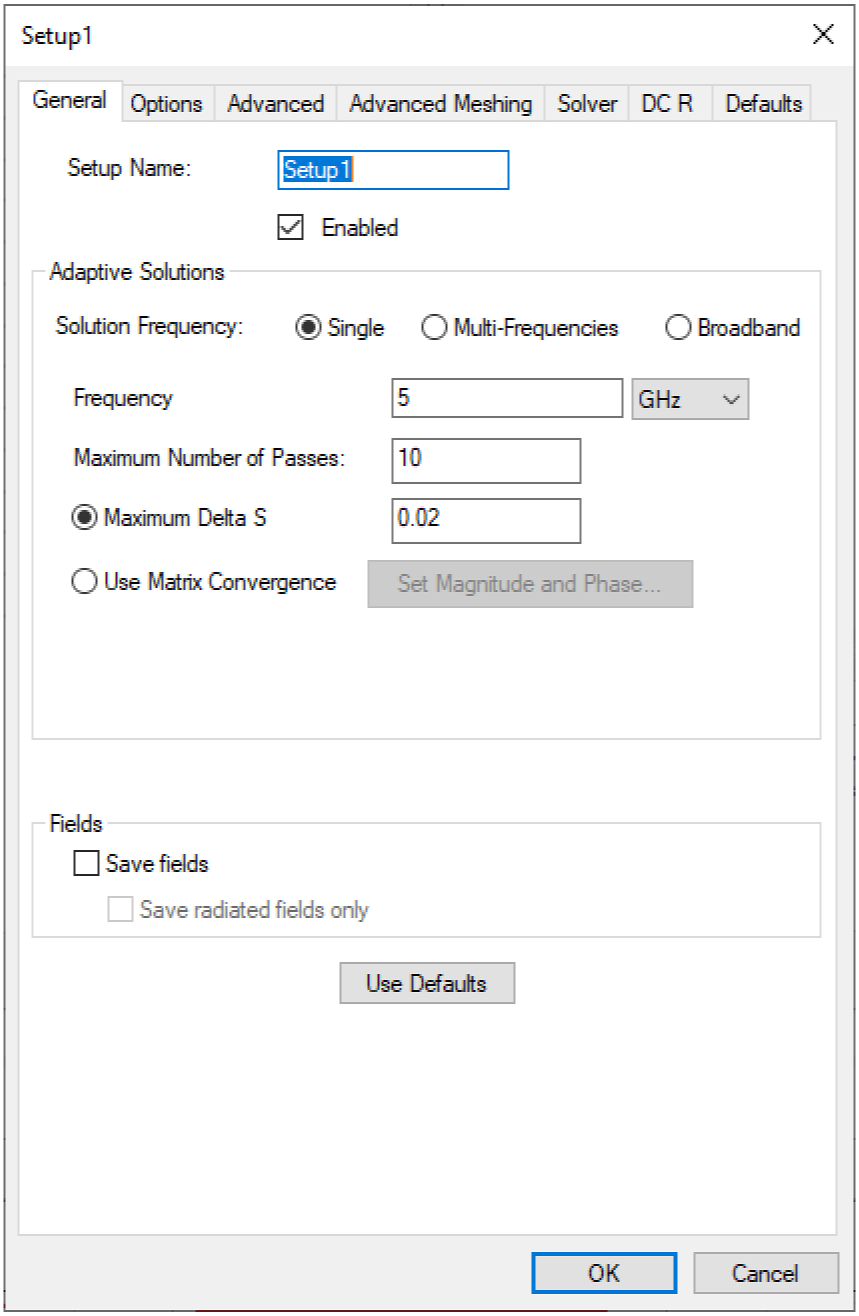
Note:

For a complete guide to HFSS simulation settings and frequency sweep setup, refer to the Help.

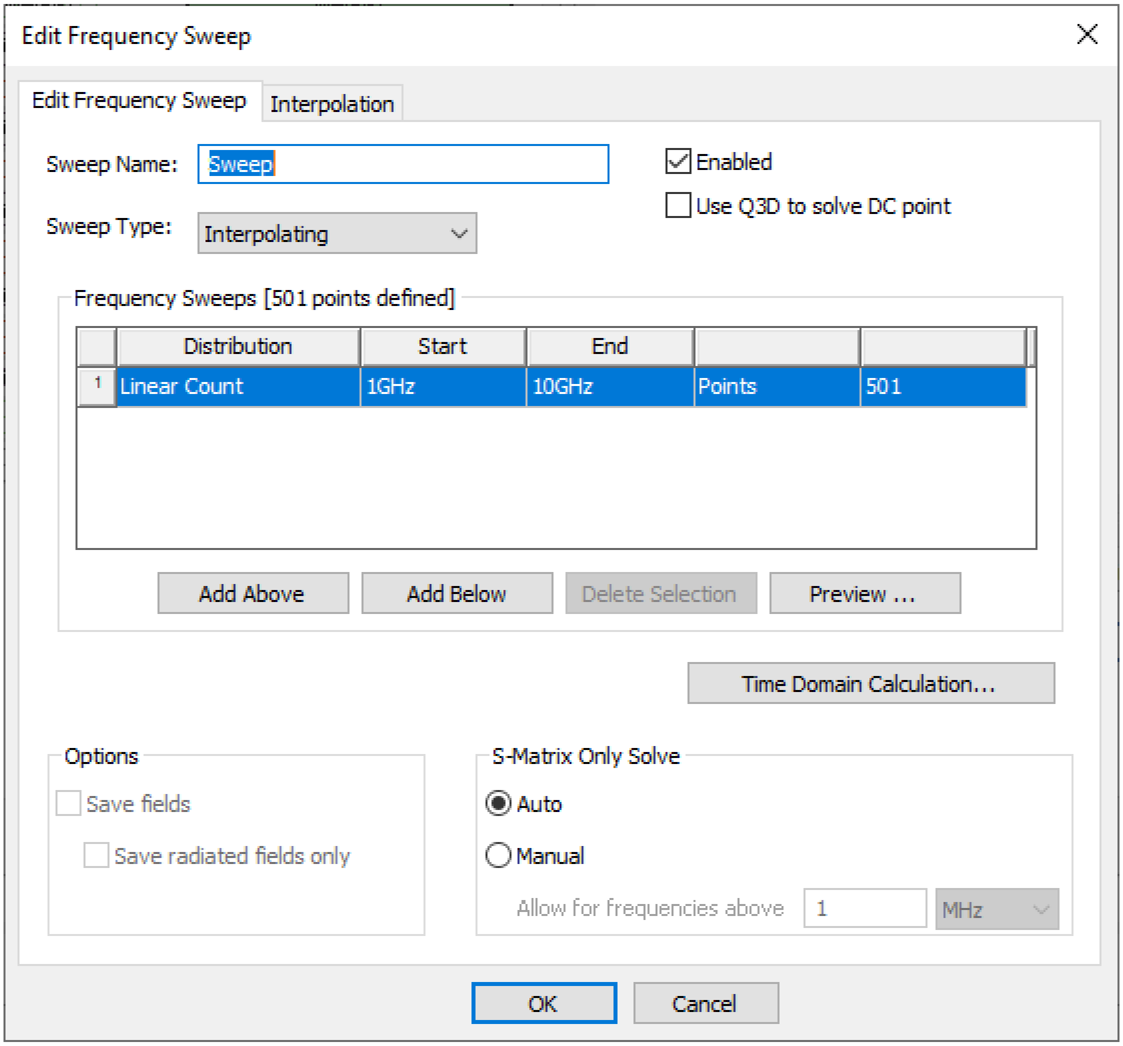
1. Click the **Via Wizard** tab to see a visualization of the newly configured via (Refer to Adding a Via).



2. From the **Edit setup** column, click **Edit** to open the HFSS simulation **Setup** window.



3. Ensure **5 GHz** is entered in the **Frequency** field.
4. Click **OK** to close the **Setup** window.
5. From the **Edit** sweep column, click **Edit** to open the **Edit Frequency Sweep** window.



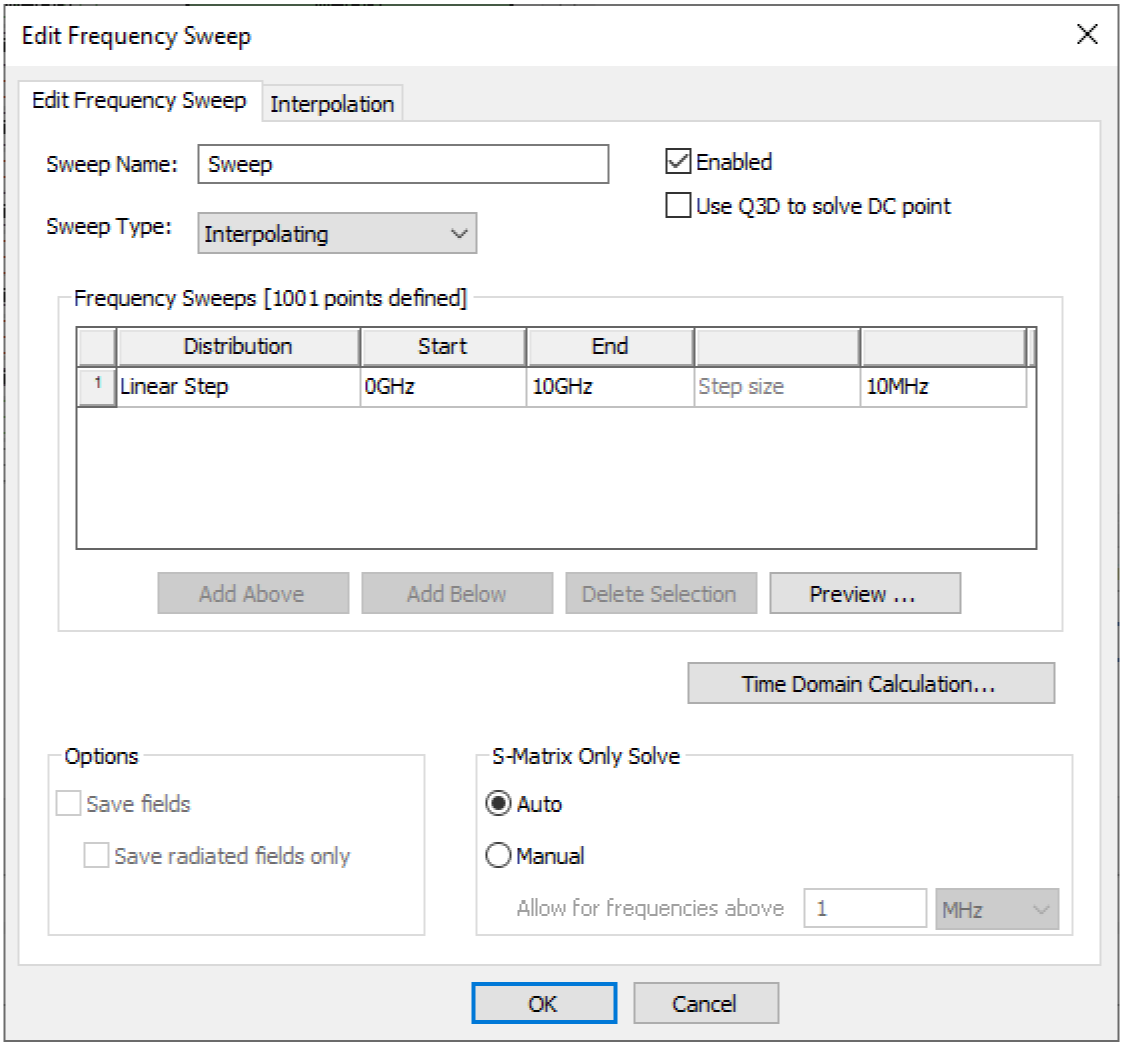
6. From the **Edit Frequency Sweep** window, do the following:

   a. Select **Linear Step** from the **Distribution** column drop-down menu.

   b. Enter **0GHz** in the Start field.

   c. Enter **10GHz** in the Stop field

   d. Enter **10MHz** in the **Step size** field.



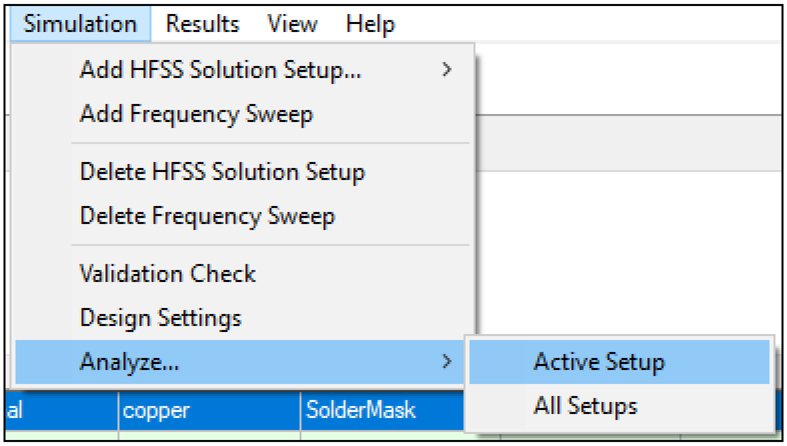
7. Click **OK** to save the modified S-parameter frequency sweep.

Continue to Analyzing a Via.

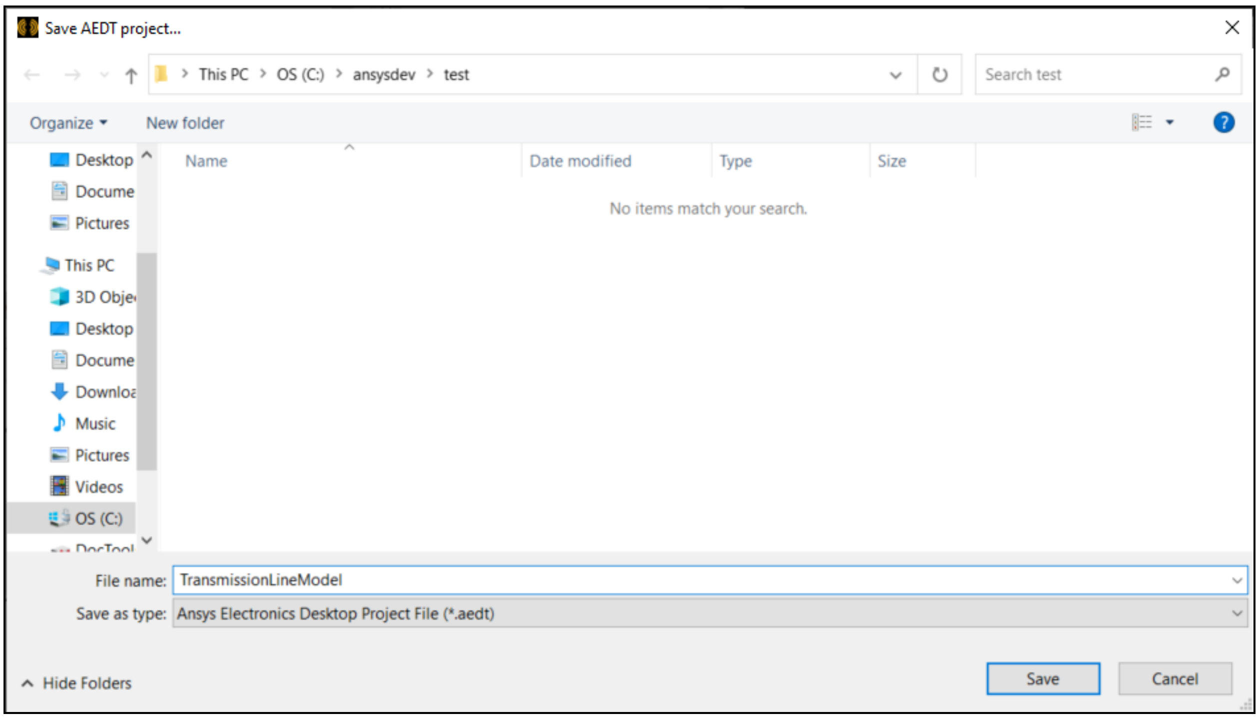
Analyzing a Via

Complete these steps after adding a simulation to a via to run the simulation and analyze the results.

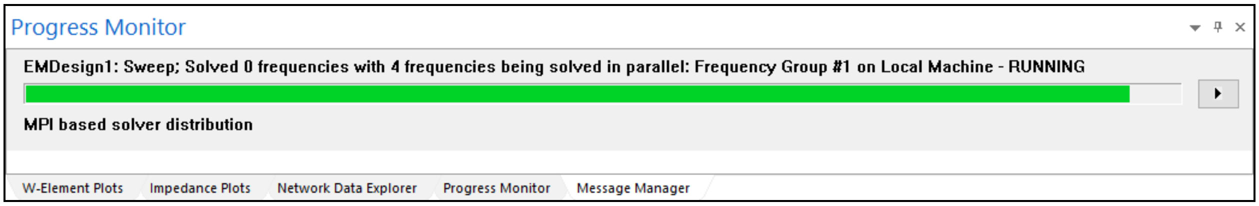
1. From **Simulation**, select **Analyze** > **Active Setup** to begin analysis.



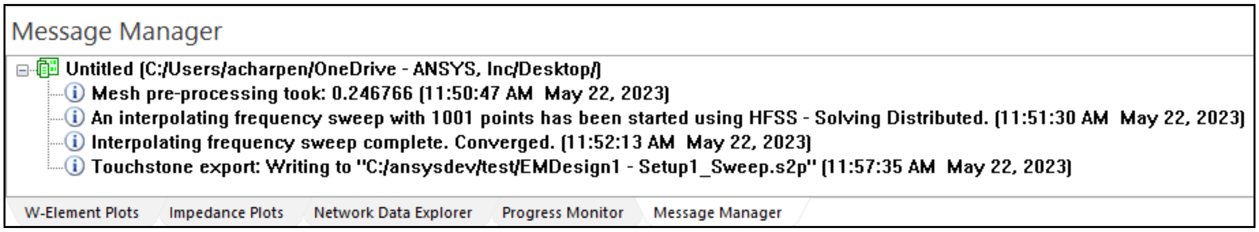
2. If the project has not already been saved, an explorer window will open prompting users to do so. Navigate to an appropriate directory and enter a **File name** for the model (e.g., **TransmissionLineModel**).



3. Click **Save** to close the explorer window and save the project.
4. Click the **Progress Monitor** tab to view the ongoing status of the analysis.

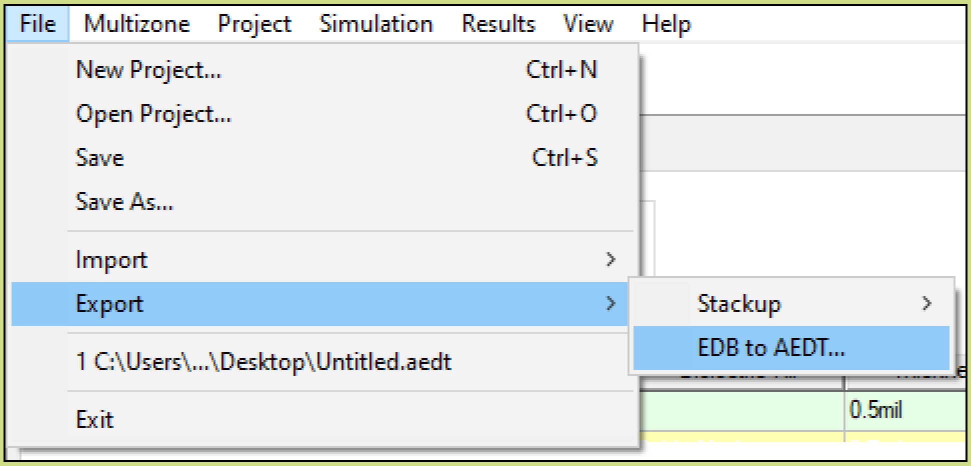


5. Click the **Message Manager** tab to view the detailed status of the analysis.

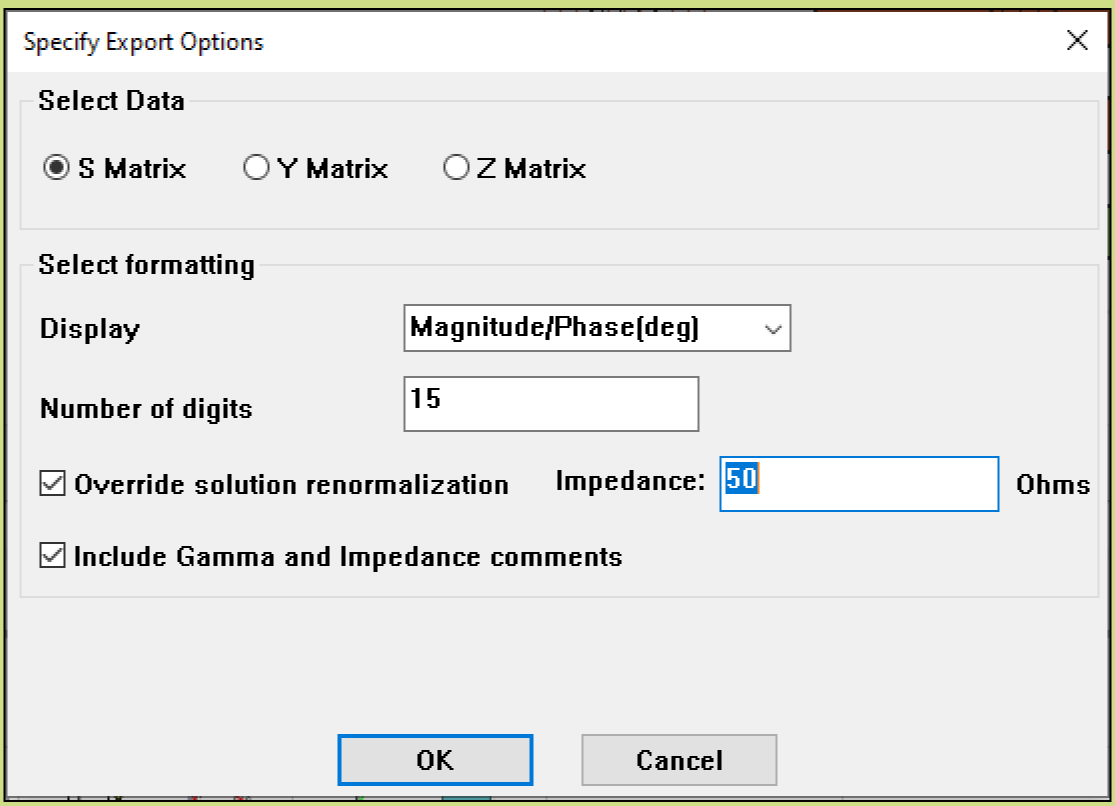


Note:

The via can also be exported to **HFSS 3D Layout**. From **File**, select **Export** > **EDB to AEDT** to open the **Specify Export Options** window.



Make any appropriate changes, then click **OK**.



Electronics Desktop will start. The via will be present in the active design.

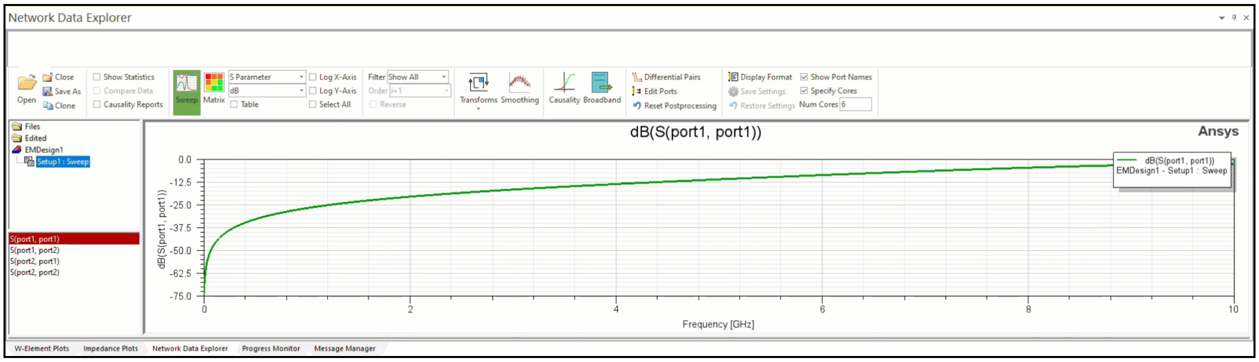
Continue to Viewing Analysis Results.

Viewing Analysis Results

To view insertion loss plots after via analysis, click the **Network Data Explorer** tab. From the project manager on the left-hand side of the **Network Data Explorer** window, click between the available plots in the list (i.e., **S(port1, port1)**, **S(port1, port2)**, **S(port2, port1)**, and **S(port2, port2)**.

Note:

Resize the **Network Data Explorer** window so the project manager list and associated plots are visible. Refer to the Resizing SI Xplorer subsection in the Introduction.

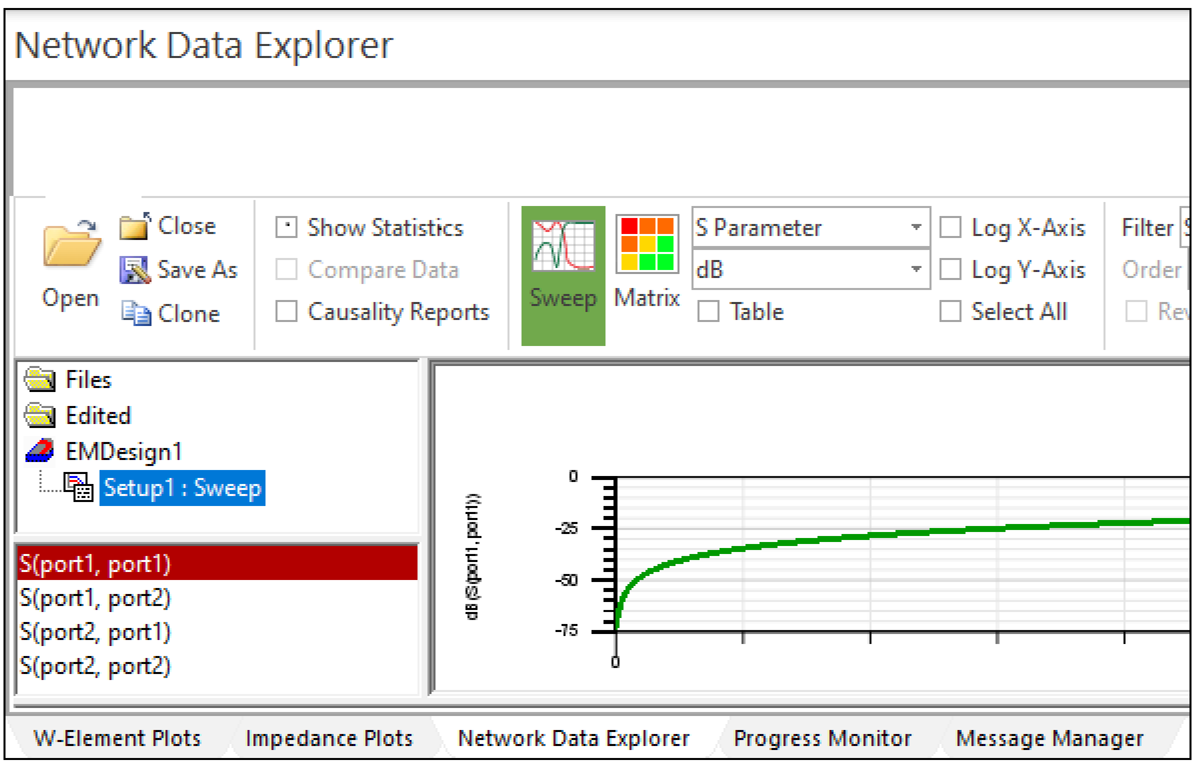


Continue to [Exporting Via S-Parameters](#).

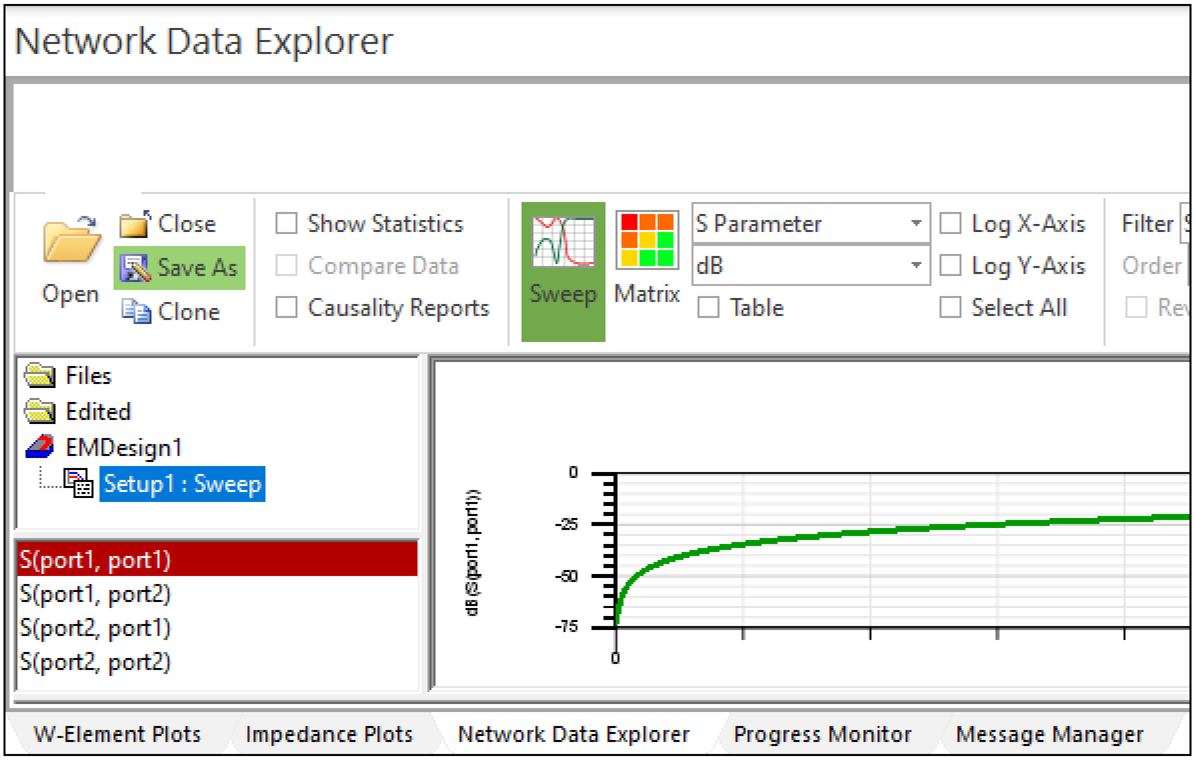
Exporting Via S-Parameters

Complete the following steps to save and export the via S-parameters.

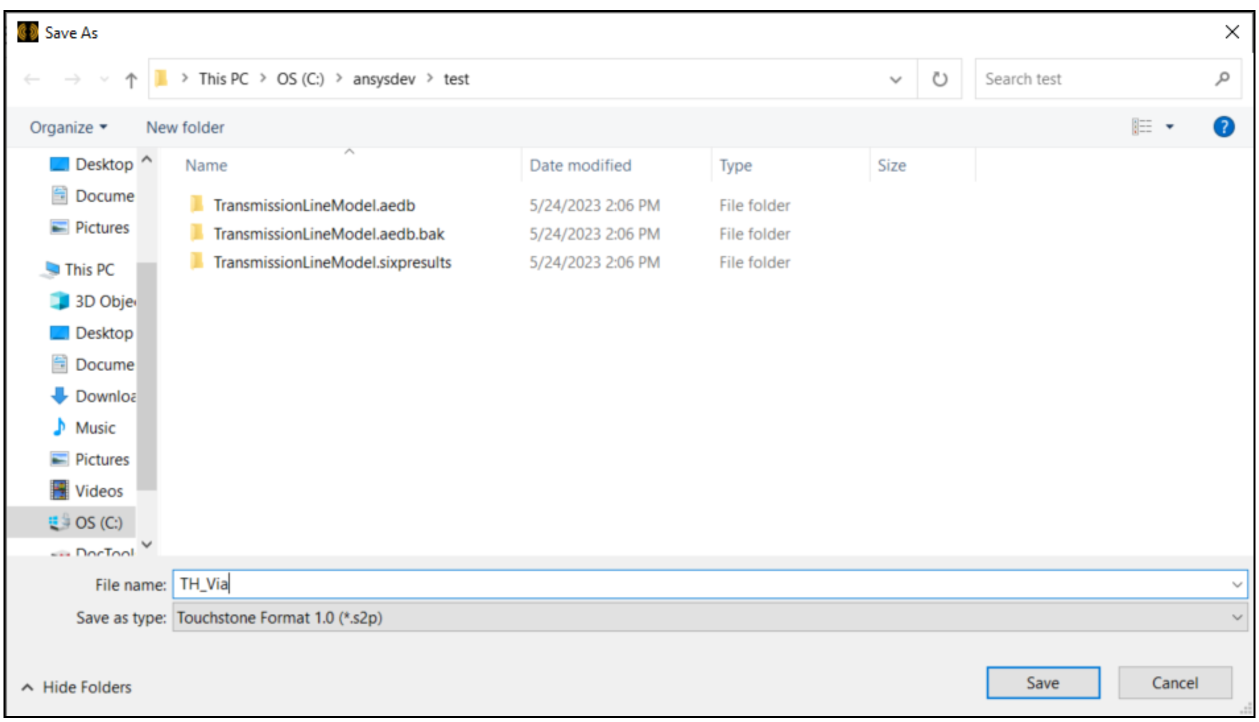
1. Click the **Network Data Explorer** tab.



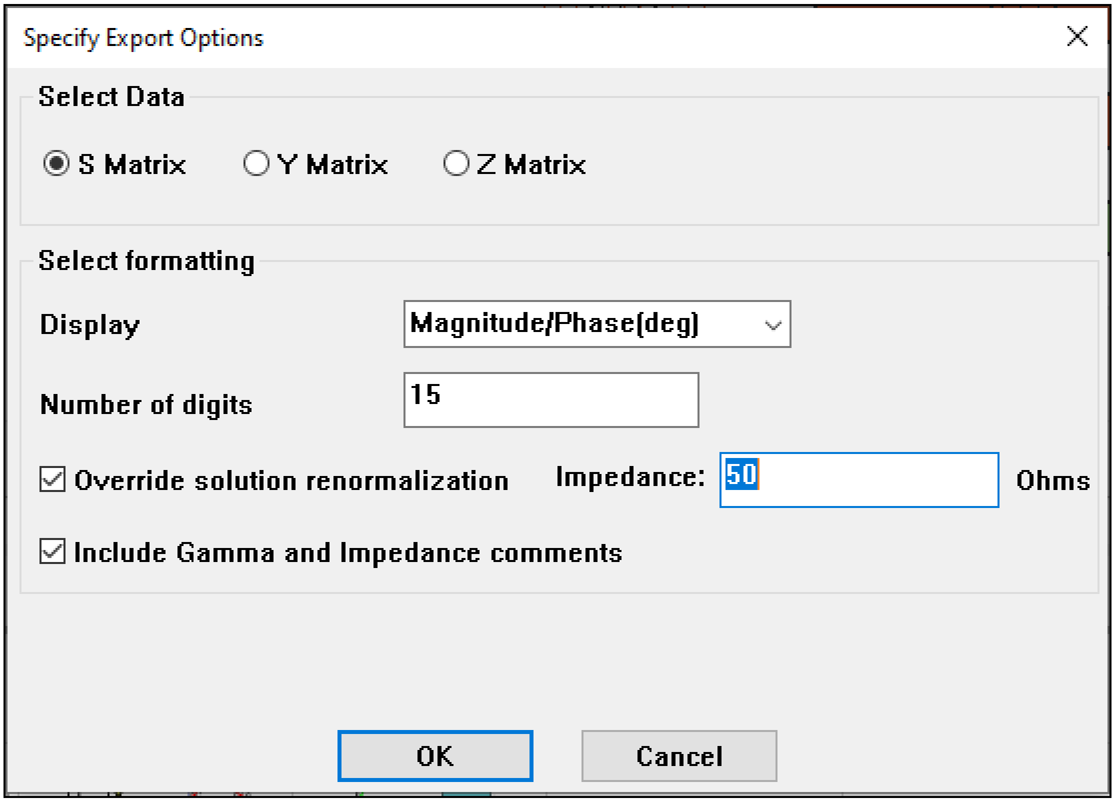
2. Click **Save As** to open an explorer window.



3. Navigate to an appropriate directory and enter a **File name** for the model (e.g., **TH_ Via.s2p**).



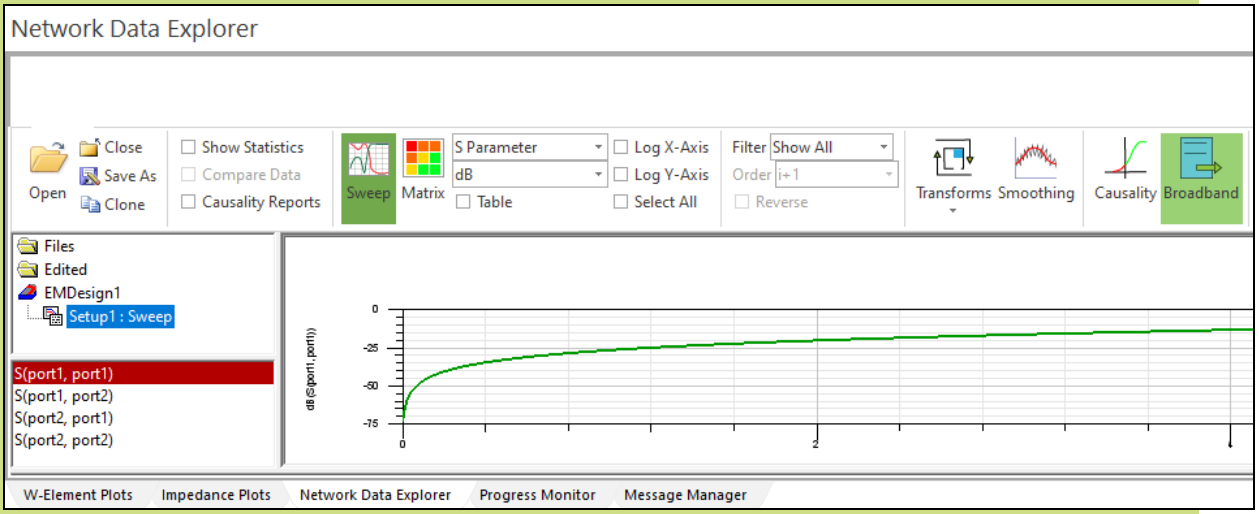
4. Click **Save** to open the **Specify Export Options** window.



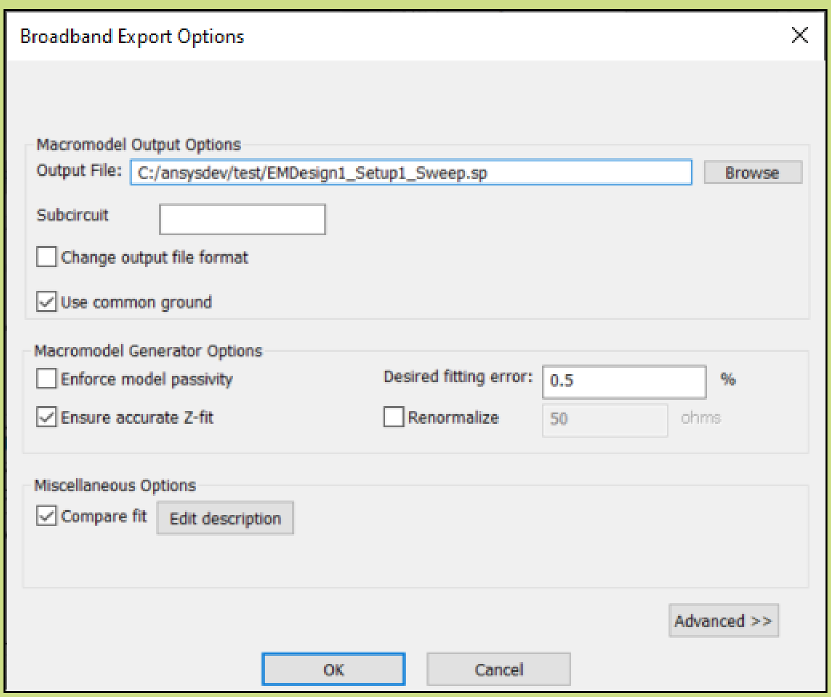
5. Make any appropriate changes, then click **OK**.

Note:

Broadband SPICE models can also be exported from the **Network Data Explorer** tab. Click **Broadband** to open the **Broadband Export Options** window.



Make any appropriate changes, then click **OK**.



Continue to Analyzing a Channel With Transmission Lines and Vias.

5 - Analyzing a Channel With Transmission Lines and Vias

Note:

Complete the Modeling a Via section before continuing.

This section explains how to perform the following tasks:

- Export an Additional Transmission Line Model
- Import Transmission Line Models into Circuit
- Import a Via into Circuit
- Edit the Circuit
- Complete a Circuit Design
- Set Up and Analyze a Linear Network Analysis
- Plotting Insertion Loss and Return Loss
- Comparing Post-Layout Results

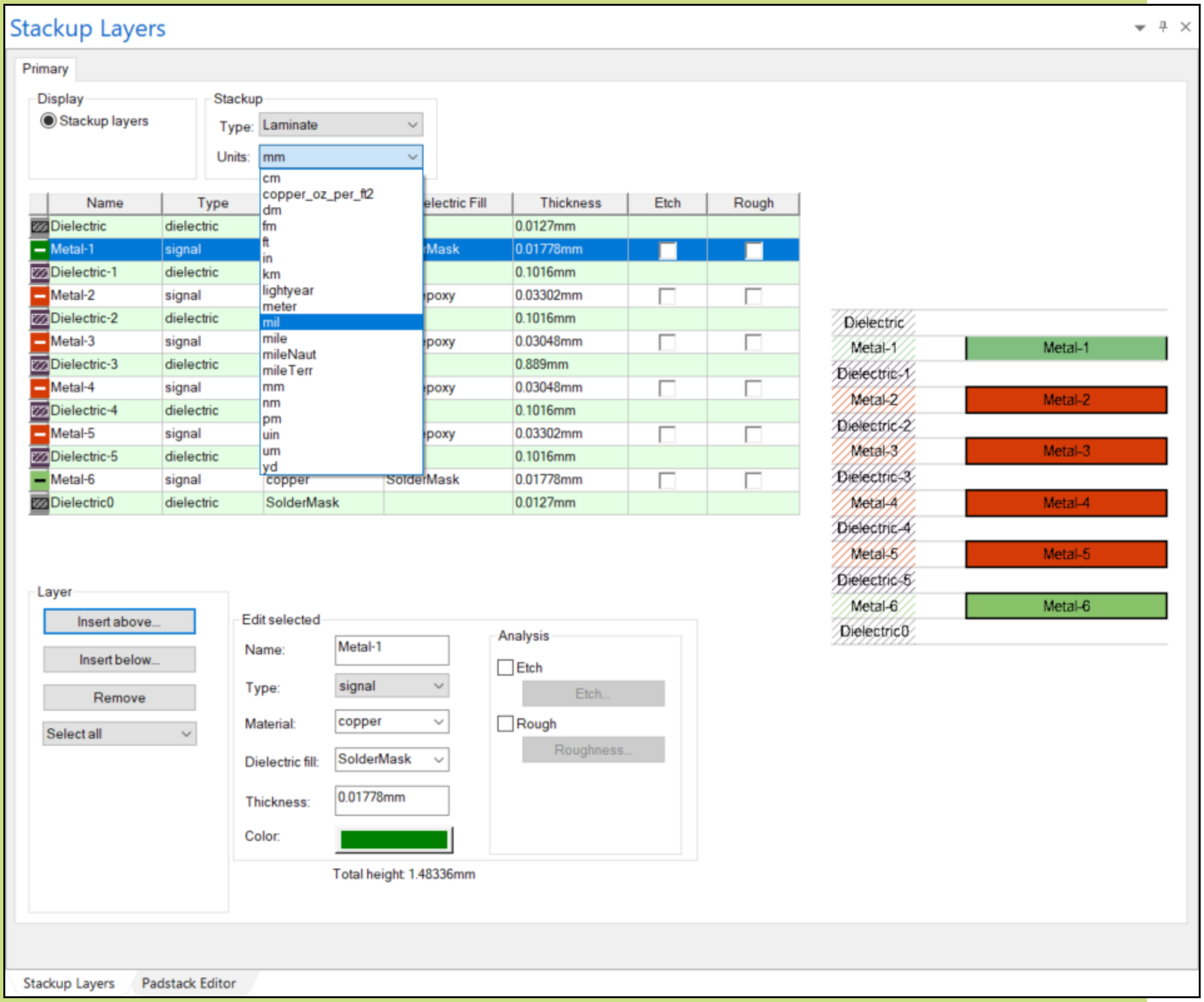
Exporting an Additional Transmission Line Model

Complete these steps to export an additional transmission line W-element model.

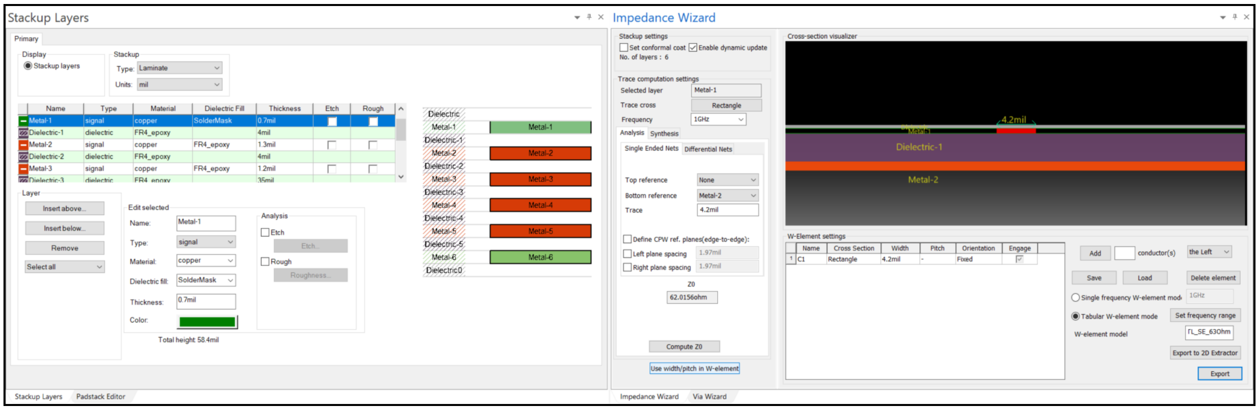
1. Ensure the **Stackup Layers** and **Impedance Wizard** tabs are selected.

Note:

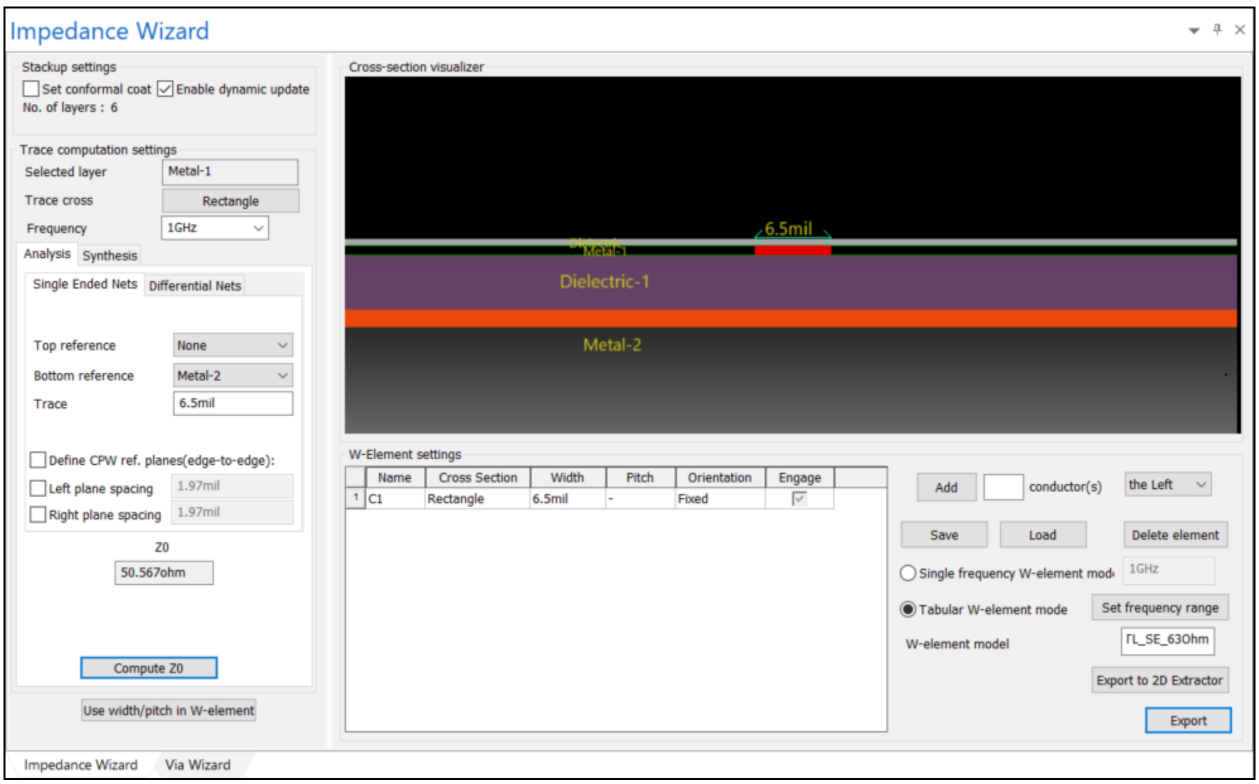
The **Stackup Layers** and **Impedance Wizard** windows use millimeters as the default unit of measurement. To change the default the unit to mils, navigate to the **Stackup Layers** window and select **mil** from the **Stackup** area > **Units** drop-down menu.



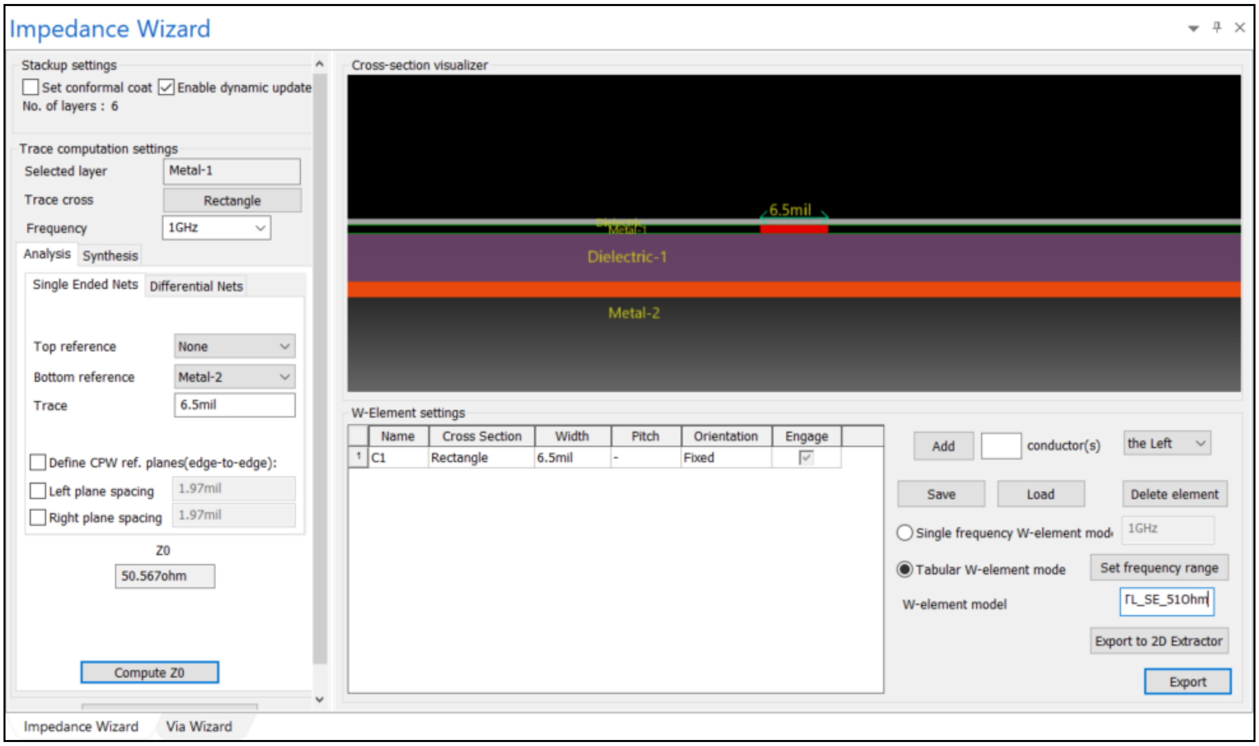
2. Select the second layer (i.e., **Metal-1**) from the **Stackup Layers** window to view its current selections in the **Impedance Wizard** window.



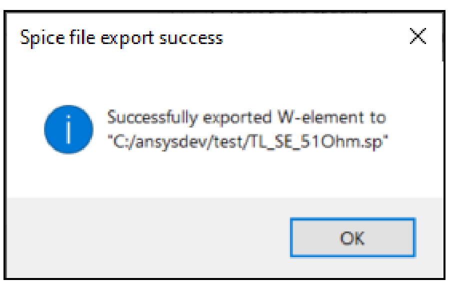
3. From the **Trace computation settings** in the **Impedance Wizard** window, do the following:
   a. Ensure **Metal-2** is selected from the **Bottom reference** drop-down menu.
   b. Enter **6.5mil** in the **Trace** width field.
   c. Click **Compute Z0** to display the impedance in the **Z0** field (i.e., **50.567 ohm**).
4. Click **Use width/pitch in W-element** to refresh the **Cross-section visualizer**.



5. Enter a new name for the model in the **W-element model name** field (e.g., **TL_SE_ 51Ohm**).



6. Click **Export** to open an explorer window. Then navigate to an appropriate directory and enter a **File name** for the model (e.g., **TL_SE_51Ohm2**).
7. Click **Save** to export the W-element model. If the export is successful, the following dialog box will appear, listing the directory and file name of the new *.*sp* (i.e., Spice) file.



Continue to Importing Transmission Line Models.

Importing Transmission Line Models into Circuit

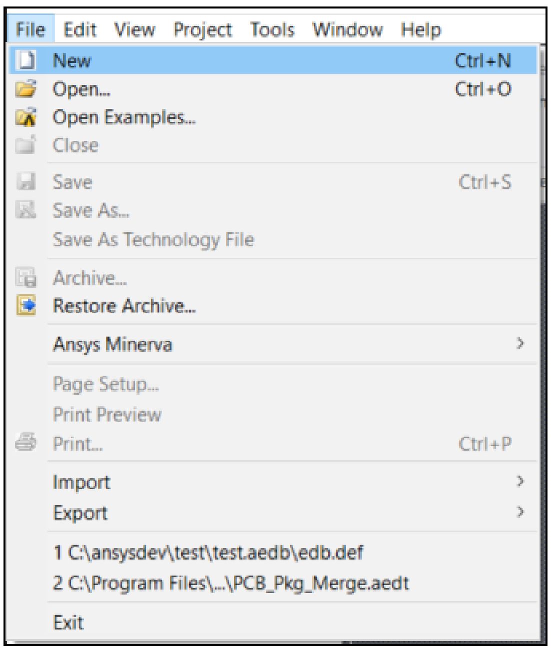
Complete the steps in the following sections to launch **Electronics Desktop**, start a new Circuit design project, and import the transmission line models created in **SI Xplorer**.

Launching Electronics Desktop

To launch **Electronics Desktop**, locate and double-click the **Electronics Desktop** shortcut icon or program file.

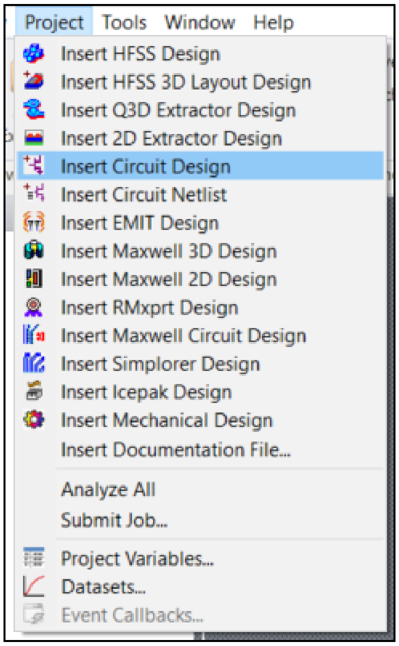
Starting a New Project

Once **Electronics Desktop** launches, a new project may appear in the **Project Manager** window. Otherwise, navigate to **File** > **New** to start a new project.

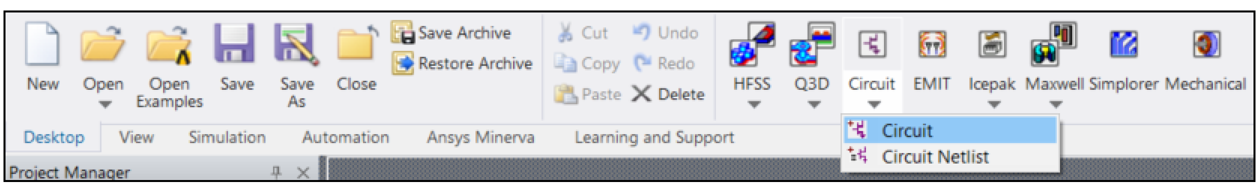


Inserting a Circuit Design

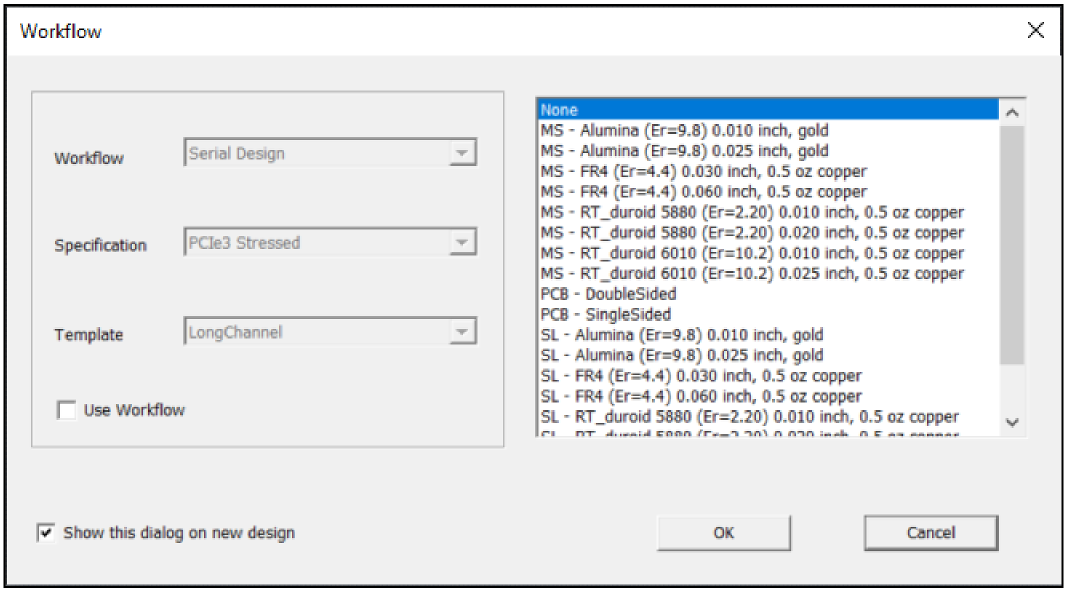
1. Do either of the following to insert a circuit design and open the **Workflow** window:
   - From **Project**, select **Insert Circuit Design**.



   - From the **Desktop** ribbon, select **Circuit** > **Circuit**.

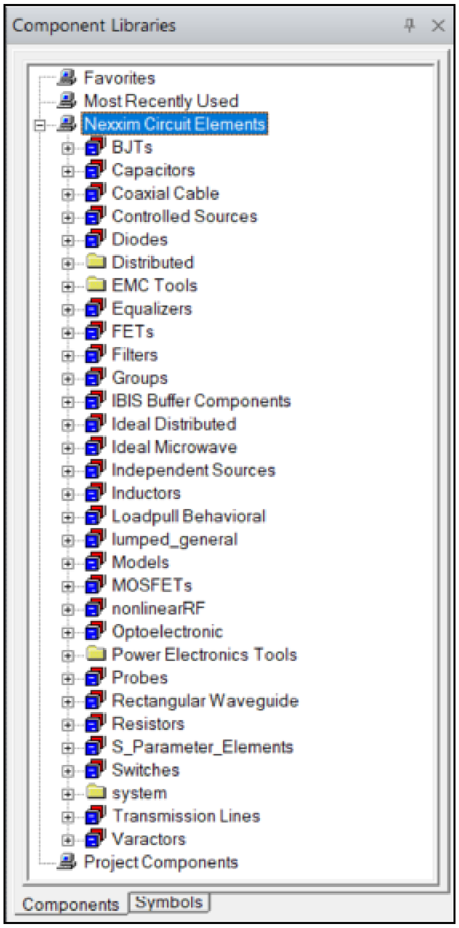


2. From the **Workflow** window, click **OK** to select the default settings (i.e., **None**).

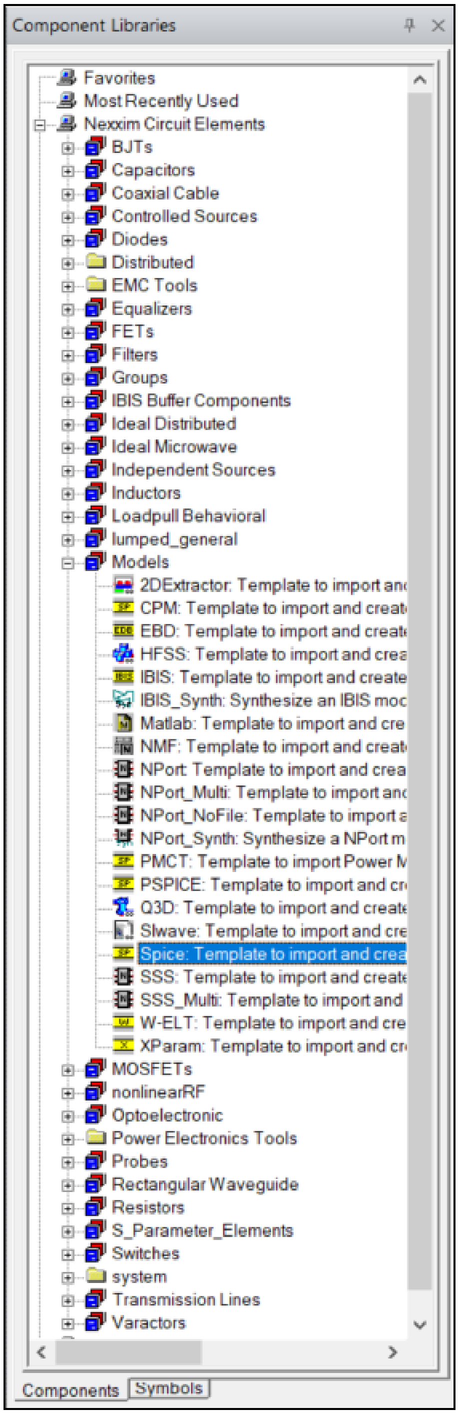


Importing the W-element Model

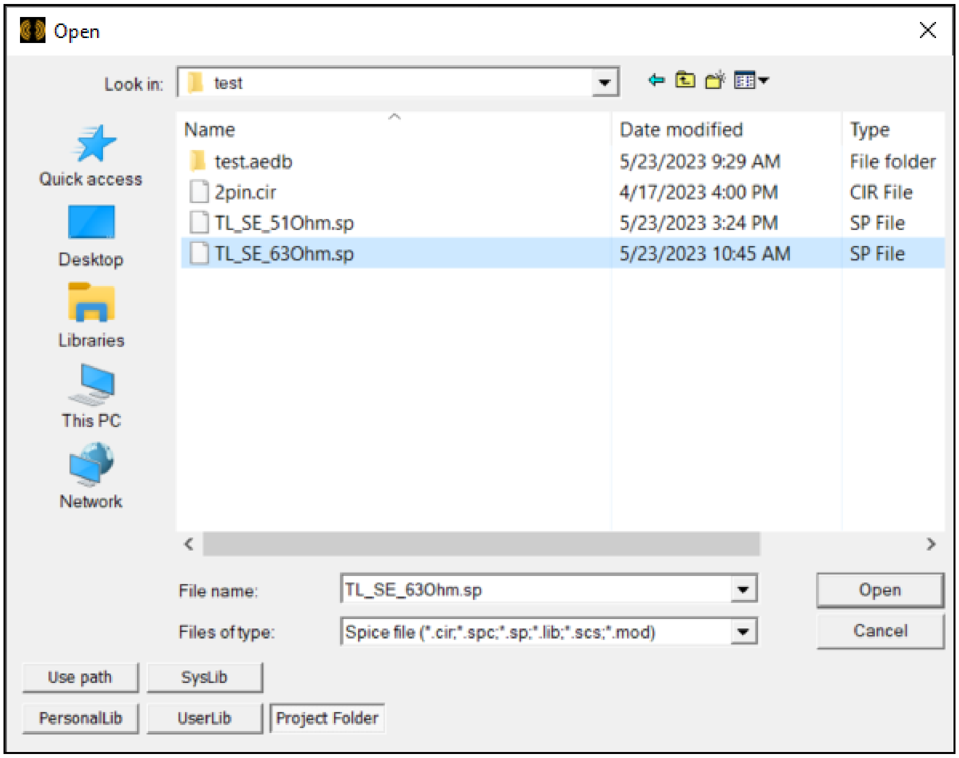
1. From the **Component Libraries** window, click the **Components** tab.



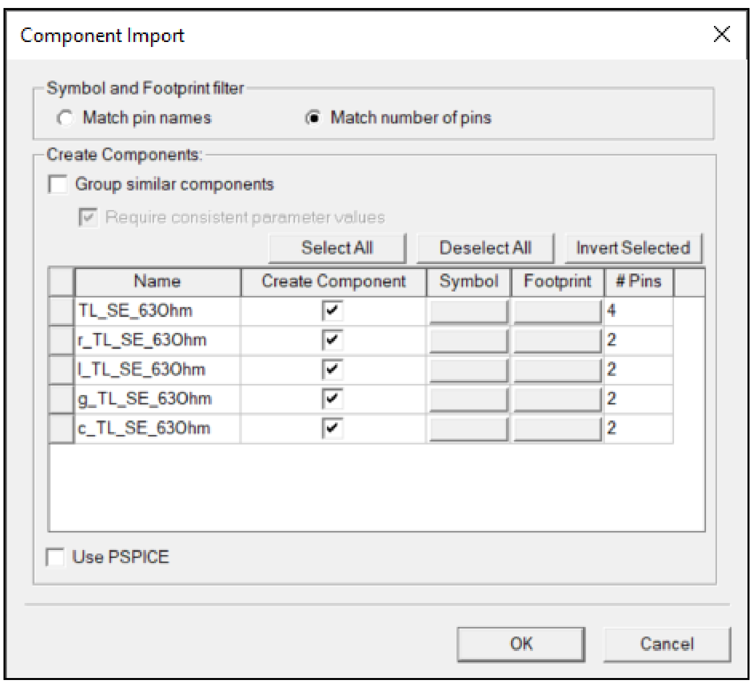
2. Expand the **Models** folder and select the **Spice** component.



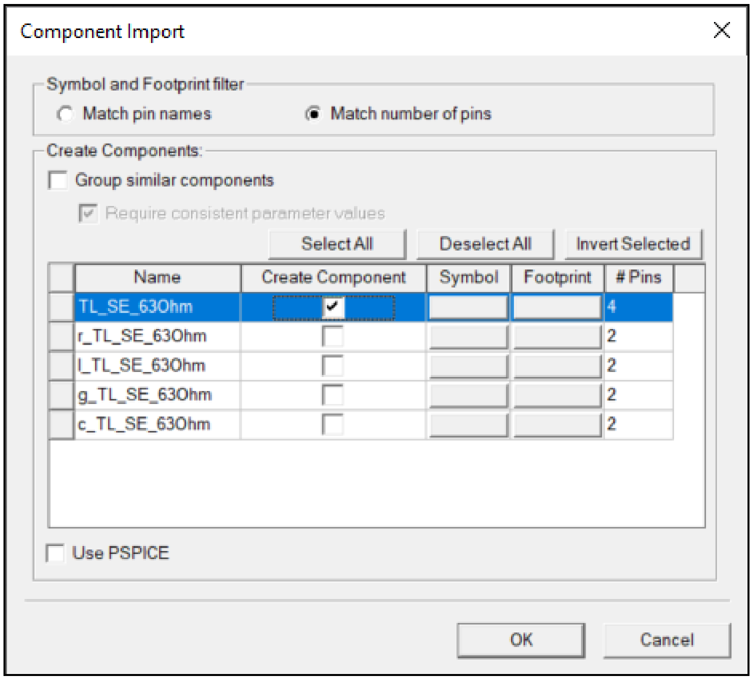
3. Attempt to **click+drag** the component to the **Schematic Editor** to immediately open an explorer window. Navigate to and select the model (i.e., **TL_SE_63Ohm.sp**).



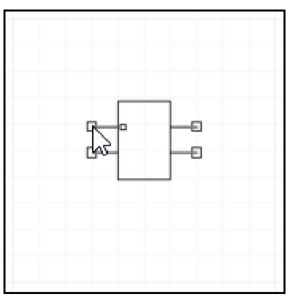
4. Click **Open** to close the explorer window and open the **Component Import** window.



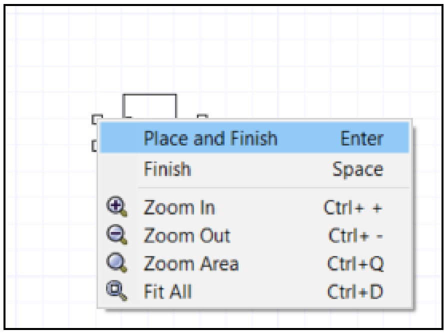
5. Uncheck the boxes in the **Create Component** column for all but one of the listed submodels (i.e., **TL_SE_63Ohm**).



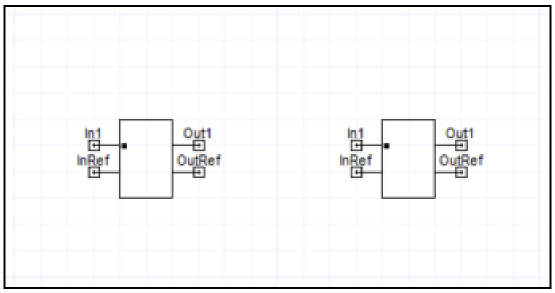
6. Click **OK** to close the **Component Import** window. The model appears, attached to the cursor.



7. Move the component to an appropriate location in the **Schematic Editor**. Then right-click and select **Place and Finish**.



8. Repeat steps 2-7 for any additional model(s) (i.e., **TL_SE_51Ohm.sp**).

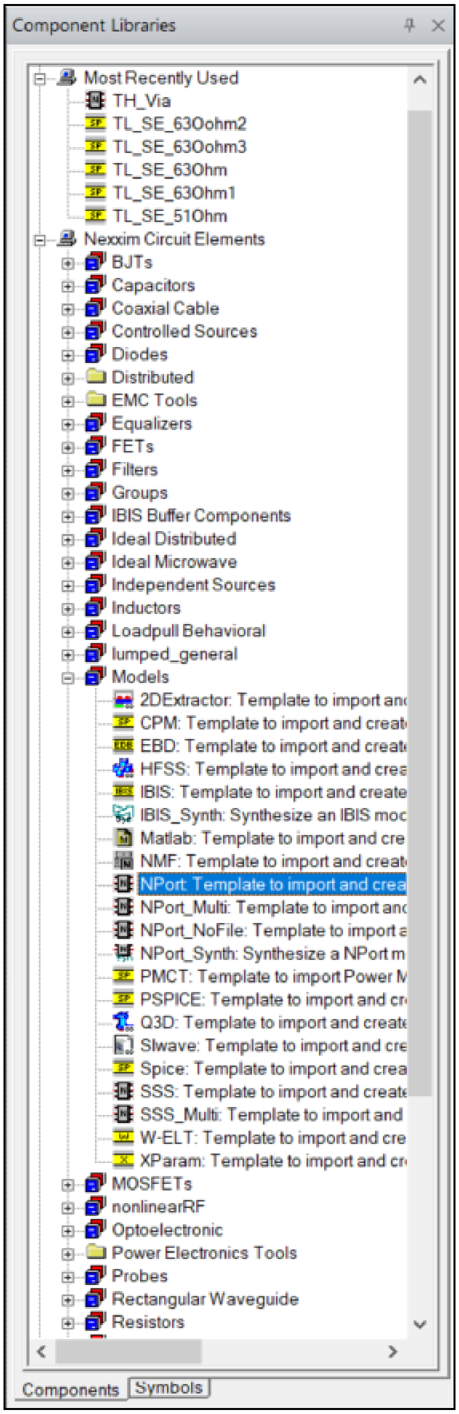


Continue to Importing a Via into a Circuit.

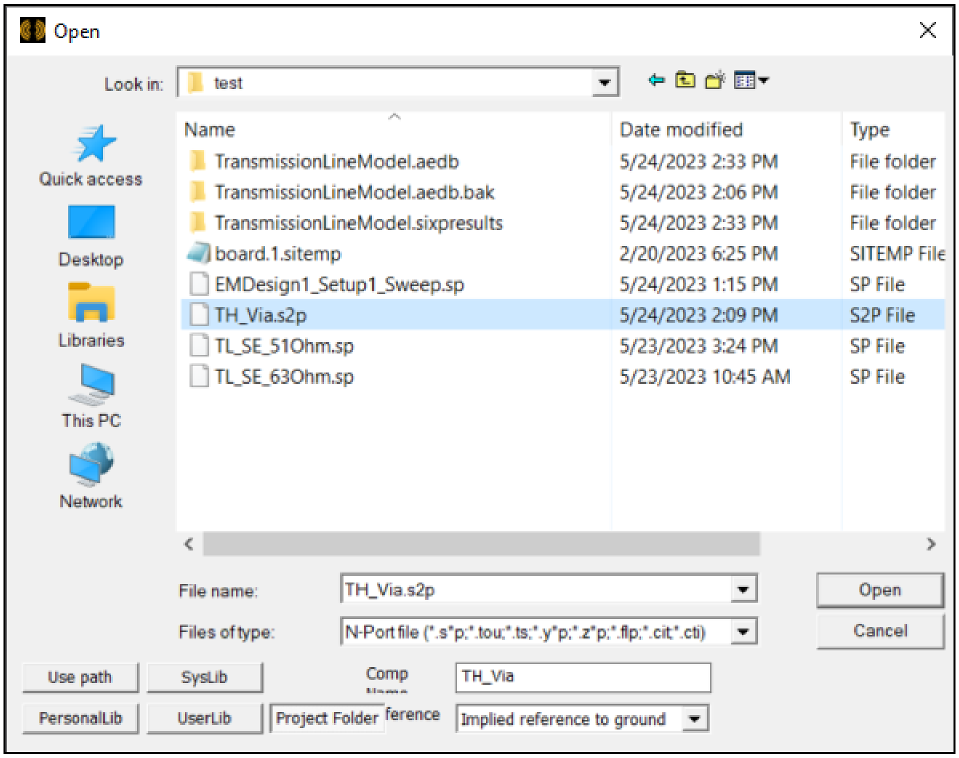
Importing a Via into Circuit

Complete the following steps to import a Touchstone file (i.e., via S-parameters) into Circuit.

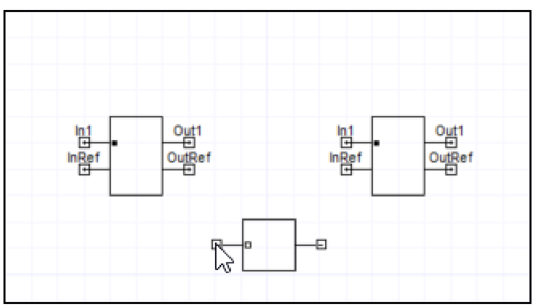
1. From the **Component Libraries** window, select the **NPort** component.



2. Attempt to **click+drag** the component to the **Schematic Editor** to immediately open an explorer window. Navigate to and select the via (i.e., **TH_Via.s2p**), then click **Open**.

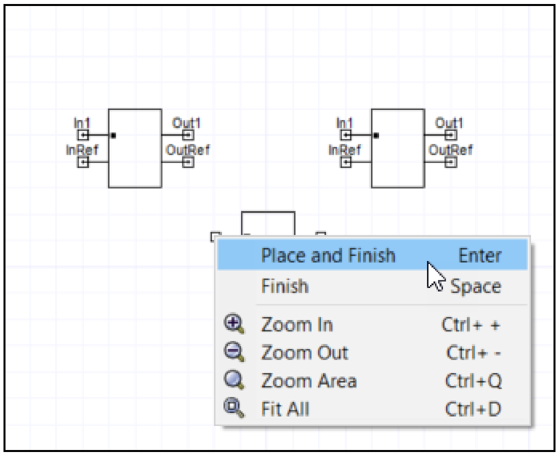


3. Click **OK** to close the **Component Import** window. The model appears, attached to the cursor.



4. Move the component to an appropriate location in the **Schematic Editor**. Then right-click

and select **Place and Finish**.

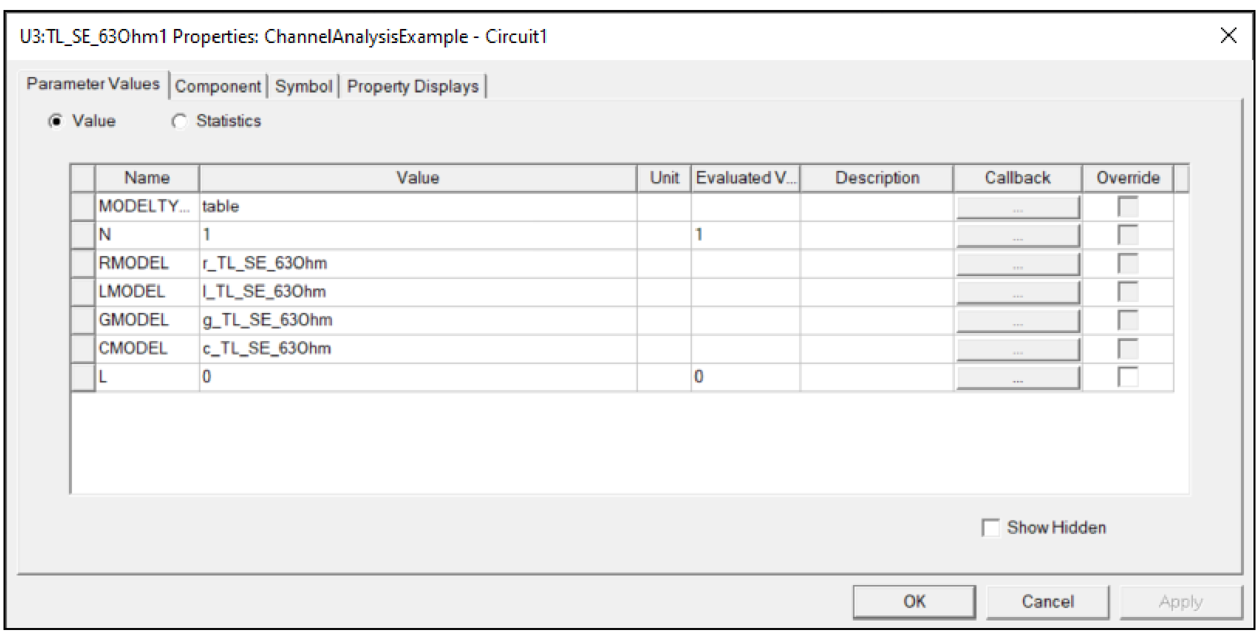


Continue to Editing the Circuit.

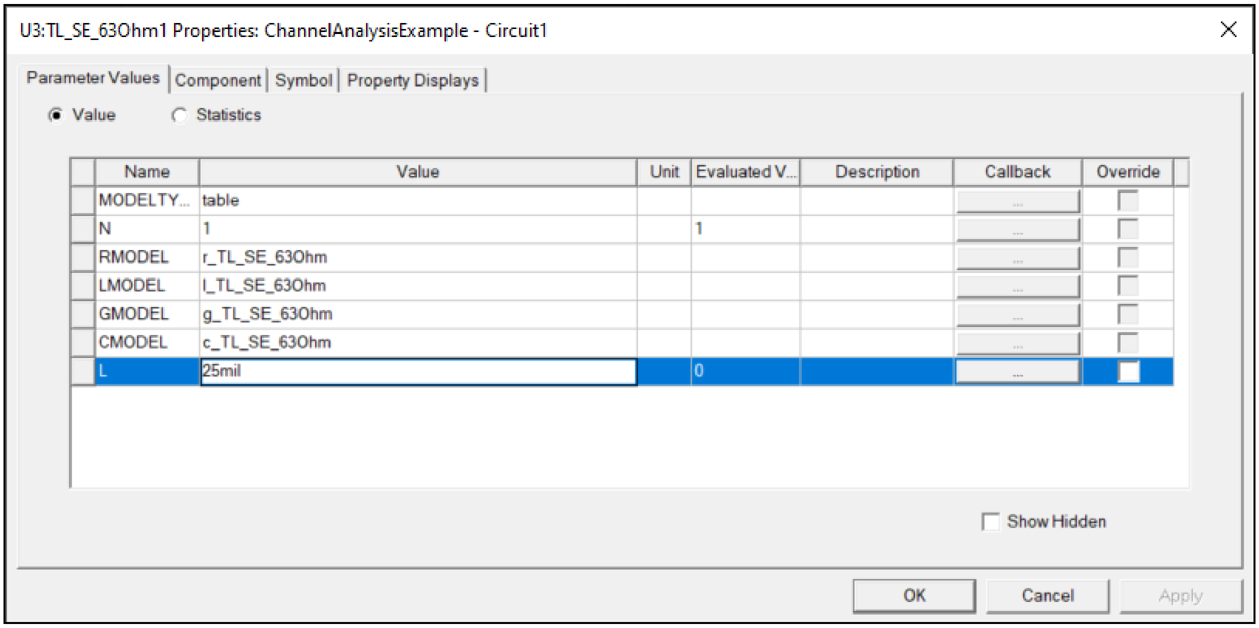
Editing the Circuit

Complete the following steps to edit the Circuit design comprised of the transmission line models and via component.

1. Double-click the **TL_SE_63Ohm** component to open its **Properties** window.

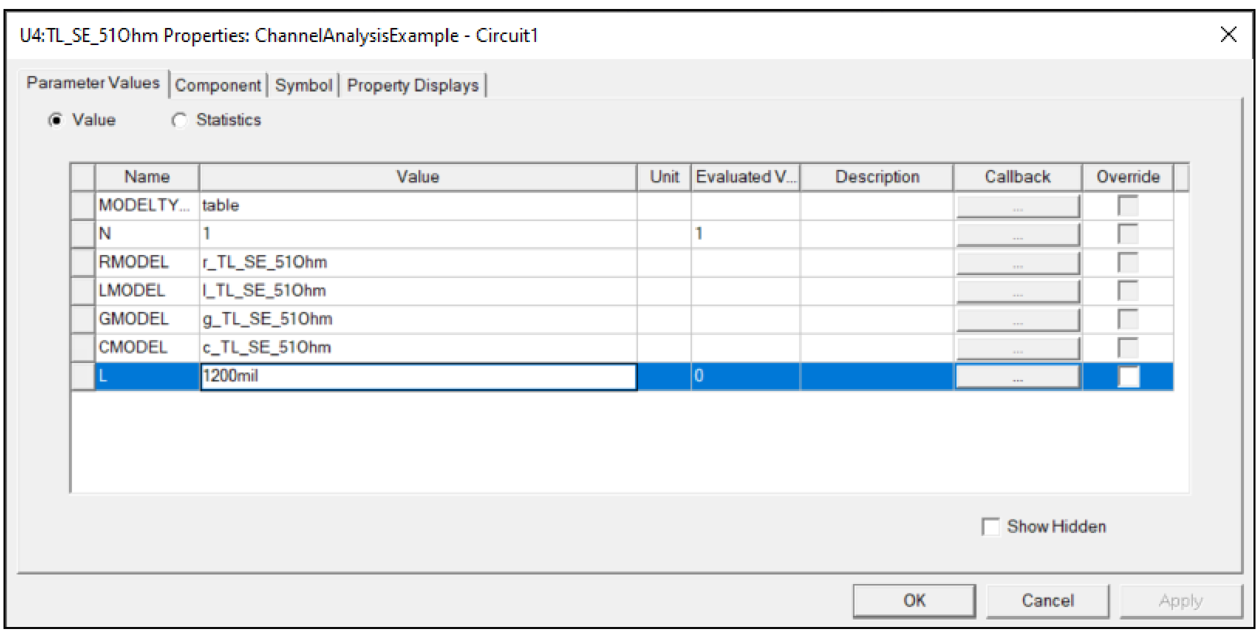


2. From the **L** row, enter **25mil** in the **Value** field.



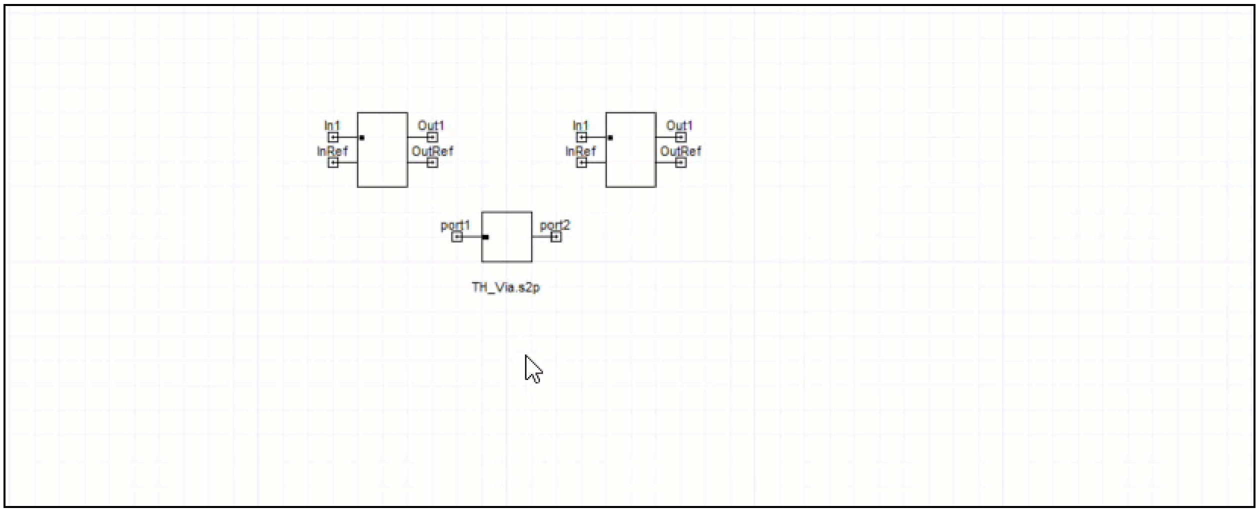
3. Click **OK** to close the **Properties** window.

4. From the **TL_SE_51Ohm** component, repeat steps 1-2. Enter **1200mil** in the **Value** field.

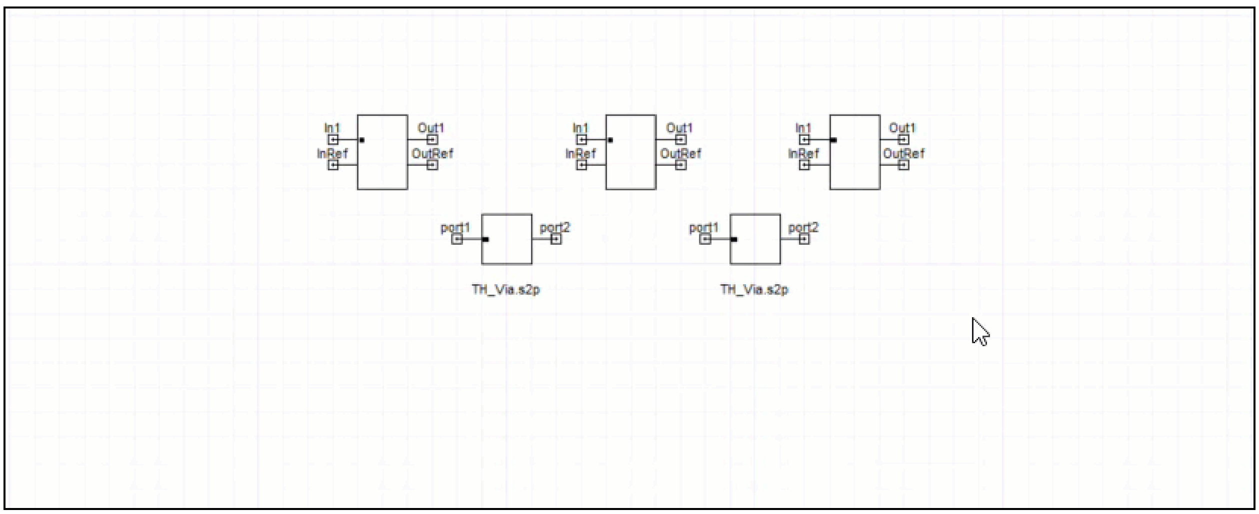


5. Click **OK** to close the **Properties** window.

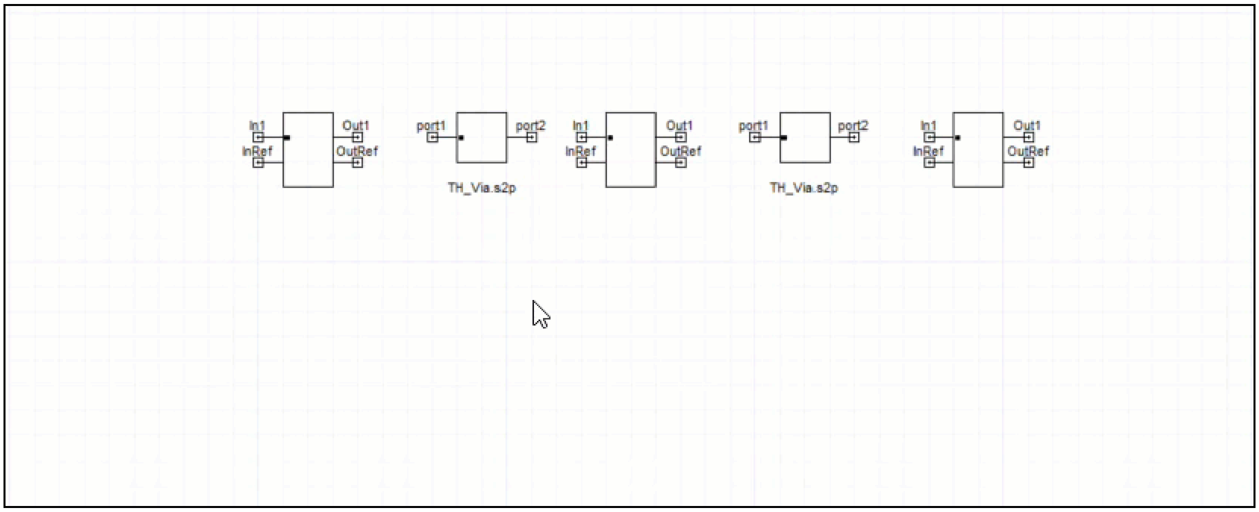
6. **Copy+paste** a second copy of the **TH_Via** component on the **TL_SE_51Ohm** component's right-hand side. Then **copy+paste** a second copy of the **TL_SE_63Ohm** component on the right-hand side of the new **TH_Via** component.



7. Arrange the components to match the following example.



8. Connect the components to match the following example.

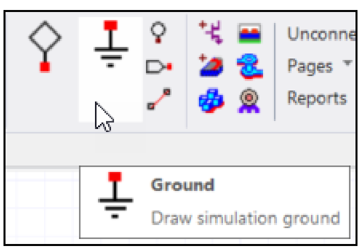


Continue to [Completing a Circuit Design](#).

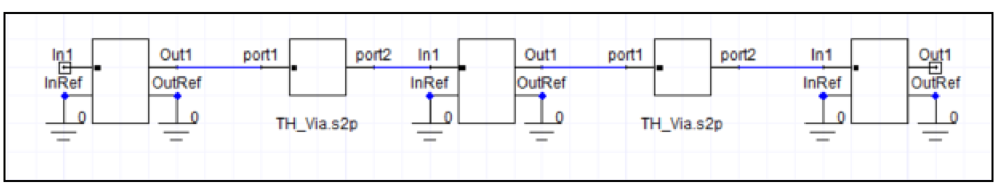
Completing a Circuit Design

Complete the following steps to finalize the Circuit design in **Electronics Desktop**.

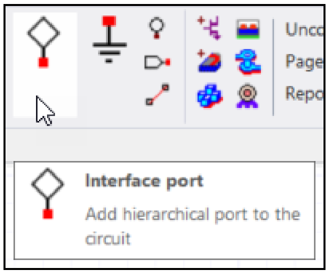
1. From the **Schematic** ribbon, click the **GND** symbol (i.e., **Ground**) to attach a ground component to the cursor.



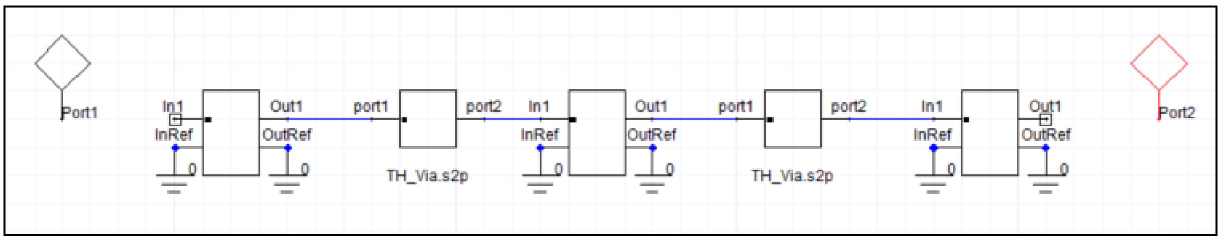
2. Click to place a ground component at each of the six available terminals in the design.



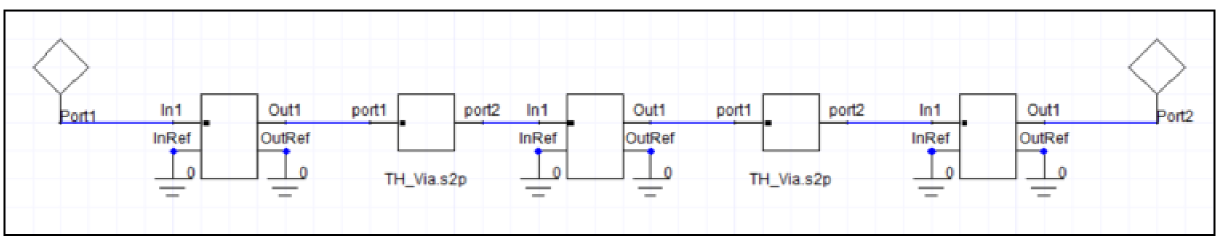
3. Click the port symbol (i.e., **Interface port**) to attach a ground component to the cursor.



4. Click to place a port adjacent to each side of the design.



5. Press **Esc** to detach the port component from the cursor.
6. Connect the ports to the adjacent open terminals using the same method employed in [Editing the Circuit](#).

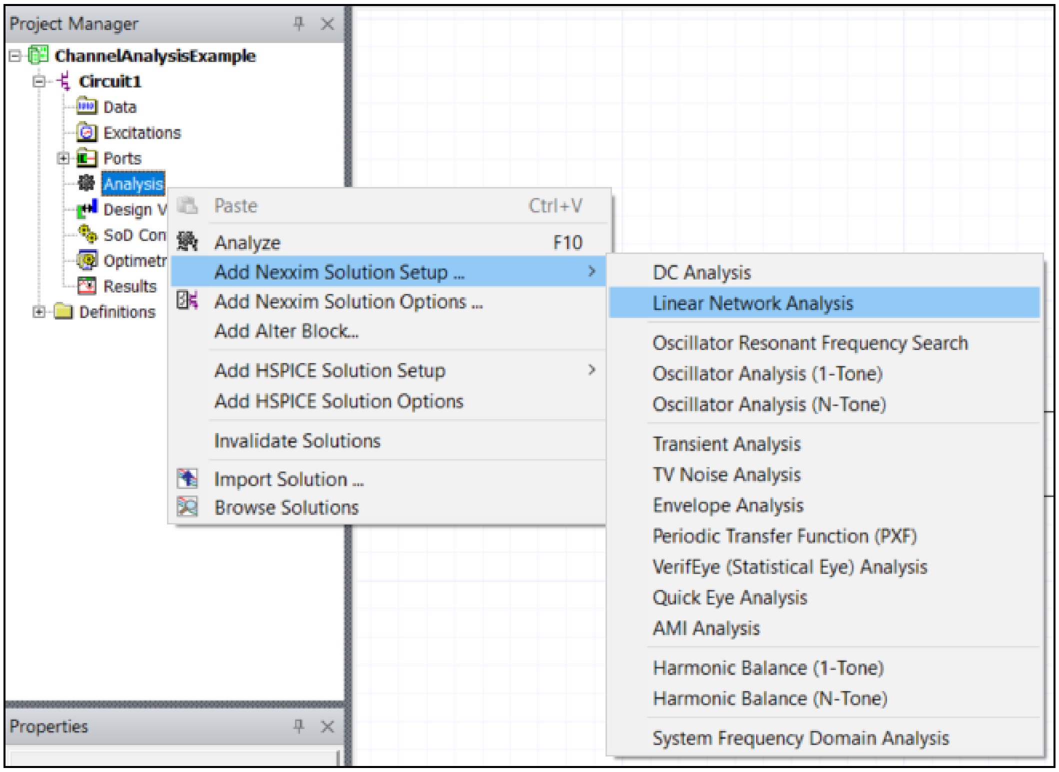


Continue to [Setting Up and Analyzing a Linear Network Analysis](#).

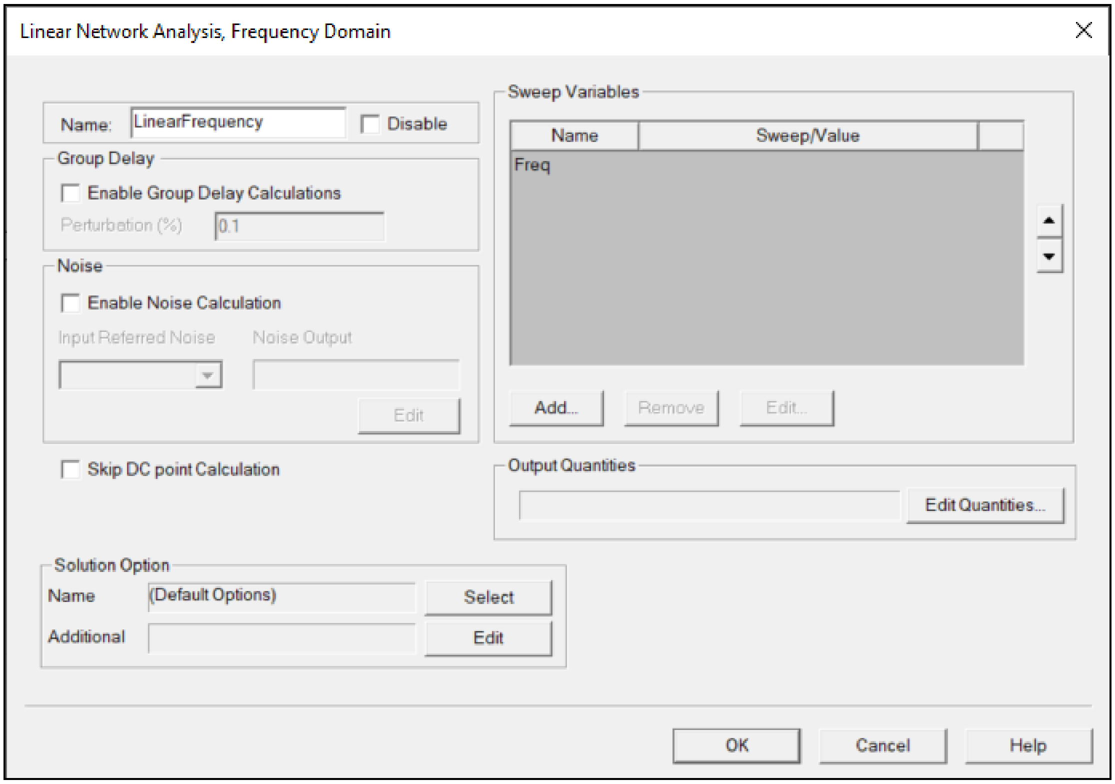
Setting Up and Analyzing a Linear Network Analysis

Complete the following steps to set up and analyze an LNA (i.e., Linear Network Analysis).

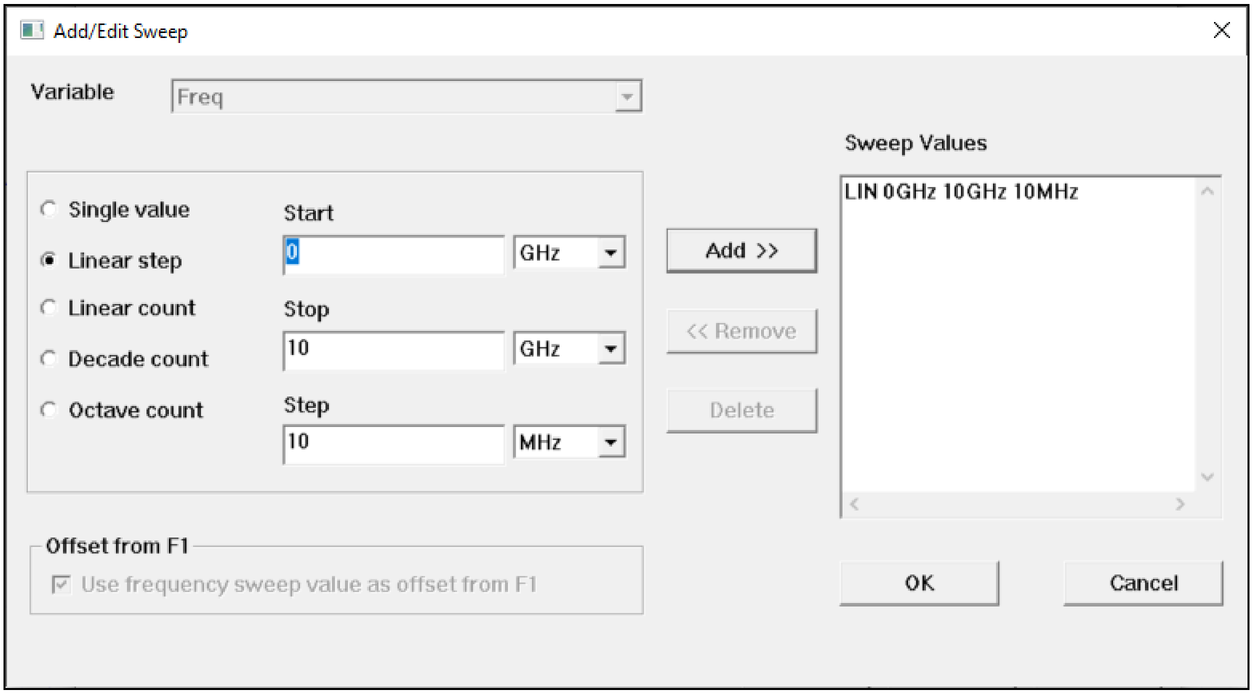
1. From the **Project Manager** window, expand the **Project Tree** and [***Active Design Folder***] (i.e., **Circuit1**). Then right-click **Analysis** and select **Add Nexxim Solution Setup** > **Linear Network Analysis** to open the **Linear Network Analysis, Frequency Domain** window.



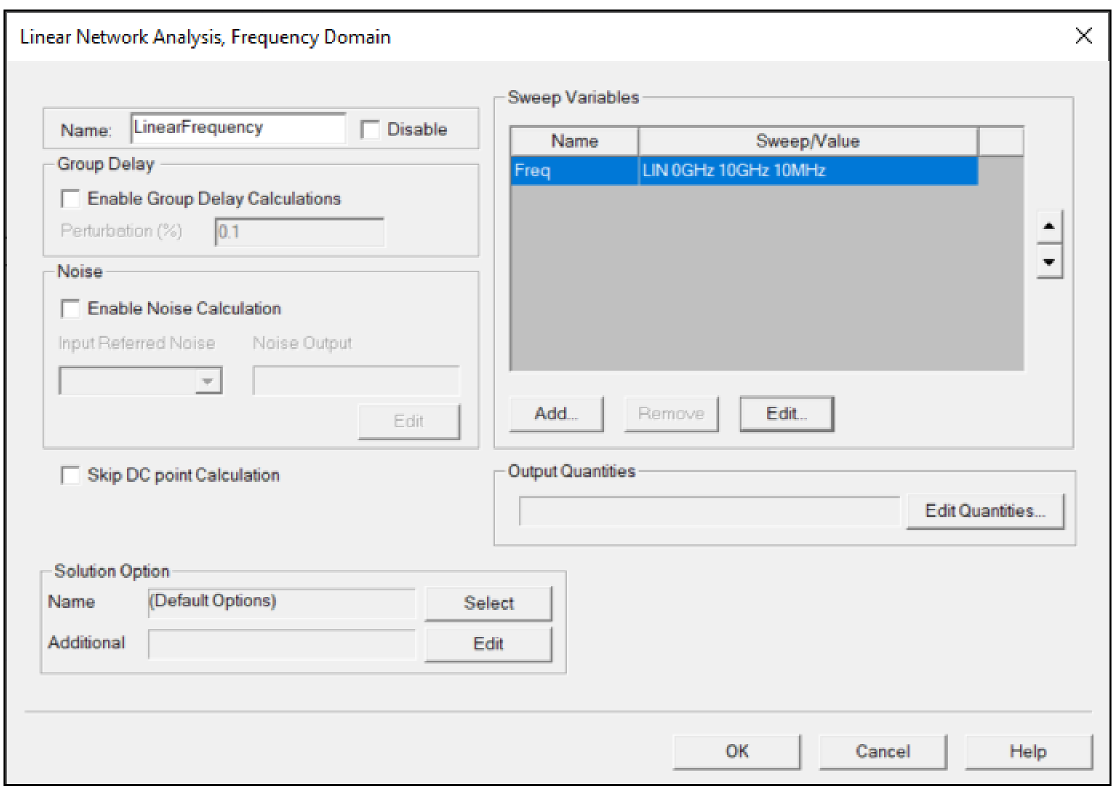
2. From the **Sweep Variables** area, select **Freq** to activate the **Edit** button. Then click **Edit** to open the **Add/Edit Sweep** window.



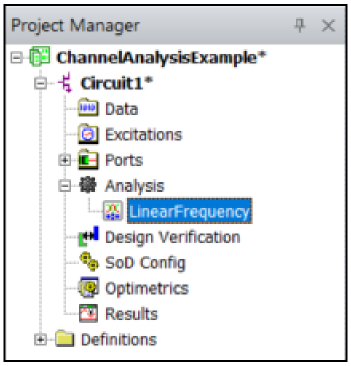
3. From the **Add/Edit Sweep** window, do the following:
   a. Select **Linear Step**.
   b. Enter **0** in the **Start** field.
   c. Enter **10** in the **Stop** field.
   d. Enter **10** in the **Step** field.
   e. Click **Add** to save the new values in the **Sweep Values** table.



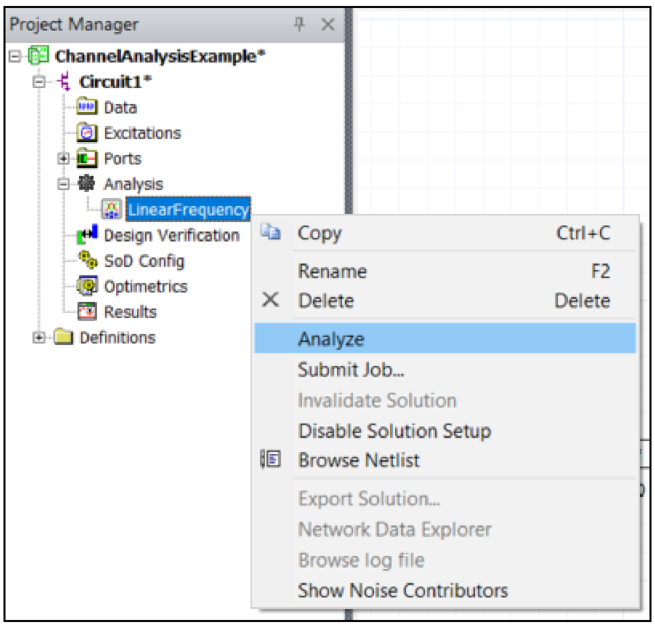
4. Click **OK** to close the **Add/Edit Sweep** window. The new frequency sweep appears in the **Sweep Variables** area of the **Linear Network Analysis, Frequency Domain** window.



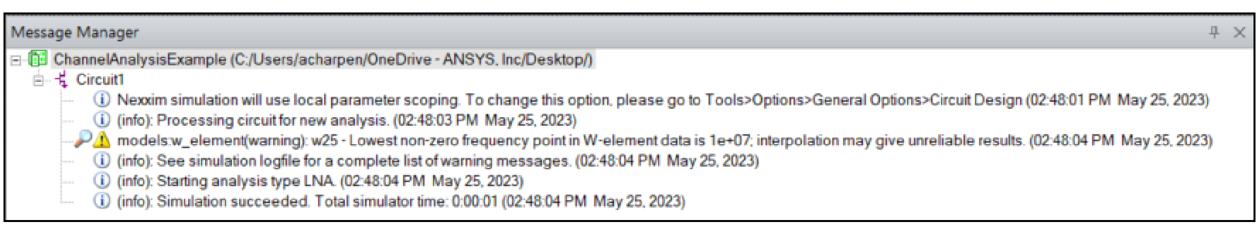
5. Click **OK** to close the **Linear Network Analysis, Frequency Domain** window. The new frequency sweep appears in the **Project Manager** window (i.e., from the **Project Manager** window, expand the **Analysis** folder).



6. Right-click on the new frequency sweep (i.e., **LinearFrequency**) and select **Analyze**.



View details related to the analysis in the **Message Manager** window.

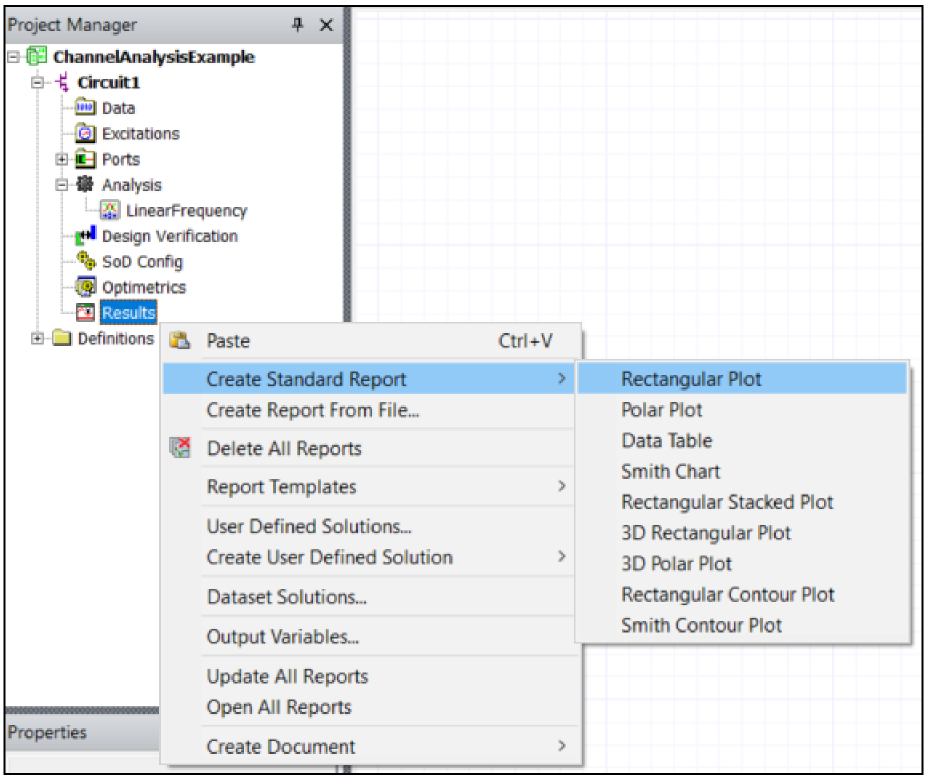


Continue to Plotting Insertion Loss and Return Loss.

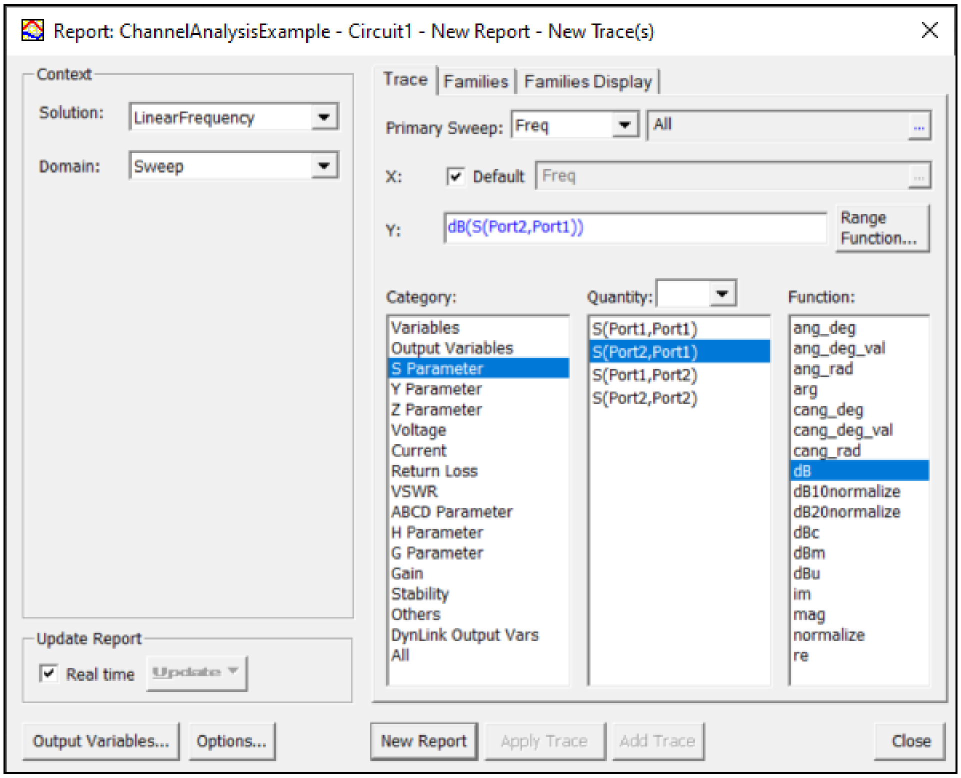
Plotting Insertion Loss and Return Loss

Complete the following steps to plot the Circuit design's insertion and return loss.

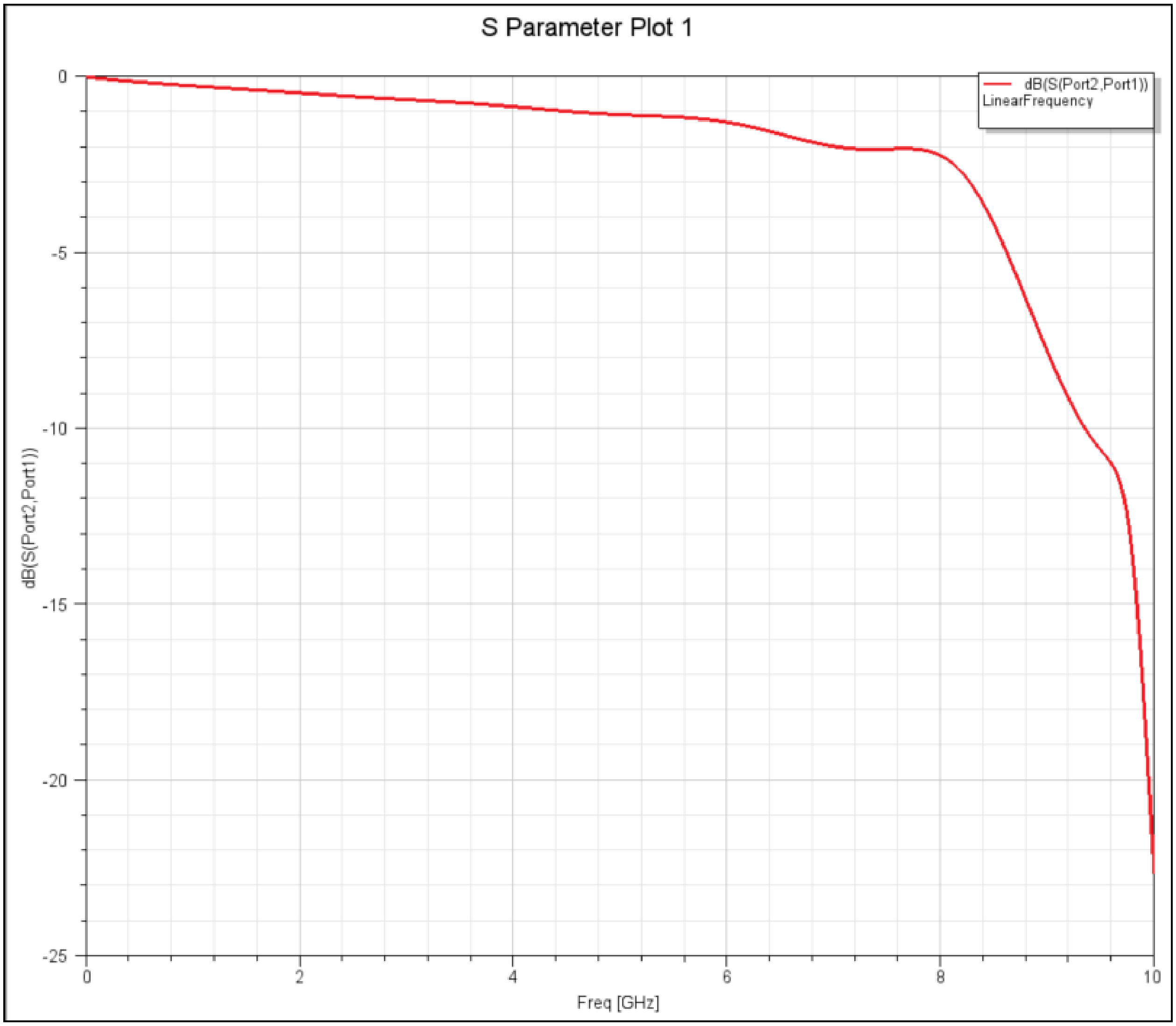
1. From the **Project Manager** window, right-click **Results** and select **Create Standard Report** > **Rectangular Plot** to open the **Report** window.



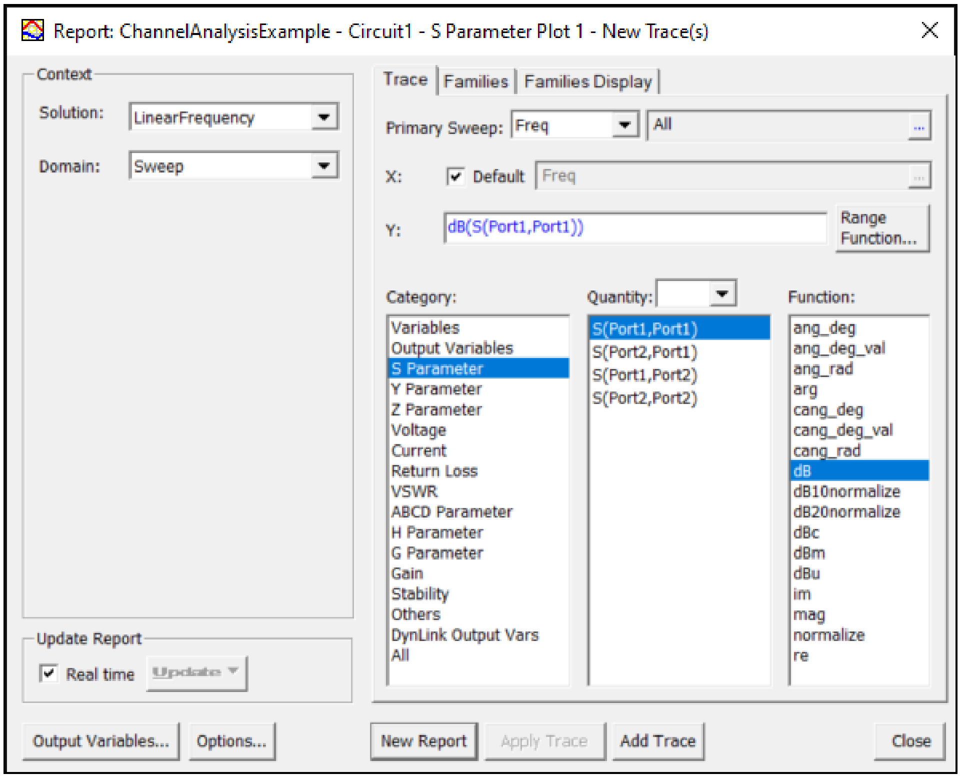
2. Select **S(Port2,Port1)** from the **Quantity** list.



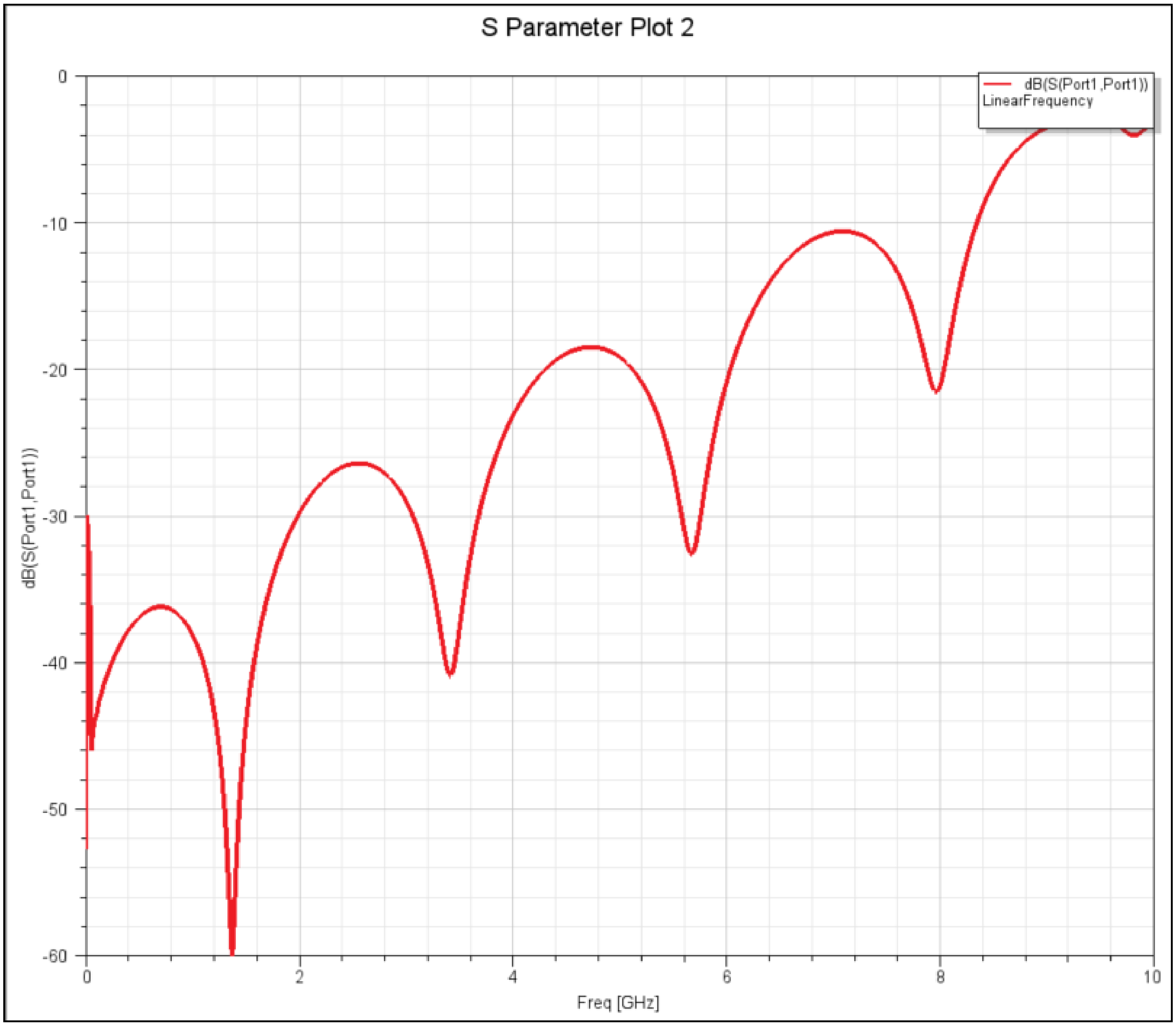
3. Click **New Report**. *Do not close the* ***Report*** *window.* After an interval, an **S Parameter Plot** opens displaying the design's insertion loss.



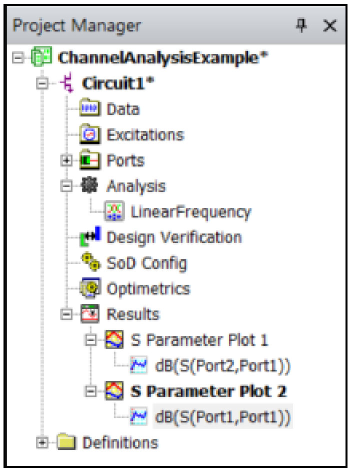
4. Navigate to the **Report** window. Then select **S(Port1,Port1)** from the **Quantity** list.



5. Click **New Report**. After an interval, an **S Parameter Plot** opens displaying the design's return loss.



6. Both plots are viewable from the **Project Manager** window (i.e., from the **Project Manager** window, expand **Results**).

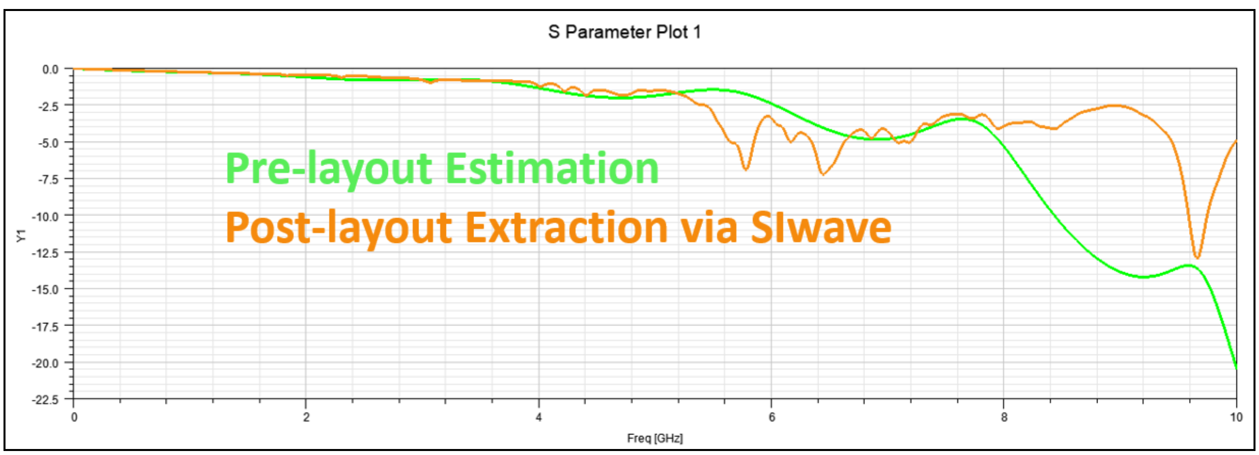


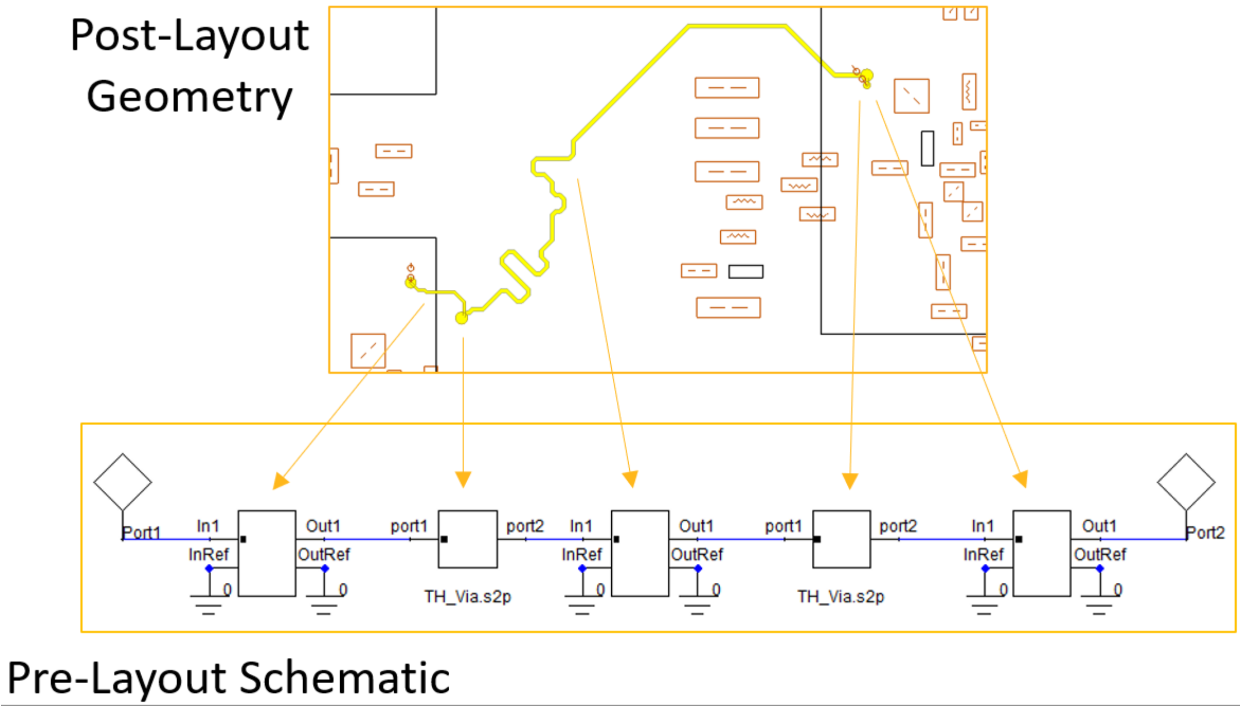
7. From the **Report** window, click **Close**.

Continue to [Comparing Post-Layout Results](#).

Comparing Post-Layout Results

Compare the pre-layout analysis to the post-layout S-parameter extraction. There is a high degree of correlation (i.e., up to 5GHz). Differences beyond 5GHz are attributed to variations in analysis length, return via location, non-ideal references (e.g., trace references of both power and ground nets on the PCB), as well as serpentine and/or cavity resonances.




Post-Layout
Geometry
Port1
In1
InRef
Out1
OutRef
port1
port2
TH_Via.s2p
In1
InRef
Out1
OutRef
port1
port2
TH_Via.s2p
In1
InRef
Out1
OutRef
Port2
Pre-Layout Schematic